Hindawi
Journal of Sensors
Volume 2022, Article ID 5075823, 16 pages
https://doi.org/10.1155/2022/5075823

Research Article

Enhancing the Accuracy and Speed of Sampling in Image Sensors by Designing Analog to Digital Converter with Power Decrease Approach

Zeinab Saeidiyan, Mohammad Hosein Fatehi, Mehdi Taghizadeh, and Mohammad Mehdi Ghanbarian

Department of Electrical Engineering, Kazerun Branch, Islamic Azad University, Kazerun, Iran

Correspondence should be addressed to Mohammad Hosein Fatehi; mh_fatehi@kau.ac.ir

Received 19 August 2021; Revised 4 November 2021; Accepted 19 November 2021; Published 24 January 2022

Academic Editor: Haibin Lv

Analog to digital converters (ADCs) enable the processing of real-world analog signals in the digital realm. These converters are widely used in sensor systems, medical components, multimedia systems, image sensors, and wireless sensor nodes. Today, in portable devices that are powered by batteries, low power consumption and small area are a major and important need. Therefore, methods that can reduce power consumption and area have a variety of applications and are of great importance. Power consumption is one of the most important features of an integrated analog to digital converter. In this paper, a new design of low-power and fast analog to digital converter is presented. This design is used for specific applications for image processing. The suggested approach for rereading the image for limited number of pixels was designed and simulated, showing a considerable power decrease compared to the suggested state that depends on the pixel values.

1. Introduction

Analog to digital converters are one of the major blocks in many electronic systems. Most of today's integrated circuits are signal-mixed (a combination of analog and digital circuits). In the most circuits, there is a digital signal processor block with inputs communicating with the outside world via analog to digital converters and sensors [1]. The expansion of portable electronic devices has encouraged the researchers to more survey the structures of analog to digital converters and to find more optimal structures with less power consumption. In this dissertation, new approaches for this objective will be surveyed.

One of the most significant factors for electronic devices that work with batteries is power consumption. The results of researchers' research in recent years show that almost every two years, the power consumption of analog to digital converters reduces by half [2]. On the other hand, the requirement of the electronics market in the coming years also calls for this decrease in power consumption and makes researchers inclined to do more research activities in this area. Thus, the decrease of power consumption in the present treatise was regarded as the major priority and solutions were suggested to push this purpose.

Image sensors have found much utilization in multiple industries, involving digital cameras, mobile cameras, cars, medical industries, and wireless sensing networks, in many of which CMOS technology is utilized. Developments in semiconductor industry and the approaches of handling electronic circuits, along with the developments and innovations which have emerged in the area of circuits of these sensors, have led CMOS sensors to snatch overtaking from the same samples today. For instance, increasing the dimensions and number of pixels of the image sensor, decreasing noise kinds, advancing the speed of image recording, and especially considerably decreasing the power consumption in

these sensors have caused these sensors to be regarded by multiple industries. One of the most significant utilizations is the medical industry, which, due to CMOS ability in the performance of low power image sensors and in a very small area, can play a significant role in the advancement of novel medical instruments and equipment. Besides, the novel utilizations of image sensors like mobile phones, cars, military industries, wireless sensor networks, and IoT have made this one of the most significant problems in modern electronic industries and systems [3].

Nowadays, among the various features of a CMOS image sensor, low power consumption is one of the most significant elements of the interest of multiple camera manufacturer companies to apply these sensors. Since the largest share of image sensors is utilized in devices and equipment which are wireless and work with the computer, the role of power consumption in these circuits is very pronounced. On the other hand, decreasing the power consumption of image sensor can be related to decreased power consumption of whole device and increasing battery life and advancing the function of other sections in the long term. Thus, after the dimensions of image sensor, power consumption can be regarded as the most significant features of these systems [4].

In recent years, many attempts were done to decrease the power consumption of various sections of image sensors. Meanwhile, the circuit part of image sensor readouts is regarded as one of the most significant consumer sections of power related to the utilization of a high number of analog to digital converters. Thus, many studies were presented to decrease the power consumption of this part due to the utilization of image sensor. Moreover, many approaches were presented so far to decrease the power consumption of analog to digital converters, showing the significance of this problem. This becomes more significant when the spatial dimensions of sensors increase day by day as the image sensor industry progresses. Thus, regarding the increase in the number of rows and columns, the number of analog to digital converters utilized increases highly by the conventional readout approach like column rereading that increases the power consumption of image sensor. In addition to the above cases, in some medical utilization like endoscopic capsules in which the size and volume of electronic equipment are regarded as significant features, by decreasing the power consumption, the physical volume of computer which is one of the bulky parts of this equipment can be decreased. Thus, research on decreasing the power of analog to digital converters for image sensor utilizations can be one of the most significant problems ahead in these systems.

2. Research Background

In [1], the auto zeroing approach that is basically a foreground approach was applied as background. In auto zeroing approach in a circle, the offset value is stored in the circuit capacitor, and in the other circle, this offset reduces from the entrance.

In [2], utilizing digital techniques to correct the error of the exclusion code of comparers, the impact of the contrasting error under calibration was compensated. Majority of three logic block compensates for the impact of comparing error under calibration.

In [3], offset error compensation is done by adjusting the voltage of the body of preamplifier-class even-entry transistor. To this purpose, each comparer has an offset calibration circuit (OSCAL). This circuit makes the needed trim voltages and uses it to the body of every transistor.

In [4], applying an efficient idea, convergence rate has increased to more than 100 times compare to other similar works, and a correlation-based calibration algorithm was presented so quickly. The presence increases the number of samples required for calibration and consequently decreases algorithm convergence rate. The cause for this issue is statistical dependence of this phrase with the in-entrance signal.

The weakening of infill signal in the calibration process was differently handled. In this article, two analogs to digitally multiple converters were utilized and similar inlet signals but with opposite polarity were used to these two converters. In the digital part, with the sum of two signals provided from two channels, indented signal is deleted and the signals containing the error remain [5].

A reference converter in [6] was applied to handle calibration. In some references, this SHADC converter is also referred to. In the suggested approach, all converters are regarded as a nonlinear system and its nonlinear behavior is lined by an ADF utilizing LMS algorithm. Two sorts of offset errors can be described in the converter structure. The first sort is the offset of the comparers (part of the sub-ADC error) which was previously described how to compensate for it utilizing redundancy in the structure. The second sort is the entrance offset which is added to the information signal, the major section of which is due to the amplifier offset between the floors and a small section of it is due to the switches. In usual, in converters, offset compensation of type II is given up because it has no impact on the structure's line function and only makes a dc shift in the transition characteristic. In the items where the designed pipeline converter is applied in some channels as time interleaving (this sort of structure will be introduced as follows), naturally, offset errors can cause harmonic distortion, so a solution must be regarded for it.

It was attempted to push much of the offset compensation analog technique to the digital part. Handling so decreases the complexity of analog hardware. To this purpose in [7], chopping technique was applied. Two sorts of nonlinear errors can be identified in every class. The first sort is a nonlinear error resulting from sub-DAC circuit. Many correlation-based calibration techniques compensate for this sort of error. The second sort of error is due to the amplifier circuit among the classes (especially up-amp). Compensating for this error is somewhat more difficult than the first sort.

In [8], Machado et al. have indicated that if the pixel step size is less than about 3 to 5 μm, we will require microlenses to advance the demanded sensitivity. Microlenses can increase the amount of efficient FF. On the other hand, the decrease of dimensions in these technologies is accompanied by an increase in metal layers, which can cause capacitor

density, which is known as an advantage if correctly designed.

Other approach is noted to decrease the power consumption of CMOS image sensor. In usual, to handle a three-step digital imagery system, storage and compression are done in a burst that needs a lot of bandwidths in ADC and memory circuits. In the second approach, compression can be performed before the storage that decreased the bandwidth needed for digital parts. If the compression can be handled before converting the signal to digital, it can be highly decreased with the bandwidth needed for ADC which will save considerably the design of analog to digital converter [9].

3. Methodology

The value of power utilized in the difference gauge converter is due to the in-entry signal activity. In this part, we analyze the power consumption of suggested converter. The power of converter is divided into some sections. The power of logical circuits, for example, power of digital to analog converter, is drawn from the voltage reference. In the item of power utilized in digital parts like counters and control circuits, as we know, it fits with the phrase $f \cdot C \cdot V_{DD}^2$, in which f indicates the working frequency and C capacitor of every circuit. Since the suggested converter is only active at the time of conversion and the counting and activity of other control circuits is handled only at the time of conversion, the power utilization of these circuits must also be computed only in this section of the complete period of every sampling [10, 11].

Thus, the power utilization of control and counter sections which make up a considerable section of the converter's power consumption is linearly proportional to the difference between two samples. For instance, if we suppose the duration of the sampling period T_s and regard it equal to the maximum possible time for conversion, T_s value will be $2^N T_{\text{CLK}}$, in which N is the number of converted bits and T_{CLK} time of the converter reference click period. Furthermore, considering the difference between two consecutive samples, the time of transducer activity alters which will be a fraction of T_s. Considering that the counting time for voltage change is equal to T_{CLK} per LSB, the conversion time can be expressed due to LSB based on the difference between two consecutive samples. Thus, the power consumption of converter is proportional to the difference among consecutive samples which can be noted as

$$P_{\text{digital}} = \frac{\Delta V_{\text{in}}}{V_{\text{FS}}} \cdot \alpha \cdot f \cdot C \cdot V_{\text{DD}^2}, \tag{1}$$

where ΔV_{in} is the difference between two consecutive samples due to V_{LSB} and V_{FS} voltage of the whole scale of converter which in the suggested converter is equal to the value of power voltage. α is also a technology-dependent coefficient. Hence, in the item of the comparator circuit, it can be computed similar to the counter circuit and control circuits. Since the approach of utilizing the comparator is such that it only consumes power at transition times, the working frequency and voltage range are also quite similar to digital circuits. Thus, the comparator's power consumption can be computed from the same formula as before. In this route, the total power consumption of digital sectors along with the comparator in the suggested converter will be linearly proportional to the difference between two consecutive samples.

In the item of digital to analog converter power related to the impact of changing on its power consumption, this approach of power reduction does not happen linearly and firstly to the original code and then to the difference between two samples. To correctly compute this amount of power due to the equation (2): [12]

$$P_{V_{\text{ref}}} = \frac{V_{\text{ref}}}{T_s} \sum_{i}^{2^N} Q_i. \tag{2}$$

In this equation, N is the number of bits, V_{ref} of the converter reference voltage, T_s sampling time period, and Q_i total load drawn from the voltage reference through i-turn to calculate; we suppose that m is the digital code corresponding to the previous sample value ($V_{\text{in}}[n-1]$), and we also indicate the difference among the samples (ΔV_{in}) due to the number of LSB with k. In this case, the digital to analog converter can be computed in two modes of one weighting and binary capacitors due to the approach utilized in [13]. To handle this, first, we compute the amount of capacitive array load for two modes of increase and decrease which is provided from the following equations:

$$\begin{aligned} Q_{i,\text{up}} &= C_0 V_{\text{ref}} \times \left(\frac{m-i}{2^N}\right), \quad i = 1, 2, \cdots, k, \\ Q_{i,\text{down}} &= C_0 V_{\text{ref}} \times \left(\frac{m+i}{2^N} - 1\right), \quad i = 1, 2, \cdots, k. \end{aligned} \tag{3}$$

Then, utilizing equation (1), we provide the power consumed in the form of

$$P_{V_{\text{ref}},\text{up}} = \frac{C_0 V_{\text{ref}^2}}{2^N T_s} \left(mk - \frac{k(k-1)}{2}\right), \tag{4}$$

$$P_{V_{\text{ref}},\text{down}} = \frac{C_0 V_{\text{ref}^2}}{2^N T_s} \left(\frac{k(2m+k+1)}{2} - 2^N k\right). \tag{5}$$

To find an intuitive understand of power achieved for capacitive DAC in the form of one-unit weighting, its power consumption was plotted due to the difference between two consecutive samples and also the value of the previous code in Figure 1 [14]. As can be observed from the figure, on average, in both increasing and decreasing modes, DAC's power consumption reduces by decreasing the difference between two consecutive samples. Hence, this is not a linear power decrease in such a way that its amount is more in the increasing kind. If we handle DAC as binary weighting, the mathematical computation approach will not be simple. That is because the number of states which can happen is very high, and the corresponding switches, in addition to

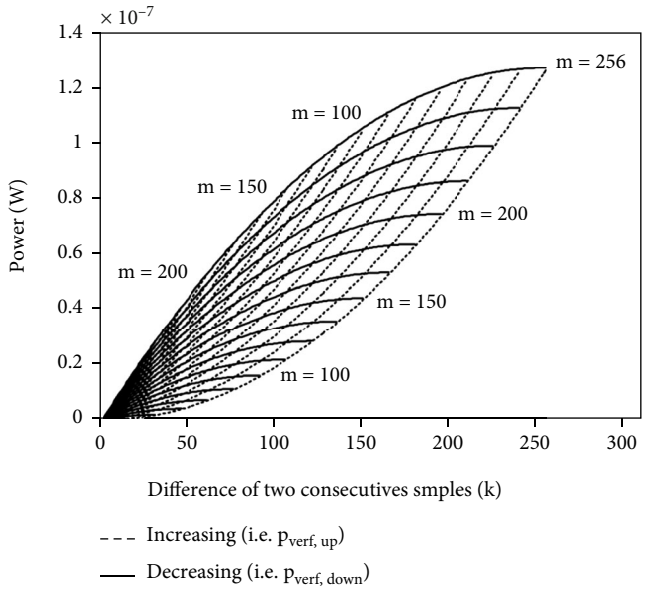

Figure 1: The computed power consumption for capacitive DAC with one-unit weighting for increasing and decreasing modes.

depending on previous code, depend on how binary numbers change which makes manual computing difficult. In this route, MATLAB software was utilized to survey how to alter the power consumption for various modes. Figure 2 indicates the value of power consumed due to the difference among consecutive samples and the previous code value for several specific modes [15].

4. Simulation and Locating of the Suggested Converter

In this part, with various simulations, we survey the accurate function of the converter, and by estimating the significant parameters of analog to digital converters, we survey the efficiency of converter for multiple inputs. Then, we survey the mode of transducer in CMOS 0.18 μm technology and compare the postlife results with simulation results. To confirm the function of the proposed converter, this converter is designed in CMOS 0.18 μm technology with a power voltage of 1.8 V with a frequency of 5 MHz. The converter is designed to fit the design for image sensors. Hence, the accuracy of 8-bit converter is chosen due to the image standard. Regarding that in the worst case scenario, the converter needs 2^N clacks to do the conversion; the sampling frequency should be less than $5\,\text{MHz}/2^8 = 19.53\,\text{kS/s}$. Binary DAC capacitors are also chosen due to the smallest value of MIM technology capacitors which is equal to 20 fF. Thus, the total value of DAC capacitor is 5.12 pF. Moreover, the resistance of switches can be identified. These amounts should be identified in such a way that in a half period of the reference block, which is equal to 100 ns, the meeting time is over.

Figure 3 indicates the simulation of difference gauge converter in exchange for the sinusoidal entrance with

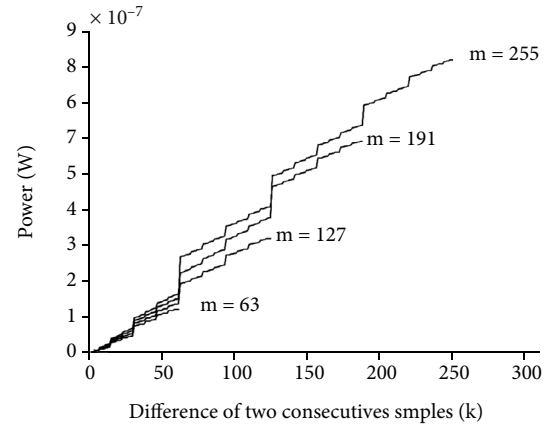

Figure 2: The power consumed for capacitive DAC with binary weighting for 4 various modes.

nyquist frequency. In the simulation, the function of converter in various phases is well indicated. As in the figure, it is also known that the time of circuit activation changes due to the way the changes are made, and in sections of the signal where the changes slow down, the activity of circuit reduces in the same proportion that reduces the total power consumption of converter. The provided results are indicated in the schematic simulation of the transducer circuit in Table 1. As predicted, since the power consumption of the suggested converter is various from the change in signal frequency, the provided effective FoM amount is also varied at different frequencies.

Thus, the specifications of converter are provided for two multiple frequencies in the table. Figure 4 indicates the changes in power consumption and SNDR due to changing the incision sinus frequency. The results indicate that SNDR value does not change much by altering the entry frequency and alters from 48 dB to 50 dB. These results indicate ENOB's destiny of about 7.8 bits. Thus, the value of power consumed in these simulations is decreased by reducing the frequency which leads to the advancement of FoM by decreasing the frequency. It should be told here that the change in the power consumption of converter at multiple entry frequencies is due to various sections of the converter which is not equally divided.

Figure 5 indicates the power consumption share of every section of converter at two frequencies of 457 Hz and 9.6 kHz. As it is known, by decreasing the inputting frequency in addition to reducing total power consumption, the share of DAC power and the comparator does not change much compared to the total power, the power consumption of counter is associated to more decrease, and the power consumption of other control circuits is fewer.

Figure 6 also indicates the locating of the difference meter converter in TSMC CMOS 0.18 μm technology in which various parts are specified on the shape. The surface of occupied silicon is about 130 μm × 250 μm. Around half of the occupied surface is due to binary capacitor DAC which is handled with minimum capacitor of technology ($C_0 = 20$ fF).

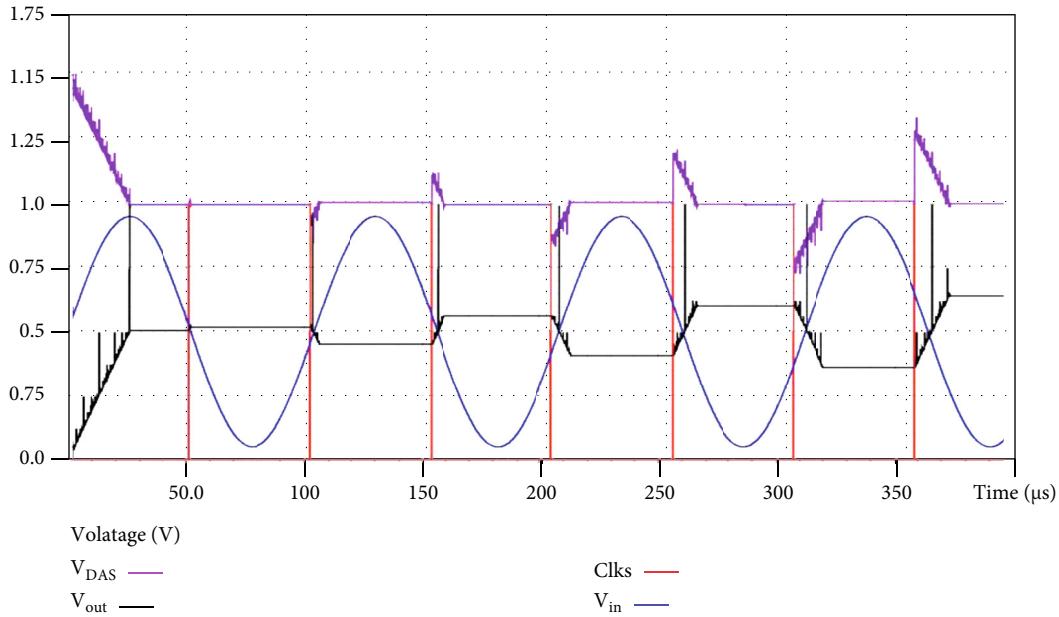

Figure 3: Simulation of the suggested converter with sinusoidal incision.

Table 1: Specifications of the proposed difference converter.

Technology	0.18 μm
Supply voltage	1 V
Sampling frequency	20 kS/s
Input range	1 V
THD	−47.5 dB@f_{in} = 10 kHz
SFDR	55.4 dB@f_{in} = 10 kHz
Power	82 nW@f_{in} = 100 Hz1.155 μW@fin = 10 kHz
ENOB	7.6 bits@f_{in} = 10 kHz
Active area	0.0325 mm^2
FoM	20 fJ/Conv.Step@f_{in} = 100 Hz 304 fJ/Conv.Step@f_{in} = 10 kHz

5. Analysis

5.1. Implementation of Image Sensor Readout Circuit Utilizing WTA. To handle the low power image sensor refresh circuit and decrease conversion time, we can group the pixels of a row or column into some sections due to the total number of pixels in the image and the ability of analog to digital converters as well as WTA circuit capability. In this route, we can convert the pixel amounts of every part into digital by arranging. In this approach, for instance, if we begin from the maximum amount, after finding the highest entry value, we use it to the converter, and until the conversion action is done, WTA circuit will find the highest amount again by deleting the highest entry from other sides. Since the next entry is always smaller than the previous entrance, the changes among consecutive samples will be decreased to the lowest possible state which is firstly optimized in the power consumption and time of the converter activity, and secondly, the conversion time, which is one of the issues of this converter, will be considerably enhanced.

By a thumbnail computation, it can be followed that if, for instance, used among all 8 entrances of this approach, in an image column with 256 pixels, the converter only needs 32 measurement times from 0 to 255. If in the difference gauge converter per pixel, the count may be repeated and this will increase the time by 8 times. Other significant problem is that related to the ordering of entering values; there is the lowest distance between the entrances that will cause a drastic decrease in power consumption. For instance, we have pixel output numbers in set {109, 84, 231, 172, 33, 61, 18, 154}. For normal difference converter, the number of pulses per hour of circuit activity is computed as follows:

$$\sum_{i=1}^{8} \Delta V_i = 109 + (109 - 84) + (231 - 84) + (231 - 172) + (172 - 33) + (61 - 33) + (61 - 18) + (154 - 18) = 686. \quad (6)$$

If the numbers are sorted as {231, 172, 154, 109, 109, 84, 61, 33, 18}, the number of clacks will be computed as follows that indicates about 36% of the savings compared to suggested converter:

$$\sum_{i=1}^{8} \Delta V_i = 231. \quad (7)$$

Besides, it is possible to handle asynchronous operations utilizing data storage per pixel to significantly decrease the conversion time that is one of the issues of suggested

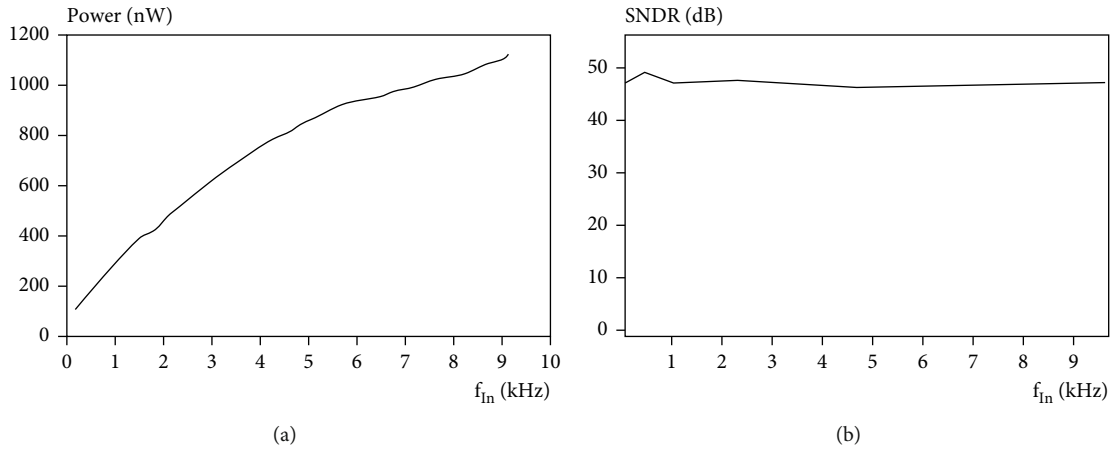

Figure 4: Changes of (a) power and (b) SNDR consumption by changing the entrance frequency of sinusoidal functions.

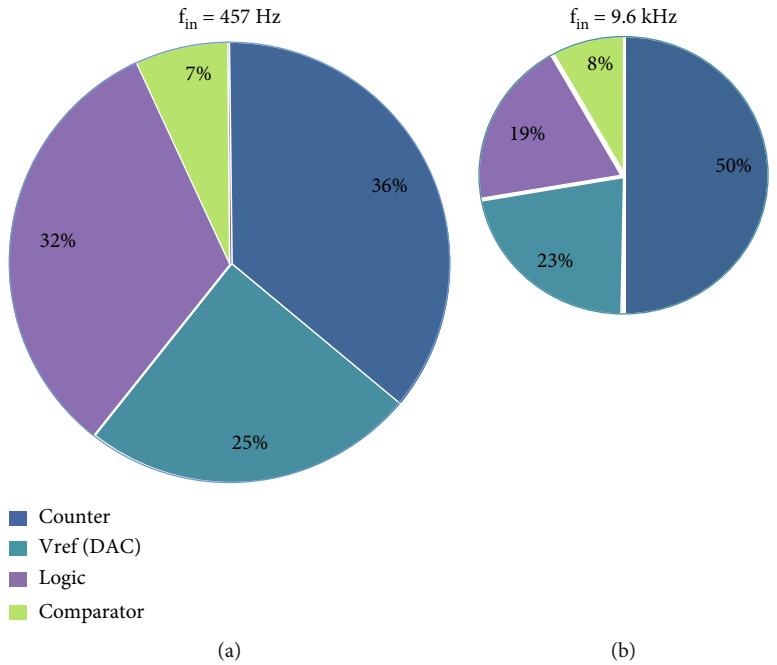

Figure 5: The share of power consumption in various sections of proposed difference converter at input frequency. (a) 457 Hz and (b) 9.6 kHz.

difference converter. Figure 6 indicates the block diagram of suggested system for image sensor readout circuit utilizing a WTA with eight entrances. Each pixel needs a storage circuit to store the value of every pixel in its memory after the measurement so that it can eventually retrieve the image in its primary form.

Regarding the large number of pixels in a row or column, it is usually not possible to process the entire row simultaneously with a WTA circuit and complete the sorting for them. Thus, as a proper solution, some WTA circuits can be applied. Therefore, regarding that the time of converting analog output of every pixel to digital value is a nearly long time compared to the comparison time in the WTA circuit, these two circuits can be utilized in a burst to find the largest input from the evaluated inputs and use it as the next instance to the converter for every analog to digital value conversion. After completing the seventh entry conversion and during the eighth entry conversion, the selector circuit uses the output amounts of next eight pixels to WTA to find the largest of them and use them as the next entry to converter. In this route, without interruption and applying only one WTA circuit, the amounts of all pixels can be used in 8 orders to the difference gauge converter to enhance the overall conversion time by 8 times and also decrease the power of suggested difference gauge converter considerably.

Figure 7 indicates the timeline of this trend. In this figure, it is found that the sample-sampling click signal of every pixel is various from the other and is provided from WTA

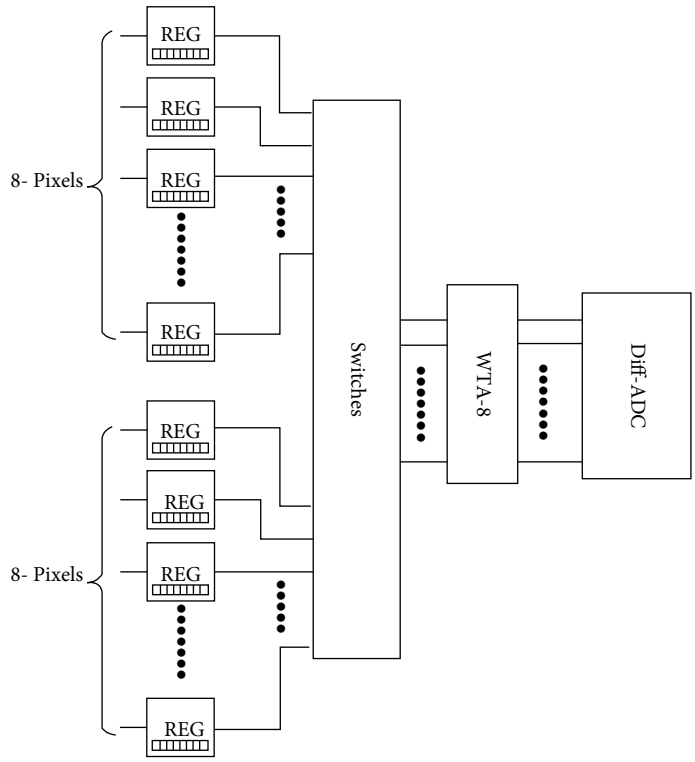

Figure 6: Block diagram of suggested readout circuit utilizing WTA.

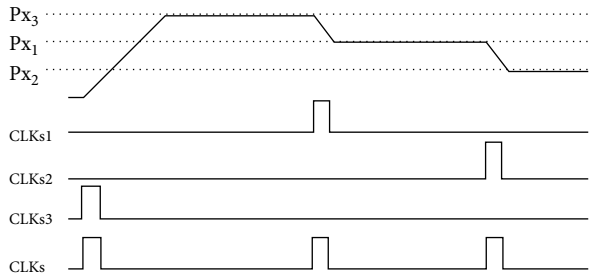

Figure 7: Time diagram of suggested rereading circuit applying WTA.

circuit response. The cost of handling this system is the addition of an eight-entry WTA circuit, a selector circuit, and switch, to the number of pixels in the column, as well as an internal memory per pixel.

As a case study, to survey the power savings in an image, we regard Lena image with dimensions of $512 * 512$. In this image, regarding that the amount of each pixel is identified by an 8-bit digital number, we can check the number of pulses in various modes to convert the value of every pixel to digital.

In the first item, the transducer is presented as an integral catcher, in the second case, the transducer is presented as a conventional SAR converter, in the third case, the difference gauge converter is done, and in the last item, we regard the difference gauge converter applying WTA. By writing the demanded program in MATLAB software and due to the column refresh approach, we compute the number of clacks necessary to estimate the whole image that is proportional to the value of power applied by analog to digital converters to convert the whole image. Table 2 indicates the number of clings required to convert the whole image to digital for four various modes.

As it turns out, to convert the whole image to digital applying a difference converter, at least 16 percent of transducer's activity will reduce compared to a common SAR. If we do the suggested approach of arranging pixels with an 8-entry WTA circuit, transducer activity reduces by about -32% compared to conventional SAR which will be almost twice the first state. This figure will be in addition to almost 8-time conversion rate advancement, which can improve the competency criterion in two dimensions without influencing the speed increase on power consumption. This advancement can be increased if the number of WTA in arrivals increases. For instance, the number reported in the table will be decreased to 1121341 for the number of total activity converted to full image, or WTA 16-entry circuit to 1121341 which shows a -47 percent decrease in circuit activity compared to a common SAR. All these computations are regardless of their additional circuits and power consumption which especially impacts the efficiency of converter.

5.2. Implementation of Maximum Finder Circuit. As noted above, the maximum finder circuits and the minimum finder are the circuits which pass between N inputs used to them the largest and smallest entry to the output or specify the address number of that entry. This circuit, which is a sort of analog input N comparator, is done in various ways and is

Table 2: Number of required clacks to convert the entire Lena image to digital for four various modes.

Converter type	Integrating	SAR	Diff-ADC	Diff-ADC-WTA
Number of clacks necessary to convert to digital	67,108,864	2,097,152	1,775,773	1,431,787

applied in different utilizations like neural networks, image processing and compression, optimization algorithms, and fuzzy control. It is widely applied. WTA circuits are done in two voltage and current approaches and have multiple architectures. One of the most significant of these architectures is the flow-carrying architecture and binary tree architecture which are utilized more than other approaches. Other significant utilization of these circuits is to find edges in images which can be highly utilized in image processing. Another utilizations of these circuits can be found in orbits due to image processing in [1–5].

5.3. Types of WTA Architectures and How They Work Overall. Various sorts of WTA circuits are divided due to how they are done in various ways. In usual, various sorts of WTA circuits can be divided into two general dimensions. In the first classification, WTA circuits are divided into two sorts of voltage and current mode circuits. Thus, other more highly utilized divisions are done due to their implementation sort, which can be divided into three general approaches of implementation. The first approach is the flow carrier approach, which is continuously determined in these circuits using parallel processing and by competing among the final output transistors. A significant characteristics of these circuits is their simultaneous processing which increases the speed on the one hand and decreases accuracy on the other. The maximum locator circuit prepared by Lazaro, which optimizes the power consumption and occupied area, is one of the best structures prepared and in practice is the basis of many circuits prepared for these sorts of circuits. Thus, it is proper for utilizations that do not need high accuracy, and the issue of power consumption is less significant. In this circuit, all entrances are used in a consistent way and applying only two transistors per entry continuously extracts the larger output. The performance of this circuit is done by applying a common node which is the same for all entrances. The two-entry sample of this circuit is indicated in Figure 8(a). Every cell is composed of a flow carrier controlled by flow which is attached to common node A. The number of entrances can simply be increased by adding two transistors per entry. Entrance currents are used to the circuit through a flow source which can be done with a PMOS. The input with the highest value identifies the voltage of node A so that other transistors are almost turned off compared to the transistor attached to the largest input, and all its current is mirrored to the output. Implementation of WTA circuits as binary tree is also one of the common methods for handling these circuits. In this sort of implementation, the entrances are compared two by two and finally the larger entrance is determined. This approach has good accuracy due to two-to-two comparison, but the needed area will be high. In binary tree approach, unlike the flow carrier approach, the competition among all the entrances occurs at the same moment, first, two to two entrances are compared with each other, and then due to the larger entrance in each stage, the winners are compared again two by two to finally identify the largest entrance. These circuits are usually much simpler to handle, but time delays along with their important area are among the disadvantages of these circuits. A binary tree method is very common in entrances with large numbers due to its accuracy depending on the number of entrances. Moreover, suitable function at low power voltages is one of the features of these sorts of WTA's. Figure 8(b) indicates this structure.

Other than these two approaches, other approaches are indicated in Figure 9, the most important of which can be noted as a general section is time-based approach. This approach was much less considered, but applying time-based circuits, these circuits have also been regarded as common implementations for WTA in recent years.

These sorts of circuits are highly consistent to the technology of day and indicate better responses at very low voltages than similar circuits. In these circuits, the input signal, which can be voltage or current, is converted to time lag and then compares the circuit of these delays, and the signal that has less delay indicates the larger signal that is indicated in the output. The main character of these circuits is the speed and accuracy along with their very low power consumption, which can solve the major issue of WTA circuits carrying current and binary trees to some level.

The major issue of these circuits is the conformity of elements. An example of these circuits in Figure 10 indicates one of these circuits. In this circuit, which is utilized in an edge detection circuit in images, the light is made with a flow light proportional to the light of decimal capacitors of each pixel of the image. A simple circuit contains two inverters which also converts the time of this voltage to the inverter threshold into a pulsed edge, which is delayed proportional to the amount of light. This approach identifies the largest signal.

5.4. WTA Circuit due to Proposed Time. To decrease the power consumption of time-based WTA circuit shape indicated in Figure 10(a), it is proposed for $N = 4$. Every WTA circuit with input N consists of N voltage-controlled delay line circuit that strengthens the delay circuit produced proportional to the inputs and increases the accuracy of comparison among the inputs. This structure is inspired by VCDL structure presented in [16], which was utilized for applying in a time-based comparator. The task of this circuit is to strengthen the created delay due to entering value. In WTA circuit, all entrances are required to delay and reinforce these delays. Thus, instead of the phase detector applied in the comparator, we require a circuit which can

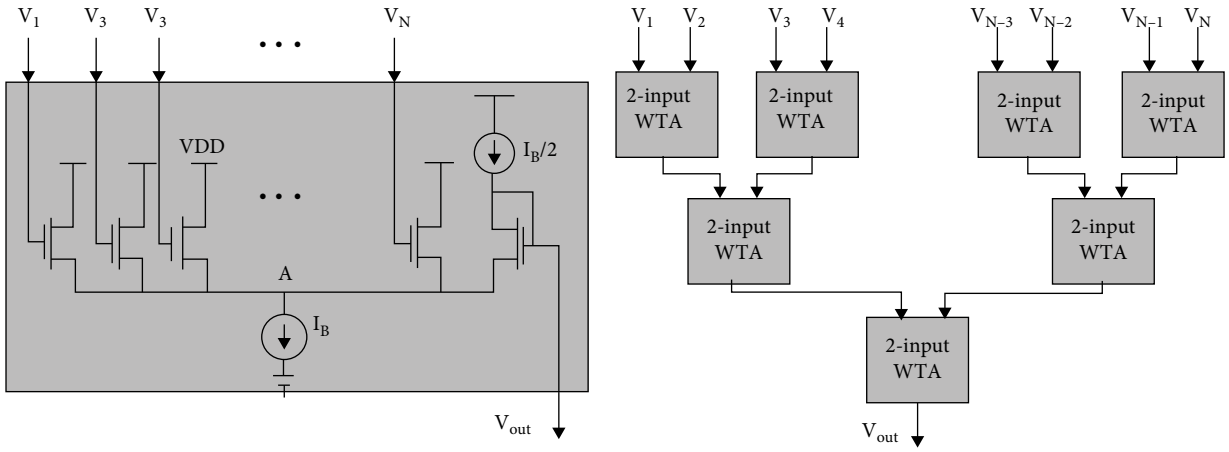

Figure 8: (a) Maximum finder circuit showed in [16]. (b) Implementation of WTA by binary tree approach.

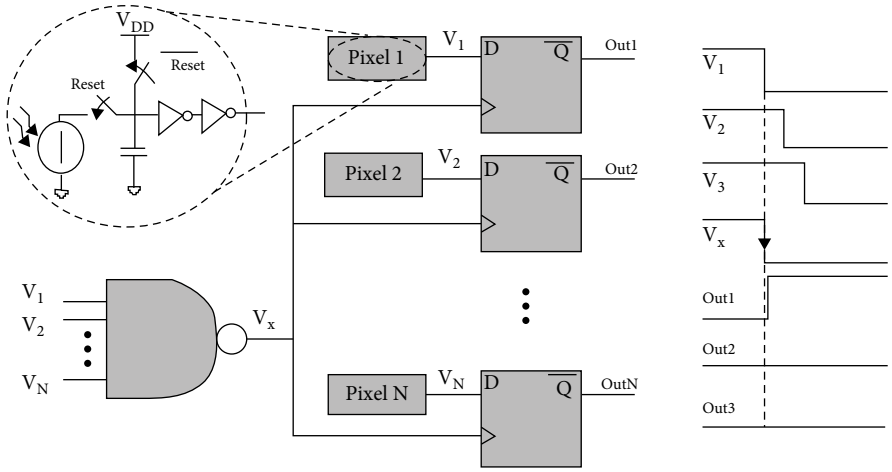

Figure 9: Time-based WTA circuit presented [16].

find among signals with various signal delays that have come faster. For this work, due to the figure, NAND circuit with input N is used in which using the positive feedback of NAND output; each branch has feedback to NAND input of all branches. By this approach, because the delay is less than the larger input signal, the output is equivalent to the larger input signal to the VDD, which causes zero of one of the inputs of other NANDs.

Thus, with one of the outputs, other outputs are directed toward zero. Hence, only one of the outputs will always be active. Figure 10(b) indicates how the circuit performed with the time diagram.

However, in Figure 11, circuit is applied to handle VCDL. This circuit, which is somewhat similar to what is presented in [16], is composed of a controlled delay line. Because, in the structure of this circuit, the common voltages of inputs are not known to us, the voltages are not compared to a given voltage. Thus, we cannot apply NMOS and PMOS transistors to control the flow at the same time, because at high voltages PMOS and at low voltages NMOS will be turned off. Regarding that we are looking for an entry with the highest voltage, PMOS transistors can be removed and utilized in the delay line as one among the NOT gate.

Because this decreases delay reinforcement rate and we have to double the classes to advance it, we have utilized an alternative approach. In suggested VCDL with a mirror, the input voltage current is inversely used to PMOS transistors (see Figure 12).

By this approach, flow control is correctly handled and there is no requirement to add classes. This also increases the working range of input voltage up to the amount of power voltage. On the other hand, to decrease the static power consumption with an NMOS key controlled by entrance clack, the current passes through the flow mirror in only half of the frequency period of the clack and does not consume any flow in the other half period when the circuit is reset.

5.5. Simulation and Locating of Proposed WTA. For the test integrity of the suggested WTA circuit and its better

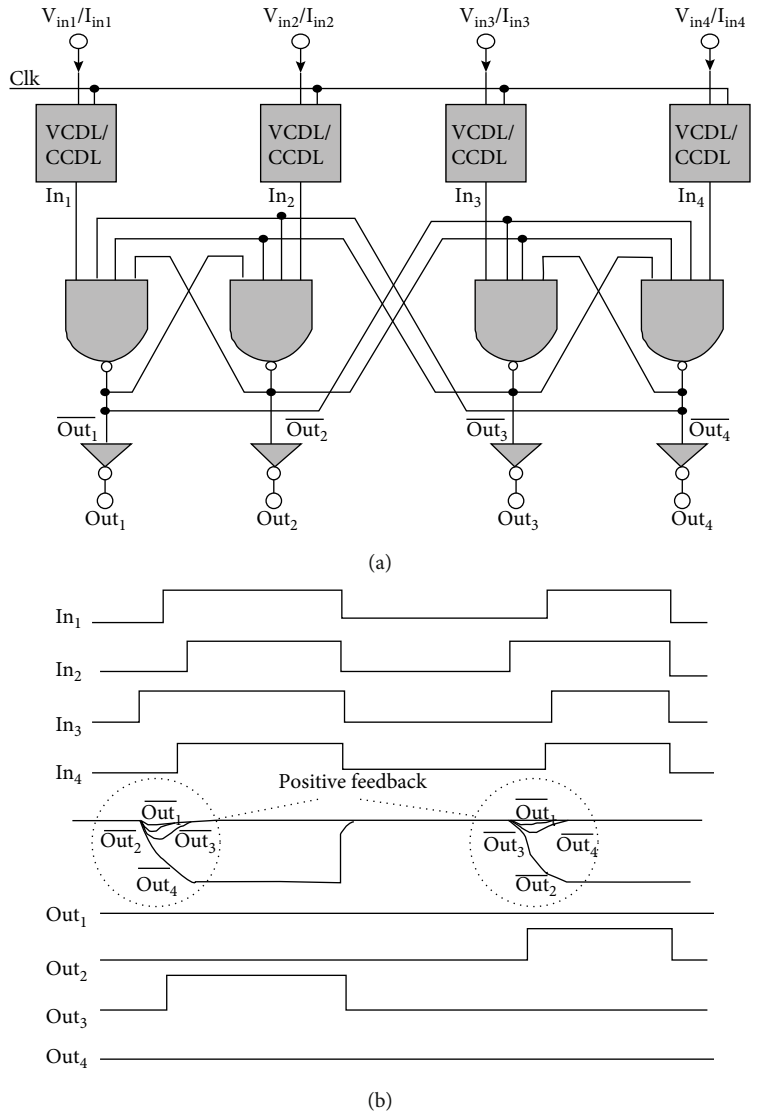

Figure 10: (a) WTA circuit due to suggested time. (b) Proposed WTA time diagram.

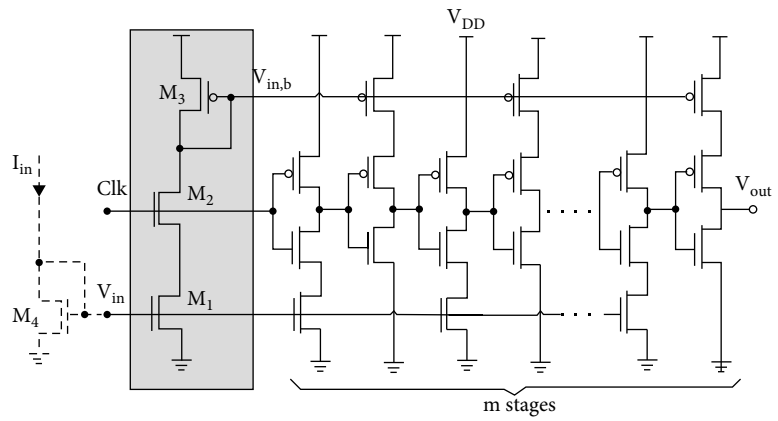

Figure 11: Proposed VCDL circuit for time-based WTA.

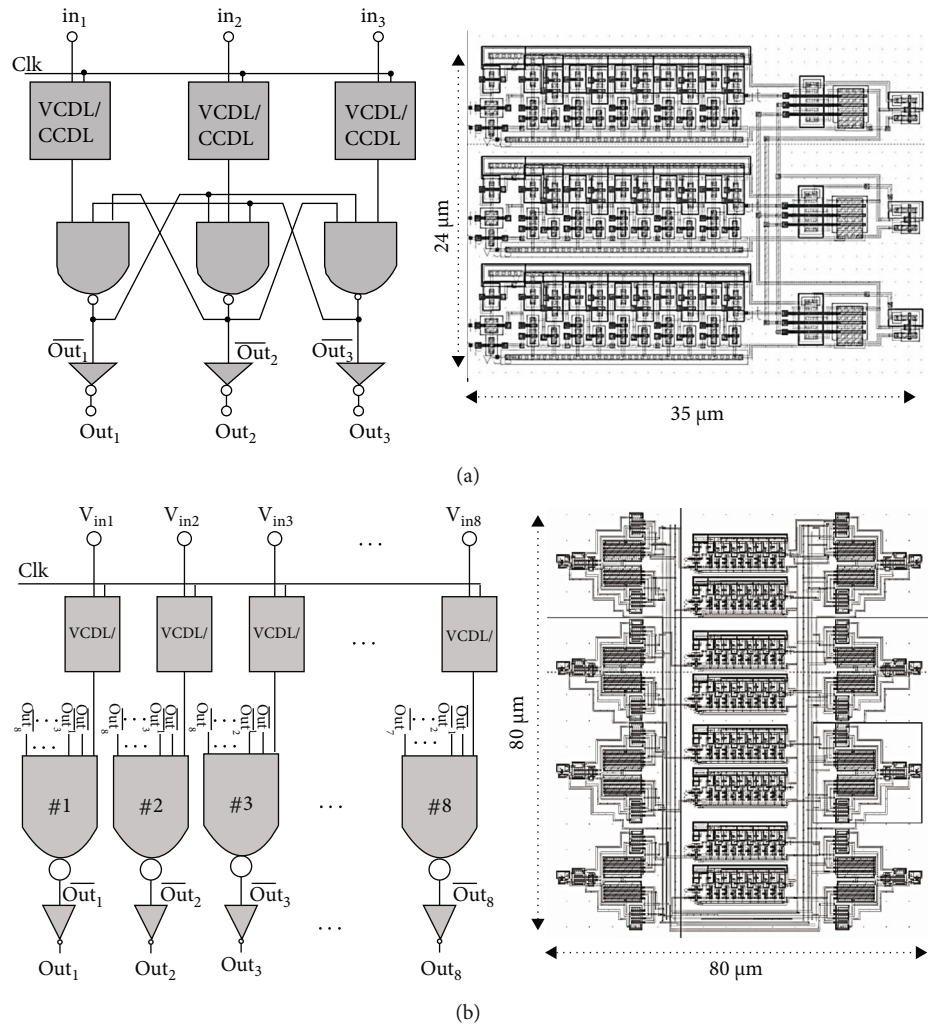

Figure 12: WTA circuit design suggested (a) three entrances and (b) eight entrances.

function than the present samples, two sorts of WTA 3 and 8 entrances were designed and done. Figure 13 indicates the circuits of these designs along with their life. WTA dimensions were provided in three entrances at $224 \times 35\,\mu$m and in eight entrances at $280 \times 80\,\mu$m. The design for 0.5 mV accuracy for 0.5 V and 1 mV feeding for 1 V feed was carried out for three and eight entry modes, respectively.

Figure 14 indicates the time waves of the applied sinusoidal inlets, along with the outputs of each floor and part of the VCDL circuit output. This form shows the correct answer to the change of the largest entrance. Moreover, how to alter the output of every VCDL circuit is specified in the section of the time. Figures 14(a) and 14(b) show diagrams of delay and power consumption of WTA circuit indicating three inputs for various winning voltages (the largest input) and altering the voltage value of the power. The delay chart is plotted due to the drastic changes in the delay chart. These diagrams indicate that firstly the greatest delay and power consumption is related to the state where the winning voltage has small values, which shows that all the inputs are small. Thus, from about half the power voltage for delay and about 0.3 V for power consumption, the diagrams do not show much change. Hence, the scope of WTA work and its working frequency create a give-and-take which is identified by a designer. Table 3 also indicates the general features of three-input WTA circuit for the working frequency of 1 MHz and the power voltage of 0.5 V in different corners of technology. The power and delay provided for winning voltage are about half the power voltage, and a computed dynamic range is acceptable for the mentioned work frequency (1 MHz). Since these sorts of analog circuits behave similarly to comparators, they need Monte-Carlo analysis to find the offset value. To measure the offset rate, Monte-Carlo simulation was done for three various modes of delay chain transistors, in which Figure 15 indicates the results of this analysis. The standard deviation value in these three cases was 23 mV, 10 mV, and 4.5 mV, respectively, which indicates that we require a higher area to achieve high accuracy. To compare WTA circuit presented with existing ones, we utilize the equation (8) as a competency criterion.

$$\text{FoM} = \frac{f * N}{\text{Power}}. \tag{8}$$

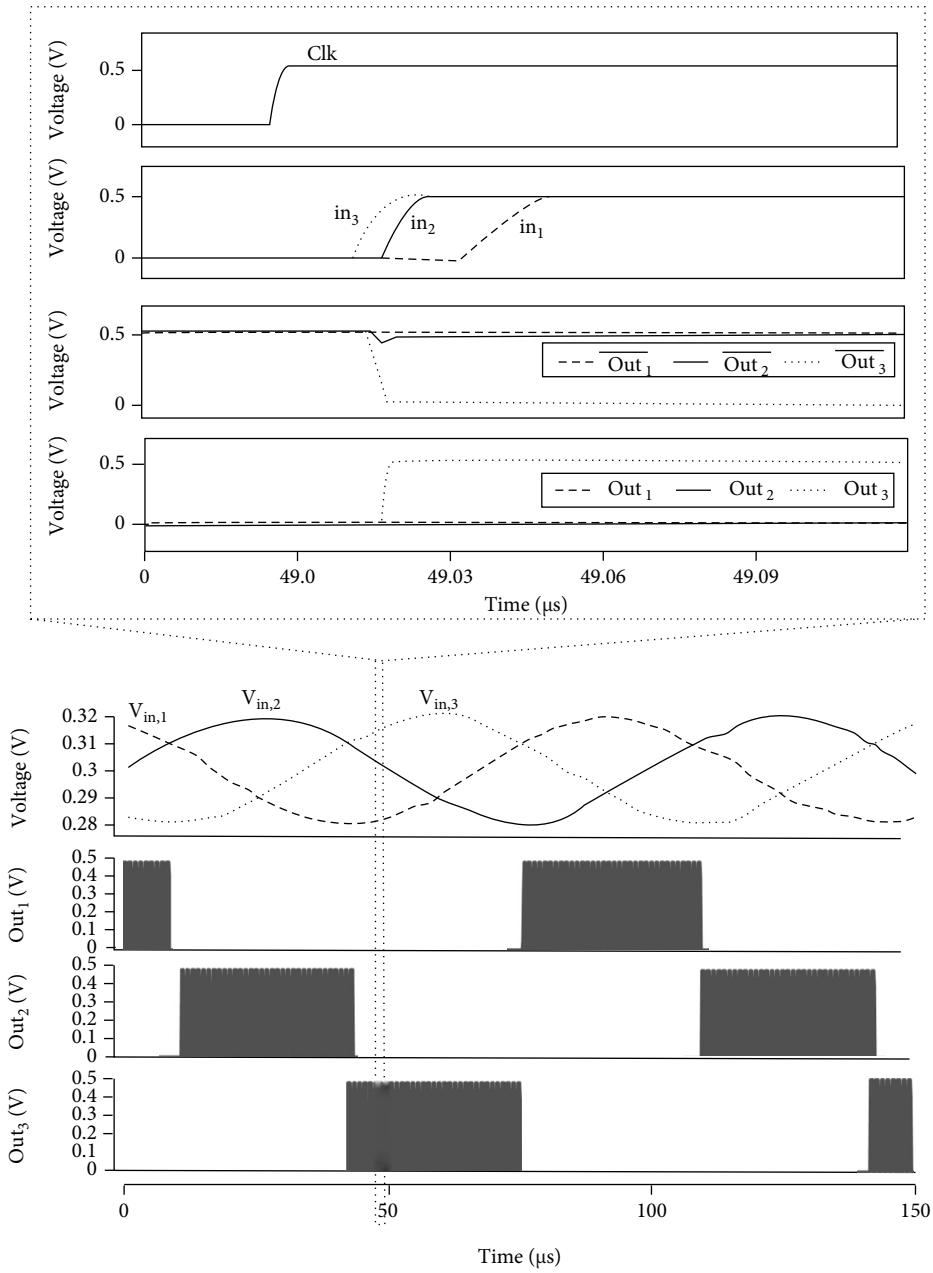

Figure 13: Input and output time diagram of three-entry MEDA with section of VCDL circuit output.

In this regard, f is the maximum working frequency, N is the number of inputs, and power is also the value of power consumed by the circuit. Table 4 makes a comprehensive comparison among existing samples of these circuits with different implementations and suggested WTA. Due to the provided results, the suggested WTA circuit has the best competency criteria among various reports.

5.6. Simulation of Proposed Difference Converter Applying Suggested WTA. The objective of designing and suggesting WTA circuit was to make optimal utilization of analog to digital difference converter structure. At present, applying novel WTA circuit, this sort of readout circuit can be optimally done. In order to implement this circuit, a control circuit is required to take the measured entrance out of the circuit after the conversion and then apply the larger entrance among the remaining entrances to the difference converter entrance. On the other hand, due to the refresh circuit system provided, there is a requirement for a registry to record the data provided for every pixel to store the amount of each pixel. Figure 16 indicates the outline of the simulated circuit for state $N = 3$. Furthermore, the time simulation of this circuit and how to convert the amount of three various entrances are indicated in Figure 17. As shown in the figure, the desired values in different time pulses create analog values and track based on the amount of pixels

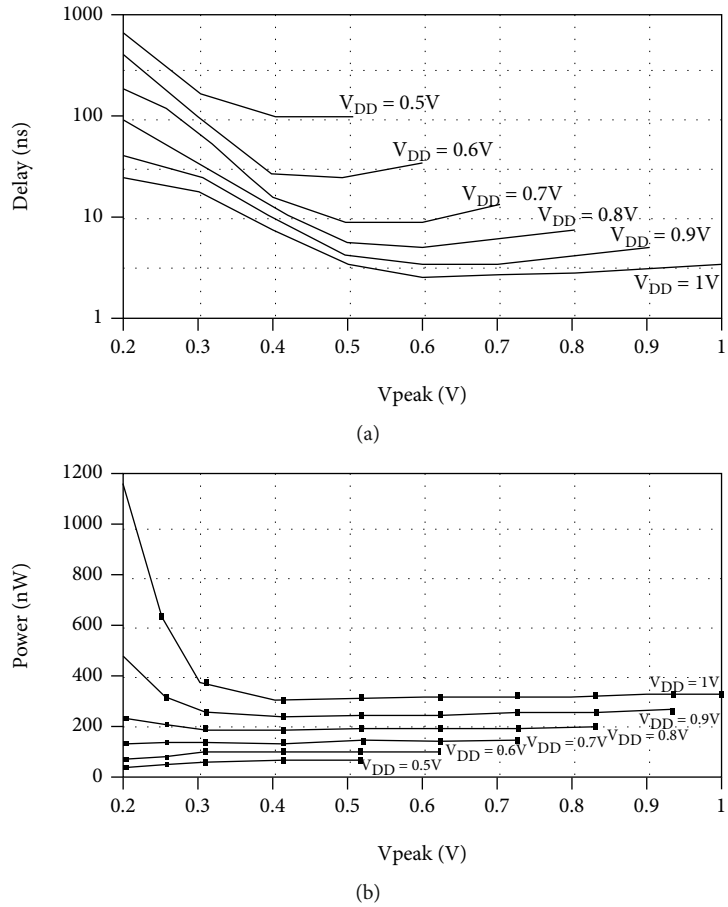

Figure 14: Changes of (a) delay and (b) power consumption due to the winning voltage changes for different power voltages.

Table 3: WTA specifications of three suggested inputs in MHZ working frequency and 0.5 V power voltage in different corners of technology.

	TT	SF	FS	FF	SS
Power (nW)	150	72	350	800	55
Delay (nS)	6	42	3	1.7	54
Dynamic range (V)	V_{DD}-0.2	V_{DD}-0.39	V_{DD}-0.37	V_{DD}-0.13	V_{DD}-0.41

measured. The tracking error in this test sample is calculated to be 0.01 V. This figure is simulated with the aim of showing the results of Figure 7, which has been able to achieve its goals well, and the sampling click signal from each pixel is different from the other pixels and is provided by the response of the WTA circuit. The cost of managing this system is to add a WTA circuit with 8 inputs, a circuit, and a selection key, to the number of column pixels as well as an internal memory per pixel.

As can be observed from the simulation, the order of converting entrances is due to the largest value to the smallest value. This conversion approach, as noted above, decreases the overall conversion time, as well as decreases the power consumption of readout circuit. The work approach is such that first, by identifying the largest entry, the sampling pulse corresponding to the larger entrance is activated and connects the inbox to the desired pixel.

Besides, to get this entry out of the next computations, a flip-flop D was placed to zero the entry corresponding to the winning value of the previous period or to disconnect the switch. In the next sampling pulse, the same process is repeated without the converted entrance in the previous period. Simulations also indicate that if we can have a WTA circuit with more entrances, more power will be saved. On the other hand, since only one difference gauge converter is applied to convert the output amounts of all pixels to digital, there is no requirement to apply a large number of WTA and we can implement this refresh circuit with only one maximum finder circuit and very low power. The added control circuit power is visible in Table 5.

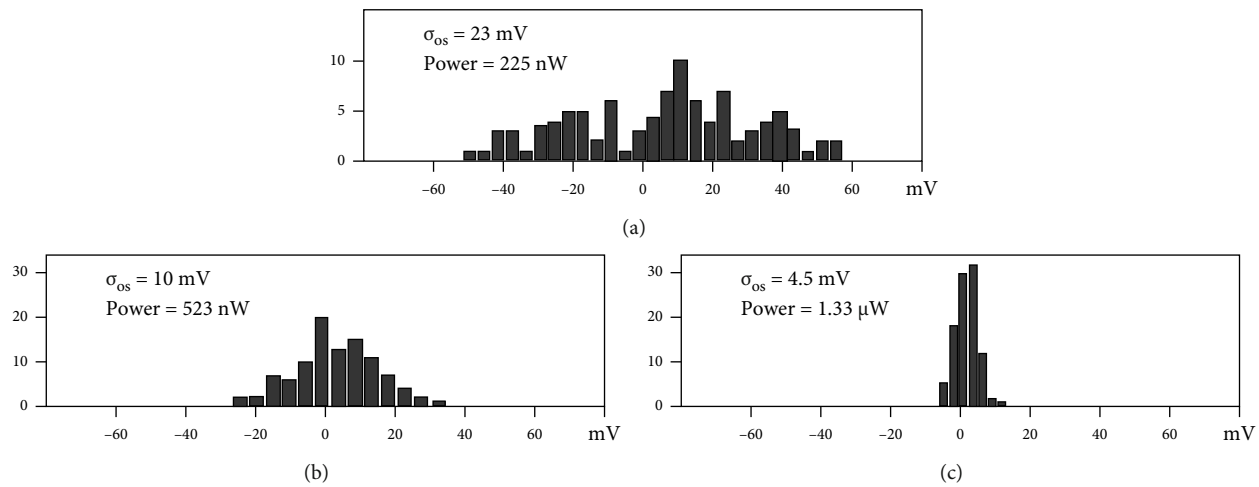

Figure 15: Suggested WTA circuit offset voltage distribution for various sizes of delay chain transistors. (a) $W = 0.25\,\mu$m, (b) $W = 2\,\mu$m, and (c) $W = 5\,\mu$m.

Table 4: Comparison between suggested WTA circuit and samples presented in recent years.

Paper	[17]	[18]	[19]	[20]	[21]	[22]	This work		
Technology	0.18 μm	0.18 μm	0.18 μm	0.35 μm	0.18 μm	0.13 μm	0.18 μm	0.18 μm	0.18 μm
Supply voltage (V)	1.8	1	0.8	2.5	1	0.5	0.5	0.5	1
No. of inputs	8	8	8	3	4096	8	3	8	8
Precision (%)	96.4	99	99.5	99.6	99.9	—	99.95	99.8	99.9
f_{max}(MHz)	29	3.5	0.383	10	10	10	1.75	1.66	10
Power per input (μW)	20	10	0.36	—	—	—	0.045	0.031	0.24
FoM (μW/MHz)	0.77	2.85	0.93	—	—	0.075	0.025	0.018	0.024
Type	CC*	BT**	BT	CC	Time based	LDO	Time based		
Measurement/simulation	Measurement	Simulation	Measurement	Simulation	Measurement	Simulation	Postlayout simulation		

*Current conveyor: a current conveyor is an abstraction for a three-terminal analogue electronic device. It is a form of electronic amplifier with unity gain. There are three versions of generations of the idealized device, CCI, CCII, and CCIII. **Binary tree.

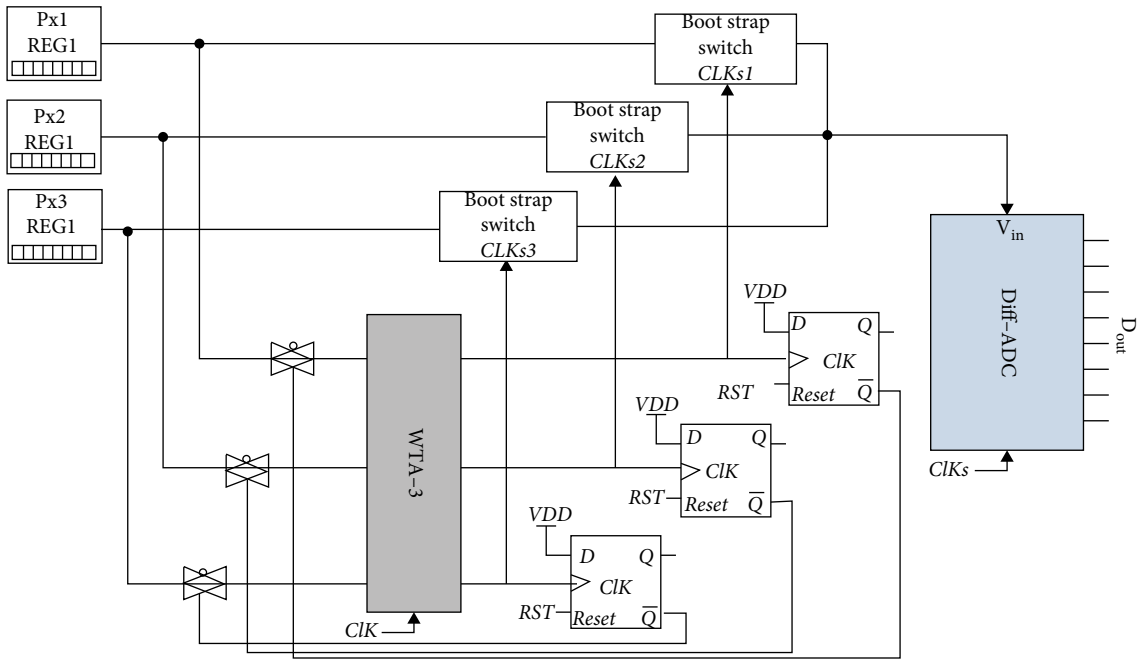

Figure 16: Outline of the rereading circuit applying WTA 3-entry.

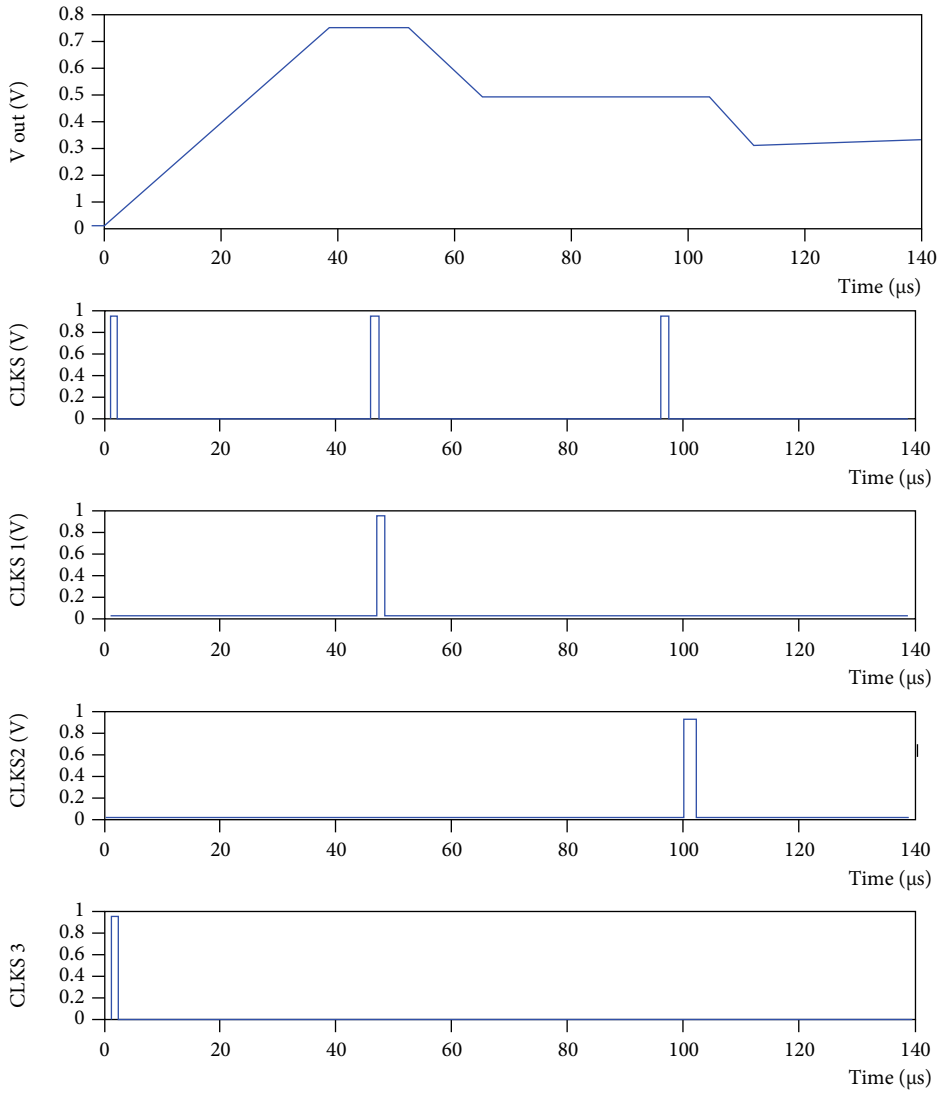

Figure 17: Simulation of the difference gauge converter applying WTA sorting.

Table 5: Power consumption of various sections of the control circuit added to the difference gauge converter per pixel.

	DFF	BSS	REG	WTA	TG
Power (nW)	9.2	1.9	11.4	7.1	0.05

6. Conclusion

Image sensors are one of the most highly applied electronic systems and one of the growing industries among various electronic devices. Thus, since an important section of image sensors involves the readout circuit and its lateral circuits, decreasing the power consumption of this section can effectively decrease the power consumption of entire image sensor. In this study, this problem was regarded, and on this basis, it was attempted to prepare an approach to decrease the power consumption of this sector. As we know, an important section of the image sensor rereading circuit is related to analog to digital converters, which have a large share of the total power of the image sensor in both the number and the amount of power consumption. A significant section of this study is dedicated to present an analog to a digital converter to compute the difference among sequential samples. This novel approach of converting analog to digital signals can be applied for all signals with low difference features among sequential samples. In the suggested converter, almost all the issues and disadvantages of previous implementation approaches have been resolved or improved. Furthermore, the desired converter was designed and implemented in 0.18 μm technology, resulting in 1 V power voltage and 5 MHz pulse frequency; the result for the power consumption of suggested converter, for the corresponding input of a standard photo, is equal to 224 nW, which is about 80% compared to the power of the converter with the input of the entire sinus scale. On the other hand, the criterion of competence of the converter made with low sine input ($f_{in} = 100$ Hz) of 42 fJ/CS was prepared.

Moreover, the power of the converter for heart signal input was tested, in which the power consumed at the sampling frequency of 10 kS/s and 1 kS/s was 114 nW and 18 nW, respectively, which indicated an important decrease in power.

Since one of the most significant issues of analog to digital converter is its suggested conversion speed, a novel rereading approach was suggested to make suggested approach more efficient in decreasing power on the one hand and increasing the conversion rate on the other hand. In this rereading approach, applying a new structure with very low power consumption for maximum finder circuits, these circuits were utilized to arrange the pixel values of an image so that by counting from the maximum value to the minimum amount of inputs, all the pixels connected to the maximum finder were converted. By this approach, the number of inputs in the maximum circuit finder increases the conversion rate, and also, the power consumption of the converter is significantly decreased compared to a normal suggested mode. The suggested approach for rereading the image for a limited number of pixels was designed and simulated, showing a significant power reduction compared to a suggested state which depends on the pixel values.

Data Availability

The data used to support the findings of this study are available from the corresponding author upon request.

Conflicts of Interest

The authors declare that they have no conflicts of interest.

References

[1] G. G. Gielen, L. Hernandez, and P. Rombouts, "Time-encoding analog-to-digital converters: bridging the analog gap to advanced digital CMOS-part 1: basic principles," *IEEE Solid-State Circuits Magazine*, vol. 12, no. 2, pp. 47–55, 2020.

[2] H. Liu, M. Liu, Z. Zhu, and Y. Yang, "A high linear voltage-to-time converter (VTC) with 1.2 V input range for time- domain analog-to-digital converters," *Microelectronics Journal*, vol. 88, pp. 18–24, 2019.

[3] E. Santin, L. B. Oliveira, and J. Goes, "Built-in self test of high speed analog-to-digital converters," *IEEE Instrumentation & Measurement Magazine*, vol. 22, no. 6, pp. 4–10, 2019.

[4] R. Magerramov and V. Zaitsev, "Design and analysis of a VCO for implementing an analog to digital converter based on PLL in 0.25-um CMOS technology," in *2020 IEEE Conference of Russian Young Researchers in Electrical and Electronic Engineering (EIConRus)*, pp. 2307–2311, St. Petersburg and Moscow, Russia, 2020.

[5] I. Chakraborty, A. Agrawal, and K. Roy, "Design of a low-voltage analog-to-digital converter using voltage-controlled stochastic switching of low barrier nanomagnets," *IEEE Magnetics Letters*, vol. 9, no. 2018, pp. 1–5, 2018.

[6] M. Müller, S. Ausländer, A. Spinnler et al., "Designed cell consortia as fragrance-programmable analog-to-digital converters," *Nature Chemical Biology*, vol. 13, no. 3, pp. 309–316, 2017.

[7] P. Harpe, "Ultra-low power analog-digital converters for IoT," in *Enabling the Internet of Things*, pp. 361–383, Springer, 2017.

[8] R. Machado, J. Cabral, and F. S. Alves, "All-digital time-to-digital converter design methodology based on structured data paths," *IEEE Access*, vol. 7, pp. 108447–108457, 2019.

[9] F. Mehdizadeh, M. Soroosh, H. Alipour-Banaei, and E. Farshidi, "All optical 2-bit analog to digital converter using photonic crystal based cavities," *Optical and Quantum Electronics*, vol. 49, no. 1, p. 38, 2017.

[10] S. Jhung, K. Ko, M. Lee, S. Cho, G. Cho, and I. Kwon, "Radiation-hardened successive approximation register analog-to-digital converter," in *2020 International Conference on Electronics, Information, and Communication (ICEIC)*, pp. 1-2, Barcelona, Spain, 2020.

[11] J. Song, S. Tian, Y.-H. Hu, and P. Ye, "Digital iterative harmonic rejection and image cancellation for LPF-less frequency-interleaved analog-to-digital converters," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 66, no. 12, pp. 2072–2076, 2019.

[12] J. Nie, G. Hu, L. Li, and Y. Zhang, "Piezotronic analog-to-digital converters based on strain-gated transistors," *Nano Energy*, vol. 46, pp. 423–427, 2018.

[13] M. Saberi and R. Lotfi, "Segmented architecture for successive approximation analog-to-digital converters," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 22, pp. 593–606, 2014.

[14] S. Chen, L. Wang, H. Zhang, R. Murugesu, D. Dunwell, and A. C. Carusone, "All-digital calibration of timing mismatch error in time-interleaved analog-to-digital converters," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 25, no. 9, pp. 2552–2560, 2017.

[15] M. H. Sani, S. Khosroabadi, and A. Shokouhmand, "A novel design for 2-bit optical analog to digital (a/D) converter based on nonlinear ring resonators in the photonic crystal structure," *Optics Communications*, vol. 458, article 124760, 2020.

[16] J. Lazzaro, S. Ryckebusch, M. A. Mahowald, and C. A. Mead, *Winner-Take-All Networks of O (n) Complexity*, California Institute of Technology, 1988.

[17] T. Talaska, M. Kolasa, R. Długosz, and P.-A. Farine, "An efficient initialization mechanism of neurons for winner takes all neural network implemented in the CMOS technology," *Applied Mathematics and Computation*, vol. 267, no. 15, pp. 119–138, 2015.

[18] M. Rahman, K. Baishnab, and F. Talukdar, "A high speed and high resolution VLSI winner-take-all circuit for neural networks and fuzzy systems," in *2009 International symposium on signals, Circuits and Systems*, pp. 1–4, Iasi, Romania, 2009.

[19] R. Ł. DŁugosz and T. Talaśka, "Low power current-mode binary-tree asynchronous Min/Max circuit," *Microelectronics Journal*, vol. 41, no. 1, pp. 64–73, 2010.

[20] A. Naderi Saatlo and S. Ozoguz, "CMOS high-precision loser-take-all circuit," *IEEJ Transactions on Electrical and Electronic Engineering*, vol. 9, no. 6, pp. 695-696, 2014.

[21] F. Pardo, C. Reig, J. A. Boluda, and F. Vegara, "A 4K-input high-speed winner-take-all (WTA) circuit with single-winner selection for change-driven vision sensors," *Sensors*, vol. 19, no. 2, p. 437, 2019.

[22] M. A. Akram, I. C. Hwang, and S. Ha, "architectural advancement of digital low-dropout regulators," *IEEE access*, vol. 8, pp. 137838–137855, 2020.