Epitaxial growth of silicon nanowires using an aluminium catalyst

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Silicon nanowires have been identified as important components for future electronic and sensor nanodevices[1]. So far gold has dominated as the catalyst for growing Si nanowires via the vapour–liquid–solid (VLS) mechanism[2–5]. Unfortunately, gold traps electrons and holes in Si and poses a serious contamination problem for Si complementary metal oxide semiconductor (CMOS) processing. Although there are some reports on the use of non-gold catalysts[6–9] for Si nanowire growth, either the growth requires high temperatures and/or the catalysts are not compatible with CMOS requirements. From a technological standpoint, a much more attractive catalyst material would be aluminium, as it is a standard metal in Si process lines. Here we report for the first time the epitaxial growth of Al-catalysed Si nanowires and suggest that growth proceeds via a vapour–solid–solid (VSS) rather than a VLS mechanism. It is also found that the tapering of the nanowires can be strongly reduced by lowering the growth temperature.

Semiconductor wires, in particular Si nanowires, have been studied for more than forty years[10]. Si nanowires can be synthesised by coating a Si substrate with a thin Au film and annealing the substrate in a vacuum chamber to obtain Au–Si catalyst particles. When a vapour-phase Si precursor is introduced at a substrate temperature above the eutectic point (that is, the lowest temperature at which the Au–Si mixture will melt, see Fig. 1), the catalyst particles become supersaturated with Si and crystalline Si nanowires will nucleate out of the melt and grow. In this vapour–liquid–solid (VLS) growth mechanism, proposed by Wagner and Ellis[10], the Au catalyst particle, located at the tip of the nanowire, is in a liquid state during growth. This liquid particle serves as the preferential site for adsorption of the Si from the vapour precursor species.

In addition to VLS growth, vapour–solid–solid (VSS) growth via a solid catalyst particle is also possible. VSS growth has been reported for $TiSi_2$-catalysed Si nanowires[11], SiO_x-catalysed InAs[12] and Au-catalysed InAs[13] and GaAs[14] nanowires. The question of whether Au-catalysed GaAs nanowire growth should be described by the VLS or the VSS mechanism is in dispute[14,15]. However, note also that in this context a mixed liquid–solid phase exists in the Au–Ga phase diagram (9–20% Ga, at 540 °C; ref. 16). Thus, in addition to VLS and VSS growth, a third possible growth mode, via a partly liquid, partly solid catalyst particle, has to be taken into account.

In this paper, we use an ultra-high vacuum chemical vapour deposition system to grow Si nanowires epitaxially on a Si (111) substrate using Al catalyst particles. Figure 1 shows the Al-rich part of the Al–Si binary phase diagram. As indicated therein, two different growth modes are possible depending on temperature: VLS and VSS. For VLS growth, the growth temperature has to be higher than the eutectic temperature of 577 °C so that the Al–Si catalyst particle is liquid. Due to the supersaturation of Si in the droplet, the position in the phase diagram will be on the right-hand side of the liquidus line, as indicated in Fig. 1. Al-catalysed non-epitaxial VLS growth of Si wires has been reported by Osada *et al.*[17] and Whang *et al.*[18], even though Al as the catalyst for Si nanowire growth has proven to be difficult[19]. In addition to the VLS growth of Si nanowires, VSS growth using temperatures below 577 °C also may be possible. In this case, the catalyst particle remains in its solid α-Al phase (Fig. 1). The Al-catalysed VSS Si nanowire growth is similar to the Al-mediated solid-phase epitaxy (SPE), by means of which epitaxial Si layers can be produced in the temperature range 350–525 °C (ref. 20, 21).

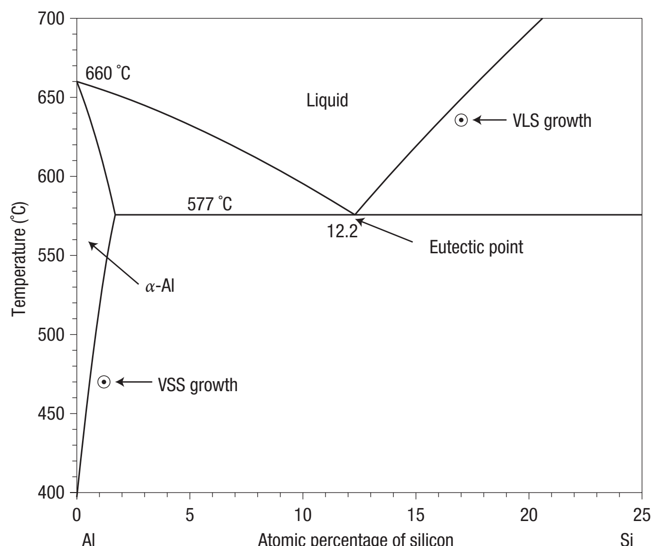

Figure 1 **Schematic of the Al-rich region of the Al–Si binary phase diagram (data from ref. 16).** VLS and VSS are indicated for arbitrarily chosen temperatures.

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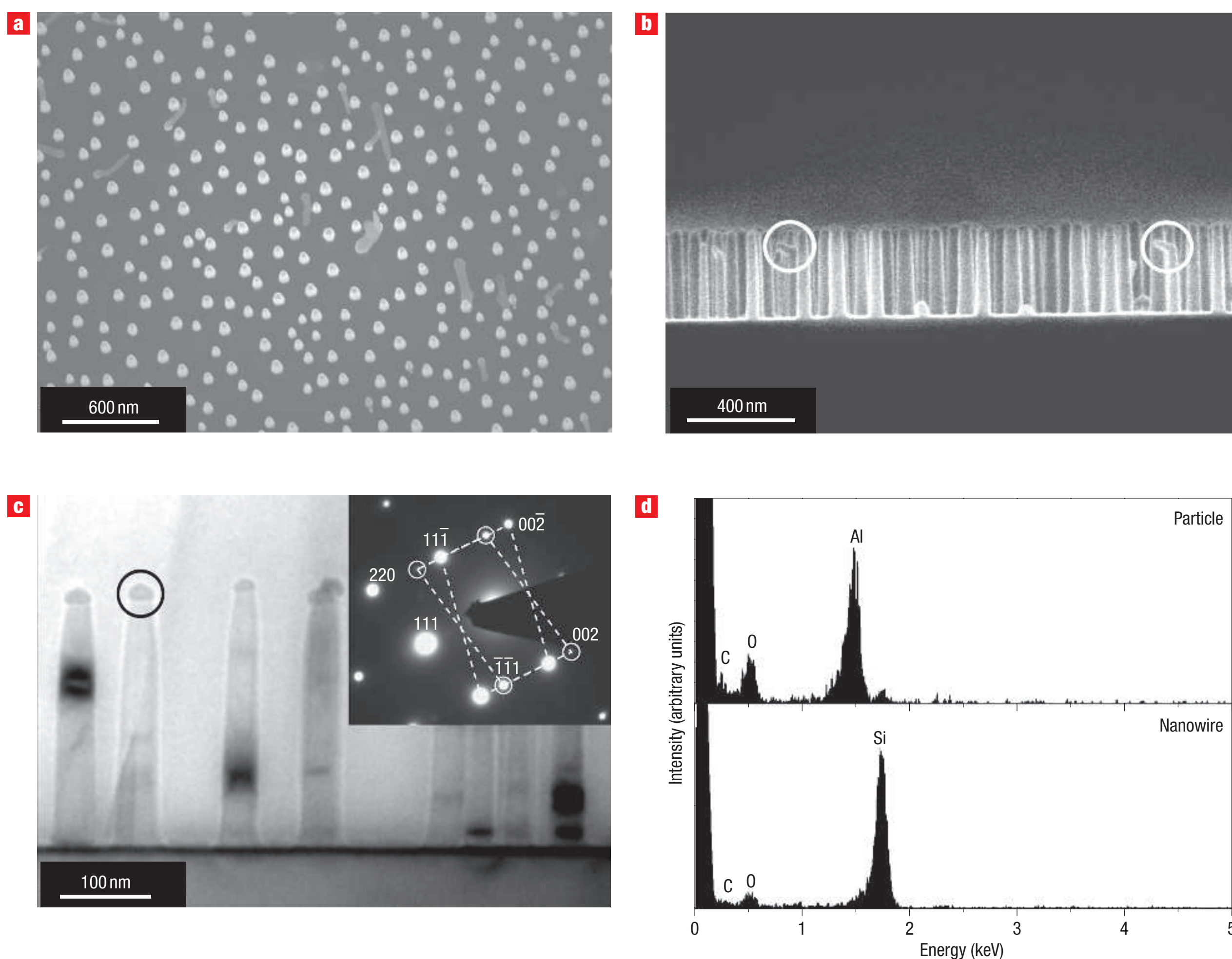

Figure 2 Characterization of the epitaxially grown Si nanowires. a, Top-view SEM image of the nanowires grown on the Si (111) substrate. **b**, Cross-sectional image of the sample shown in plane view. **c**, TEM and SAED pattern (inset) taken with the electron beam parallel to the $[\bar{1}\bar{1}2]$ and $[1\bar{1}0]$ directions of the Si (111) substrate, respectively. **d**, EDS spectra taken from the particle and nanowire, respectively.

Note that in contrast to VSS growth, where a gaseous Si precursor is used as the Si source, a solid Si layer serves as the Si source for SPE. Both processes, SPE and VSS, occur in the same region of the phase diagram, and in both cases Si has to diffuse through a layer/particle of solid Al. Compared with the VLS growth mode, the Al-catalysed VSS growth of Si nanowires offers two major advantages. First, the growth temperature can be lowered to the technologically important regime below 500 °C, and second, the solubility of Si in the catalyst particle is reduced by about one order of magnitude. This low Si solubility of about 2% might become decisive if, for example, Si–Ge heterostructure nanowires with sharp interfaces are to be produced.

Figure 2 shows scanning electron microscopy (SEM) and transmission electron microscopy (TEM) images of well-aligned Si nanowires grown on a Si (111) substrate using Al catalyst particles. The first step of the nanowire synthesis is the room-temperature deposition of an Al film onto the hydrogen-terminated silicon substrate followed by the annealing of the substrate at 580 °C for 20 min. Upon annealing, the Al film breaks up into a distribution of Al–Si alloy particles. After the annealing, the temperature is lowered to the growth temperature of 465 °C. According to Fig. 1 this temperature reduction should, assuming the catalyst particles have been liquid during annealing, cause a solidification of the Al–Si alloy particles. A considerable reduction of the eutectic temperature due to size effects is not expected, as these only become significant for diameters less than 10 nm (ref. 22), whereas the catalyst particles in our experiment typically have diameters of ~35 nm. The resulting nanowires grow preferentially along the [111] direction perpendicular to the substrate surface. This can best be inferred from the top-view SEM image (Fig. 2a), in which nanowires that grow vertically from the (111) substrate are projected along their length as spots. The [111]-directed growth can also be seen in Fig. 2b, which shows an SEM image of the cross-section. Note that only a very small percentage of the nanowires initially grown along the [111] direction perpendicular to the substrate are kinked (white circles in Fig. 2b) particularly compared with the ~30% of kinked wires typically present if Au-catalysed wires of comparable diameters are grown at comparable temperatures[23,24].

The TEM image shown in Fig. 2c reveals that the nanowires are slightly tapered. The catalyst particles at the nanowire tip are clearly visible in Fig. 2c (black circle). In addition, the inset of Fig. 2c shows a selected area electron diffraction (SAED) pattern of one individual Si nanowire. The two sets of diffraction spots visible in the SAED pattern reveal that this particular Si nanowire contains a twin. X-ray energy dispersive spectroscopy (EDS)

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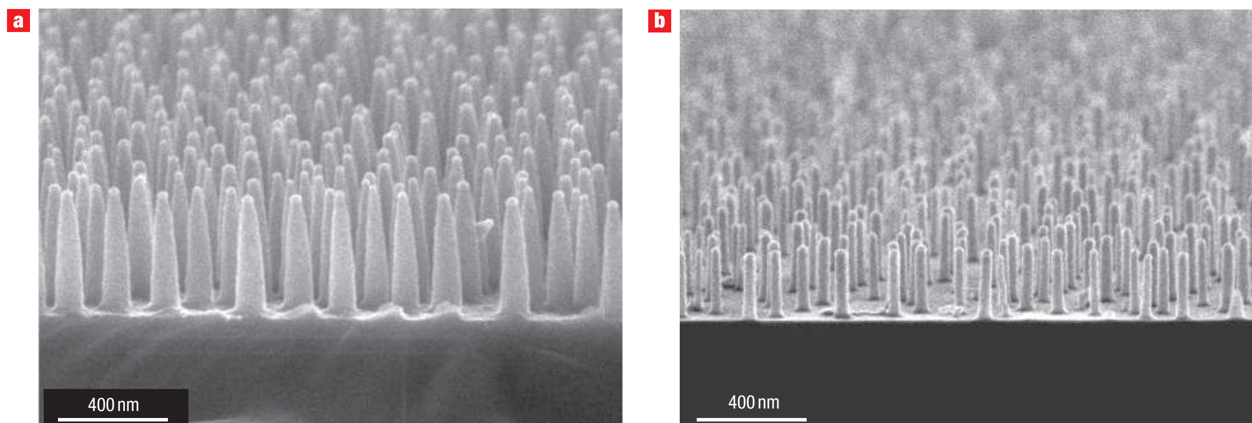

Figure 3 Effect of growth temperature on the tapering of nanowires. a,**b**, SEM cross-sectional images (tilt 10°) of Si nanowires grown at different temperatures: 490 °C (**a**) and 430 °C (**b**).

spectra taken from the nanoparticle and the nanowire (Fig. 2d) confirm that the tip mainly consists of Al, whereas the nanowire mainly consists of Si. The limited sensitivity of the EDS measurements can only place an upper limit on the Al concentration in the wire of approximately 10%. However, SPE experiments carried out at 530 °C indicate a strong p-doping of Si by Al of about 2×10^{18} cm^{-3} (0.004%) (ref. 25). This can be compared with a greater Au concentration of 4×10^{19} cm^{-3} (0.07%) (ref. 26) in high-temperature (1,300–1,450 K) grown Si wires.

In order to verify if growth via a solid particle is plausible, we need to estimate the concentration gradient ΔC across the solid particle that is necessary to transport Si from the vapour phase, through the solid Al catalyst particle, to the Si nanowire. Using the relation $\Delta C = \rho v r / D$, where ρ is the atomic density of Si (5.0×10^{22} cm^{-3}), v the growth rate (0.3 nm s^{-1}), r the radius of the particle (17 nm), and D the diffusion constant for Si in solid Al (1.54×10^{-14} m^2 s^{-1} at 430 °C; ref. 27) we obtain $\Delta C \approx 2.0 \times 10^{19}$ cm^{-3}. A comparison with the equilibrium concentration of Si in solid Al (3.0×10^{20} cm^{-3} at 430 °C; ref. 16) shows that a relative concentration change of 7% within the catalyst particle is sufficient to transport the necessary amount of Si through the solid particle. This demonstrates that a liquid catalyst particle is not required, and that VSS growth is possible.

Although well-aligned epitaxial Si nanowires could be synthesized using Al as a catalyst, it was found that the Si nanowires obtained tended to be tapered (Fig. 3a). This effect was predicted by Nebol'sin *et al.*[8]. Tapering is disadvantageous, and in contrast, Si nanowires grown with Au as the catalyst are in most cases uniform in diameter. Growth experiments were carried out at temperatures between 430 °C and 490 °C while keeping the other experimental conditions constant. Comparison of Fig. 3a (490 °C) with Fig. 3b (430 °C) shows that the tapering of the nanowires can be strongly reduced by lowering the temperature. In order to give a more quantitative description of this effect, we define the tapering parameter σ as

$$\sigma = \frac{d_1 - d_2}{2L} \tag{1}$$

where L is the length of the Si nanowire, and d_1 and d_2 are the diameters of the nanowire at its bottom and tip, respectively. In Fig. 4 the parameter σ (averaged over 10 measurements for each temperature) is plotted on a logarithmic scale as a function of the inverse of the growth temperature. One can see that by lowering the temperature from 490 °C to 430 °C, the tapering parameter σ can be reduced by about one order of magnitude. Furthermore, Fig. 4 implies that σ can be approximated by an exponential function of the inverse of the growth temperature ($\sigma \propto \exp(-2 \times 10^4\ \mathrm{K}/T)$). The exponential dependence signifies that, in the temperature range in question, the degree of tapering can be halved by a temperature reduction of about 17 K. Some reports have pointed out that the tapering of the nanowires is caused by uncatalysed deposition of Si on the sides of the nanowires[28–30], causing a radial growth of the nanowires with velocity v_{radial}. Introducing the axial nanowire growth velocity v_{axial}, σ can equally be expressed as the ratio $v_{\mathrm{radial}}/v_{\mathrm{axial}}$. In our case, the strong temperature dependence of σ is most likely caused by the strong temperature dependence of the radial growth velocity v_{radial}. Although the detailed physical mechanism behind

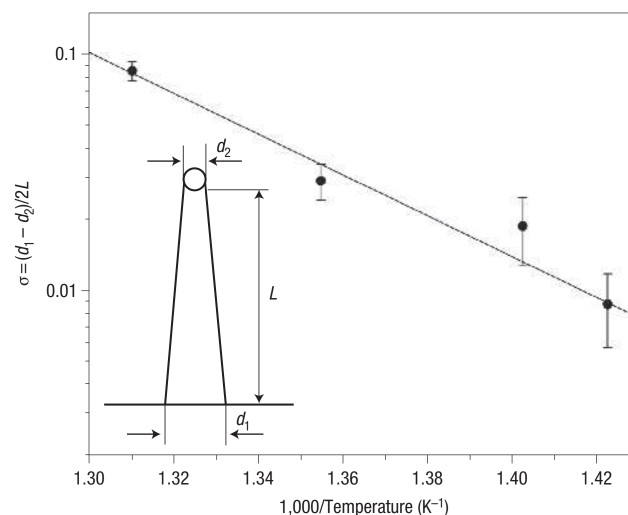

Figure 4 Temperature dependence of tapering of the Si nanowires. The tapering parameter σ is defined as $\sigma = (d_1 - d_2)/2L$. For each growth temperature, σ is obtained from the average of 10 nanowires. Error bars indicate one standard deviation.

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this phenomenon remains unclear, one possible explanation could be a temperature-dependent change of the surface termination of the nanowire flanks.

In summary, we have demonstrated in this paper that Al can be used as a catalyst to grow Si nanowires epitaxially on Si (111) substrates at temperatures in the range ∼430–490 °C. These temperatures are considerably lower than the eutectic temperature of the Al–Si binary phase diagram (577 °C), so the Al–Si catalyst particle is most probably in its solid α-Al phase during growth. This would imply that growth should be described by the VSS mechanism. Further evidence for VSS growth could possibly be verified by *in situ* diffraction experiments using TEM, RHEED (reflection high-energy electron diffraction) or X-rays. In contrast with the use of Au as catalyst, Al-catalysed wires have a tendency to be tapered. However, by lowering the growth temperature, the degree of tapering can be strongly reduced.

METHODS

NANOWIRE SYNTHESIS

Si nanowire growth experiments were carried out in an ultrahigh vacuum chemical vapour deposition (UHV-CVD) system with a base pressure 1.0×10^{-10} mbar. The low pressure avoids the oxidation of aluminium that prevented the successful use of Al as a catalyst in earlier investigations[19]. All our experiments were performed using silane, diluted to 5% in argon, as the vapour-phase silicon source. N-type phosphorus-doped Si (111) wafers were used as substrates in our experiments. The substrates were prepared by a standard two-step wet chemical cleaning and then dipped in 2% hydrofluoric acid to obtain a hydrogen-terminated Si surface. The wafers were immediately transferred into the UHV-CVD system. The Al film was then evaporated in situ onto the substrate by a thermal evaporation source at a rate of less than 0.1 nm min^{-1}. The thickness of the deposited film was monitored by a quartz crystal sensor. Directly after depositing an Al film of ∼0.6 nm thickness onto the Si wafer, the wafer was annealed for 20 min at ∼580 °C. Subsequently, Si nanowires were grown at temperatures ranging from 430 °C to 490 °C. The growth time was 20 min and the partial pressure of silane was kept at 0.25 mbar.

CHARACTERIZATION

The synthesized Si nanowires were characterized using scanning electron microscopy (JEOL, JSM6340). TEM investigation and X-ray energy dispersive spectroscopy analysis of the $[1\bar{1}0]$ and $[\bar{1}\bar{1}2]$ cross-sectional specimens prepared using a standard thinning approach were carried out in a CM20 TEM (Philips).

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References

1. Cui, Y. & Lieber, C. M. Functional nanoscale electronic devices assembled using silicon nanowire building blocks. *Science* **291,** 851–853 (2001).
2. Schmidt, V., Senz, S. & Gösele, U. Diameter-dependent growth direction of epitaxial silicon nanowires. *Nano Lett.* **5,** 931–935 (2005).
3. Gao, D., He, R. H., Carraro, C., Howe, R. T., Yang, P. D. & Maboudian, R. Selective growth of Si nanowire arrays via galvanic displacement processes in water-in-oil microemulsions. *J. Am. Chem. Soc.* **127,** 4574–4575 (2005).
4. Hannon, J. B., Kodambaka, S., Ross, F. M. & Tromp, R. M. The influence of the surface migration of gold on the growth of silicon nanowires. *Nature* **440,** 69–71 (2006).
5. Wu, Y., Cui, Y., Huynh, L., Barrelet, C. J., Bell, D. C. & Lieber, C. M. Controlled growth and structures of molecular-scale silicon nanowires. *Nano Lett.* **4,** 433–436 (2004).
6. Morales, A. M. & Lieber, C. M. A laser ablation method for the synthesis of crystalline semiconductor nanowires. *Science* **279,** 208–211 (1998).
7. Weyher, J. Some notes on the growth kinetics and morphology of VLS silicon crystals grown with platinum and gold as liquid-forming agents. *J. Cryst. Growth* **43,** 235–244 (1978).
8. Nebol'sin, V. A. & Shchetinin, A. A. Role of surface energy in the vapor–liquid–solid growth of silicon. *Inorg. Mater.* **39,** 899–903 (2003).
9. Givargizov, E. I. *Highly Anistropic Crystals* 104–105 (Terra Scientific Publishing Company, Tokyo, Japan, 1987).
10. Wagner, R. S. & Ellis, W. C. Vapor–liquid–solid mechanism of single crystal growth. *Appl. Phys. Lett.* **4,** 89–90 (1964).
11. Kamins, T. I. *et al.* Chemical vapor deposition of Si nanowires nucleated by $TiSi_2$ islands on Si. *Appl. Phys. Lett.* **76,** 562–564 (2000).
12. Mandl, B. *et al.* Au-free epitaxial growth of InAs nanowires. *Nano Lett.* **6,** 1817–1821 (2006).
13. Dick, K. A. *et al.* Failure of the vapor–liquid–solid mechanism in Au-assisted MOVPE growth of InAs nanowires. *Nano Lett.* **5,** 761–764 (2005).
14. Persson, A. I., Samuelson, L. & Wallenberg, L. R. Solid-phase diffusion mechanism for GaAs nanowire growth. *Nat. Mater.* **3,** 677–681 (2004).
15. Harmand, J. C., Patriarche, G. & Glas, F. Analysis of vapor–liquid–solid mechanism in Au-assisted GaAs nanowire growth. *Appl. Phys. Lett.* **87,** 203101–1, 3 (2005).
16. Massalski, T. B. *et al.* (ed.) *Binary Alloy Phase Diagrams* 2nd edn Vol. 1 (ASM International, Materials Park, Ohio, 1998).
17. Osada, Y. *et al.* Growth and structure of silicon fibers. *J. Electrochem. Soc.* **126,** 31–36 (1979).
18. Whang, S. J. *et al.* High quality single crystal Al-catalyzed Si nanowires. (Conference abstract, 210th ECS Meeting, Cancun, Mexico, 2006).
19. Civale, Y., Nanver, L. K., Hadley, P. & Goudena, E. J. G. Aspects of silicon nanowire synthesis by aluminum-catalyzed vapor-liquid-solid mechanism. Proceedings of the 7th Annual Workshop on Semiconductor Advances for Future Electronics (SAFE), Veldhoven, The Netherlands, 2004, 692–696.
20. Boatright, R. L. & McCaldin, J. O. Solid-state growth of Si to produce planar layers. *J. Appl. Phys.* **47,** 2260–2262 (1975).
21. Civale, Y. *et al.* Sub-500 °C solid-phase epitaxy of ultra-abrupt p^+-silicon elevated contacts and diodes. *IEEE Electron. Dev. Lett.* **27,** 341–343 (2006).
22. Tanaka, T. & Hara, S. Thermodynamic evaluation of binary phase diagrams of small particle systems. *Z. Metallkd.* **92,** 467–472 (2001).
23. Westwater, J., Gosain, D. P., Tomiya, S., Usui, S. & Ruda, H. Growth of silicon nanowires via gold/silane vapor-liquid-solid reaction. *J. Vac. Sci. Technol. B* **15,** 554–557 (1997).
24. Schmidt, V., Senz, S. & Gösele, U. UHV chemical vapour deposition of silicon nanowires. *Z. Metallkd.* **96,** 427–428 (2005).
25. Majni, G. & Ottaviani, G. Large-area uniform growth of <100> Si through Al film by solid epitaxy. *Appl. Phys. Lett.* **31,** 125–126 (1977).
26. Shchetinin, A. A. *et al.* Distribution coefficient of the initiating impurity and its influence on the electrical resistivity of filamentary silicon crystals. *Inorg. Mater.* **27,** 1137–1139 (1991).
27. Fujikawa, S. I., Hirano, K. I. & Fukushima, Y. Diffusion of silicon in aluminum. *Metall. Trans. A* **9A,** 1811–1815 (1978).
28. Wagner, R. S. & Ellis, W. C. The vapor–liquid–solid mechanism of crystal growth and its application to silicon. *Trans. Metall. Soc. AIME* **233,** 1053–1064 (1965).
29. Givargizov, E. I. Fundamental aspects of VLS growth. *J. Cryst. Growth* **31,** 20–30 (1975).
30. Bootsma, G. A. & Gassen, H. J. A quantitative study on the growth of silicon whiskers from silane and germanium whiskers from germane. *J. Cryst. Growth* **10,** 223–234 (1971).

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Competing financial interests

The authors declare that they have no competing financial interests.

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