Equalization and Clock and Data Recovery Techniques for 10-Gb/s CMOS Serial-Link Receivers

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***Abstract*—Two equalizer filter topologies and a merged equalizer/CDR circuit are described that operate at 10 Gb/s in 0.13-μm CMOS technology. Using techniques such as reverse scaling, passive peaking networks, and dual- and triple-loop adaptation, the prototypes adapt to FR4 trace lengths up to 24 inches. The equalizer/CDR circuit retimes the data with a bit error rate of 10^{-13} while consuming 133 mW from a 1.6-V supply.**

***Index Terms*—Adaptive equalization, analog equalization, broadband receivers, DFE, FFE, high-speed links, lossy channel, reverse scaling.**

I. Introduction

THE frequency-dependent loss of traces on FR4 printed circuit boards (PCBs) poses increasingly more difficult design challenges as data rates approach 10 Gb/s and trace lengths reach tens of inches. Preemphasis in the transmitter can partially compensate for the channel loss but at the cost of dynamic range. For example, the 12 dB preemphasis in [1] requires a supply voltage of 2.5 V to accommodate the large amplified components without sacrificing the low-frequency swings. Thus, low supply voltages and channel losses as high as 25 dB dictate that most of the equalization be performed in the receiver. Examples include a bipolar implementation consuming 195 mW [2] and a CMOS realization suffering from high intersymbol interference (ISI) and lacking automatic adaptation [3].

Recent work [1], [4], [5] has incorporated nonlinear (e.g., decision-feedback) equalizers so as to accommodate sharp notches in the channel due to impedance discontinuities and also avoid the amplification of crosstalk due to high-frequency peaking. The complexity and power dissipation of such realizations (e.g., 210 mW for the 6.25-Gb/s 0.13-μm CMOS receiver in [5]) are justified for only demanding applications.

This paper describes adaptive equalization and clock and data recovery (CDR) techniques suited to 10-Gb/s binary receivers. The concepts introduced here address the problem of high losses. Loss compensation is achieved by using linear equalization techniques that tend to amplify crosstalk noise. If crosstalk and impedance discontinuities due to connectors and vias also become critical, these techniques can be combined with other equalization methods [6] so as to mitigate both effects.

Section II presents various gain peaking methods that are used in Section III to develop two equalizer filter topologies. Section IV describes an adaptive equalizer architecture and Section V the merged equalizer/CDR circuit. Section VI summarizes the experimental results for the two prototypes.

II. Gain Peaking Techniques

A. General Considerations

Copper traces designed as transmission lines on FR4 substrates suffer from both skin effect and dielectric loss. For example, a 30-in trace exhibits a loss of approximately 21 dB at 5 GHz and 34 dB at 10 GHz (Appendix I). The equalizer filter must therefore provide adequate gain peaking around 5 GHz so as to equalize the signal spectrum.

The design of gain-peaking circuits must satisfy many difficult requirements: 1) sufficient boost at high frequencies; 2) matching the inverse loss profile of the channel with reasonable tolerance; 3) minimal low-frequency loss to minimize the noise accumulation in cascaded stages and provide sufficient swings for the CDR; 4) well-behaved phase response to achieve a low jitter; 5) reasonable linearity so that the equalizer transfer function indeed acts as the inverse of the channel loss profile; 6) small input capacitance to satisfy the S_{11} requirements; and 7) tunability of the boost to allow adaptation.

In addition, the challenges typically encountered in the design of low-voltage broadband amplifiers–such as limited bandwidth and drive capability–persist here as well.

B. Peaking By Complex Poles or Real Zeros

The availability of monolithic inductors may suggest the use of underdamped complex poles to provide the required boost at high frequencies. For example, the shunt-peaking circuit of Fig. 1(a) yields a transfer function of the form

$$T(s) = \frac{k(s+\omega_z)}{s^2 + \frac{\omega_0}{Q}s + {\omega_0}^2} \tag{1}$$

where $|\omega_z| = R_D/L_D$, $\omega_0 = 1/\sqrt{L_D C_P}$, $Q = (1/R_D)\sqrt{L_D/C_P}$. While providing enough boost to match the inverse of the FR4 frequency response, high-Q complex poles introduce substantial phase distortion. As an example, a cascade of two such stages is designed to equalize a 30-in trace [Fig. 1(b)], yielding the equalized eye shown in Fig. 1(d).

This issue restricts realizations to non-feedback structures containing real zeros and poles or feedback structures having

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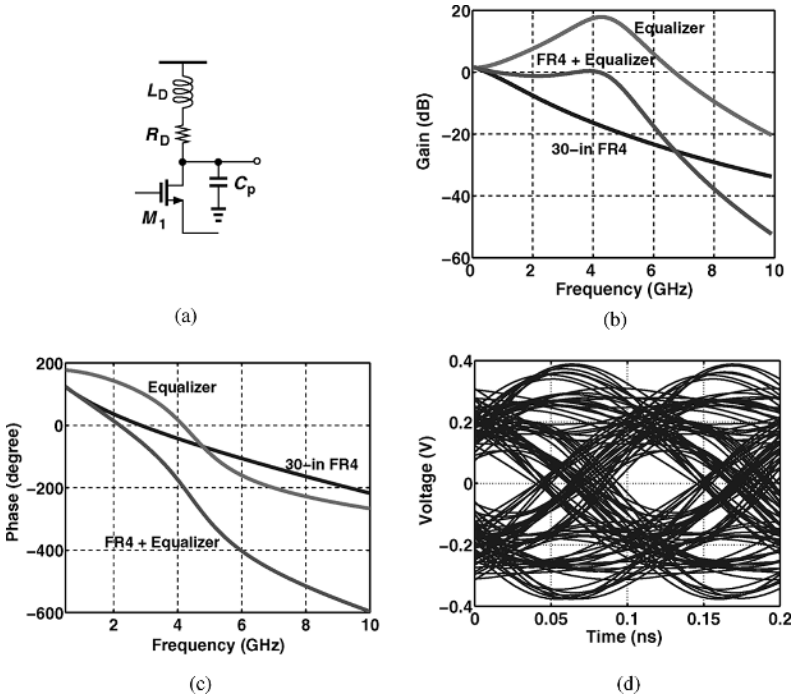


Fig. 1. Complex pole peaking circuit. (a) Implementation. (b) Magnitude response. (c) Phase response. (d) transient response.

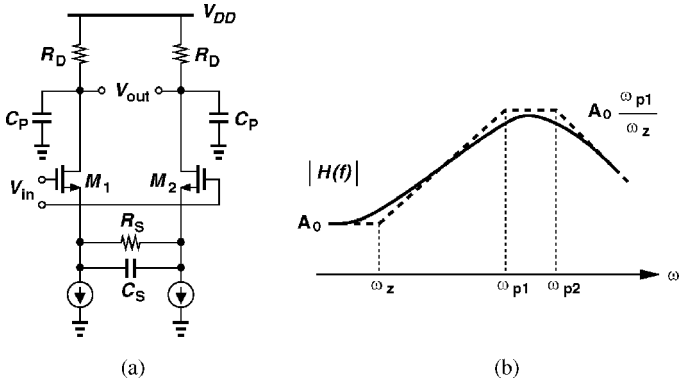


Fig. 2. *RC*-degenerated differential pair. (a) Circuit implementation. (b) Frequency response: actual response (solid line); bode approximation (dashed line).

low-Q complex poles. Of course, inductors can still act as shunt-peaking elements to broaden the bandwidth of equalizer stages.

An efficient method of boosting by means of real zeros is capacitive degeneration. Fig. 2(a) shows a degenerated differential pair that yields a zero at $|\omega_z| = 1/(R_S C_S)$ and poles at $|\omega_{p1}| = 1/(R_D C_P)$ and $|\omega_{p2}| = [1 + (g_m + g_{mb})R_S/2]/(R_S C_S)$, with a low-frequency gain of $A_0 = g_m R_D/[1 + (g_m + g_{mb})R_S/2]$. Fig. 2(b) depicts the frequency response. Improving the linearity of the stage, degeneration nonetheless creates a trade-off between the low-frequency gain and the boost factor, ω_{p1}/ω_z. Interestingly, one can write

$$A_0 \frac{\omega_{p1}}{\omega_z} \omega_{p2} \approx \frac{g_m}{C_P} \tag{2}$$

concluding that the product of the gain, the boost factor, and the bandwidth of the stage is limited by the f_T of the technology.[1]

It is important to appreciate the impact of the limited f_T (about 75 GHz in 0.13-μm CMOS technology) on equalization. For a small-signal gain of 2, an undegenerated differential pair with an overdrive voltage of 300 mV and fanout of unity yields a bandwidth of less than 12.5 GHz. The degenerated structure trades this gain-bandwidth product for the boost factor, the low-frequency gain, and the linear range.

With the performance envelope imposed by (2), a cascade of stages such as the circuit of Fig. 2(a) fails to provide the required boost factor while accommodating a data rate of 10 Gb/s and a reasonable low-frequency gain (e.g., −6 dB–0 dB). As the number of stages in the cascade increases to achieve a higher boost factor, the overall bandwidth tends to drop unless a greater low-frequency loss is allowed in each stage. Simulations indicate that, for a total boost factor of 22 dB at 5 GHz and an overall bandwidth of 5.5 GHz,[2] three degenerated stages with a low-frequency loss of 6 dB per stage are required. Such a high loss results in a sensitivity degradation of about 3 dB.

C. Peaking By Passive Networks

We propose the use of passive high-pass networks to provide boost at the front end of an equalizer, thus relaxing the linearity and gain peaking of the subsequent active stages and saving power consumption. Fig. 3(a) depicts an example where the zero and pole frequencies are respectively given by $|\omega_z| = 1/(R_1 C_1)$ and $|\omega_p| = 1/[(R_1 \| R_2)C_1]$ and the boost factor by $1 + R_1/R_2$ if C_{in} is neglected. To avoid degrading the input

[1]Here, C_P includes the input capacitance of the next stage.

[2]The overall bandwidth refers to that of the FR4 trace along with the equalizer circuit.

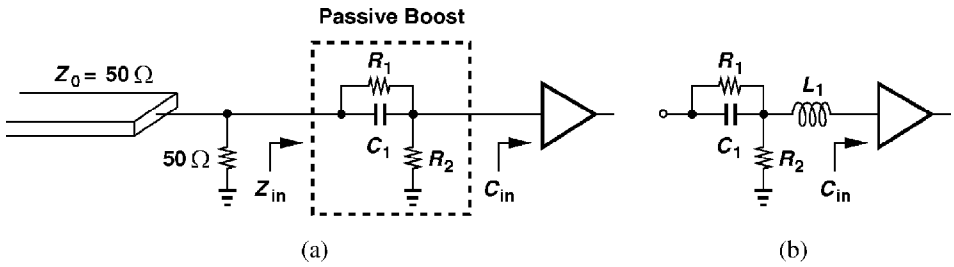


Fig. 3. (a) Passive network. (b) Proposed passive network with series-inductive peaking.

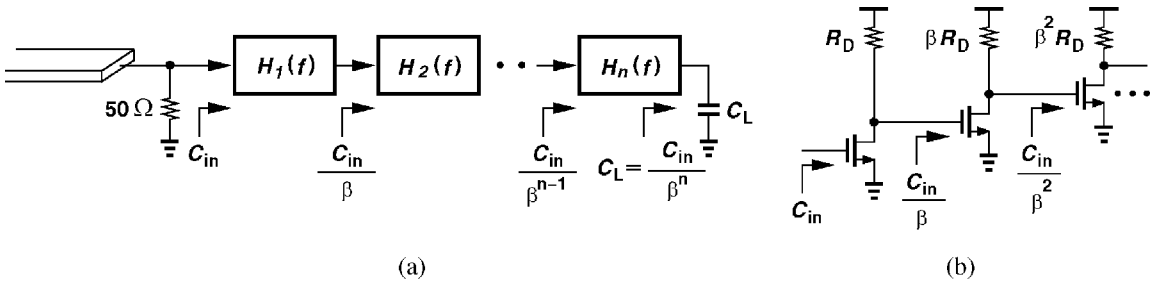


Fig. 4. Illustration of the reverse scaling technique. (a) Block diagram. (b) Single-ended circuit realization.

return loss, R_1, R_2, and $(C_1 s)^{-1}$ must be chosen high enough so that $|Z_{in}| \gg 50\ \Omega$. Also, since the input capacitance, C_{in}, lowers the pole frequency to $1/[(R_1 \| R_2)(C_1 + C_{in})]^{-1}$, we require that $C_{in} \ll C_1$. For example, if $R_1 = 500\,\Omega$, $R_2 = 700\,\Omega$ (for a boost of 4.7 dB), and $C_1 = 200$ fF, then C_{in} must remain below 20 fF, restricting the size of the transistors in the first active stage.

The above restriction can be eased through the use of series inductive peaking [Fig. 3(b)]. Here L_1 provides additional peaking at frequencies above 5 GHz even for large values of C_{in}. For example, if $R_1 = 500\,\Omega$, $R_2 = 700\,\Omega$, $C_1 = 200$ fF, and $C_{in} = 70$ fF, the network yields a boost factor of 8 dB and an S_{11} of -10 dB at 10 GHz.

D. Reverse Scaling

With the trade-offs described above, the peaking circuits presented thus far provide a boost of approximately 8 dB at 5 GHz, dictating the use of at least three peaking stages in the equalizer. Moreover, the cumulative low-frequency loss requires two additional gain stages to restore the signal level.

If n identical stages are cascaded, the overall small-signal bandwidth is given by [7]

$$BW_{tot} = BW_0 \sqrt[m]{2^{1/n} - 1} \tag{3}$$

where BW_0 denotes the bandwidth of a single stage and m is equal to 2 for first-order stages and 4 for second-order stages. Thus, if $m = 2$, then the small-signal bandwidth drops by a factor of 2.6 for five stages. For example, with three peaking and two gain stages, the bandwidth of the equalizer falls below 4 GHz if no bandwidth enhancement techniques are employed.

Reverse scaling [8] provides bandwidth improvement in applications where the input impedance need not be very high. In this work, we propose the concept of reverse scaling for equalizer design [9]. As illustrated in Fig. 4, successive stages are scaled down in size by a factor of β such that the gain and

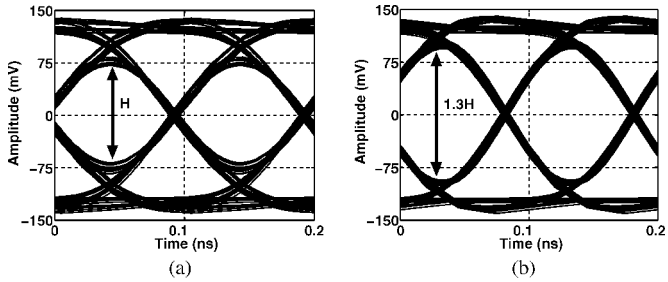


Fig. 5. Transistor-level simulations of a five-stage equalizer with (a) no scaling, and (b) reverse scaling.

boost characteristics are maintained but the time constant at the output node of each stage is reduced. The total capacitance seen at the interface between stages k and $k+1$ can be expressed as $C_{T,k} = C_{out,k} + C_{in,k+1}$, where $C_{out,k}$ includes the junction and overlap capacitances at the output of the kth stage and $C_{in,k+1}$ the input capacitance of the $(k+1)$th stage. In a reverse-scaled design [Fig. 4(b)], the corresponding time constant is given by

$$\tau_{\text{scaled}} = \beta^{k-1} R_D \left(\frac{C_{out,1}}{\beta^{k-1}} + \frac{C_{in,1}}{\beta^k} \right) \tag{4}$$

revealing a bandwidth improvement resulting from the second term in the parentheses. For example, with $C_{out,1} = 25$ fF, $C_{in,1} = 75$ fF, and $\beta = 1.5$, the bandwidth increases by about 33%.

As evident from the relationship $C_L = C_{in}/\beta^n$, the value of β is dictated primarily by three factors: 1) the maximum tolerable value of C_{in}; 2) the minimum acceptable value of C_L (the input capacitance of the CDR circuit); and 3) the minimum acceptable number of stages. The first component is determined by the required input bandwidth and/or return loss. If the equalizer path directly drives the CDR circuit, the minimum acceptable value of C_L is given by the total input capacitance of the

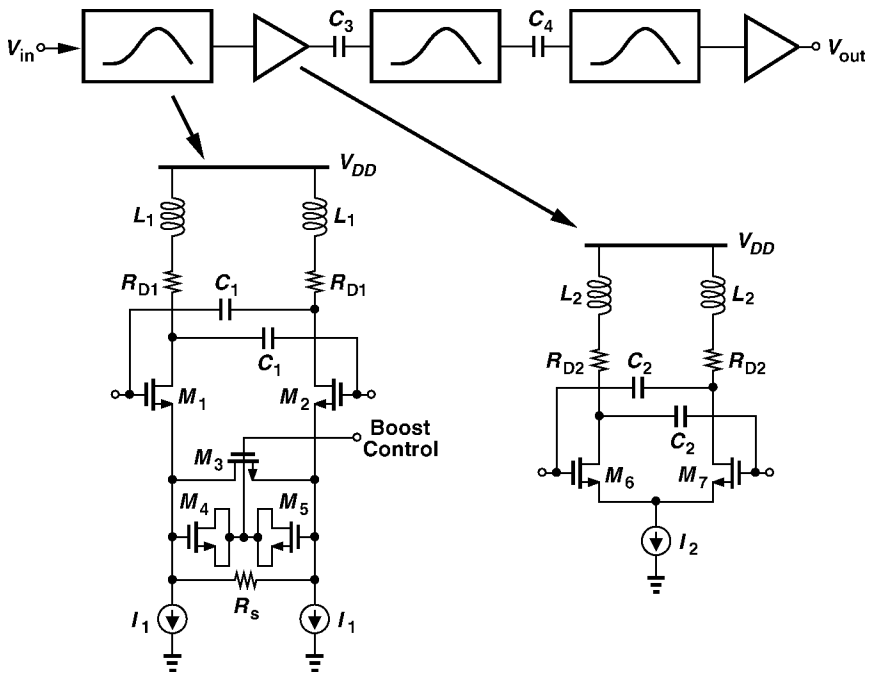


Fig. 6. Equalizer filter I with reverse scaling.

phase detector—a rather large value. Thus, a simple gain stage preferably follows the equalizer. In our design, $C_L \approx 20$ fF. As mentioned above, the minimum number of stages is dictated by the trade-off between the required peaking and the bandwidth. For example, a five-stage cascade necessitates a bandwidth of 14 GHz at each node, limiting the total input capacitance to 450 fF. On the other hand, an $|S_{11}|$ of 10 dB at 10 GHz translates to a total input capacitance of 213 fF. Allowing for ESD and pad capacitance, we assume $C_{in} \approx 100$ fF.[3] Also, $C_L \approx 20$ fF. Thus, $\beta \approx 1.39$.

In this work, a scaling factor of 1.3 is chosen to achieve an improvement of 22% in speed. Fig. 5 shows the simulated outputs of the equalizer for scaled and unscaled designs.[4] The eye opening increases by approximately the same factor.[5]

Note that the use of monolithic T-coils [10] can greatly increase the tolerable input capacitance and hence provide additional bandwidth improvement with reverse scaling.

III. Equalizer Filter Design

In this section, the peaking techniques presented in Section III are used to design equalizer filters. These designs also incorporate adaptive boosting so as to allow different trace lengths.

A. Equalizer Filter I

Shown in Fig. 6, the first equalizer [9] intersperses three peaking stages with two gain stages to provide a boost factor of about 22 dB at 5 GHz while exhibiting a low-frequency loss of less than 3 dB.[6] The design exploits the reverse scaling technique described in Section II but with slight variation in the value of β from one stage to the next to allow optimization for high-frequency peaking and low-frequency loss.

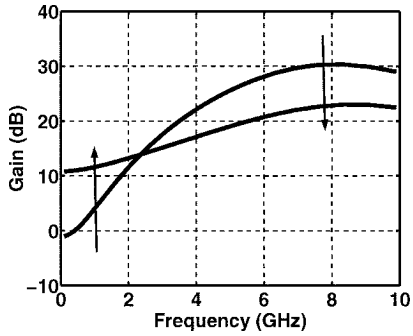


Fig. 7. Tuning behavior of five-stage cascade.

As mentioned in Section II, simple resistively-loaded differential pairs cannot yield the required bandwidth. Thus, inductive peaking and negative Miller capacitances [11] have been added to improve the speed without sacrificing the voltage headroom. To save area, only three of the stages incorporate inductive peaking.

The peaking stages in the equalizer path employ a variable degeneration resistance along with MOS varactors M_4 and M_5 to provide a wide boost range. As the control voltage rises, the on-resistance of M_3 falls and so does the capacitance of M_4 and M_5, raising the magnitude of the zero. Note that the simultaneous change of the resistance and capacitance greatly simplifies the adaptation loop (Section IV). Fig. 7 illustrates the simulated tuning behavior of the cascade as the control voltage is swept from 0.1 V to 1.1 V.

As indicated in Fig. 6, the cascade employs capacitive coupling between some stages to isolate common-mode

[3]For the sake of simplicity, these calculations do not include the use of passive peaking at the front end.

[4]The details of this circuit are shown in Fig. 6.

[5]These designs incorporate other broadband techniques as well (Section III).

[6]The two gain stages partially compensate the loss of the peaking stages, providing an output swing of approximately 1 V_{pp}.

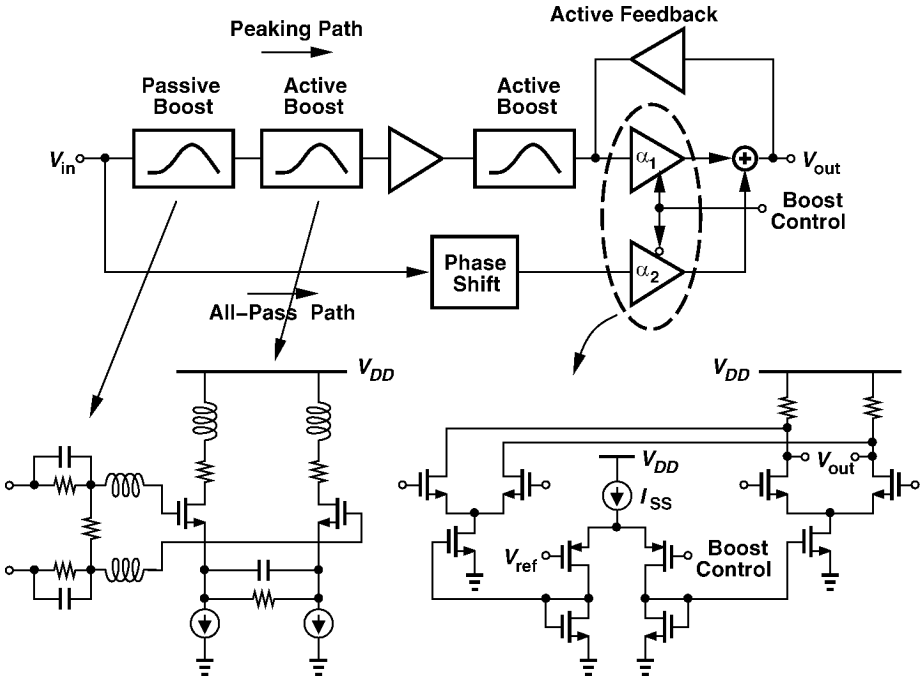


Fig. 8. Equalizer filter II architecture.

(CM) levels. This mitigates the voltage headroom issue and, more importantly, avoids variability in the CM level seen by M_3-M_5 due to the preceding stage, thus maintaining a constant tuning range. The capacitors ($= 0.25$ pF) are realized using multi-finger fringe structures having a parasitic component of about 3%. The CM level is generated using a resistive divider. The corner frequency associated with this capacitive coupling is around 3 MHz, resulting in negligible droop with encoded data.

B. Equalizer Filter II

In Section II, the high-pass passive network was introduced to provide a peaking profile. The use of this network in the equalizer filter can save power consumption by relaxing the linearity and gain peaking requirements of the active stages. Fig. 8 shows the second equalizer filter architecture [12], which incorporates both passive peaking and reverse scaling. In contrast to the first equalizer, this design performs boost tuning by interpolation between a peaking path and an all-pass path (set by coefficients α_1 and α_2), thus achieving a wider tuning range than that obtained by means of MOS varactors and variable resistors. Also, a constant (linear) degeneration resistance in the differential pairs yields higher linearity and a more accurately-defined low-frequency gain.

The use of interpolation nonetheless presents a difficulty for intermediate line lengths, i.e., if $\alpha_1\alpha_2 \neq 0$. The disparate delays through the two paths result in substantial ISI after their corresponding outputs are summed. Realized as a degenerated differential pair, the phase shift block in the all-pass path partially corrects this error. The zero of this differential pair is positioned such that the phase response approximates the effective response of the three zeros in the peaking path for the frequency range of 1–4 GHz. The pole provides additional adjustment of the overall phase response in the all-pass path.[7]

The use of series inductive peaking (with 3-nH inductors) in the passive boost stage allows wide input transistors (w $=$ 36 μm) in the first differential pair and hence reverse scaling through the cascade. The low-frequency loss of 7 dB in the passive network degrades the sensitivity to some extent. With inductive peaking and negative Miller capacitances, the bandwidth of each active stage reaches 18 GHz. The summing stage incorporates active feedback [10] to improve the speed while avoiding inductors. Since active feedback trades low-frequency gain for bandwidth, it has been applied to only one stage.

The choice between the two types of equalizers described above somewhat depends on the application. The former does not incorporate a passive network at the input, providing greater sensitivity but consuming a higher power. The latter achieves a higher linearity and wider tuning range.

IV. Adaptive Equalizer

Fig. 9 shows the first adaptive equalizer architecture [9], where the equalizer filter is followed by a slicer, and two loops control the boost in the filter and the swing in the slicer. The equalized data, D_{out}, is sensed at node *A* rather than *B* because the slicer incorporates some peaking to improve convergence of the loops, thereby leading to larger jitter at *B* than at *A* when the loops reach steady state. The need for the swing control loop is justified as follows.

High-speed adaptive equalizers set the peaking in the filter stages so as to compensate for the high-frequency loss of the channel. To this end, the equalizer output is sharpened by a slicer and the adaptation loop adjusts the peaking according to the

[7]Simulations indicate that a 20% delay mismatch produces less than 5 ps of ISI jitter at the equalizer output.

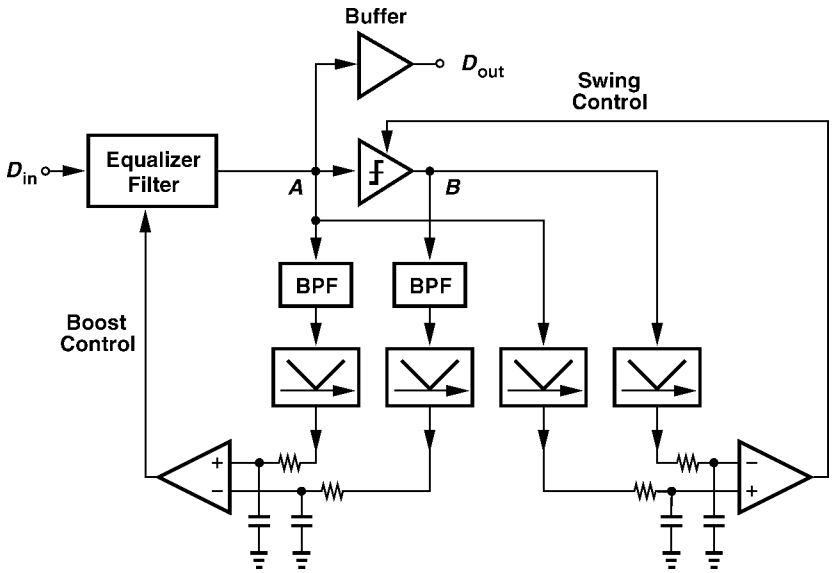


Fig. 9. Proposed adaptive equalizer architecture.

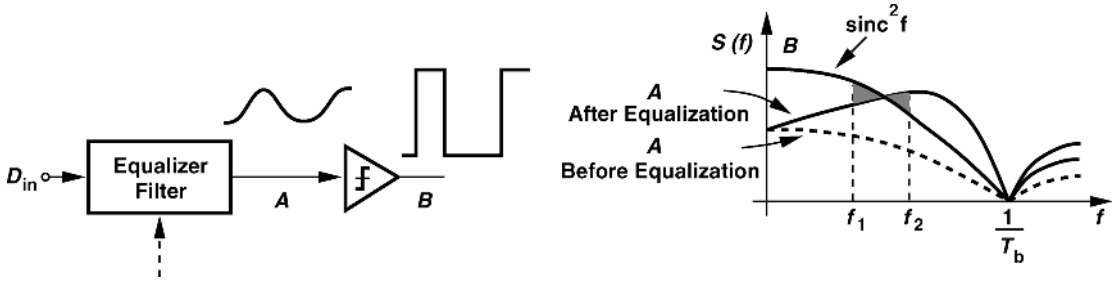


Fig. 10. Spectrum before and after slicer with swing mismatch.

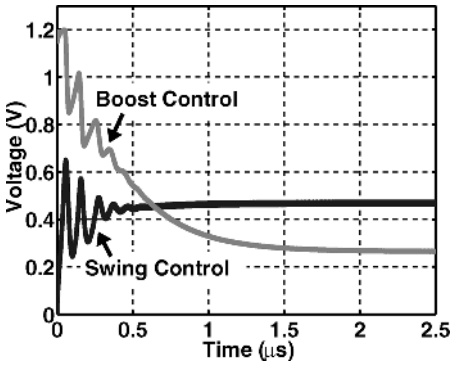


Fig. 11. Simulated dynamics of the swing and boost control loops.

difference between high-frequency contents of the data before and after slicing [2], [13], [14]. Note that the slicer generates a random binary sequence having a $\mathrm{sinc}^2 f$ spectrum. If operating optimally, the equalizer must do the same.

The adaptation requires that the equalizer *not* slice (hard-limit) the data. Otherwise, the input and output of the final slicer carry similar spectra, and the error in the adaptation loop approaches zero even with incomplete equalization. This issue in turn necessitates adequate linearity in the equalizer path,[8] leading to two important effects: 1) the equalizer output swing is a function of the transmitted signal level and other parameters in the signal path, whereas the slicer output is not; and 2) the equalizer circuitry is fundamentally different from that in the slicer. For example, the differential pairs in the equalizer may not experience complete switching whereas those in the slicer must.

Thus, as illustrated in Fig. 10, the adaptation may settle such that the signals at *A* and *B* exhibit equal high frequency energies (between f_1 and f_2) while *A* is very poorly equalized. The above difficulty can be alleviated by adding a loop for low-frequency adaptation to maintain equal swings at *A* and *B* [15]. In [15], however, the swings in the equalizer path are adjusted, potentially limiting the tuning range and interfering with the main adaptation loop. The approach introduced in this work is shown in Fig. 9, where the input and output swings of the slicer are compared after rectification, and the resulting error is used to adjust the slicer output swing rather than the equalizer output swing. The swing is controlled by adjusting the tail current of a limiting differential pair in the slicer. The slicer therefore generates swings that match the equalizer output swings, allowing nearly complete overlap of spectra at *A* and *B* after equalization.

Unlike implementations that precede the rectifiers with high-pass filters (HPFs) [13]–[15], this design employs bandpass filters (BPFs) to measure the energy in a band $[f_1, f_2]$ around 5 GHz. This is because the gain peaking occurs in the vicinity of this frequency and must be controlled accurately.

[8]A variable-gain amplifier can precede the equalizer to ensure linearity.

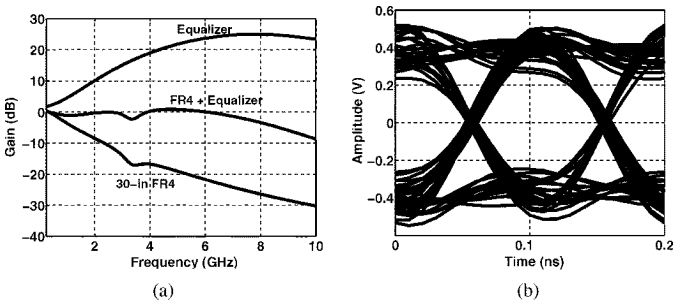


Fig. 12. Response of the adaptive equalizer to a 25% mismatch in the line. (a) Frequency response. (b) Eye diagram.

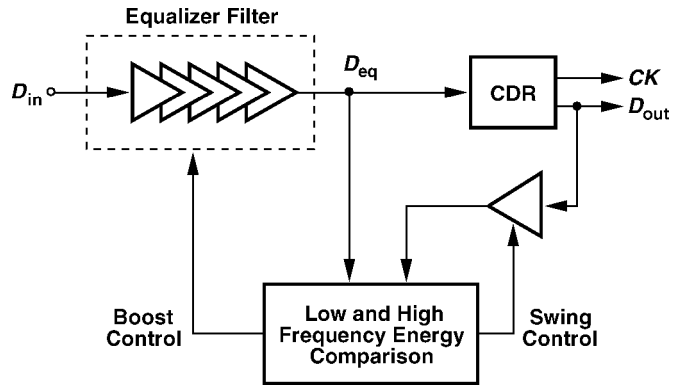


Fig. 13. Proposed merged adaptive equalizer/CDR architecture.

The two dynamic feedback loops in the architecture of Fig. 9 can potentially "fight" each other, thus failing to converge to appropriate settings. Such a conflict is avoided by choosing substantially different time constants for the two loops, namely, 65 ns for swing control and 105 ns for boost control. Fig. 11 depicts the simulated dynamics of the two loops as they settle to their final values for worst-case initial conditions. (This simulation is performed on the transistor-level implementation of the circuit.)

A possible point of concern is the sensitivity of the proposed adaptive equalizer to mismatches in the transmission line. Fig. 12 shows the response of the adaptive equalizer for a 25% mismatch in the transmission line at 3.4 GHz. As expected, there is only a gradual degradation in the eye compared to the transmission line with minimal mismatch [Fig. 5(b)]. This design may be followed by a multi-tap decision-feedback equalizer to remove the resulting ISI.

V. Merged Adaptive Equalizer/CDR Circuit

In broadband receivers, the equalizer is typically followed by a CDR circuit. The two functions can simply be cascaded but we recognize that the retimed data produced by the CDR circuit exhibits the properties of a sliced waveform, obviating the need for an explicit slicer. Since slicers typically consume several inductors and considerable power to achieve the required bandwidth and gain, the consolidation of equalizer and CDR circuits can yield savings in area and power dissipation.

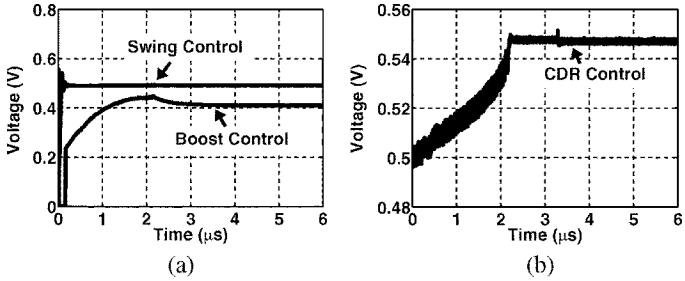


Fig. 14. Simulated dynamics of (a) boost and swing control signals, and (b) the control voltage of the VCO in the CDR loop.

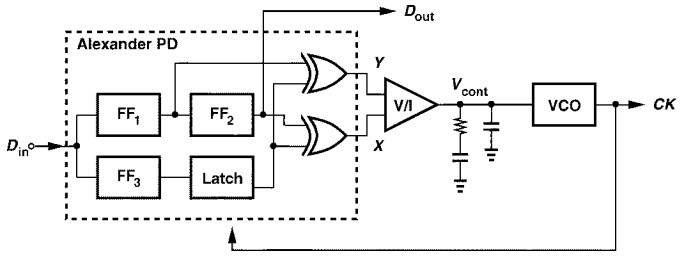


Fig. 15. CDR architecture.

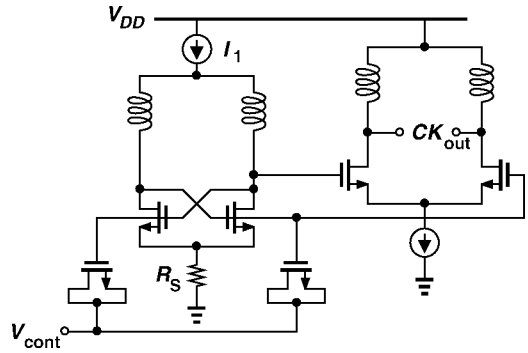


Fig. 16. VCO and buffer circuit.

A. Architecture

Shown in Fig. 13 is the architecture of the merged equalizer/CDR circuit [12]. The retimed data, D_{out}, provides both low-frequency and high-frequency information for adjusting the boost and swing controls. The swing adjust circuit is realized as a single differential pair while the filter and the energy comparison mechanisms are similar to those in Figs. 8 and 9, respectively.

The architecture in Fig. 13 entails a start-up issue. With high intersymbol interference (e.g., for a 24-in trace), if the equalizer begins with minimum boost, then each data edge applied to the CDR spans several bit periods, thus prohibiting proper phase-lock. The architecture contains three feedback loops whose time constants must be chosen carefully to ensure convergence. Fig. 14 shows the dynamics of the three loops as they reach steady state. Only with proper phase lock can the CDR provide the retimed data to the feedback loop; hence, the CDR loop must settle before the boost control loop. Note that the boost control loop is initially reset, providing maximum peaking and enabling the CDR to lock. Also, even without phase-lock, the retimed data from the CDR is sufficient for

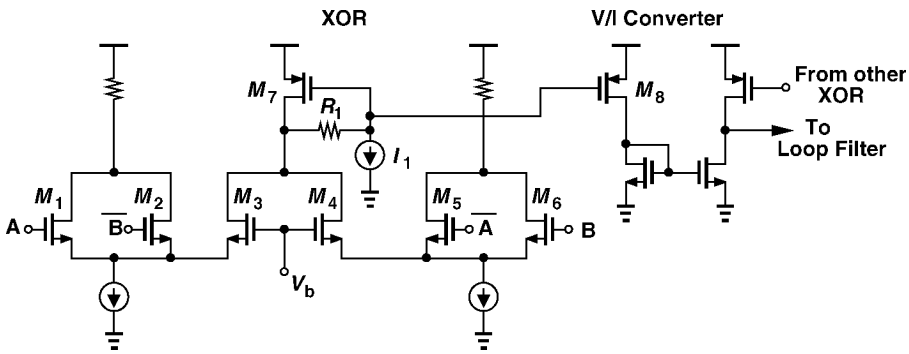


Fig. 17. XOR and V/I circuit.

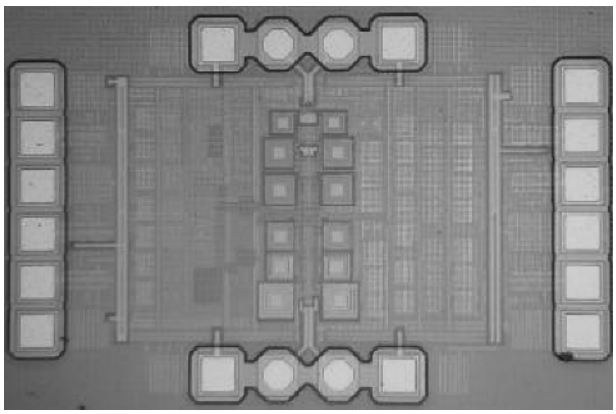


Fig. 18. Die photograph of adaptive equalizer.

the swing control loop to converge. Thus, in this design, the swing control loop is the fastest, and the boost control loop, the slowest.

The merging of the equalizer and the CDR saves about 19 mW in power dissipation. Furthermore, it obviates several inductors that would otherwise be necessary in the slicer.

The overall performance of the equalizer/CDR cascade depends on the residual ISI, additive noise, and clock jitter. It is therefore necessary to quantify the trade-offs among these parameters so that a reasonable jitter budget can be allocated to each stage. A framework for the analysis of these effects is proposed in Appendix II.

B. CDR Circuit

This work employs a full-rate CDR circuit consisting of an Alexander phase detector (PD) [16] and an LC voltage-controlled oscillator (VCO) (Fig. 15). While operating as a bang-bang circuit and exhibiting a high gain, the Alexander PD produces no output in the absence of data transitions, thus leaving V_{cont} undisturbed. The high gain of the PD obviates a charge pump and permits the use of a simple voltage-to-current (V/I) converter to drive the loop filter. Note that nodes *X* and *Y* need not provide a high bandwidth as only their average voltages are sensed by the V/I converter—an important advantage of this realization over those using charge pumps.

The speed, jitter, and driving capability required of the oscillator point to the use of an LC implementation. Fig. 16 depicts the VCO and its buffer. Resistor R_S sets the core common-mode voltage to approximately $V_{\rm DD}/2$, maximizing the capacitance range of the MOS varactors and hence the tuning range of the oscillator. The buffer isolates the core from the large capacitances associated with the PD devices and interconnects while suppressing the data transitions that would otherwise couple from the PD flip-flops to the VCO core.

The VCO phase noise is dominated by the modulation of the varactor capacitances due to the noise current of I_1. In this design, the simulated phase noise of the free-running VCO as predicted by SpectreRF is approximately equal to -106 dBc/Hz at 1-MHz offset.

The XOR gates used in the PD of Fig. 15 must exhibit symmetry with respect to their two inputs and operate with a low supply voltage. Shown in Fig. 17 along with the V/I converter, the XOR gate is a modified version of that in [17]. Here M_1–M_6 form the XOR core and M_7 copies the average output current into M_8. To allow low-voltage operation, the drain voltage of M_7 is raised by $I_1R_1 \approx |V_{THP}|$ above its gate voltage, thus saving one threshold in the headroom. The reference voltage V_b is approximately equal to the common-mode level of *A* and *B*.

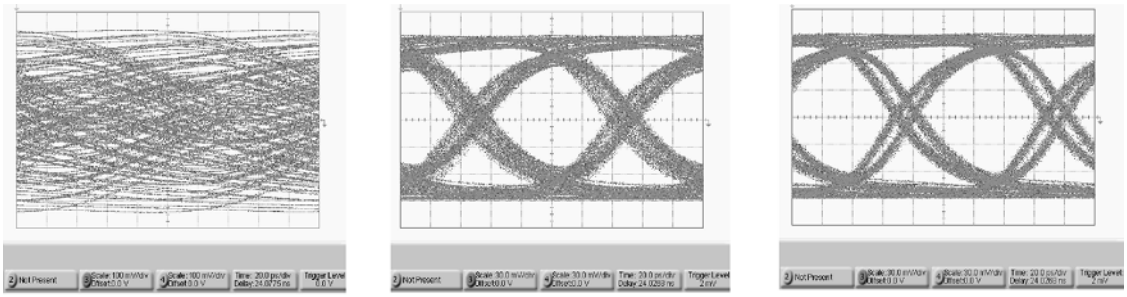
The V/I converter copies the average output current of the XOR, providing nearly rail-to-rail swings for the oscillator control line. Sensing the average voltage produced by the XOR, the V/I converter remains free from a dead zone.

VI. Experimental Results

This section presents experimental results for the two circuits described in Sections IV and V. Both are fabricated in 0.13-μm CMOS technology.

A. Adaptive Equalizer I

Fig. 18 shows a photograph of the die, which measures 0.45 mm $\times$ 0.36 mm. The circuit has been tested on a high-speed probe station while sensing 10-Gb/s data that has traveled on an FR4 board. The pseudorandom bit sequence follows a 2^7-1 pattern. Fig. 19 shows the equalizer input and output waveforms at 10 Gb/s for 30-in and 6-in differential traces on the FR4 board without any external changes in the bias or other circuit conditions. In this setup, the 30-in FR4 trace has a loss of 21 dB at 5 GHz. The results show that the high-frequency adaptation loop accommodates varying loss conditions. To check the operation of the low-frequency adaptation loop, the pattern generator output swing was varied from 520–700 $\rm mV_{pp}$ and similar results were obtained. Note that the pattern generator



(a) (b) (c)

Fig. 19. Measured results before and after equalization at 10 Gb/s for FR4 traces, (horizontal scale: 20 ps/div.): (a) before equalization for 30-in FR4 (vertical scale: 100 mV/div.), (b) after equalization for 30-in FR4 (vertical scale: 100 mV/div.), (c) after equalization for 6-in FR4 (vertical scale: 100 mV/div.).

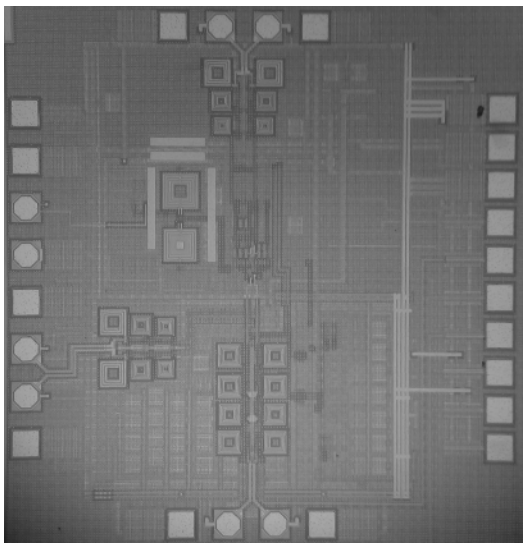


Fig. 20. Die photograph of merged adaptive equalizer/CDR.

itself suffers from a peak-to-peak jitter of 15 ps. The circuit (excluding the output buffer) consumes 25 mW from a 1.2-V supply.

The double trace visible in Fig. 19(c) for a 6-in line results from approximately 2 dB of ripple in the cascade frequency response of the FR4 board and the equalizer. Confirmed by simulations, this ripple possibly arises from the imperfect match between the peaking profile provided by the equalizer and the inverse of the channel frequency response.

B. Merged Equalizer/CDR Circuit

Fig. 20 shows the photograph of the die, which measures 0.94 mm $\times$ 0.65 mm. The merged equalizer/CDR circuit utilizes the equalizer filter architecture proposed in Section III.B. The circuit has been tested in a chip-on-board assembly with a 10-Gb/s 2^7-1 bit sequence.

Fig. 21 depicts the measured input and output eye diagrams for an FR4 trace length of 24 inches having a loss of 18 dB at 5 GHz. For this setup, the equalizer/CDR circuit was tested with a supply voltage of 1.6 V. The sensitivity of the merged circuit is plotted in Fig. 22, indicating a bit error rate (BER) of less than 10^{-13} for a differential transmitted voltage of 640 $\mathrm{mV_{pp}}$. This sensitivity can be improved by adding a simple gain stage after the equalizer. The circuit consumes 133 mW, of which 41 mW is dissipated in the equalizer and 92 mW in the CDR.

Fig. 23(a) shows the recovered clock spectrum for a 24-in FR4 at 10 Gb/s, displaying a phase noise of -109 dBc/Hz at 1-MHz offset. The jitter histogram in Fig. 23(b) suggests an rms jitter of 2.22 ps. The VCO provides a tuning range from 8.9 GHz to 11.6 GHz.

VII. Conclusion

The high loss of long traces on FR4 boards can be compensated through the use of equalization techniques such as passive peaking networks, reverse scaling, and capacitive degeneration. To adapt to the line length, equalizers must incorporate both boost and swing control while guaranteeing smooth, conflict-free convergence. Finally, the equalization and CDR functions can be merged to eliminate slicers. This work has demonstrated these concepts for a data rate of 10 Gb/s and trace lengths of 24 inches in 0.13-μm CMOS technology.

Appendix I
Line Modeling

Fig. 24(a) plots the loss profile of a differential 30-in microstrip line on an FR4 board. Designed for a differential characteristic impedance of 100 Ω, the two traces have a width of 6 mil and a spacing of 12 mil. (This profile is obtained by simulation of the structure in SONNET.) The skin effect and dielectric loss exhibit approximately $\sqrt{f}$ and f dependencies, respectively, and the loss profile can be represented as

$$|T(f)| = \exp(-\alpha_1 l\sqrt{f} - \alpha_2 l f) \tag{5}$$

where α_1 and α_2 depend on the trace and board properties, respectively, and l denotes the trace length. Thus, skin effect is dominant at lower frequencies and dielectric loss, at higher frequencies. In this example, skin effect loss becomes equal to dielectric loss at approximately 2.5 GHz. The strong frequency dependence of the losses in the microstrip makes it difficult to use the standard transmission line model [Fig. 24(b)], where the series resistance R_S and the parallel conductance G remain constant with frequency.

While broadband models have been developed for skin effect [18], an accurate model is not available for dielectric loss. It is

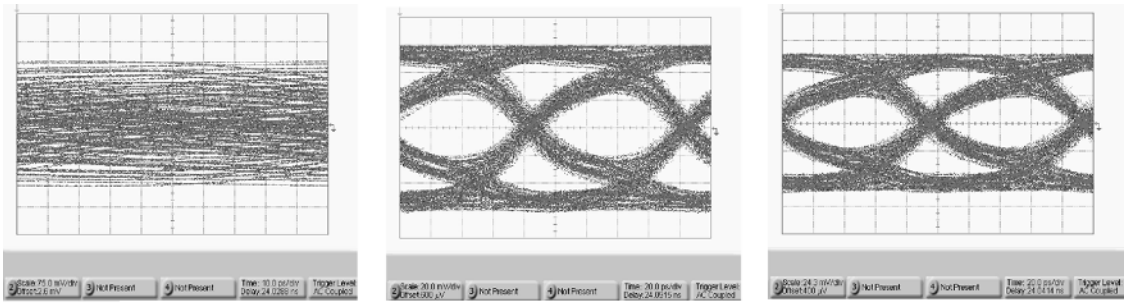


Fig. 21. Measured results before and after equalization/data recovery at 10 Gb/s for FR4 traces (horizontal scale: 20 ps/div.): (a) before equalization/data recovery for 24-in FR4 (horizontal scale: 10 ps/div., vertical scale : 75 mV/div.), (b) after equalization/data recovery for 24-in FR4 (horizontal scale: 20 ps/div., vertical scale : 20 mV/div.), (c) after equalization/data recovery for 6-in FR4 (horizontal scale: 20 ps/div., vertical scale: 20 mV/div.).

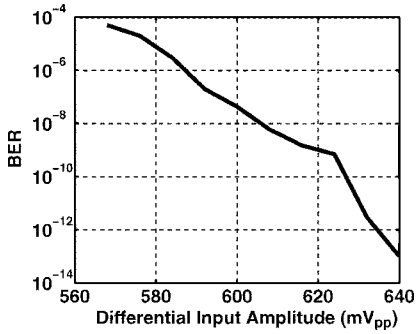


Fig. 22. BER sensitivity graph for equalization/data recovery for 24-in FR4 at 10 Gb/s.

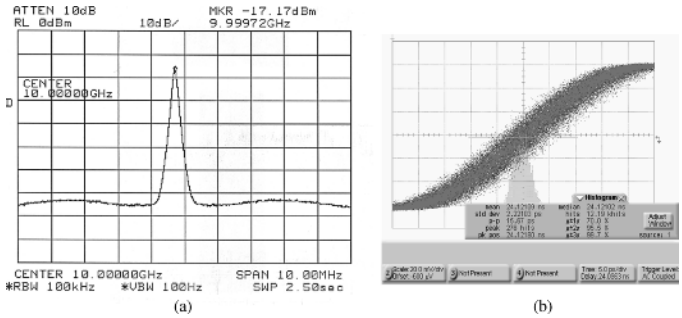


Fig. 23. Measured results after equalization/clock recovery for 24-in FR4 at 10 Gb/s. (a) Recovered clock spectrum. (b) Recovered clock jitter histogram (horizontal scale: 5 ps/div.).

possible to extract the S-parameters of a given line across a frequency band using a vector network analyzer or a field simulator and provide it to a tool capable of generating a spice model (e.g., SONNET). However, this approach provides little intuition and, more importantly, requires entirely different sets of data for different line lengths. It is therefore desirable to develop a physical, scalable circuit model that includes frequency-dependent dielectric loss and easily lends itself to circuit simulations. Such a model must also represent the phase profile of the line with reasonable accuracy.

Modeling begins with a correction of the circuit in Fig. 24(b) to accommodate frequency-dependent skin effect. Illustrated in Fig. 25(a), the section consisting of R_{S2} and L_2 is added [18], with R_{S2} ($\ll R_{S1}$) modeling the low-frequency resistance of the line and L_2 forcing the high-frequency current through R_{S1},

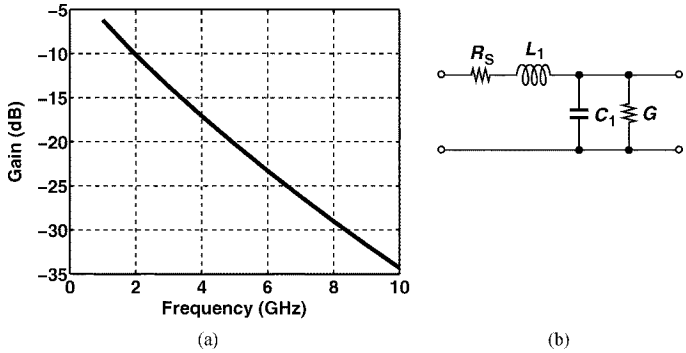


Fig. 24. (a) Loss profile of 30-in microstrip on FR4 board. (b) Narrowband loss model.

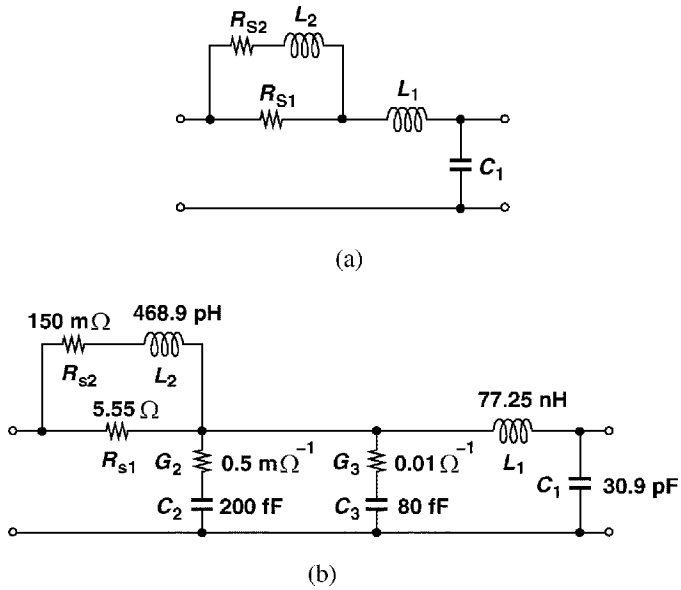


Fig. 25. (a) Model for variable skin effect. (b) Proposed broadband model for a 1-in trace.

thus raising the loss at higher frequencies. Additional sections can be added to refine the model, but simulations indicate that one branch is adequate for modeling up to 7 GHz.

In order to include the dielectric loss, the constant parallel conductance, G, in Fig. 24(b) is replaced with a frequency-dependent impedance that incurs greater loss at higher frequencies

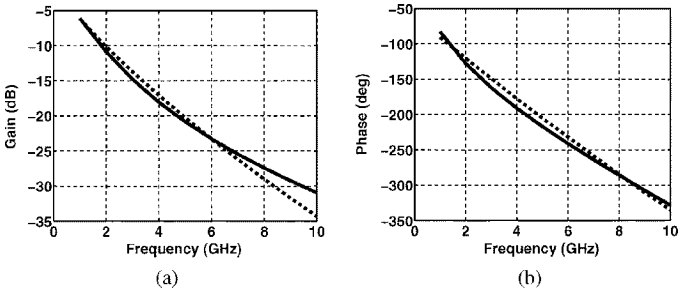


Fig. 26. Profiles of actual microstrip (dashed lines) and scalable model (solid lines) for a 30-in trace. (a) Magnitude profile. (b) Phase profile.

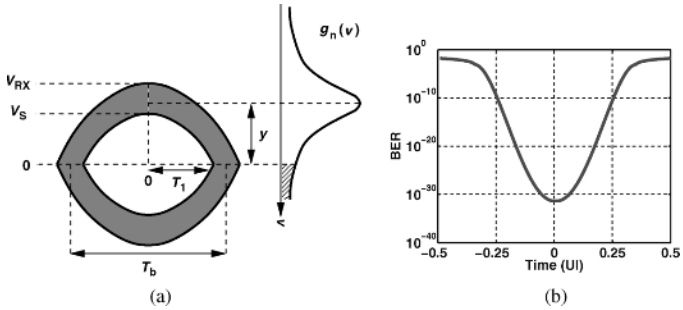


Fig. 27. (a) Error due to additive noise based on the sampling points in the eye. (b) BER as a function of clock skew.

[Fig. 25(b)]. The conductance to the substrate, therefore, increases with frequency. Accurate modeling of the dielectric loss necessitates at least two such sections: the loss in the G_2–C_2 branch becomes appreciable above 0.4 GHz and that in the G_3–C_3 branch above 20 GHz, thus providing good accuracy up to 7 GHz. The above model can simply be cascaded to represent longer traces. Fig. 26 compares the loss and phase profiles for a 30-in trace as predicted by field simulations and the model, demonstrating a reasonable fit.[9]

APPENDIX II
BER ESTIMATION

The BER of equalizer/CDR chains is a function of additive noise, ISI, and CDR skew and jitter. In this section, we propose a method of estimating the BER based on these parameters. The objective is to develop an intuitive understanding of the tradeoffs and hence arrive at a reasonable compromise.

Consider the eye diagram shown in Fig. 27(a), where V_{RX} and V_S denote the peak received swing and the peak eye opening, respectively. We first exclude clock jitter. The ISI due to limited bandwidth or incomplete equalization leads to a roughly uniform distribution of the amplitude between V_S and V_{RX}. Denoting this distribution by $g_{ISI}(y)$ and that of additive Gaussian noise by $g_n(y)$, we observe that an error occurs if noise causes a level between $+V_S$ and $+V_{RX}$ to fall below zero (or a level between $-V_S$ and $-V_{RX}$ to exceed zero). Thus, the probability of error is given by

$$P_e = \int_{V_S}^{V_{RX}} g_{ISI}(y) \left[\int_y^{\infty} g_n(v) dv \right] dy. \tag{6}$$

Also,

$$g_{ISI}(y) = \frac{1}{2(V_{RX} - V_S)} \qquad V_S < y < V_{RX}, \tag{7}$$

$$= 0 \qquad y < V_S \text{ or } y > V_{RX} \tag{8}$$

and

$$g_n(y) = \frac{1}{\sqrt{2\pi}\sigma_n} \exp \frac{-y^2}{2{\sigma_n}^2} \tag{9}$$

where σ_n denotes the rms value of noise. Carrying out the integration in (6) and neglecting higher-order terms, we have

$$P_e \approx \frac{\sigma_n}{V_{RX} - V_S} \left(0.0284 \left[Q\left(\frac{V_S}{\sigma_n}\right) - Q\left(\frac{V_{RX}}{\sigma_n}\right) \right] + 0.0118 \left[\frac{V_S}{\sigma_n} \exp\left(\frac{-V_S^2}{2\sigma_n^2}\right) - \frac{V_{RX}}{\sigma_n} \exp\left(\frac{-V_{RX}^2}{2\sigma_n^2}\right) \right] + 0.1023 \left[\exp\left(\frac{-V_{RX}^2}{2\sigma_n^2}\right) - \exp\left(\frac{-V_S^2}{2\sigma_n^2}\right) \right] \right). \tag{10}$$

For example, with $V_S = 140$ mV, $V_{RX} = 200$ mV, $\sigma_n = 12$ mV_{rms},[10] and sampling in the middle of the eye, we obtain $P_e \approx 10^{-32}$.

In the presence of clock skew and jitter, the sampling point deviates from the maximum eye opening, rapidly raising the BER. (Since the ISI-induced jitter in the data waveform contains predominantly high-frequency components [19], the CDR circuit fails to track the corresponding phase variations.) For $t = 0$ to $t = T_1$ in Fig. 27(a), we approximate the eye opening as $V_{S,\text{eff}} = V_S[-(t/T_1)^2 + 1]$ and plot P_e as a function of the clock skew [Fig. 27(b)]. Here, the above values of V_S, V_{RX}, σ_n are used and $T_1 \approx 0.35\,T_b$.

We can now incorporate the effect of clock jitter by weighting (10) according to the jitter distribution, $g_{CK}(T_S)$, where T_S denotes the random departure of the sampling point from the center of the eye. As illustrated in Fig. 28(a), if g_{CK} places the sampling instant at T_S, then $V_{S,\text{eff}}$ is lower and the effect of g_n more pronounced. The error probability density function across the bit period can therefore be expressed as

$$g_{err}(T_S) = P_e|_{V_S(T_S)} \cdot g_{CK}(T_S). \tag{11}$$

Plotted in Fig. 28(b) for a Gaussian jitter distribution having an rms value of $\sigma_n = 4$ ps, this result reveals that errors are most likely to occur in the vicinity of $T_S = \pm 30$ ps, where the dramatic rise in P_e still compensates for the fall in g_{CK}. Beyond this point the clock jitter becomes so improbable that errors are less and less likely to occur.

The framework developed above can be used to formulate the trade-offs between required swings, additive noise, ISI, and tolerable clock jitter. For example, with $\sigma_n = 12$ mV_{rms} and $V_S/V_{RX} = 0.7$, the plots in Fig. 29 can be generated, where

[9]Simulations indicate that if the proposed model is altered to incur one more dB of error, the equalizer output suffers from 2.6 dB of additional vertical closure and 0.03 UI of additional jitter.

[10]The additive noise is obtained by integrating the noise at the output of the equalizer path up to 100 GHz.

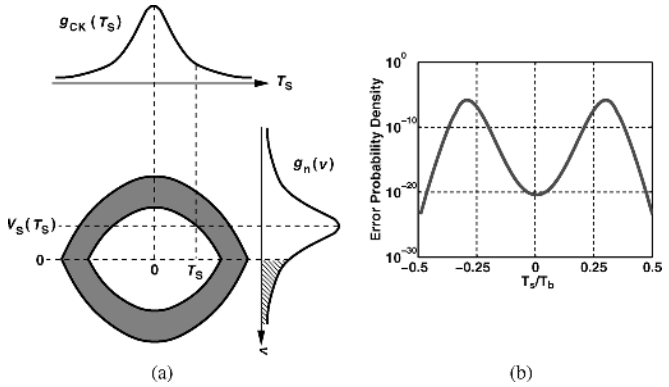


Fig. 28. (a) Error due to additive noise and clock skew. (b) Error probability density across the bit period.

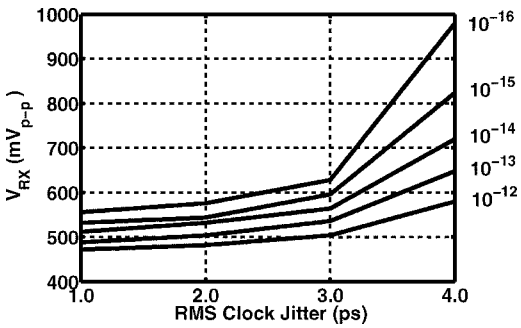


Fig. 29. BER curves for different combination of received swings and clock jitter.

each curve represents the acceptable combination of V_{RX} and σ_{CK} that yields a given BER. Worth noting here is the sharp rise in the required swing as the clock jitter exceeds 3 $\mathrm{ps_{rms}}$. Also, the experimental result in Fig. 23(b) indicates an rms jitter of 2.2 ps, which from Fig. 29, would dictate a minimum swing of 520 $\mathrm{mV_{pp}}$ for BER $= 10^{-13}$. This value is fairly close to the measured result of 640 $\mathrm{mV_{pp}}$ in Fig. 22.

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