Equalization and FEC Techniques for Optical Transceivers

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***Abstract*—In this tutorial paper, we present the application of well-known DSP techniques used in lower speed wireline and wireless applications, to high-speed optical communications. After an introduction on today's optical network architecture and typical optical channel impairments, we study techniques such as fiber equalization, maximum likelihood detection, and current and next generations Forward Error Correction (FEC), with special emphasis on VLSI implementation.**

***Index Terms*—Block processing, differential mode dispersion, fiber equalization, forward error correction, metropolitan-area networks, multi-mode fiber, polarization-mode dispersion, Reed–Solomon codes, single-mode fiber, turbo product codes, Viterbi detection, wide-area networks.**

I. Introduction

THE EXTREMELY rapid scaling of speed and bandwidth in optical networks over the past few years—close to a factor of two every nine months—has created a major challenge for electronic circuits used at the interface of the optical physical layer links [1]. For integrated circuits, Moore's law predicts the same factor of two scaling in 18 months. With the advent of dense wavelength division multiplexing (DWDM), a new degree of freedom was introduced to allow increasing capacity of optical networks independently from electronic circuits. The development of several key optical components allowed tremendous increase of the flexibility of DWDM networks and opened the possibility of efficiently performing networking functions directly in the optical domain. Example of such devices are optical amplifiers, optical add–drop multiplexers (OADM) (OADM devices are based on, for example, Bragg grating and optical wavelength mux/demux) [2] and optical cross connects using micromirror arrays based on micro-electro-mechanical systems (MEMS) technology [3], [4]. These systems offer a great cost-saving alternative to the more conventional time-domain multiplexing (TDM) approach (for example, SONET/SDH add/drop mux) which requires a large number of optical/electrical conversions (one per wavelength in a DWDM system). All-optical networks have therefore become possible and are today deployed in the core of the wide-area networks (WANs) for both economical and flexibility reasons. Electronic conversion circuits appear on the edge of the all-optical WAN infrastructure.

In local-area networks (LANs) and metropolitan-area networks (MANs) links are relatively short (less than 80 km) and recently based on simple point-to-point connections (e.g., gigabit and 10-Gb Ethernet). On the other hand, in the WAN, optical signals may traverse long distances (up to thousands of kilometers) and encounter numerous optical devices such as add/drop multiplexers, optical cross connects, and optical amplifiers. This causes degradation of the signal due to optical impairments in the long-haul link (discussed in Section II). Some of these impairments, such as chromatic dispersion, can be compensated optically. Dispersion compensating fiber (DCF) and optical polarization-mode dispersion (PMD) compensators are examples of such optical components. Optical compensation techniques have the advantage of not requiring high-speed IC technology. However, due to a lack of flexibility and the high cost of these solutions, electronic compensation may be a better choice for LAN/MAN point-to-point applications—where optical/electrical and electrical/optical conversions are a given. Section III describes integrated solutions for implementing fiber equalization in electronics integrated circuits using high-speed analog and DSP techniques. To counter the limitation of performance due to poor signal-to-noise ratio of the received signal, forward error correction (FEC) is today commonly used in high-speed (10 Gb/s and beyond) long-haul applications. FEC devices have widely been used in many lower speed applications; however, at speeds beyond 10 Gb/s, their implementation becomes extremely challenging due to excessive complexity and power consumption. Section IV of this paper is dedicated to FEC for optical applications.

II. Optical Channel Impairments

Historically, the optical fiber used to be considered as an infinite bandwidth medium. For current generation data rates, the optical fiber cannot be considered a perfect channel. In optical networks, signal degradation can be caused by a combination of electronic circuits, optical components, and fiber optics. In the electronics, interface circuits introduce timing jitter, shot noise in avalanche photodetectors, and thermal noise (e.g., trans-impedance amplifier). There are also optical sources of noise, such as relative intensity noise (RIN) in lasers and amplifier spontaneous emission (ASE) noise in optical amplifiers. Optical fibers introduce loss, dispersion, and nonlinearities (causing the well-known four-wave mixing effect in DWDM networks). In this paper, we will neglect contributions

Manuscript received July 25, 2001; revised October 16, 2001.

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Publisher Item Identifier S 0018-9200(02)01697-9.

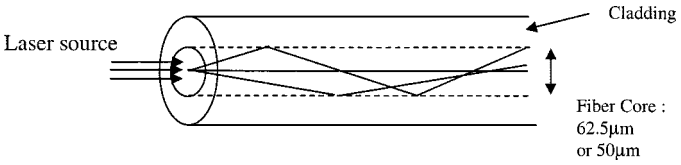


Fig. 1. DMD in MMF.

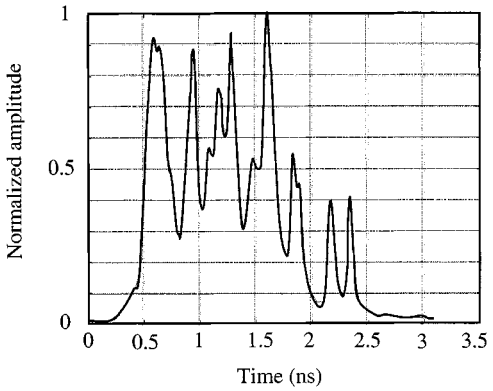


Fig. 2. Measured impulse response of a MMF.

from nonlinearities (this is possible for low transmit power levels, on the order of a few milliwatts). A general overview of impairments in optical fibers is presented in [5] and [6]. To better understand the optical channel, we briefly describe dispersion in multi-mode and single-mode fibers.

A. Multi-Mode Fiber

Multi-mode fibers (MMFs) are used in LANs and back-plane applications over short distances (up to 300 m) in the enterprise networks. Due to their thicker core (typically 62.5 μm) compared to single-mode fiber (SMF) (9 μm) and ease of termination, they are usually the fiber of choice for vertical backbones inside a building (LAN infrastructure). They are also used in conjunction with lower cost laser technology such as vertical-cavity surface-emitting lasers (VCSELs). There are different propagation delays for each mode of the fiber, which causes a dispersion called differential mode dispersion (DMD), illustrated in Fig. 1.

As a consequence in the case of MMF, the impulse response of the optical fiber is a set of discrete pulses (corresponding to different modes of propagation) appearing with different amplitudes at different time instances. A measured impulse response for a 1-km MMF, with 850-nm VCSEL is shown in Fig. 2.

When taking into account bandwidth limitations in the electronics circuits used with MMF, the overall impulse response has a Gaussian shape (in the above measurement, wide-band equipment was used). The spread of the fiber impulse response is on the order of few bit periods at gigabit rates, and few tens of bit periods at 10-Gb/s rates. This causes inter-symbol interference (ISI) which can be compensated using equalization techniques as described in Section III. To a first order, the spread of the impulse response grows linearly with the length of MMF.

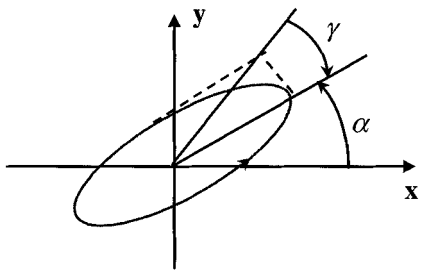


Fig. 3. Representation of polarization states.

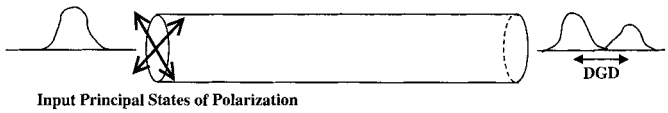


Fig. 4. Polarization mode dispersion in SMF.

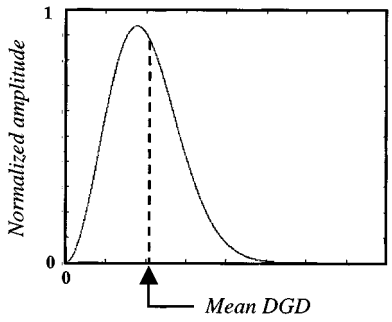


Fig. 5. DGD statistical distribution.

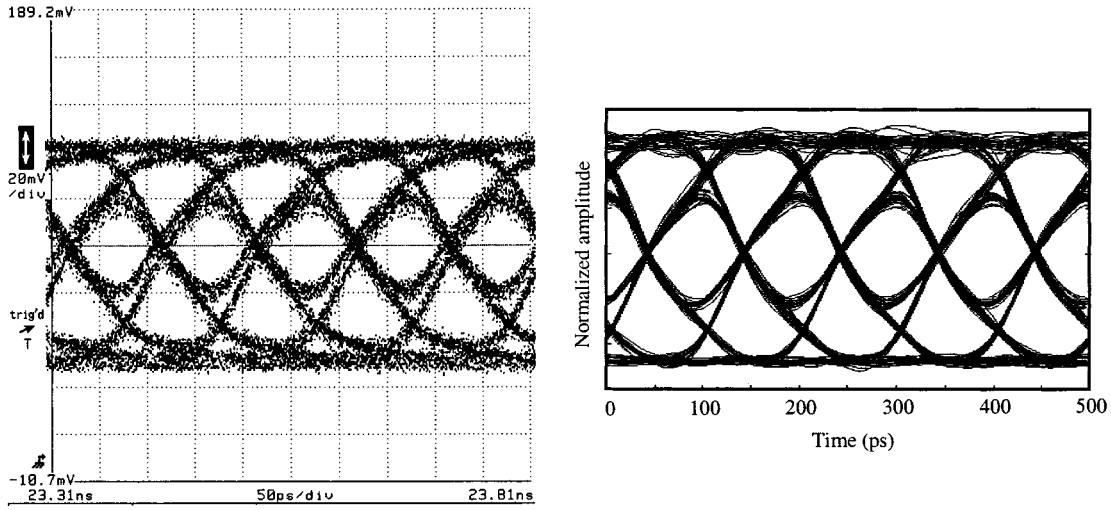
B. Single-Mode Fiber (SMF)

As indicated by their name, ideal SMFs have only one mode of propagation, thus avoiding the previous type of dispersion. However, over long distances (beyond tens of kilometers), irregularities such as random variations in the geometrical section of the fiber and nonsymmetrical mechanical stresses (bending, spinning) induce birefringence in the SMF (a very slight difference of refractive index for different cross-sectional orientations). This produces severe signal degradations at speeds of 10 Gb/s and beyond.

Let us choose a cross-sectional x–y reference frame to describe the optical field components. By normalizing the amplitude of the optical signal $|s\rangle$, all states of polarizations can be obtained by considering two parameters: the relative phase difference and the relative amplitude of the propagating waves along the x and y axes. With these two degrees of freedom, the state of polarization is mathematically described using the Jones representation

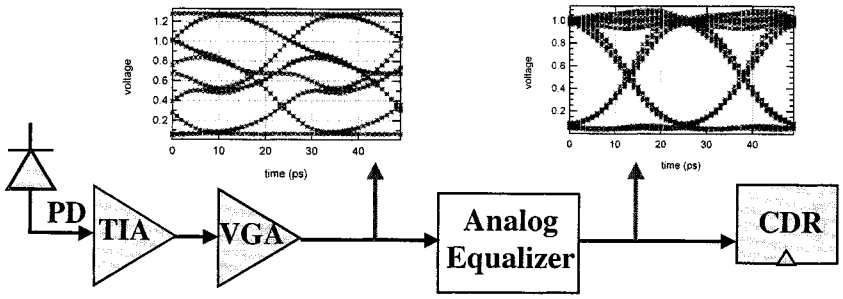
$$|s\rangle = \begin{pmatrix} \cos(\theta/2)e^{-i\Delta/2} \\ \sin(\theta/2)e^{+i\Delta/2} \end{pmatrix} \cong \begin{pmatrix} \cos(\alpha)\cos(\gamma) - i\sin(\alpha)\sin(\gamma) \\ \sin(\alpha)\cos(\gamma) + i\cos(\alpha)\sin(\gamma) \end{pmatrix}.$$

The parameters (α, γ) give a graphical representation of the states of polarization in the x–y plane (Fig. 3). Named after this latter graphical representation, polarization is in general elliptic, linear ($\gamma = 0$), or circular ($\gamma = \pm\pi/4$).

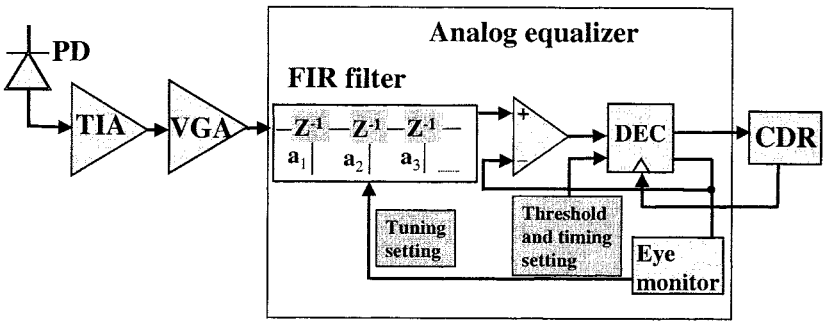


(a) (b)

Fig. 6. (a) Measured and (b) simulated PMD in an SMF.



(a)



(b)

Fig. 7. (a) Analog fiber equalization simulation results. (b) Analog feed-forward equalizer architecture.

Birefringence gives rise to a fast and a slow principal state of polarization. A single pulse at the fiber input is split into two pulses at the output of the fiber, as shown in Fig. 4. The difference of their arrival time at the other end of the link is called differential group delay (DGD).

Birefringence can be considered as a random variable that grows in a random-walk fashion along the fiber propagation axis. Consequently, the DGD follows a Maxwellian distribution (Fig. 5). The DGD value could vary statistically to large numbers and PMD compensation systems may need to handle relatively large DGD values even if the average DGD is reasonably small with respect to the bit period. The statistical information given by those random quantities is applicable to a population of fibers built through similar manufacturing processes and used in similar field conditions. Another important property of PMD was discovered by Foschini and Poole, who showed—through stochastic analysis—that the rms DGD is proportional to the square root of the fiber length [7], or in other words, the magnitude of PMD doubles when the length of the fiber link quadruples. The proportionality coefficient (often expressed in $\mathrm{ps}/\sqrt{\mathrm{km}}$) quantifies the magnitude of this random phenomenon independently of the length of the link and is a reference number used to characterize a homogeneous population of fibers (provided by fiber manufacturers) with respect to PMD.

In the case of a first-order model, it can be shown that the output electrical signal ($signal(t)$) can be expressed as

$$signal(t) = \kappa s\left(t - \frac{\tau_0}{2}\right) + (1-\kappa)s\left(t + \frac{\tau_0}{2}\right)$$

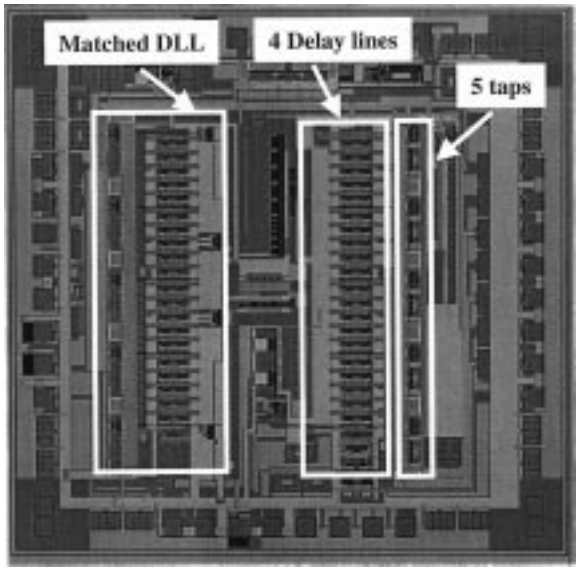


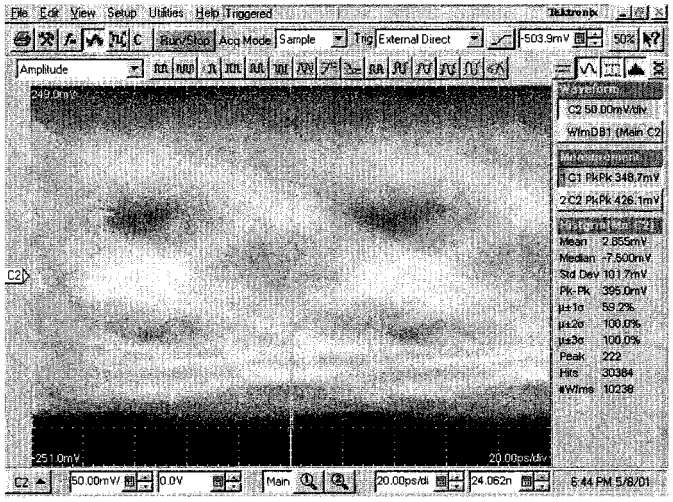
Fig. 8. A 10-Gb fiber equalizer micrograph.

where $s(t)$ is the input electrical signal, κ is a parameter which depends on the input polarization conditions ($0 \leq \kappa \leq 1$), and τ_0 is the value of the DGD. The overall channel in the above equation is linear. Fig. 6 shows measured and simulated eye diagrams at the output of a high PMD optical link. In this experiment, we generated PMD by concatenating two short High-Birefringence fibers (50 ps DGD each).

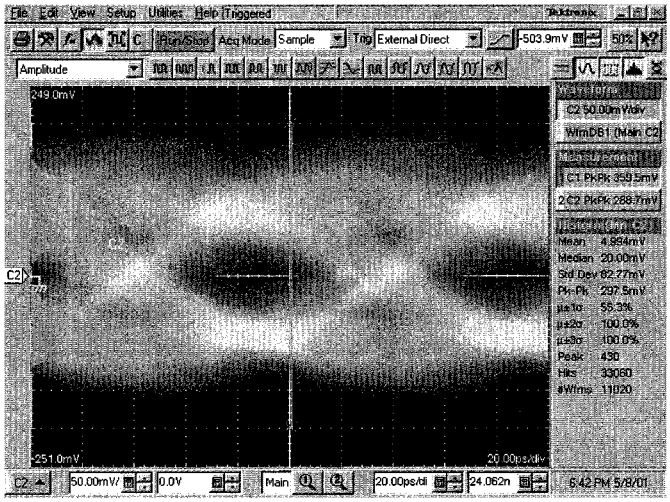
Higher order PMD effects result in general in nonlinear effects in the electrical domain, despite the fact that the channel is linear in the optical domain. Using simulation models, it is possible to produce fairly accurate simulation results for PMD in SMF (without optical nonlinearities) as demonstrated in Fig. 6(a) and (b), which shows, respectively, measured and simulated eye diagrams of a 10-Gb/s bit-stream distorted by ISI caused by PMD. Fig. 6 shows a good agreement between measurements and simulations based on simple theoretical fiber models. Having introduced dispersion, we now present techniques for electrically compensating dispersion in single-mode and multi-mode fibers in Section III.

III. Fiber Equalization

Adaptive equalization has been widely used in communications applications such as voice-band modems, wireless, digital subscriber lines, and ISDN, and even at rates close to 1 Gb/s in disk drives. However, implementation of equalization at rates exceeding 10 Gb/s for optical applications is not so straightforward. Previous work [8] proposed the general concept of electrical compensation of DMD in MMFs, and in [9]–[11] board-level implementations of 10-Gb/s electrical fiber equalization have been reported. The main challenge in the implementation of high-speed digital equalization resides in the design of a >10 GS/s analog-to-digital (A/D) converter. Therefore, purely analog equalization can be a more practical alternative to digital equalization [Fig. 7(a) and (b)]. Fig. 7(a) shows how an analog equalizer is inserted within a conventional receiver path that contains a linear transimpedance amplifier



(a)



(b)

Fig. 9. A 10-Gb SMF equalization. (a) Optical channel output (input to equalizer). (b) A 10-Gb/s fiber equalizaer output eye diagram.

(TIA), a linear variable gain amplifier (VGA), and the clock and data recovery (CDR) on the other hand. Fig. 7(b) shows some of the internal details of the analog equalizer chip, implemented using analog delay lines, wide-band digitally programmable multipliers, and a digital tap adaptation algorithm. Tap adaptation can be performed using the least-mean square (LMS) algorithm or eye monitoring techniques [11]. Such an equalizer can be used for extending distances of 10-Gb/s bit streams over MMF up to 300 m, and compensating up to 50 ps DGD for SMF, increasing operating distances of SONET/SDH and emerging 10-Gb Ethernet networks. This equalizer was implemented in a 0.25-μm SiGe technology of Agere Systems (Fig. 8). The chip size is 2.5×2.5 mm^2. Fig. 9 illustrates measured results of SMF equalization using this device. In this experiment, the signal bit rate was 10 Gb/s and the channel was an SMF of PMD $= 50$ ps (using a PMD emulator), with a receiver that had less than 10-GHz bandwidth.

Assuming high-speed A/D conversion can be implemented at high rates of 10 GS/s and beyond, DSP based equalization offers a more accurate and higher performance alternative to analog equalization. The general structure of a DSP-based fiber

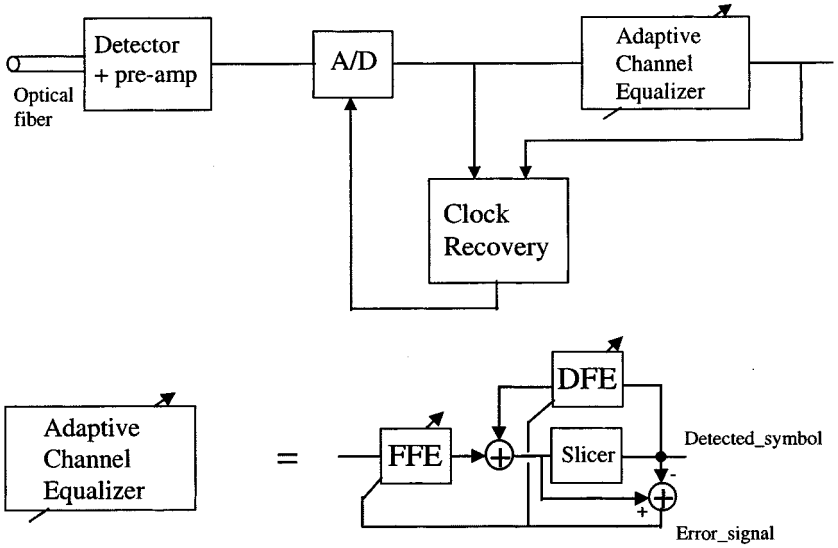


Fig. 10. DSP-based fiber equalization.

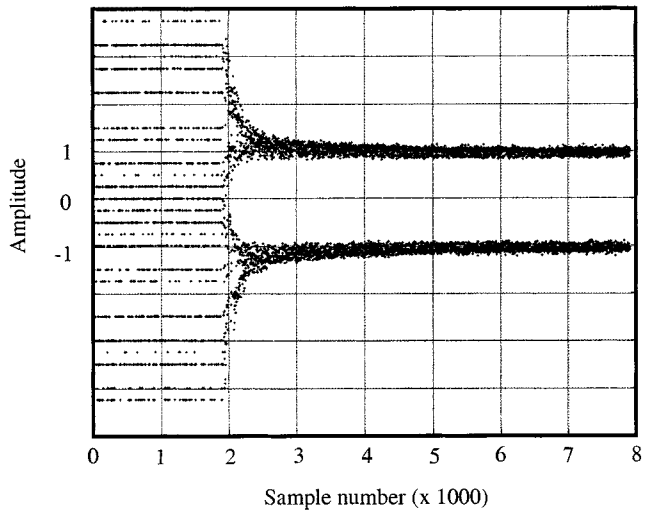


Fig. 11. DSP equalization experiment with MMF.

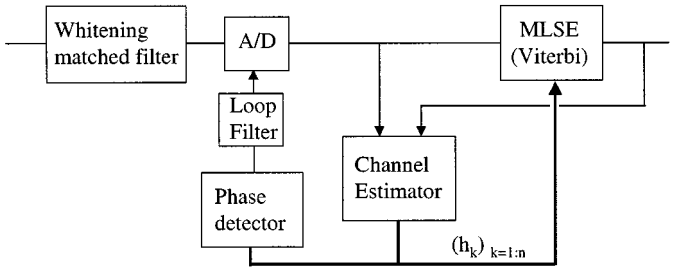


Fig. 12. MLSE optical receiver.

equalizer setup described here is shown in Fig. 10. In this experiment, a 1-km-high DMD MMF was used in conjunction with an 850-nm VCSEL delivering an 8-b/10-b encoded 1.25-Gb/s bit-stream (Gigabit Ethernet 1000BASE-X).

It is obviously very important that the optical detector must be kept linear (no internal hard decisions or slicing), otherwise performance of the digital equalizer would be compromised. Here, A/D conversion was performed using a 4-GS/s digitizing scope, which generated a long electrical waveform. This waveform was then oversampled by a large factor to create an approximation of a continuous-time waveform. The setup of Fig. 10 was then implemented using MATLAB simulations of timing recovery (absolute transmit frequency was unknown) and adaptive digital equalization. In this experiment, design parameters were: 5-b A/D, five-tap feed-forward equalizer (FFE), and three-tap decision feedback equalizer (DFE). Ninety-six ps peak-peak jitter was added to the input signal sampling phase. Achieved output SNR was 24 dB after equalization. Fig. 11 shows the simulation result showing a completely closed eye, and a "clean" nonreturn-to-zero (NRZ) signal after equalization (equalizer tap adaptation starts at sample #2000).

Performance can be further improved using maximum likelihood sequence estimation (MLSE). MLSE is commonly used in disk drives. However, as opposed to disk-drive applications where the recording channel can be characterized beforehand, optical channels (depending on fiber type and length) are not known *a priori*. This requires channel estimation, and flexible trellis decoding (or adaptive Viterbi decoding) as shown in Fig. 12. In the case of the above MMF channel, MLSE provides 3-dB improvement over the adaptive equalizer.

In Fig. 12, channel estimation provides the discrete impulse response of the channel. This is used to construct the trellis corresponding to the ISI channel, as well as to generate a timing function for baud-rate timing recovery.

Now let us discuss the main implementation challenge: how to implement A/D conversion and digital signal processing functions at multi-gigabit rates. One solution to alleviate speed limitations in the A/D converter and DSP implementation is to use parallel processing or interleaving, as illustrated in Fig. 13. The circuit design difficulty is now concentrated in the design of an interleaved up-front track and hold. In a 10-GS/s system, this would require accurate 100-ps spacing between subsampling phases.

Even though in the case of feed-forward equalization block processing seems relatively straightforward, it is not so simple in the case of a DFE, due to the feedback loop and quantization

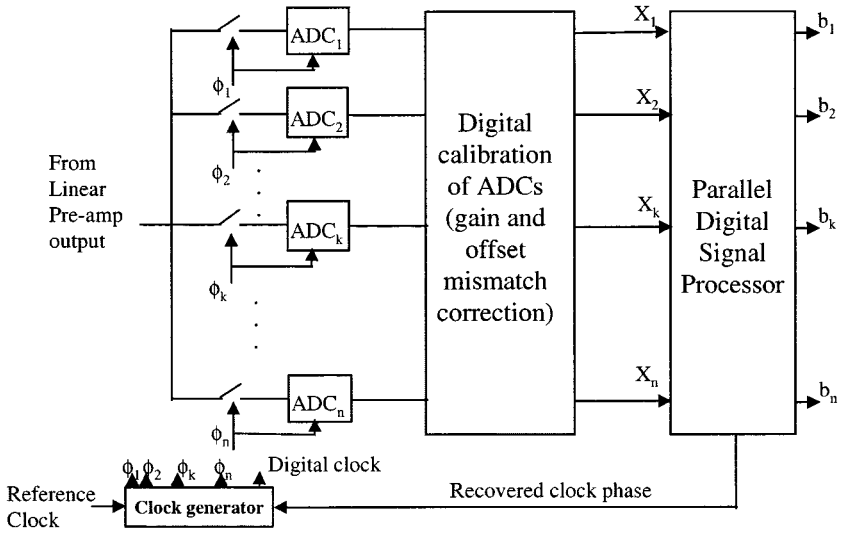


Fig. 13. Block processing DSP architecture.

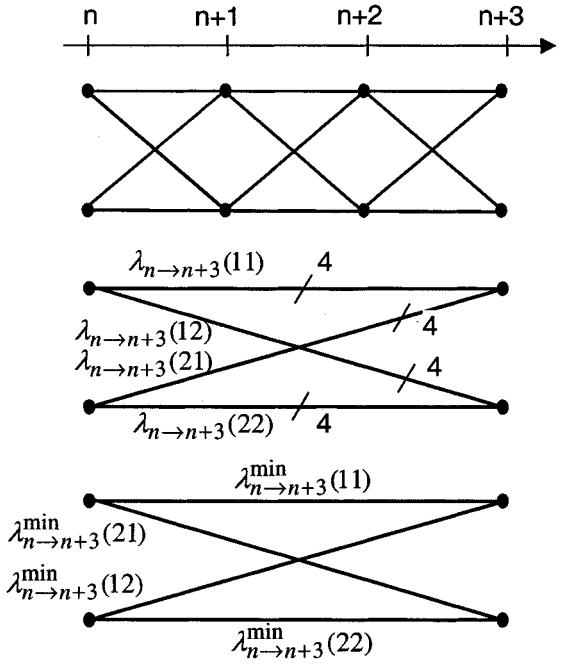


Fig. 14. Trellis collapsing Viterbi decoder.

within the loop. However, a look-ahead architecture with speculative computations can be introduced to arbitrarily speed up the DFE [12]. Viterbi decoders can also be implemented using parallel processing as reported in [13]–[15].

One technique is based on trellis collapsing [13], shown in Fig. 14. In the example of Fig. 14, three time steps are merged into a single step by considering all possible transitions (4 in this case) from a starting state (time n) to an ending state (time instant $n+3$). By computing the minimum distance path for each [starting state $\rightarrow$ ending state] transition, a branch metric can be obtained (Fig. 14).

Another technique called "sliding window Viterbi" has the interesting feature that the complexity increases only linearly with the parallel processing factor [13]–[15]. Viterbi decoding is performed on overlapping windows of data. A high-throughput decoder is implemented using many Viterbi decoders in parallel, where each of them is sequentially decoding its own time window and does not require information from other decoders. In order to allow for synchronization (initial state is unknown) and trace-back operation, it is necessary to allow for some overhead as shown in Fig. 15.

IV. Forward Error Correction

FEC is already used in many long-haul optical systems. It helps to relax SNR requirements by introducing a relatively small overhead in the transmitted signal (overhead on the order of few percent). In long-haul applications, there are currently two FEC standards. "In-band" FEC is used in SONET/SDH framing protocol, where redundant bits are inserted inside available overhead bytes of SONET/SDH frames. Due to the limited number of available bytes, the code chosen was a 3-bit error-correcting BCH code. For greater coding performance, submarine systems have recommended a coding that requires increase of the transmitted rate by 7% (out-of-band signaling) and provides a simple framing with a synchronization byte. This code is based on a Reed–Solomon RS(255, 239) code and is specified in the ITU-T G.975 recommendations.

Reed–Solomon codes are a nonbinary subclass of BCH codes [16]. The RS(255, 239) code can correct up to $t = 8$ random symbol errors. The RS(255, 239) code has a coding gain of around 5.5 dB at a bit error rate (BER) of 10^{-12} and the output BER can be reduced to 10^{-15} given an input BER of 10^{-4}. Another interesting property of RS codes is their burst-error-correcting capability. A single RS(255, 239) code can correct bursts of length up to 64 bit. This can be further increased using block interleaving, where encoding is carried out row-wise while codeword symbols are transmitted column-wise such that long bursts of errors get distributed into multiple code words and essentially the number of errors in each code word gets reduced. A 16-way interleaved RS(255, 239) code is recommended by ITU-T [17] which can correct bursts up to 1024 bit. In this section, we first give an overview of the encoding and decoding of RS codes, then present

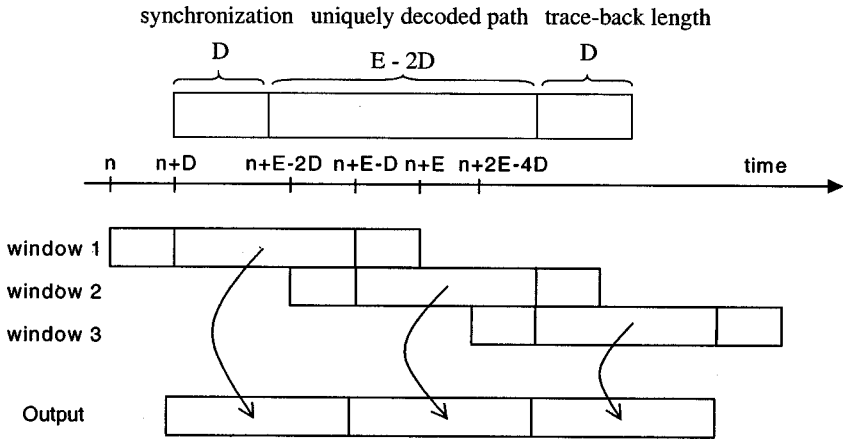


Fig. 15. Sliding window Viterbi decoding.

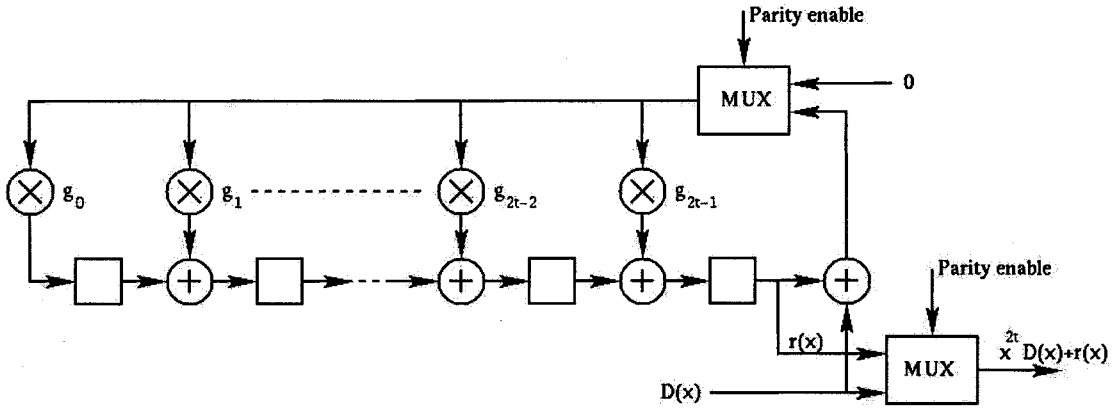


Fig. 16. RS encoder architecture.

the design and implementation results of a single-chip quad 2.5-G/10-G FEC device for optical communication. Finally, we recommend other candidate FEC codes with larger coding gains for future optical communication systems.

A. RS Encoding

RS codes are linear cyclic codes and hence can be defined by a generator polynomial $G(x)$. The generator polynomial of RS(255, 239) code is chosen such that 16 consecutive powers of α are roots of $G(x)$, i.e.,

$$G(x) = \prod_{i=0}^{15} (x - \alpha^i)$$

where α is a root of a binary primitive polynomial $p(x)$ of degree 8 that generates the Galois field GF(2^8). All valid code word polynomials are multiples of $G(x)$.

Suppose that $D(x)$ is an information polynomial. RS encoding can be carried out as follows:

$$c(x) = D(x) \cdot x^{16} + \langle D(x) \cdot x^{16} \rangle_{G(x)}$$

where $\langle \cdot \rangle_{G(x)}$ denotes the remainder polynomial after division by $G(x)$, whose coefficients correspond to the parity check bytes $r(x)$. It is not difficult to verify that the code word polynomial $c(x)$ obtained in such a way is a multiple of the generator polynomial $G(x)$. Hence, encoding of an RS code involves long polynomial divisions over GF(2^8). A serial RS encoder can be implemented using a linear feedback shift register as shown in Fig. 16, which has a throughput rate of one symbol per cycle.

B. Decoding

Suppose that $c(x)$, $v(x)$, and $e(x)$ are the transmitted code word polynomial, the received polynomial, and the error polynomial, respectively, with the relation $v(x) = c(x) + e(x)$. The syndrome-based RS decoding consists of three steps [16]:

1) Compute the syndrome polynomial $S(x) = \sum_{i=0}^{2t-1} s_i x^i$, where $s_i = v(\alpha^i)$, $i = 0, \ldots, 2t$.
2) Solve the key equation $S(x) \cdot \Lambda(x) = \Omega(x) \bmod x^{2t}$, to find the error locator polynomial $\Lambda(x)$ and error evaluator polynomials $\Omega(x)$.
3) Compute the error locations and error values using Chien Search and Forney's algorithm, respectively.

C. A Quad 2.5G/10G FEC Device

An FEC optical networking interface device that implements both an in-band BCH-3 code as well as an out-of-band RS(255, 239) code has been designed and fabricated. This device supports an 8-way interleaved BCH-3(4359, 4320) code, as well as 16-way interleaved RS FEC in quad 2.5-Gb/s mode, and 16/64-way interleaved RS FEC in 10-Gb/s system payload rates.

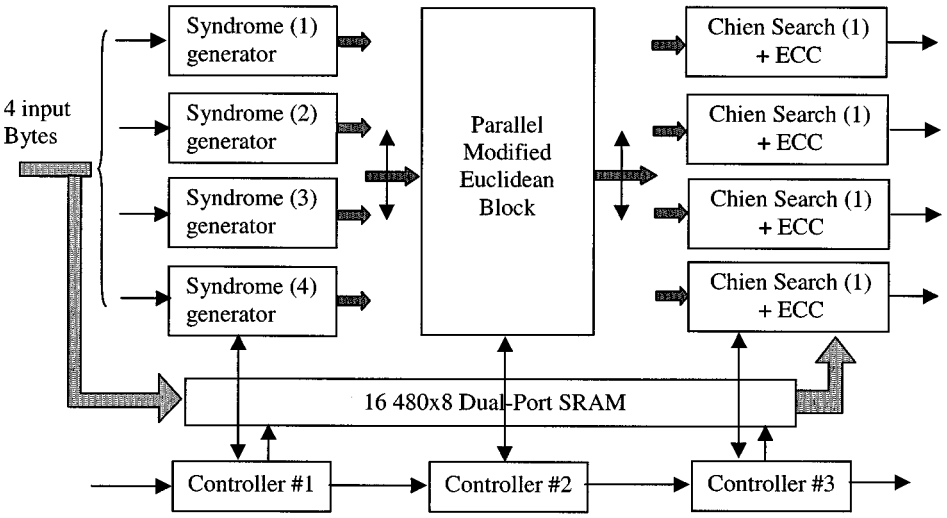


Fig. 17. Block diagram of one decoder slice.

The architecture design and some implementation results of the RS decoder in this device are presented in this section.

1) Decoder Data Path Architecture: Sixteen hardware decoders are implemented to support 16/64-way interleaving. These are partitioned into four decoder slices to support the four independent channels in the Quad 2.5-Gb/s operating mode. Each decoder slice contains four syndrome generators, one shared key equation solver block, and four Chien Search blocks. The latency of the syndrome generator and the Chien Search block is 255 cycles, while the key equation solver block has a latency of 16 cycles. Time-multiplexing one key equation solver block among four decoders leads to substantial hardware savings as it is the most complicated block in RS decoding. The top-level block diagram of one decoder slice is shown in Fig. 17.

2) Parallel Implementation of the Modified Euclidean Algorithm: The second step in RS decoding of solving the key equation is the most challenging process. In general, it can be carried out using either the Berlekamp–Massey algorithm or the Euclidean algorithm [16]. Both algorithms find the error locator polynomial $\Lambda(x)$ and error evaluator polynomial $\Omega(x)$ within $2t$ iterations (where t is the maximum number of correctable errors), and each iteration requires Galois field multiplication and division operations. These are not suitable for high-speed implementations. Fortunately, the expensive division operation in both algorithms can be replaced by multiplications. A modified division-free Euclidean algorithm can be found in [18]. An inversion-less Berlekamp–Massey algorithm can be found in [19], [20]. When the actual number of errors is less than t, the error locator and error evaluator polynomials can be found in less than $2t$ cycles. We took advantage of this fact to design a low-power parallel implementation of the modified Euclidean algorithm by terminating the computation earlier and putting the entire block into a built-in low-power mode. Readers are referred to [21] for a detailed description of this parallel implementation and comparisons with a serial implementation of the Euclidean algorithm, as well as implementations of the Berlekamp–Massey algorithm.

3) Control Mechanism for Power Reduction: As the functional blocks of the RS decoder are naturally divided into three subblocks according to the three decoding steps, three control circuits are implemented in the RS decoder, one for each decoding step. The start-of-frame pulse resets and starts a new computation in the syndrome generator controller. Upon completion and in case of errors, this syndrome generator controller issues a start-pulse signal to trigger the computation of the key equation solver block; then completion of the key equation solving triggers the Chien Search and error correction.

A testing circuit is implemented after the syndrome generator to check if there are errors in the received block. If all syndromes are zero, then the rest of the decoder is put into low-power mode and the received block is output unaltered. For an input BER of around 10^{-4}, errors occur about 20% of the time; for an input BER of 10^{-5}, only the syndrome generator needs to be active most of the time. As a result, the three-step control circuitry allows the decoder to take advantage of the input BER statistics to save average power consumption.

4) Automatic Disable of Error Correction Upon Detection of Uncorrectable Errors: A salient feature of this RS decoder is that it can disable the error correction automatically when uncorrectable errors are detected, hence prevent the decoder from further corrupting the data. In the case when the number of symbol errors is $N_e \leq t$, the error locator polynomial $\Lambda(x)$ computed in the previous step has exactly N_e roots in GF(2^8) which can be found through exhaustive search (Chien Search). However, when the number of errors exceeds the maximum number of correctable errors t, this case can be detected by a discrepancy between the degree of $\Lambda(x)$ and the number of roots found from Chien Search. When uncorrectable errors are found, error correction is automatically disabled and the decoder is bypassed.

5) Implementation Results: The decoder outputs the decoded data as well as the error correction information, including the total number of corrected symbols and the total number of uncorrectable blocks within one frame. Implemented in Agere Systems 0.16-μm CMOS technology, the encoder has a gate count of about 100 K; the decoder has a gate count of 1.8 M and an estimated power consumption of 350 mW. The die photo of this device is shown in Fig. 18.

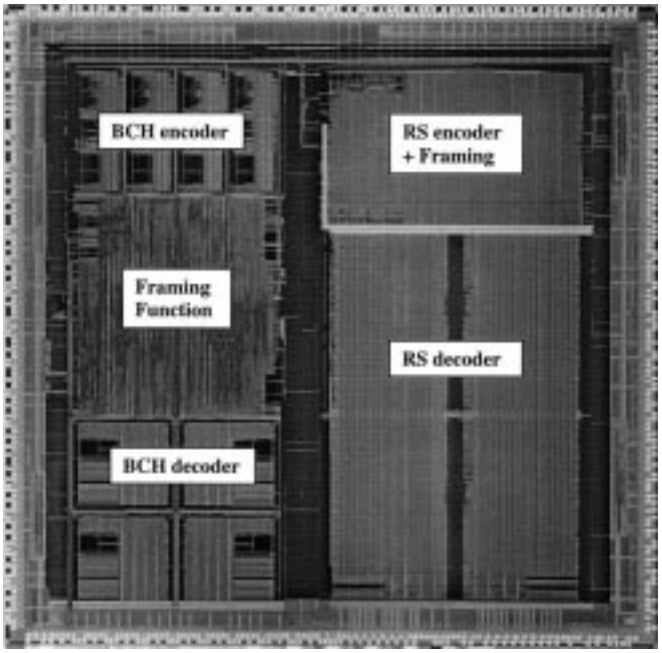


Fig. 18. TFEC—10-Gb/s FEC die photo.

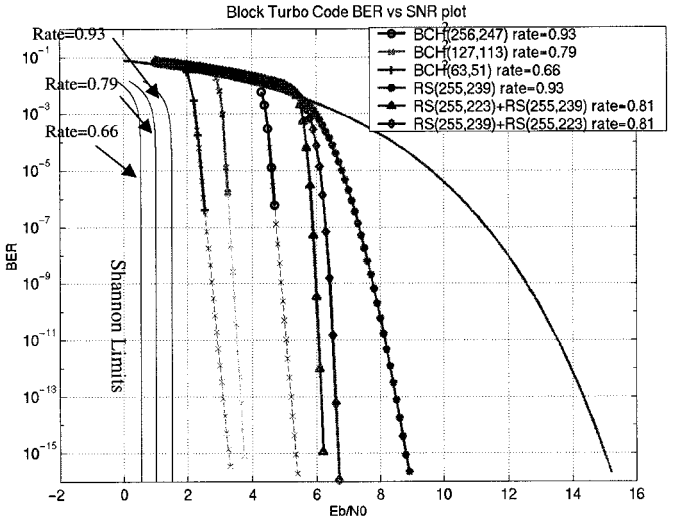


Fig. 19. Block turbo code performances for different component codes.

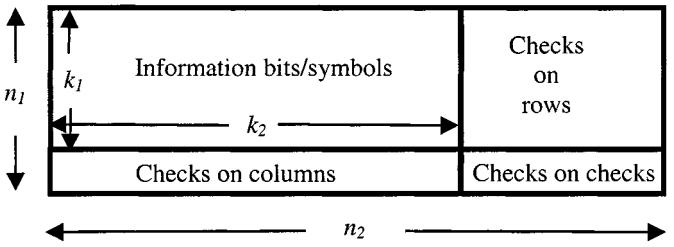


Fig. 20. A 2-D product code.

D. Future FEC

1) Higher Performance Codes: For optical communication systems with a bit rate of 10 Gb/s and beyond, more powerful FEC codes with larger coding gain and relatively low overhead are desirable. Some possible candidate codes include, but are not limited to, concatenated Reed–Solomon codes [22] and block turbo codes [23]. Fig. 19 shows the performance of these codes and their distance from the Shannon limit. As can be seen, the concatenated RS code has 1–2 dB additional coding gain; and the block turbo code can add around 5-dB gain in addition to the 5.5-dB coding gain of the RS(255, 239) code.

2) Block Turbo Codes: Product codes are serially concatenated codes of two or more dimensions. Turbo product codes or block turbo codes (BTC) are product codes decoded with a turbo decoding process. A commonly used two-dimensional (2-D) product code is shown in Fig. 20. Each row is a systematic code (n_1, k_1, d_1) and each column is a systematic code (n_2, k_2, d_2). The component error correction codes are usually algebraic codes such as BCH or Reed–Solomon codes. Each information bit is thus protected by two independent codes and will be checked twice or have more than one opportunity to be corrected. Interleaved product codes have traditionally been used in applications where long burst errors are common and high coding gain is required, such as in CD-ROMs.

Traditional product codes use an iterative decoding process—hard decisions are sent to the decoder and decoding is done by rows and then by columns and then iteratively. An uncorrectable bit error, in one dimension, can be—quite possibly—corrected by the other dimension. A product code is thus much more powerful than its component codes. The minimum Hamming distance of a product code is $d_1 * d_2$, where d_1 and d_2 are the minimum Hamming distances of the component codes [23]. A turbo decoding process for product codes with soft decisions was first proposed by Pyndiah [23]. In this decoding technique, the decoder takes soft inputs and generates soft outputs containing reliability information or log–likelihood ratio (LLR) defined as $\log[P(d = +1|x)/P(d = -1|x)]$), where d is a symbol, and x is the observation (soft value). The increased knowledge gained from the decoding is referred to as "extrinsic" information and is fed back to the decoder. Initially no *a priori* knowledge is given and the LLRs are therefore initialized to 0 [since $p(d = 0) = p(d = 1) = 0.5$]. However, through iterative decoding and LLR updates, [$p(d = 0)$, $p(d = 1)$] will hopefully approach either $[0, 1]$ or $[1, 0]$. The number of iterations required is usually fairly small, around 4 to 6 [23], [24].

Each decoding iteration consists of sequential soft decision decoding of rows followed by soft decision decoding of columns. This step in turn is followed by another iteration of sequential horizontal and vertical decoding. Since conventional BCH decoding is based on hard decision decoding, Pyndiah suggested to allow for soft decision decoding by using the following simple search procedure: p least reliable bits are first chosen in a code word to form 2^p possible test error patterns. Each test pattern is then corrected using a standard one-dimensional hard-decision BCH decoder. The corrected results are stored and the best (with the minimum Euclidean distance to the received vector) is chosen as the output code word, and used to compute new LLR information.

BTCs have the potential to achieve a performance close to the Shannon limit. Because of the power of turbo iterative decoding and the complexity involved, the component codes of

BTCs are usually chosen to be simple codes. The performance of BTCs with component codes of BCH(256, 247), BCH(127, 113), and BCH(63, 51) are shown in Fig. 19. Their performances are very similar to other turbo codes and are relatively close to the Shannon limit. As a comparison point, Fig. 19 also shows the performance of RS(255, 239) and its two variants of concatenation with RS(255, 223) (RS1 + RS2 designates RS1 is the inner code and RS2 is the outer code). Unlike other high-performance codes (e.g., low-density parity check codes), BTCs are very regular and thus lead to regular architectures. Furthermore, the component codes of BTCs are usually very simple and use simple decoding procedures. These properties make BTC a good candidate for future high-speed optical systems.

V. Conclusion

With extremely rapid scaling of capacity in optical networks, the number of optical wavelengths (as well as the bit rate per wavelength) has dramatically increased; so have impairments in the optical channel. It has become necessary to compensate impairments such as PMD and chromatic dispersion. Recently system-level electrical compensation circuits have been reported for 10-Gb/s PMD compensation. In this paper, we described integrated analog and DSP-based implementation techniques for compensating dispersion. In order to relax SNR requirements, it has also become necessary to implement complex FEC schemes at rates in excess of 10 Gb/s. After an architectural overview of a Reed–Solomon code used in 10-Gb/s optical systems and a reference VLSI design, we presented a performance comparison of several candidate codes such as concatenated RS codes and BTCs, for use in next-generation optical networks.

Acknowledgment

The authors wish to thank S. Hunsche and T. Woodward of Lucent Technologies for providing them with lab data of multimode fiber impulse responses and measured output waveforms, Z. Yu for help with MMF equalization simulations, and A. Healey from Agere Systems for help with the fiber equalizer test setup and measurements.

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