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Equivalent Circuit Model Analysis of Vertical Impact Ionization MOSFET (IMOS)

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Abstract

In this paper, an equivalent circuit model is proposed that describes the avalanche and snapback characteristics of Vertical Impact Ionization MOSFET (IMOS). The equivalent circuit model is constructed using MOS transistors that represent the avalanche characteristics. The main goal is to predict the vertical IMOS integrated circuits by using circuit simulations. The vertical IMOS is predicted to have a lower subthreshold slope and high ratio of current. Besides that, the equivalent circuit model is explained which is include the parasitic bipolar transistor with a generated-hole-dependent base resistance. The models for parasitic bipolar is combined with a PSPICE MOS transistor model and it is represented the gate bias dependence of snapback characteristic. The equivalent circuit parameters are extracted from the reference experimental values of previous research and modified to reproduce the measured avalanche and snapback characteristic of the vertical IMOS transistor. The results show that 90% of the analysis subthreshold slope value of circuit simulations similar to the reference experimental value. The ratio of the current also shows almost the same behavior. Therefore, the equivalent circuit model for vertical IMOS can be used in circuit simulations.