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Equivalent Circuit Model of a Pulse Planar Transformer and Endurance to Abrupt dv/dt

Loreine Makki[2], Antoine Laspeyres[1], Corentin Darbas[1], Anne-Sophie Descamps[1], Marc-Anthony Mannah[2], Christophe Batard[1] and Nicolas Ginot[1]

1. CNRS, IETR UMR 6164, Nantes Université, F-44000 Nantes, France
2. Lebanese international University

***Abstract*—Wide band gap (WBG) semiconductor materials offer faster and more reliable power electronic components in electric energy conversion systems. However, their faster switching speed and abilities to operate at higher frequency than silicium devices have brought new challenges such as Electromagnetic interference (EMI) issues. In gate driver applications, EMI issues must be tackled given the close proximity between gate driver systems and WBG power modules. This paper focuses on planar pulse transformers for gate drivers in high power applications (3,3kV, 500A SiC module). This study tries to give a standard procedure to design then simulate pulse transformers with their electrostatic shielding. First, a design guideline using Altium Designer is proposed to respect European standards. A method to extract the transformer design from Altium to Ansys is also proposed. Finally, a frequency analysis is discussed to use in Ansys simulations and parameters extraction. Tests have been performed to check the proposed transformers EMC immunity under a $125\,\mathrm{kV\,\mu s^{-1}}$ common mode transient immunity (CMTI) test.**

***Index Terms*—SiC MOSFET, driver circuits, pulse transformer, planar transformer, Altium Designer, Ansys Q3D, ElectroMagnetic Compatibility (EMC)**

I. Introduction

In high power applications ($>100\,\mathrm{kW}$), dedicated gate drivers are often used to operate power semiconductor devices. They must provide an optimal command for power semiconductors using an electrically insulated circuit. Gate drivers design can be divided into 4 functions [1]: the transmission of command orders through the galvanic isolation, the isolated power supply, the output stage and the protection functions such as short circuit protection.

A. Gate driver functions

The transmission of command orders through the galvanic isolation is often realized by digital isolators or pulse transformers. Fig. 1 illustrates a typical structure used in recent gate drivers such as the CMT-TIT8244 from Cissoid [2] or the CGD1700HB3P-HM3 from Wolfspeed [3].

To drive power semiconductors, an open loop DC-DC converter is used for the isolated power supply. Transformer based converters using push-pull topologies are widely used. As the power consumption is low in gate driver applications ($<5\,\mathrm{W}$), these topologies' efficiency and good EMI while being simple to design make them attractive [4].

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The output stage circuit is placed as close to the power semiconductor as possible to drive it. Even if the mean power consumption is low, a gate current inrush of several amperes is needed to turn-on and turn-off power semiconductors. The output stage allows signal buffering in order to drive the gate voltage of the power transistor. To drive SiC MOSFETs, gate voltage applied by the output stage ranges from +20/-5 V for second generation SiC devices to +15/-4 V for third generation ones.

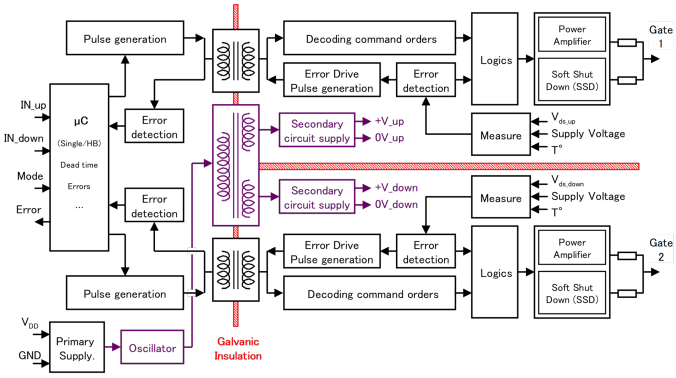

Fig. 1. Basic structure for gate drivers using pulse transformers [1]

In recent gate drivers, various protection functions are implemented. This allows the gate driver to detect or prevent abnormal operations of the power component. In high power applications, three main features are often available. An overcurrent detection method detects short circuits and turns off the power component as fast as possible to avoid short circuit failure and the component destruction. Anti-overlap protection system prevents both power components to turn on at the same time to avoid short-circuit situations. Under voltage lockout (UVLO) systems are also used to detect low power supply in the gate driver which can lead to fail operation of the power component.

B. Isolation technology and EMC issues

Wide bandgap (WBG) semiconductors such as SiC MOSFETs allow higher frequency switching power electronics for better efficiency [5]. Nevertheless, as switching frequency increases, WBG poses new EMI issues such as switching oscillations [6], [7], [8]. Given the close proximity between gate drivers and power component, this EMI sources create common currents though the gate driver as illustrated in Fig. 2. To ensure common mode current does not trigger the output

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stage, close attention must be paid to reduce the parasitic capacitance of the transmission line through the galvanic isolation. CMTI defines the maximum tolerable rate of rise or fall of the common mode voltage applied between both isolated circuits which will not trigger the detection circuits. This ensures both transmitter side and receiver side of the isolated transmission line to function without error within the specified application.

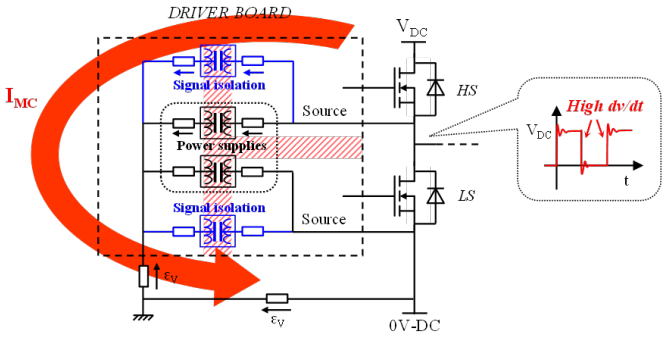

Fig. 2. Common mode current path in electrically isolated gate drivers in half bridge (HB) configuration [9]

In high power applications, opto-isolator technologies are rarely used given their parasitic capacitance and the difficulties for integration of optical fibers commands. Recent gate drivers mainly use two technologies: Digital isolators and pulse transformers.

Digital capacitive isolators allow unidirectional isolated data transmission. A single-ended input signal is split into two differential signal components to pass through the isolation barrier. Each signal component is differentiated to be compared to one another. These transient inputs are then converted into short pulses thanks to Schmitt triggers. As long as the positive input of a comparator has a higher potential than its negative input, the comparator output will present a logical high, thus converting an input transient into a short output pulse. The input signal is then reconstructed with a NOR-gate flip-flop (Fig. 3).

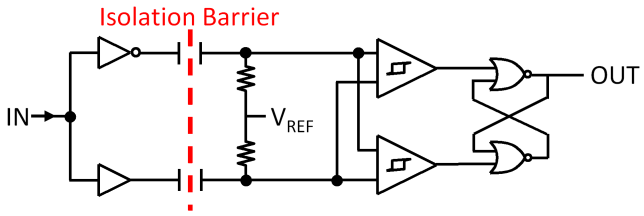

Fig. 3. Block diagram of a digital capacitive isolator [10]

In pulse transformer-based drivers, the transient signal is applied to the pulse transformer. The transient signal is then decoded on the other side of the pulse transformer. A serial capacitance is connected with the primary to prevent DC magnetic field in the pulse transformer which can lead to the core saturation. Bidirectional communication is possible by applying a longer pulse to the secondary winding of the pulse transformer. Error message is usually sent using this method in order to not increase the parasitic capacitance by adding a dedicated transmission line (Fig. 4).

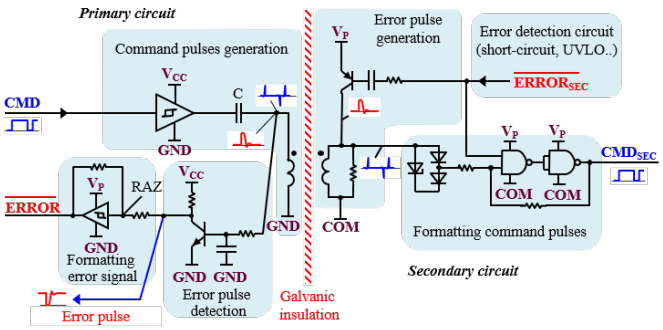

Fig. 4. Pulse transformer block diagram with error pulse circuit [1], [11]

In order to reduce the circuit size, new gate driver integrated circuits (ICs) using coreless transformer technology have been developed [12]. This design allows smaller parasitic capacitance and a greater operating limit because of the core saturation. Table. I provides additional information of each solutions.

TABLE I
COMPARISON BETWEEN THE DIFFERENT SOLUTIONS FOR ISOLATED GATE DRIVING [12]

Parameter	Planar Pulse transformer	isolated gate-driver IC (coreless pulse transformer)	Digital capacitive isolator
isolation level	Reinforced, basic or functional	Reinforced, basic or functional	Reinforced, basic or functional
propagation delay	$\geq 35\,\text{ns}$	$\approx 35\,\text{ns}$	$\approx 50\,\text{ns}$
Parasitic in-out capacitance	$\leq 10\,\text{pF}$	$\leq 2\,\text{pF}$	$\approx 1\,\text{pF}$
CMTI	$\geq 150\,\text{kV}\,\mu\text{s}^{-1}$	$\geq 150\,\text{kV}\,\mu\text{s}^{-1}$	$\geq 100\,\text{kV}\,\mu\text{s}^{-1}$

This study focuses on planar transformers technology in order to improve their CMTI while reducing the parasitic capacitance as low as possible by adding electrostatic shielding. The targeted application is the transmission line of high-power gate driver for a 3300 V, 500 A MOSFET SiC module. The operating voltage chosen is 2.5 kV. First, a design method for pulse planar transformers with Altium Designer is proposed. Then a simulation methodology of said pulse transformers using Ansys is exposed. Finally, experimental results are compared to Ansys simulation using $125\,\text{kV}\,\mu\text{s}^{-1}$ dv/dt to simulate the switching of a power transistor connected to the gate driver.

II. Pulse transformer design using Altium Designer

Pulse transformer is one of the mainstream solutions used to drive power components in Half Bridge configuration. This

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transformer must provide galvanic isolation between the controller connected to the primary side and the power component connected to the secondary side. Moreover, pulse transformers are often used as a DC supply to drive the power components [12]. Recent gate drivers (CMT-TIT8244, CGD1700HB3P-HM3) often use a dedicated DC power supply to power new features such as UVLO or short circuit detection. In such applications, pulse transformers do not need to supply DC energy reducing the risk of magnetic saturation. In aeronautical applications, planar design present two advantages : a reduced footprint and a good reliability due to the isolation properties of FR-4 epoxy [1].

Due to EMC issues and common mode current issues, the pulse transformer integrates electrostatic shielding between the primary and the secondary windings. Electrostatic shielding act as a Faraday cage to block the effect of an electric field. They can reduce the electrostatic field created by common mode currents while being transparent to pulses as they are ineffective against magnetic field. These screens are commonly linked to their respective ground in order to drain common mode currents and reduce EMC noises. Planar topology allows easier screen design and integration. The pulse transformer structure is detailed in Fig. 5.

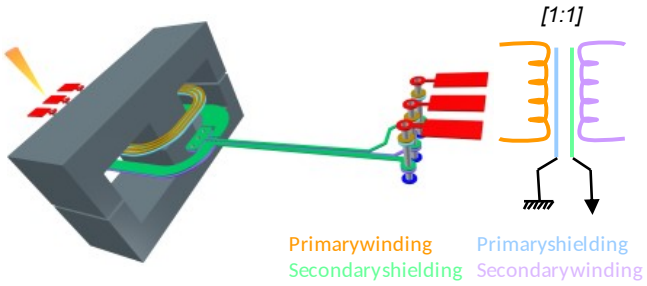

Fig. 5. Pulse transformer overview with Altium Designer

A. Standard requirement

Pulse transformers must provide galvanic isolation between the primary side and the secondary side. As the secondary side is connected to the power component, its potential can rise from 0 V to the power component maximum potential (2.5 kV in this study). To ensure people safety who are connected to the primary side, the pulse transformer must respect electrical standard isolation. In planar applications, electrical standards can be divided into three measures : clearance, creepage distance and solid isolation. Fig. 6 highlights the three standard parameters.

Clearance is the shortest distance in the air between two conductors. This standard value ensures conductors will not arc through the air. In planar transformer applications, one must know ferrite cores are considered as conductors. Thus, the distance between two conductors must be clearance distance plus ferrite cores' width. Creepage distance is the shortest distance to another conductor along the surface of the insulating material of the PCB. This distance ensures conductors will not arc if conductive dust particles were to settle on the PCB. Finally, solid isolation gives the peak voltage solid isolators such as FR4-Epoxy must hold to ensure conductors will not arc. When dealing with solid isolation, planar transformers design usually considers the direct path between both conductors. Red arrow in Fig. 7 illustrates this path. As stated previously, ferrite cores offer a zero length path for electricity as their are electrical conductors. Thus, one must take into consideration the electrical path going through the ferrite core. One example of such a path is shown in yellow in Fig. 7.

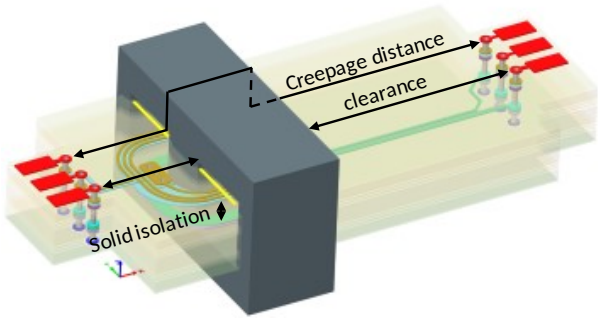

Fig. 6. Pulse transformer standard considerations

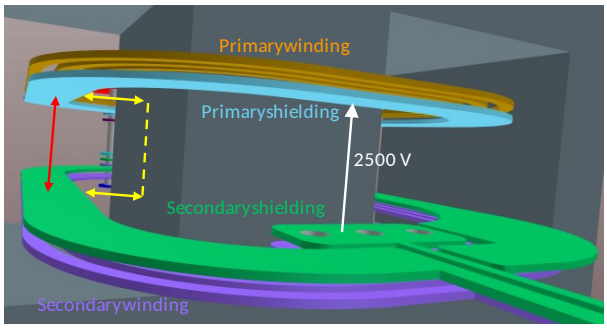

Fig. 7. Pulse transformer solid isolation considerations

B. Pulse transformer design

1) Standard requirements: The pulse transformer design focuses on a 3300 V, 500 A SiC MOSFET module. The operating voltage chosen is 2.5 kV. The European standard EN 50178 [13] is used as a requirement for aeronautical purposes. The reinforced isolation was used. The European standard gives a 22.9 mm clearance as well as a 25 mm creepage distance. According to the standard, solid isolation must withstand a 18.4 kV impulse voltage. The MCL-E-679F (J) FR4 epoxy multi-layer material is used for solid isolation because of its high dielectric strength ($\geq 40\,\mathrm{kV\,mm^{-1}}$). Therefore, the solid isolation between each conductor must be higher than 460 µm.

2) Magnetic core requirements: In pulse transformer applications, a rectangular shape pulse is applied across the transformer winding. If a voltage V is applied to a coil of N turns during Δt time, a magnetic flux density ΔB will build up. To avoid saturation of the magnetic core, the core

area A must be chosen to respect the basic pulse transformer (1) [14].

$$V \cdot \Delta t = N \cdot A \cdot \Delta B \tag{1}$$

In this paper, $25\,\mathrm{ns}$ long pulses are used under a $15\,\mathrm{V}$ voltage constant (see Fig. 10). To reduce the transformer size as much as possible, the smallest planar core from ferroxcube was used (E14/3.5/Core 5/R). Assuming a maximum magnetic flux density ΔB = $50\,\mathrm{mT}$ to reduce core loss, (1) gives a minimum of turns N = 0.7.

3) Coil turn requirements: To simply pulse transformers transient behavior analysis for operation with rectangular pulse, IEEE standardized the equivalent circuit of pulse transformers [15]. In this simplified model 2 resulting criteria are mainly discussed : the overshoot and the rising time of the rectangular pulse. In their study, Bortis and al [16] discussed about the transformer leakage inductance and capacitance impact regarding these criteria. To have the fastest rising time possible, leakage inductance must be kept as low as possible. Nevertheless, if the transformer leakage inductance is too low, high voltage overshoot are to be expected.

As, leakage inductance is proportional to N^2 [16], a balance must be achieved to keep a fast rising time while minimizing the resulting overshoot. Several designs with N $\in$ [1;5] were simulated using Ansys. A number of turns N=3 was finally chosen.

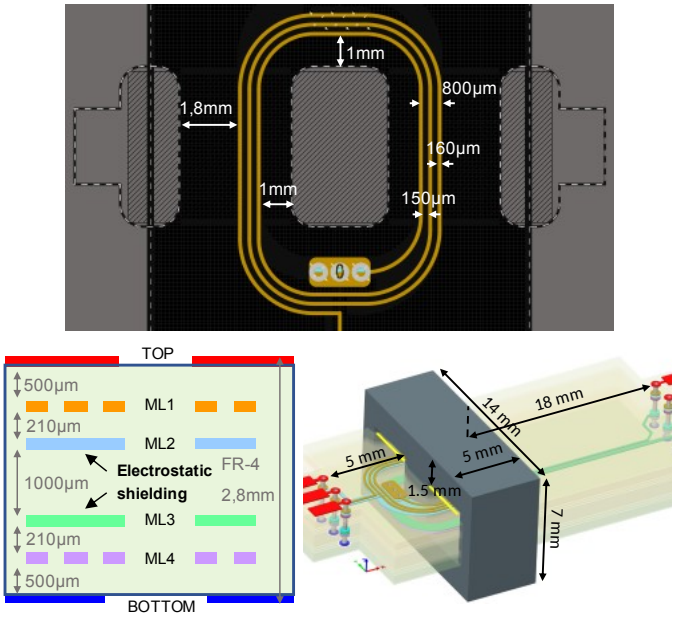

Fig. 8. Pulse transformer design and overview with Altium Designer

4) Resulting design: The pulse transformer is composed of three turns with an electrostatic screen $210\,\mu\mathrm{m}$ away from the primary side. The secondary side is a mirror of the primary side to get a winding ratio of 1 between primary and secondary circuit. As solid isolation is critical in planar transformer application, a safety factor of 2 was applied to the standard impulse voltage resulting. Thus, each side is separated from the other by a $1\,\mathrm{mm}$ FR-4 epoxy distance to respect standard. A minimum distance of 1mm was also applied between conductors and the ferrite according to Fig. 7. To design such transformer a glued double E core is used as it is not a typical PCB thickness of $1.6\,\mathrm{mm}$. Fig 8 summarises the planar transformers characteristics.

III. Pulse transformer simulation Methodology

The employed simulation process in ANSYS included alternative software tools. The model being primarily implemented in Altium designer was imported into ANSYS SIWAVE using specific data exchange files. After being verified in terms of layer stack up, thickness, and material assignment, it was exported into ANSYS Q3D Extractor which can be dynamically linked with ANSYS Circuit Design for further analysis.

Being the leading extraction parasitic tool, ANSYS Q3D Extractor was employed to simulate and analyze the planar pulse transformer model. The electromagnetic field simulations conducted by this software are vital for the extraction of resistance, conductance, partial inductance and capacitance, known as RLGC parameters [17]. The central objective is to ensure compliant simulation and experimental results which will establish a reliable foundation for imminent experimentations. Q3D Extractor exploits the Finite Element Method (FEM) and method of moments to provoke an electromagnetic field solution. It relies on the simplification of Maxwell's equations, termed quasistatic approximation by anticipating that the size of the analyzed design is diminutive compared to the wavelength of maximum sought frequency where the coupling between magnetic and electric fields can be ignored [18].

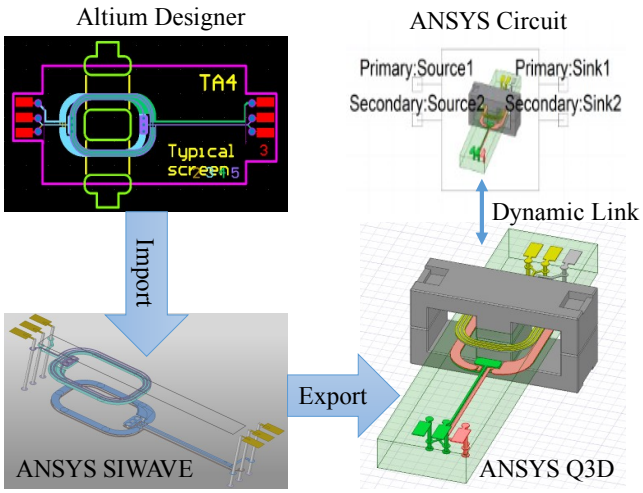

Fig. 9. Simulation methodology of the analysed pulse transformer

As depicted in Fig. 9, the modelled design in Altium designer was imported into ANSYS SIWAVE to verify layer stack up and material assignment before being exported into ANSYS Q3D Extractor. The complete analysis performed in the latter allows the determination of RLGC parameters. The analyzed model can be dynamically linked with ANSYS Circuit design as it grants coordinated simulation of the subcircuit with the project original simulator. This will permit the

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determination of the transformer Scattering (S) parameters and effectively analyze the transformer equivalent circuit model which will be demonstrated in the sections thereafter. The model reveals the copper windings and shielding layers which are integrated in an FR4 Epoxy dielectric material, all secured by an EE 3F36 ferrite core.

IV. Transformer Scattering Parameters

A. Transformer Eligible Frequency Band

As the pulse transformer was exported into ANSYS, a spectral analysis is need to estimate the frequency band used in short pulse transmission. The method used to pass data through the galvanic isolation can be described as follow: a positive pulse on the primary winding means a rising edge of the PWM input and a negative pulse means a falling edge. With WBG semiconductors and the rising in the switching frequency, short pulses were chosen to maximize the gate driver switching frequency. Based on the pulse generator (UCC27517DBV) used, 25 ns long short pulse was targeted. Pulse parameters can be seen in Fig. 10.

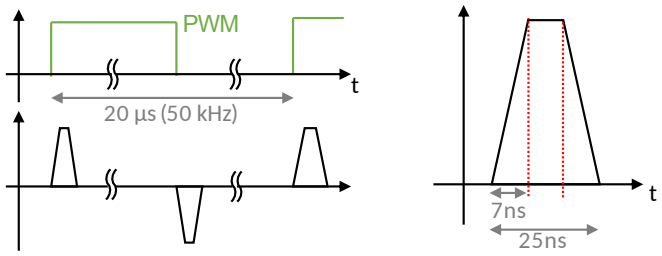

Fig. 10. Pulse parameters used in this study

The signal of Fig. 10 was implemented on Matlab and a frequency bandwidth analysis was performed using the *obw* function. Fig. 11 shows the function result. A 50 kHz PWM was chosen with a duty cycle of 50 %. Sampling time is 0.7 ns.

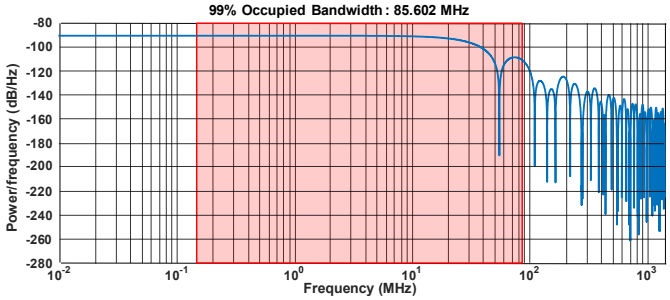

Fig. 11. Power spectral density of the pulse signal

The signal processing analysis gave back a 99 % occupied bandwidth of 84.3 MHz ranging from 149.7 kHz to 85.75 MHz (Fig. 11).

B. S Parameter Simulation

Intending to study the electrical behavior of the planar transformer and demonstrate a reliable simulation criterion, S parameter simulation analysis was implemented and compared to experimental results. In order to achieve this evaluation, the pulse planar transformer was simulated in ANSYS Q3D Extractor by assigning a frequency sweep in accordance to the eligible frequency band ranging from 100 kHz till 85 MHz. Furthermore, the model was analyzed based on designating all conductors as nets which allows the computation of GC matrices, whereas AC/DC RL analysis requires the assignment of source and sink excitations which signify where the current enters and exits the windings respectively.

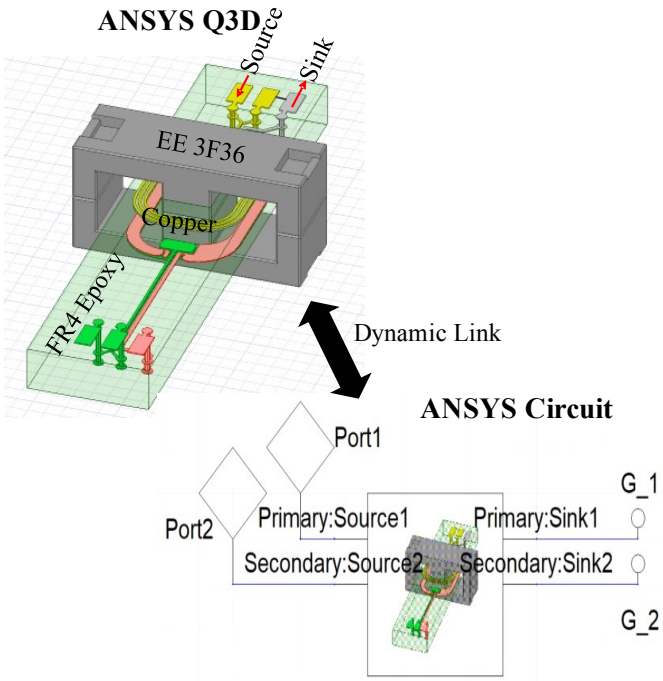

Fig. 12. Simulation arrangement of S parameter evaluation

After a successful analysis, the model was dynamically linked to ANSYS Circuit design as a four port sub-circuit demonstrated with the source and sink excitations of the primary and secondary winding as shown in Fig. 12. In order to reproduce an experimental examination, 50 Ω impedance interface ports were connected to the source pin of each winding, and distinctive ground ports to the sink pins.

A frequency domain analysis is realized by setting up a Linear Network Analysis (LNA) over the previously specified frequency band. This final step will enable the computation of the frequency-dependent scattering parameters which will be compared to the experimental measurements revealed in section IV-C.

C. S Parameter Experimental Validation

To authenticate the simulation results, the pulse planar transformer was fabricated in accordance to the design modelled in Altium designer. S parameter measurements were conducted using a two-port, fifty-ohm Vector Network Analyzer (VNA). Fig. 13 correlates the agreeable S parameter results over a frequency band from 100 kHz to 100 MHz. The dashed lines represent the simulated results, whereas solid lines depict

the experimental ones. S11 and S22 refer to the reflection coefficients of ports 1 and 2, respectively, yet S21 and S12 identify the transmission coefficients from ports 1 to 2 and contrarily, respectively [19]. The symmetrical structure of the planar transformer explains the parity of S11 and S22, and S12 and S21.

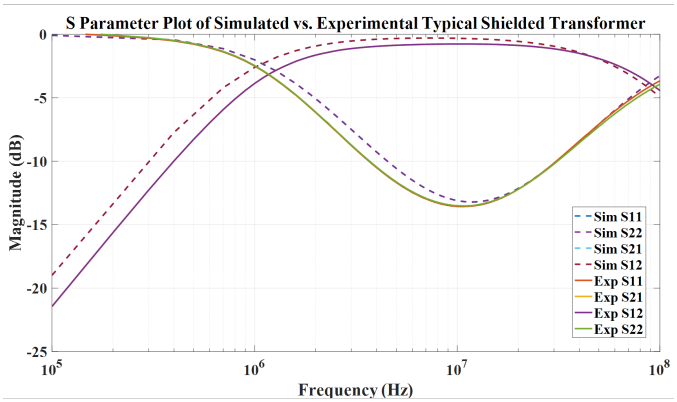

Fig. 13. Experimental vs. simulated S parameter results of a typically shielded transformer

It is imperative to proclaim that this experimental verification was performed to reveal result conformity which grants reliable reliance on the simulation analysis implemented. Thus, fortifying the ability to propose an equivalent circuit model of the planar transformer relying on ANSYS Q3D Extractor RLGC parameters conferred thereafter.

V. ElectroMagnetic Compatibility Adherence

Medium-Voltage (MV) Silicon Carbide (SiC) Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) acquire significant intrinsic properties, making it viable to intensify the switching frequency of converters from a few hundred kHz to the MHz region [20], [21]. Nonetheless, with every upgrade, researchers encounter challenges and restrictions to achieve enhanced power converter designs. Advantageous rapid switching frequency realization becomes detrimental when resulting in high dv/dt amounting to $100\,\mathrm{kV\,\mu s^{-1}}$, generating electromagnetic disturbances in gate driver circuits due to the passage of Common Mode (CM) currents through parasitic capacitances, known as interwinding capacitances [22]. Hence, being responsible for invoking semiconductor switching orders, critical attention is required when designing pulse planar transformers. This section will reveal the endurance of the pulse planar transformer to a steep dv/dt occurrence by performing an innovative simulation test of an equivalent circuit model and complying the results to experimental examination, whilst ensuring Electromagnetic Compatibility (EMC) standards.

A. Pulse Transformer Equivalent Circuit Model

A generic and symmetrical equivalent high-frequency circuit model of the pulse planar transformer is presented in Fig. 14. The electrical model comprises an ideal transformer with a turn's ratio m, magnetizing inductance L_m, core resistance R_c, leakage inductances L_P and L_S, winding resistances R_P and R_S and stray capacitances C_w, C_{mc1} and C_{mc2}. This model mainly focuses on the values of the interwinding capacitances C_{mc1} and C_{mc2} as they are the common mode current passage route connecting the primary and secondary winding which will be quantifies in the section thereafter.

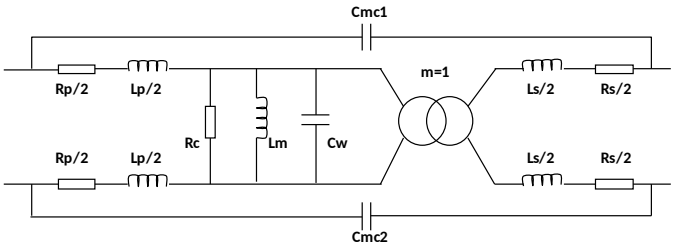

Fig. 14. Common-mode current modeling of the pulse planar transformer

B. Pulse Transformer Parameter Extraction

In order to extract the parasitic parameters of the simulated pulse planar transformer and establish an equivalent circuit model, ANSYS Q3D Extractor tool was utilized [23]. As previously illustrated in Fig. 12, the model is set up by assigning material characteristics, net identifications and conductor excitation allocations. RLGC parameters were quantified over a sufficient frequency band extending from $100\,\mathrm{kHz}$ till $85\,\mathrm{MHz}$. The reduce matrix feature in ANSYS Q3D was used to evaluate the resistance, inductance and capacitance values of the transformer model. The main objective is to investigate the susceptibility of the equivalent circuit model of the planar transformer to an application of high dv/dt switching transition.

TABLE II
ANSYS Q3D EXTRACTOR RLC PARAMETERS

Frequency (MHz)	**ANSYS Q3D Parameter Extraction**						
	$\mathbf{C}_{mc1}$ (pF)	$\mathbf{C}_{mc2}$ (pF)	$\mathbf{R}_P$ (Ω)	$\mathbf{R}_S$ (Ω)	$\mathbf{L}_P$ (nH)	$\mathbf{L}_S$ (nH)	$\mathbf{L}_m$ (μH)
0.1	0.47	0.61	0.47	0.47	249	249	10.1
1	0.47	0.61	0.52	0.52	246	246	10.1
10	0.46	0.58	0.99	0.99	230	230	10.1
20	0.45	0.58	1.3	1.3	226	226	10.1
30	0.45	0.58	1.55	1.55	225	225	10.1
40	0.45	0.57	1.77	1.77	224	224	10.1
50	0.45	0.57	1.96	1.96	223	223	10.1
60	0.45	0.57	2.12	2.12	223	223	10.1
70	0.45	0.57	2.28	2.28	222	222	10.1
80	0.45	0.57	2.42	2.42	222	222	10.1

Table II demonstrates the consistency of the parameters L_P, L_S , L_m, C_{mc1} and C_{mc2} over the desired frequency

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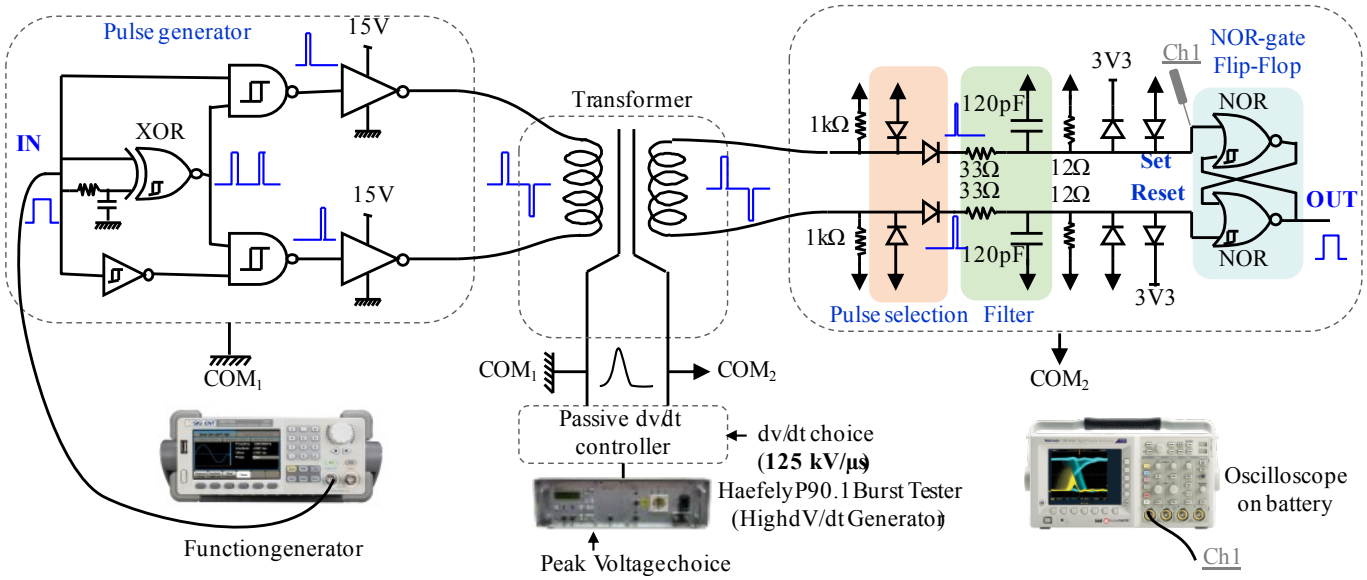

Fig. 15. Circuit to test pulse planar transformer's susceptibility to an application of $125\,\mathrm{kV\,\mu s^{-1}}$ dv/dt between both primary and secondary ground

span which holds remarkable significance. The variation of R_P and R_S is common due to skin effect phenomenon, however, negligible over the tested frequency range.

Several simulations were conducted to create a definitive model of the transformer independent of the applied frequency. The examination was implemented based on two approaches. The first approach was by averaging the value of each element over the frequency span. The second approach was testing the model at a frequency of $10\,\mathrm{MHz}$ and $50\,\mathrm{MHz}$ separately. Nevertheless, the simulation results of all the aforementioned propositions yielded to an agreeable outcome.

Hence, the equivalent circuit model illustrated in Fig. 14 at a peculiar frequency of $50\,\mathrm{MHz}$ is considered with m=1, R_C=500 Ω and C_w=21.37 pF. The aim is to perform a high dv/dt application on this model and compare the results to an actual experimented observation which will be subsequently discussed.

C. dv/dt Simulated Immunity Test Setup

ANSYS Circuit design software was used to simulate a dv/dt application on the modelled pulse transformer [24]. To replicate a severe switching condition of power semiconductors, a steep dv/dt of $125\,\mathrm{kV\,\mu s^{-1}}$ was applied between the primary and secondary windings' disparate grounds as revealed in Fig. 15. Firstly, on the primary side short $25\,\mathrm{ns}$ pulses with a $15\,\mathrm{V}$ amplitude are connected to transmit turn on and turn off signals intended to switch a 1200V SiC MOSFET. At the secondary side, pulse selection is essential to segregate positive and negative pulses, and a filter stage necessary to curtail the signal noise for a 0-3.3 V logic at the output. After setting up and verifying the design, a transient analysis from 0 till $2000\,\mathrm{ns}$ was applied to evaluate the results.

D. dv/dt Experimental Immunity Test Setup

The pulse generator is composed of 2 NAND gates which receive respectively the input signal (IN) and its inverted counterpart. This allows to select the rising edge of the input or its falling edge. A NXOR gate is used to convert the input signal into transient signals whenever there is a change in its state. The duration of the transient signal is dictated by the RC filter time response τ = RC. Then, 2 gate drivers buff the signal to pass through the pulse transformer. Fig. 15 illustrates the experimental circuit.

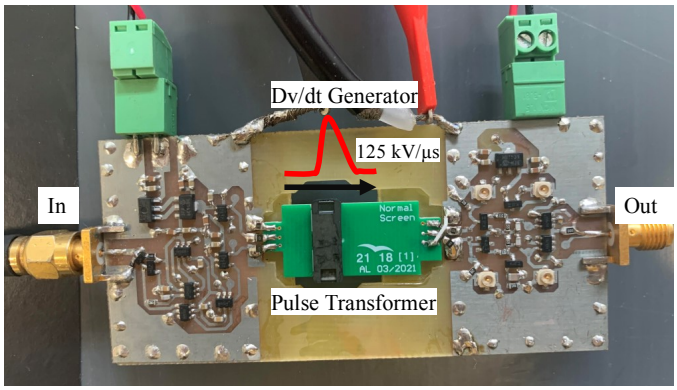

Fig. 16. Experimental setup of pulse transformer sensitivity to a high dv/dt

The pulse planar transformer was tested at IETR lab using the circuit described in Fig. 15. A $50\,\mathrm{kHz}$ PWM signal is generated with a 0.5 duty cycle by the function generator. A Haefely generator is connected to both ground to perform a steep dv/dt immunity test between the primary side and the secondary side of the pulse transformer. A series of bursts are generated in sync with the PWM signal to simulate the power semi-conductor switching. A $125\,\mathrm{kV\,\mu s^{-1}}$ voltage slope is used which is the theoretical maximum switching speed of the power module multiplied by a safety factor of 4. The installation of the experimental setup of the planar pulse transformer CMTI test is revealed in Fig. 16.

E. dv/dt Immunity Test results

Static CMTI monitors the output stage of the pulse planar transformer when a CMT strike happens. Testing conditions cover the input logic condition and the CMT waveform. In high power gate driver, parasitic turn on is a major issue as it can lead to short circuit situations. In this application, the input is tied in logic low (i.e power component turned off). At $0.8\,\mu s$, a transient signal is sent in the input to simulate a switch on. Then, at $1\,\mu s$, a common mode transient voltage (CMTV) of $125\,kV\,\mu s^{-1}$ is generated between the primary and the secondary side. Noise sustainability results are taken from the SET input of the NOR-gate Flip-Flop in Fig. 15 to check if the CMTV triggers the output stage. Fig. 17 displays the experimental CMTV generated by the Haefely generator. To match the experimental setup, a similar CMTV was used in the simulated test.

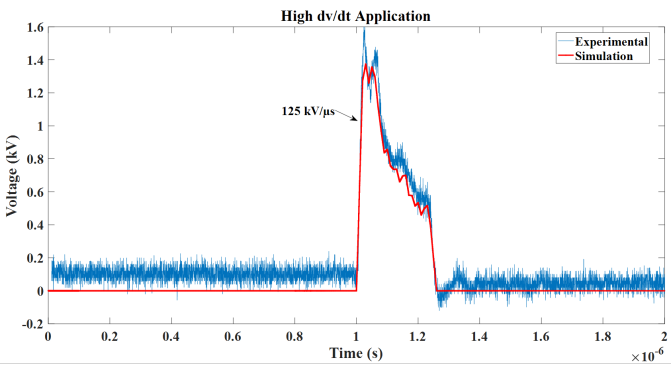

Fig. 17. Experimented vs. Simulated steep dv/dt application

Fig. 18 demonstrates convenient experimental and simulation results after applying the input signal. CMTI results show a good correlation between the experimental results and the simulated ones, with $0.55\,V$ CMT parasitic voltage and $0.45\,V$, respectively in the Flip-Flop input. The values are minor with respect to the threshold voltage (VT+ = $1.88\,V$) of the Schmitt-trigger logic gate circuitry [25].

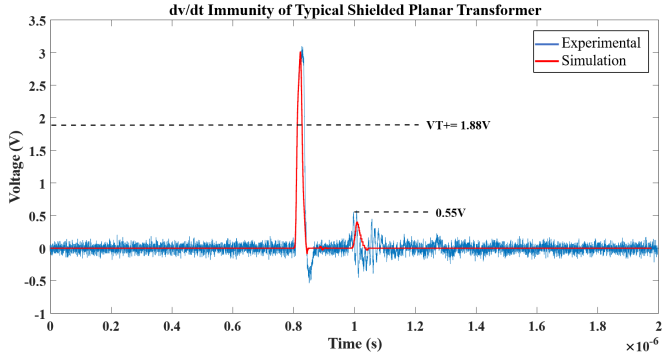

Fig. 18. Pulse planar transformer sustainability to abrupt $125\,kV\,\mu s^{-1}$ dv/dt with shielding

In order to compare the shielding effect on the pulse transformer sustainability, another transformer was produced without shielding. Ansys simulation gives an increase of the C_{mc1} and C_{mc2} values by a factor 2. CMTI results show again a good correlation between the experimental results and the simulated ones, with near $1\,V$ CMT parasitic voltage and $0.9\,V$, respectively in the Flip-Flop input.

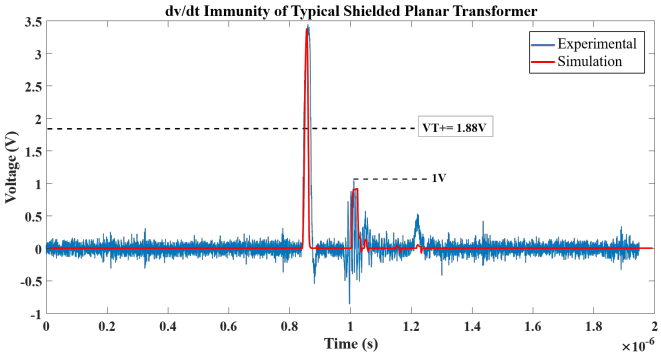

Fig. 19. Pulse planar transformer sustainability to abrupt $125\,kV\,\mu s^{-1}$ dv/dt without shielding

In the end, both transformers give minor voltage spikes under a $125\,kV\,\mu s^{-1}$ applications with respect to the threshold voltage of the Schmitt-trigger logic gate circuitry. In the shielded pulse transformer case, a higher CMTI is achieved.

VI. Conclusion

A planar pulse transformer using electrostatic shielding for $3.3\,kV$ applications with respect to European standard EN 50178 was proposed in this paper. The simulation analysis used alternative software tools, Altium Designer to design, and ANSYS Q3D with dynamic links to further analyze the transformer.

After performing a spectral analysis on the applied pulse signal, an eligible frequency band was identified to extract RLGC parasitic parameters in ANSYS Q3D Extractor that revealed coherent results. The study contributed to construct an equivalent circuit model of the transformer at a specific frequency and investigate the latter under abrupt dv/dt conditions which simulate the rapid switching of power semiconductors. Convenient CM noise results reveal EMC conservancy and simulation analysis reliability.

In this paper, 2 pulse transformers were designed : one with shielding and one without. In both cases, a CMTI test was performed using a $125\,kV\,\mu s^{-1}$ dvdt. The shielded transformer show a better dvdt immunity than the non shielded one by a factor 2.

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