Equivalent Circuit Model of ESD Protection Devices

● Hiromi Anzai ● Yoshiharu Tosaka ● Kunihiro Suzuki
● Toshio Nomura ● Shigeo Satoh

(Manuscript received December 15, 2002)

In this paper, we propose an equivalent circuit model that describes the snapback characteristics of ESD (ElectroStatic Discharge) protection devices constructed using MOS transistors. Our goal was to predict the ESD immunity of CMOS integrated circuits using circuit simulations. The ESD immunity can be predicted from the high-current behavior (the snapback characteristics) of the protection devices. In this paper, we explain our equivalent circuit model, which includes a parasitic bipolar transistor with a generated-hole-dependent base resistance. Because the models for parasitic elements are combined with a SPICE MOS transistor model, our model can represent the gate bias dependence of snapback characteristics. The equivalent circuit parameters are extracted from the device simulations and modified to reproduce the measured snapback characteristics of the MOS transistor. Therefore, our equivalent circuit model for MOS protection devices can be used in ESD circuit simulations.

1. Introduction

In the development of VLSI technologies, in addition to high performance, low power, and low cost, reliability is also an important issue. Damage caused by ESD (ElectroStatic Discharge) is a serious threat to VLSI reliability, so it is important to provide ESD protection in these devices.[1), 2)]

If an ESD stress current flows into internal circuits, it can cause internal damage. Therefore, it is necessary to predict ESD immunity, which depends on the circuit design and layout. At present, ESD stress tests are carried out during trial manufacturing. If the circuit does not pass the tests, we must investigate the cause of the ESD damage and reexamine the design rule and process conditions. However, it takes a lot of time and expense to repeat trial manufacturing. ESD simulations for the protection circuits are effective for solving this problem.[3)-8)] Our purpose is to construct an ESD circuit simulation system based on the SPICE circuit simulator.

Because ESD immunity can be predicted by simulating the protection devices, we examined an equivalent circuit model[9)-12)] that describes the snapback characteristics of MOS protection devices. In this paper, we explain our equivalent circuit model, which includes a parasitic bipolar transistor with a generated-hole-dependent base resistance. The models for the parasitic elements are combined with the SPICE MOS transistor model, and therefore our model represents the gate bias dependence of snapback characteristics. Equivalent circuit parameters are extracted from device simulations and then modified to reproduce the measured snapback characteristics of a MOS transistor. Therefore, our equivalent circuit model for MOS protection devices can be used for ESD circuit simulations.

In Section 2, we explain the snapback characteristic. In Section 3, we explain our equivalent circuit model of ESD protection devices. In Section 4, we describe the model parameter ex-

traction procedure and present the calculation results. In Section 5, we modify the equivalent circuit parameters to reproduce actual snapback characteristics. Section 6 describes an ESD circuit simulation example, and Section 7 is our conclusion.

2. Snapback

Snapback is a phenomenon that occurs in ESD protection devices that has an important effect on ESD immunity. **Figure 1** shows this phenomenon in the drain current I_D versus drain voltage V_D curve of an nMOS protection device. Region (1) is the linear region governed by standard MOS equations and modeled in SPICE.[13] Region (2) is the saturation region, which is also governed by the standard MOS equations and modeled in SPICE. Region (3) is the avalanche breakdown region, where the standard MOS equations are no longer valid. Region (4) is the bipolar or snapback region. Our task was to extend the SPICE model into the high-current regions (i.e., Region (3) and Region (4)). **Figure 2** shows the snapback mechanism.[1)-3)] If the drain voltage V_D increases beyond the saturation region, many electron-hole pairs are generated by impact ionizations and the current reaches the avalanche region. Electrons that occur due to impact ionizations flow to the drain (the collector of the parasitic transistor), and holes flow to the substrate (base). We denote this hole current as I_{DSUB}. When a sufficiently large number of holes have collected in the substrate, the parasitic bipolar transistor switches on and the drain current reaches the snapback region. Furthermore, electrons injected from the source are accelerated by the electric field in the drain depletion layer and consequently cause impact ionizations. This increases the hole current I_{DSUB}, which increases the number holes in the substrate. If the drain current increases, a failure occurs in the protection device, for example, the gate oxide breaks down or a wire melts.

3. Equivalent circuit model

We propose an equivalent circuit model for the MOS protection device shown in **Figure 3**.[10),11)] We assumed a MOS structure with no gate so we could focus on the parasitic bipolar transistor model. The drain, source, and substrate are equivalent to the collector, emitter, and base of a bipolar transistor.

In this model, there are two current sources,

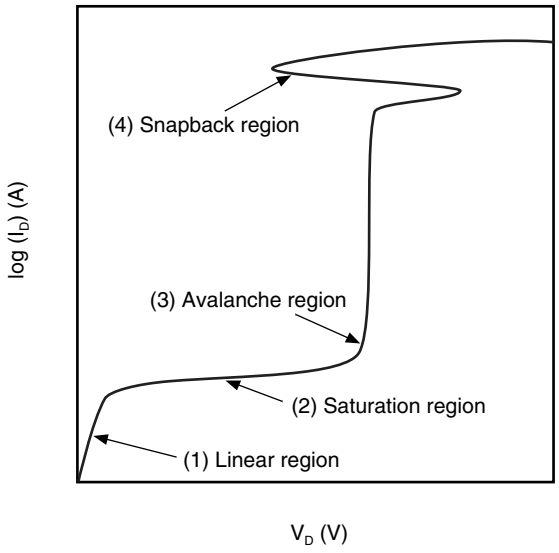


Figure 1
Snapback characteristic.

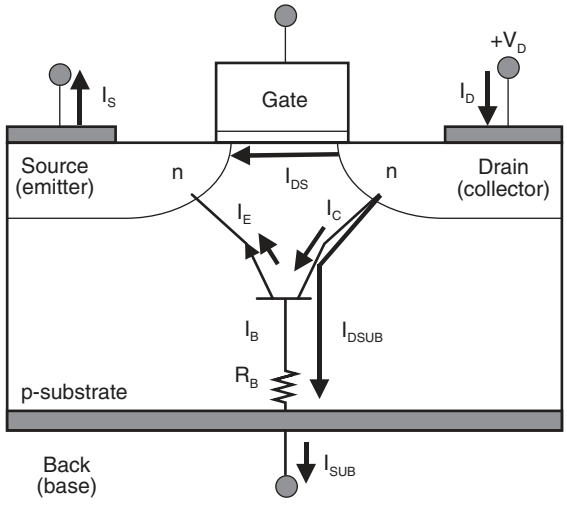


Figure 2
Mechanism of snapback characteristic.

I_{LeakC} and ξI_C (ξ is the impact ionization rate), and a capacitance C_D. We must also include I_{LeakC}, ξI_E, and C_E in the source side when we consider the symmetry of the device; however, they are omitted for simplicity. I_{LeakC} is the leakage current due to electron-hole pairs that are thermally generated in the junction depletion layer between the drain and substrate. The hole current ξI_C is due to the impact ionization. When electrons from the source are accelerated by the electric field, electron-hole pairs are generated and hole current ξI_C flows to the substrate. As shown in Figure 3, there is a bipolar transistor in the middle of the equivalent circuit. In addition, the base resistance is expressed as R_{BS} and R_B, which are connected in parallel. This base resistance model adequately expresses the generated-hole-dependent effect of the base resistance. When the hole current flows dominantly from the drain, the base resistance is constant and is equal to R_B. On the other hand, when the hole current flows dominantly from the substrate, the base resistance varies and is equal to R_{BS}.

In this work, we use HSPICE[13] for circuit simulations, Medici[14] for device simulations, and TSUPREM4[15] for process simulations. We extract I_{LeakC} and C_D from the Medici data and model them by setting up a table. The parameters of the bipolar transistor, coefficient ξ, parallel base resistances R_{BS} and R_B, and source and drain resistances R_S and R_D are also extracted from the Medici data.

Next, we combine the parasitic elements in Figure 3 with the MOS transistor model shown in **Figure 4**. We use BSIM3[16] for the MOS transistor model. The final equivalent circuit model for the MOS protection device is shown in **Figure 5**. Our model represents the gate bias dependence of snapback in the MOS transistor.

4. Comparisons with device simulations

We will now explain the parameter extraction procedure for the nMOS transistor shown in **Figure 6**.

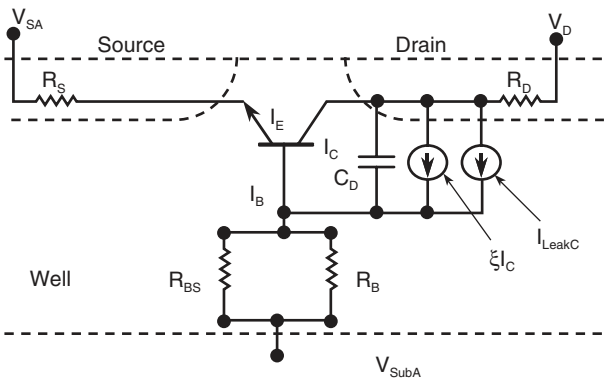


Figure 3
Equivalent circuit model for parasitic elements in MOS protection device.

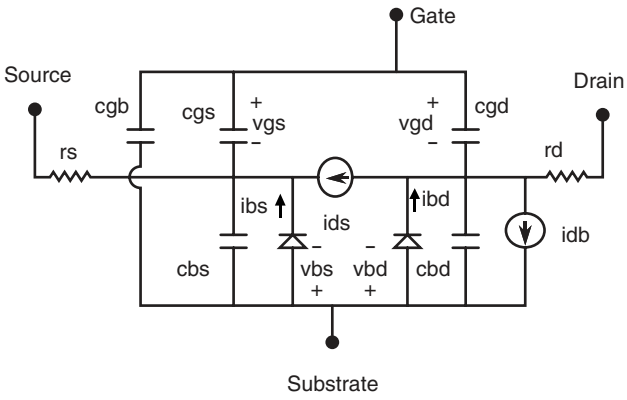


Figure 4
MOS transistor model in HSPICE.

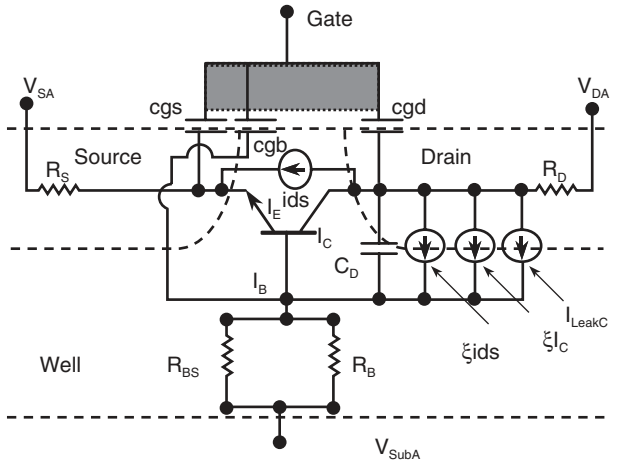


Figure 5
Equivalent circuit of protection device.

First, we perform process simulations to obtain the transistor structure data and then perform device simulations. **Figure 7** shows the snapback characteristics of the nMOS transistor for gate voltages of 0, 0.5, 1.0, 1.5, and 2.0 V as simulated using Medici.

Next, we produce the structure without the gate (Figure 3) by etching the gate electrode of the nMOS transistor in Figure 6 using TSUPREM4. We then use Medici to perform the necessary simulations, for example, the snapback characteristics and the bipolar characteristics, in order to extract the circuit parameters in the equivalent circuit model. **Figure 8** shows the snapback characteristics obtained using Medici and HSPICE for the structure without the gate. Although the Medici and HSPICE results are slightly different where the drain voltage increases again after snapback, the overall agreement between the two is very good.

Next, the parasitic elements and extracted parameters are combined with the BSIM3 model and we perform HSPICE simulations using our equivalent circuit model (Figure 5). **Figure 9** shows the snapback characteristics simulated with HSPICE for gate voltages of 0, 0.5, 1.0, 1.5, and 2.0 V. There is a strong similarity between these characteristics and the Medici-simulated characteristics shown in Figure 7.

Figure 10 compares the gate voltage dependences of the snapback characteristics of the nMOS transistor as simulated using HSPICE and Medici. The HSPICE results are almost the same as the Medici results. The slight differences when the gate voltage is low may be due to the extraction method of current source I_{LeakC}, because the

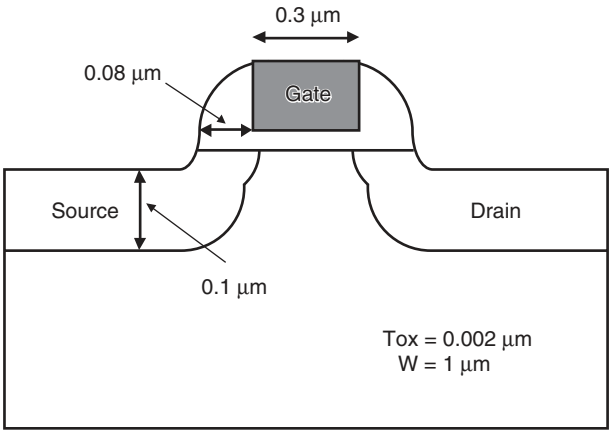


Figure 6
nMOS transistor structure.

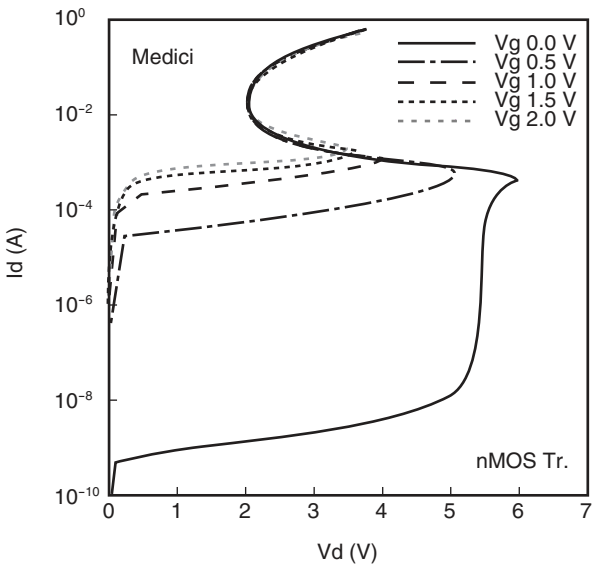


Figure 7
Snapback characteristics simulated with Medici.

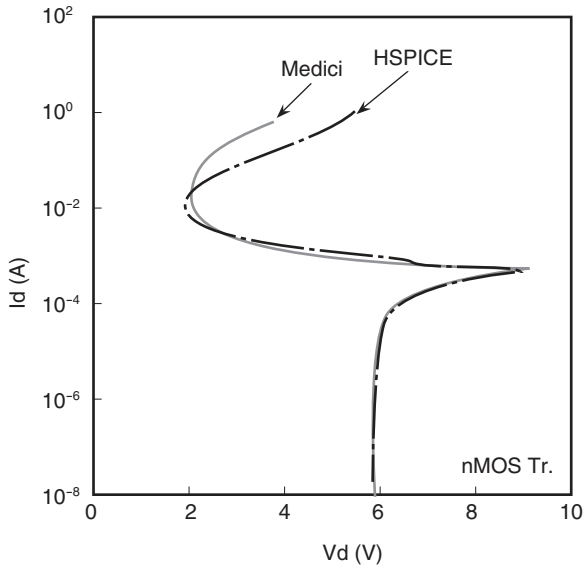


Figure 8
Snapback characteristic of nMOS transistor with no gate. HSPICE results are compared with Medici results.

gate was not considered when the leakage current was extracted.

Figures 11 and **12** show the results for a pMOS transistor with our equivalent circuit model. The results for the pMOS transistor are similar to those for the nMOS transistor shown in Figures 8 and 10.

5. Comparison with measurements

We extracted equivalent circuit parameters from device simulation results. However, to per-

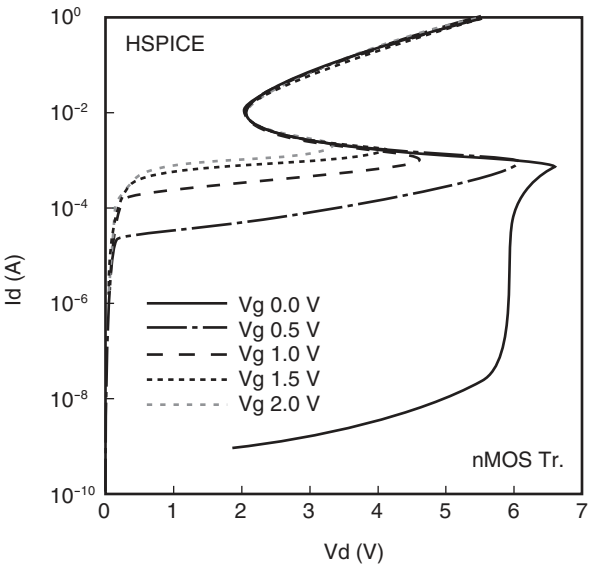


Figure 9
Snapback characteristics simulated with HSPICE.

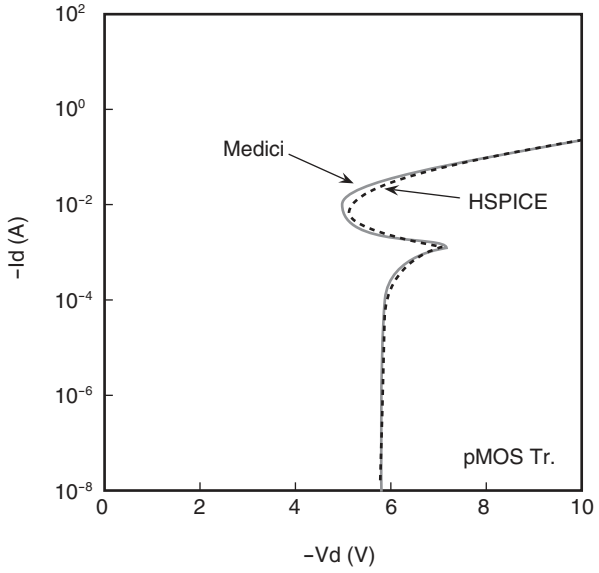


Figure 11
Snapback characteristic of pMOS transistor with no gate. HSPICE results are compared with Medici results.

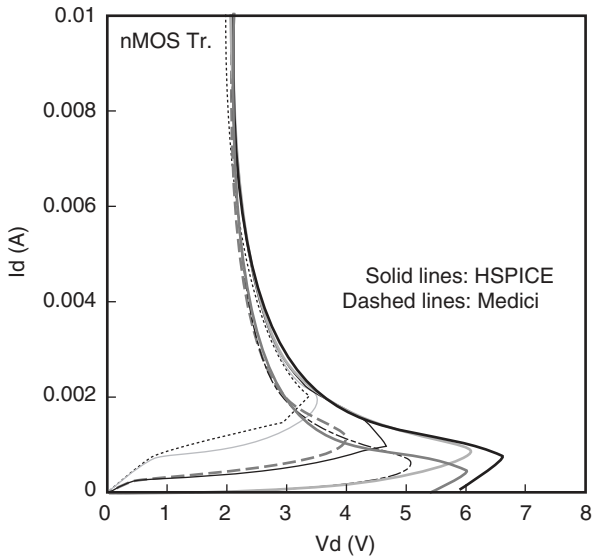


Figure 10
Snapback characteristics of nMOS transistor.
HSPICE results are compared with Medici results with Vg of 0.0, 0.5, 1.0, and 2.0 V.

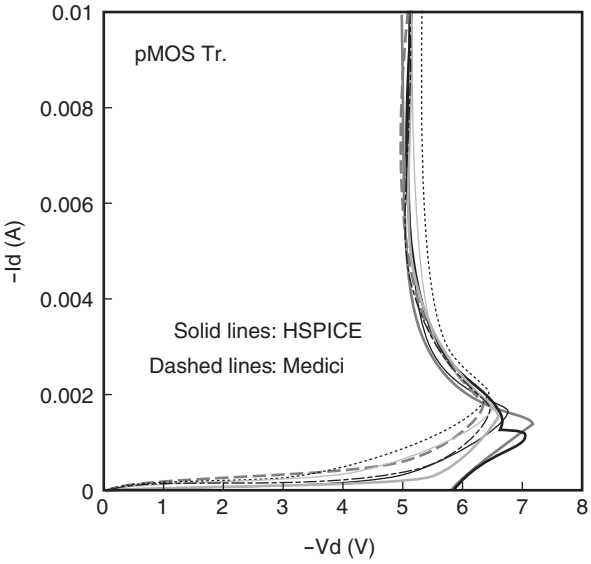


Figure 12
Snapback characteristics of pMOS transistor.
HSPICE results are compared with Medici results with Vg of 0.0, 0.5, 1.0, and 2.0 V.

form accurate ESD circuit simulations using our equivalent circuit model, the model has to reproduce the snapback characteristics of actual devices. Hence, we tried to modify the equivalent circuit parameters to reproduce the actual snapback characteristics of the protection device using measured data.

Figures 13 and **14** show measured snapback characteristics of, respectively, the nMOS and pMOS transistors at a 0 V gate bias. These results were obtained from TLP (Transmission Line Pulsing) measurements[1)] of nMOS and pMOS test structures that were fabricated for investigations of ESD characteristics. We modified some of the equivalent circuit parameters, which were previously extracted from device simulations, to reproduce the measured results.

Figure 13 shows the simulated snapback characteristic of the nMOS transistor with the modified parameters and the TLP measurements. Although the characteristics are slightly different around a drain voltage of 4.5 V, the HSPICE results are well-matched to the TLP measurements. The parameters that were modified for the HSPICE simulation were the source resistance (R_S), drain resistance (R_D), well resistance (R_{Well}), and impact ionization rate ($\xi = f1 \times \xi_0$). The values of these parameters in the simulation were as follows:

$R_S = R_D = 110\ \Omega$.
$R_{Well} = 4000\ \Omega$.
f1 = 0.14.

The original values of impact ionization rate ξ_0 were $7.03 \times 10^5\ cm^{-1}$ for the nMOS and $1.528 \times 10^6\ cm^{-1}$ for the pMOS. A correction factor f1 was introduced to reproduce the measured snapback characteristic.

The snapback characteristic of the pMOS transistor as simulated with the modified parameters is shown in Figure 14. The HSPICE results almost match the measurement results. The values of the modified parameters in the HSPICE simulation were as follows:

$R_S = R_D = 77\ \Omega$.
$R_{Well} = 3600\ \Omega$.
f1 = 0.17.

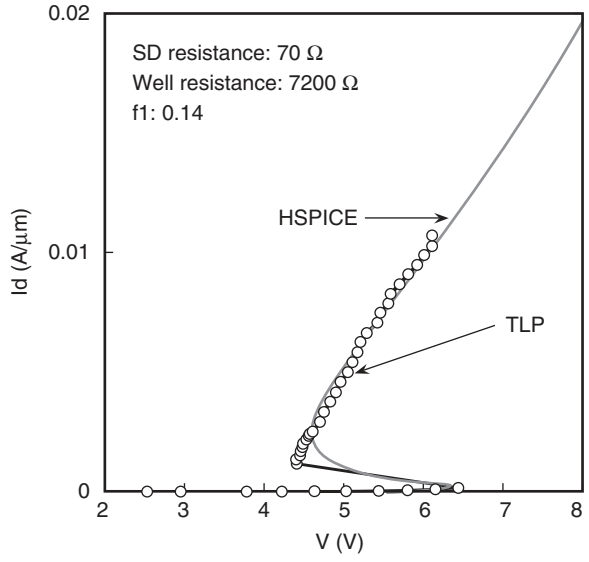


Figure 13
Snapback characteristic of nMOS transistor. Parameters in HSPICE simulations are modified to reproduce results of TLP measurements.

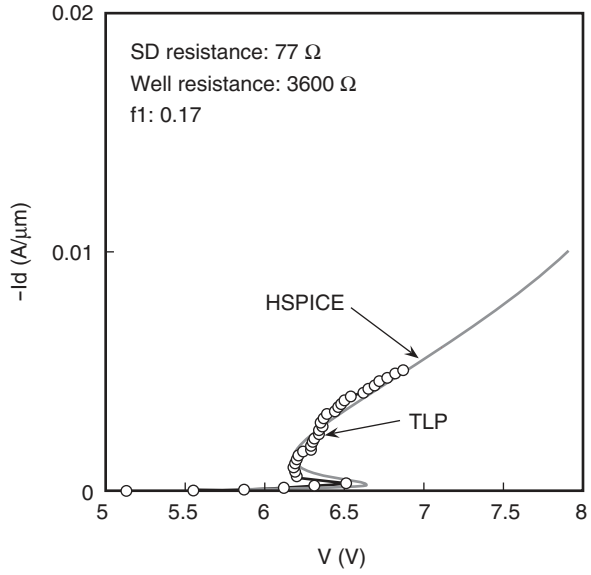


Figure 14
Snapback characteristic of pMOS transistor. Parameters in HSPICE simulations are modified to reproduce results of TLP measurements.

These resistance values do not always agree with the values for actual devices, and this may be because our simulations do not include the effects of heat.

Figures 13 and 14 show that we can extract equivalent circuit parameters that reproduce the measured snapback characteristics of MOS protection devices. Therefore, our equivalent circuit model for MOS protection devices can be used in ESD circuit simulations.

6. Circuit simulation example

Our model and the extracted parameters can be used in ESD circuit simulations. **Figure 15 (a)** shows a typical I/O circuit that we simulated. We applied our model to the ESD protection and driver transistors of this circuit and performed an HSPICE simulation under the HBM[1)] (Human Body Model) condition. The simulation results are shown in **Figure 15 (b)**.

Our circuit simulation methodologies can be used to analyze snapback characteristics and ESD immunity in arbitrary I/O circuits that include MOS protection devices.

7. Conclusion

In this paper, we proposed an equivalent circuit model for MOS protection devices that includes a parasitic bipolar transistor with a generated-hole-dependent base resistance. The models for parasitic elements were combined with a BSIM3 transistor model. Our model accurately represents the gate bias dependence of snapback characteristics. Equivalent circuit parameters were extracted from device simulations and then modified to reproduce the snapback characteristic of a MOS transistor as measured by TLP. We also described an ESD circuit simulation example. Our results suggest that our model is effective for ESD circuit simulations.

The simulation technology described in this paper is suitable for various kinds of ESD protection circuits, and it will be used in various applications in future work. Future tasks will include the improvement of our model, for example, by including the effects of heat.

References

1) A. Amerasekera and C. Duvvury: ESD in Silicon Integrated Circuits. New York, Inc.,

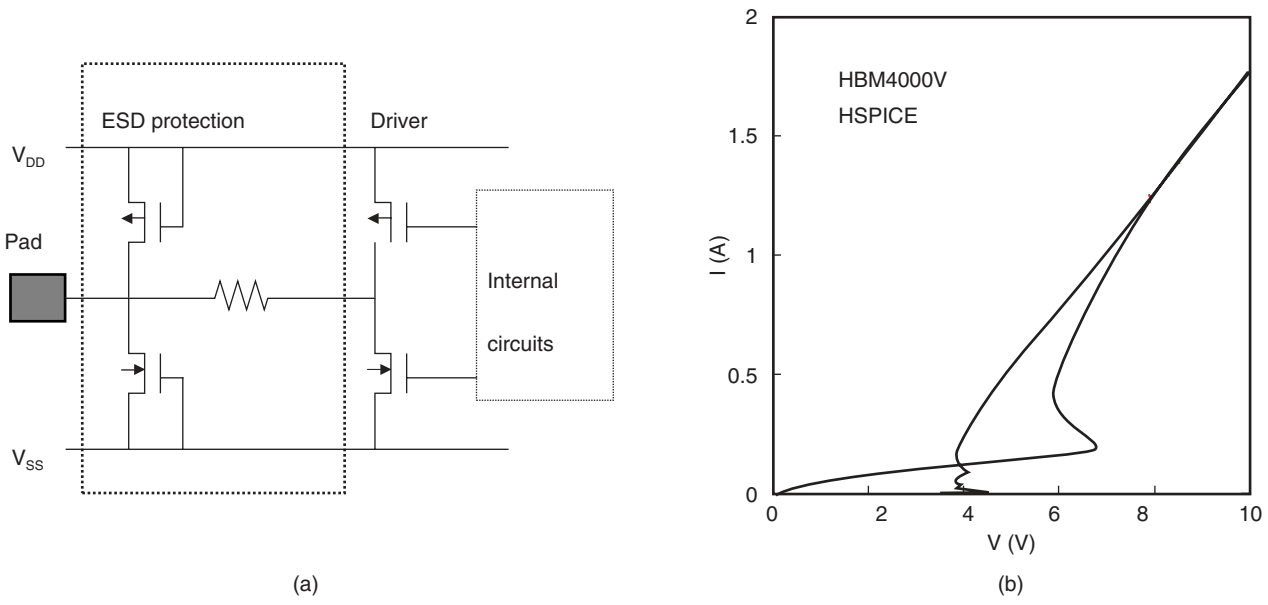


Figure 15
(a) Typical I/O circuit with protection devices and (b) simulated snapback characteristic for I/O under HBM stress.

John Wiley & Sons, 2002.

2) S. H. Voldman: The State of the Art of Electrostatic Discharge Protection: Physics, Technology, Circuits, Design Simulation, and Scaling. *IEEE Journal of Solid-State*, **34**, 9, p.1272-1282 (1999).

3) A. Amerasekera, S. Ramaswamy, Mi-C. Chang, and C. Duvvury: Modeling MOS Snapback and Parasitic Bipolar Action for Circuit-Level ESD and High Current Simulations. Proc. IEEE 1996 International Reliability Physics Symposium (IRPS), p.318-326.

4) J. Z. Chen, A. Amerasekera, and C. Duvvury: Design Methodology and Optimization of Gate-Driven NMOS ESD Protection Circuits in Submicron CMOS Processes. *IEEE Trans. on Electron Devices.*, **45**, p.2448-2456 (1998).

5) S. G. Beebe: Simulation of Complete CMOS I/O Circuit Response to CDM Stress. Proc. EOS/ESD Symp., 1998, p.259-270.

6) M. P. J. Mergens, W. Wilkening, G. Kiesewetter, S. Mettler, H. Wolf, J. Hieber, and W. Fichtner: ESD-level Circuit Simulation-Impact of Gate RC-Delay on HBM and CDM Behavior. Proc. EOS/ESD Symp., 2000, p.446-455.

7) S. L. Lim, X. Y. Zhang, Z. Yu, S. Beebe, and R. W. Dutton: A Computationally Stable Quasi-Empirical Compact Model for the Simulation of MOS Breakdown in ESD-Protection Circuit Design. Proc. 1997 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD), p.161-164.

8) X. Y. Zhang, K. Banerjee, A. Amerasekera, V. Gupta, Z. Yu, and R. W. Dutton: Process and Layout Dependent Substrate Resistance Modeling for Deep Sub-Micron ESD Protection Devices. Proc. IEEE 2000 International Reliability Physics Symposium (IRPS), p.295-302.

9) H. Anzai, S. Satoh, and K. Suzuki: Investigation of ESD protection device by circuit simulator. (in Japanese), Technical Report of IEICE, VLD99-58, p.47-53.

10) K. Suzuki, H. Anzai, T. Nomura, and S. Satoh: Parasitic Bipolar Transistor Model Using Generated-Hole-Dependent Base Resistance. Proc. IEEE 2001 International Reliability Physics Symposium (IRPS), p.246-252.

11) H. Anzai, Y. Tosaka, K. Suzuki, T. Nomura, S. Satoh, and H. Oka: An Equivalent Circuit Model of ESD Protection Devices. (in Japanese), Technical Report of IEICE, VLD2001-68, p.1-6.

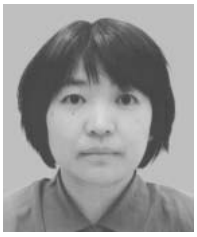
12) H. Anzai, Y. Tosaka, K. Suzuki, T. Nomura, S. Satoh, and H. Oka: An Equivalent Circuit Model ESD Protection Devices. (in Japanese), Technical Report of IEICE, VLD2002-73, p.25-29.

13) Star-Hspice User's Manual Version 2002.2, Synopsis, Inc.

14) TSUPREM-4 User's Manual Version 2002.2, Synopsis, Inc.

15) Medici User's Manual Version 2002.2, Synopsis, Inc.

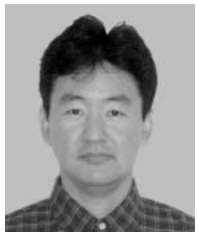
16) Y. Cheng and C. Hu: MOSFET MODELING & BSIM3 USER'S GUIDE. Inc. 2002.



Hiromi Anzai received the B.S. and M.S. degrees in Physics from Nihon University, Tokyo, Japan in 1985 and 1987, respectively. She joined Fujitsu Laboratories Ltd., Atsugi, Japan in 1987, where she has been researching the ESD reliability of MOS devices. Her current research interests are simulations of semiconductor processes, devices, and circuits. Ms. Anzai is a member of the Japan Society of Applied Physics.

Yoshiharu Tosaka received the B.S., M.S., and Ph.D. degrees in Physics from Niigata University, Niigata, Japan in 1985, 1987, and 1990, respectively. He joined Fujitsu Laboratories Ltd., Atsugi in 1990. His current research interests are reliability phenomena in semiconductors, especially those related to ESD and soft errors, and simulations of processes, devices, and circuits. Dr. Tosaka is a member of the Japan Society of Applied Physics and the Physical Society of Japan.

Kunihiro Suzuki received the B.S., M.S., and Ph.D. degrees in Electronics Engineering from Tokyo Institute of Technology, Tokyo, Japan in 1981, 1983, and 1996, respectively. He joined Fujitsu Laboratories Ltd., Atsugi, Japan in 1983, where he has been engaged in design and modeling of high-speed bipolar and MOS transistors. He was a visiting researcher at the Swiss Federal Institute of Technology (ETH) Zurich, Switzerland in 1996 and 1997, where he studied process modeling. His current interests are process and device modeling. He is a senior member of the IEEE.



Toshio Nomura received the B.S. and M.S. degrees in Electronic Engineering from Tokai University, Kanagawa, Japan in 1984 and 1986, respectively. He joined Fujitsu Ltd., Kawasaki, Japan in 1986, where he has been engaged in the process integration of CMOS devices.

Shigeo Satoh received the B.S. and M.S. degrees in Instrument Engineering from Keio University, Tokyo in 1984 and 1986, respectively. He joined Fujitsu Laboratories Ltd., Atsugi, Japan in 1986. He has been engaged in the design and modeling of CMOS devices at Fujitsu Ltd. He is a member of the Japan Society of Applied Physics.