Erratic Fluctuations of SRAM Cache Vmin at the 90nm Process Technology Node

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Abstract

Erratic bit phenomena have been reported in advanced flash memories, and have been attributed to trapping/detrapping effects that modify the threshold voltage. This paper describes for the first time the observance of erratic behavior in SRAM Vmin, defined as the minimum voltage at which the SRAM array is functional. Random telegraph signal (RTS) noise in the soft breakdown gate leakage is shown to be the cause. The erratic Vmin phenomenon can be eliminated for 90nm SRAMs by process optimization. However, erratic Vmin behavior gets worse with smaller cell sizes and represents another constraint on the scaling of SRAM cells and on the minimum operating voltage of the SRAM array. A combination of process and circuit solutions will likely be needed to enable continued SRAM cell scaling.

Introduction

Previous literature [1] on flash memory arrays has shown that flash cells can exhibit erratic erase behavior due to carrier trap-ping/de-trapping that modifies the threshold voltage of the cell. Several studies [2,3] have indicated that a soft breakdown mode may be responsible for these fluctuations. Single electron trapping/de-trapping has been observed for some time on discrete transistors as RTS noise induced by soft break-down. This paper will demonstrate that erratic fluctuations can occur in the Vmin of 90nm SRAM arrays and that these fluctuations are due to soft breakdown induced RTS noise events in the NMOS pull-down device of a few random 6-T SRAM cells.

Erratic Vmin SRAM Behavior

This study utilizes an SRAM array consisting of a large number of 1.15 μm^2 SRAM cells and was fabricated in our 90nm logic technology [4]. Unit level measurements of unstressed SRAM arrays have shown erratic bit behavior during early stages in process development. We observed that the Vmin on some SRAM arrays varied from one measurement to the next. This erratic behavior can be characterized by simply examining the Vmin on each unit as a function of the number of measurements. Plotting the range of the fluctuation as a function of sampling in Figure 1

illustrates that the amplitude of the fluctuations is a direct function of the number of observations. As the number of observations increases, the range of the erratic fluctuations also increases. Such a behavior indicates that the study of erratic bit phenomena in SRAM arrays requires extensive sampling to properly characterize the maximum range of the erratic bit phenomena.
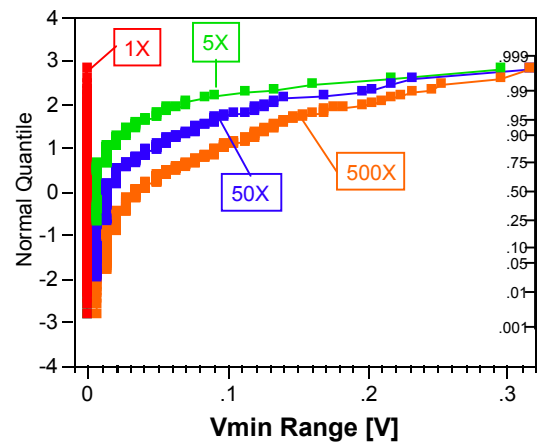
Figure 1: The tail of the Vmin range distribution increases as more observations are taken. Data indicates that observation of erratic fluctuations is directly dependent on amount of sampling.

As shown in figure 2, transforming the erratic data from the time domain to the frequency domain clearly shows a 1/f behavior and indicates a trapping/de-trapping mechanism.

A raster level analysis of the array shows that the erratic unit level behavior is due to a single limiting bit moving between the tail and bulk of the bit level distribution and that the location of the fluctuating bit is spatially random. The spatial independence of the limiting bit is especially important since it eliminates the possibility of a local die-level process marginality. In addition, the movement of the erratic bit between the bulk and tail of the distribution shows that the erratic behavior must be characterized using statistical sampling techniques since tracking the behavior of a single bit does not accurately capture the behavior of the entire cell level distribution.
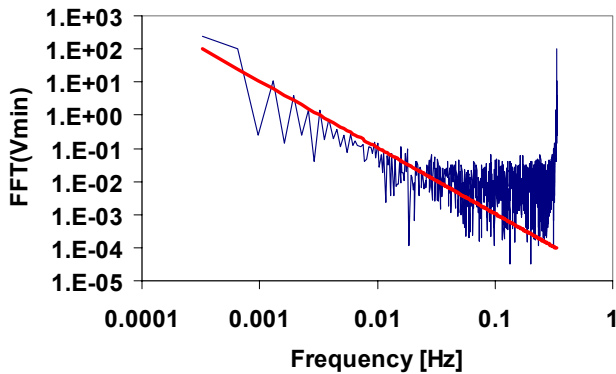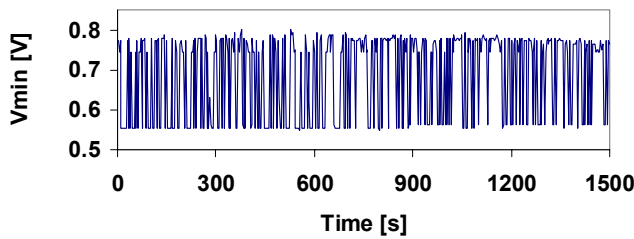
Figure 2: Time domain and spectral analysis of a single SRAM unit's Vmin behavior shows that the noise spectrum follows a 1/f dependence.

Discrete pico-probing of individual erratic cells on over 20 units have consistently showed the time varying gate-to-source leakage noise seen in figure 3 on one of the NMOS pull-down devices of the 6-T cell. Circuit simulations of an SRAM cell using the fault model shown in figure 4 have demonstrated that the measured gate leakage fluctuations are consistent with the observed Vmin fluctuation of the limiting bits in the array.
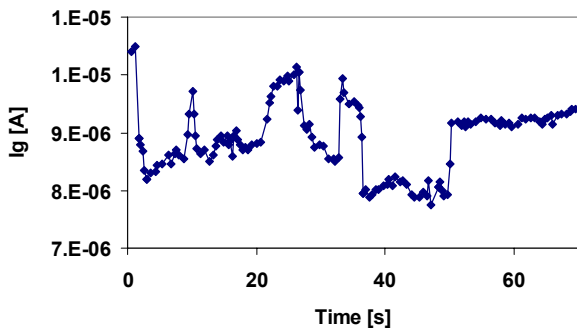

Figure 3: Electrical probing of an erratic cell in the SRAM shows large fluctuations in the gate current in one NMOS pull-down. The other NMOS pull-down has over an order of magnitude lower leakage and is time invariant.
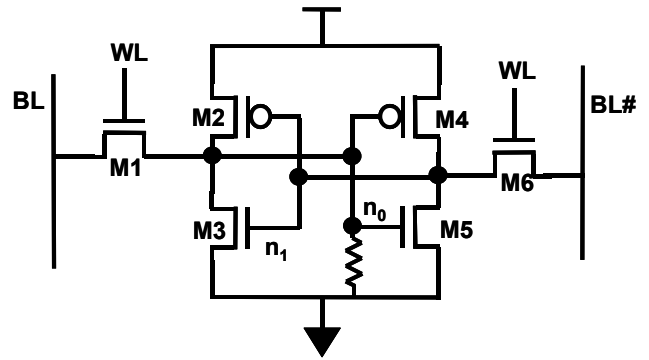
Figure 4: SRAM cell with gate oxide leakage between the gate and source of M5 which can result in Vmin stability problems.

Single SRAM Cell Results

Simulation data in figure 5 shows that the Vmin behavior is very sensitive to the gate leakage of the NMOS pull-down device and indicates that small fluctuations in gate leakage could lead to large fluctuations in Vmin. The key point is that the high sensitivity to gate leakage fluctuations is only apparent at high levels of gate leakage and can only occur when the device has reached gate oxide soft breakdown.
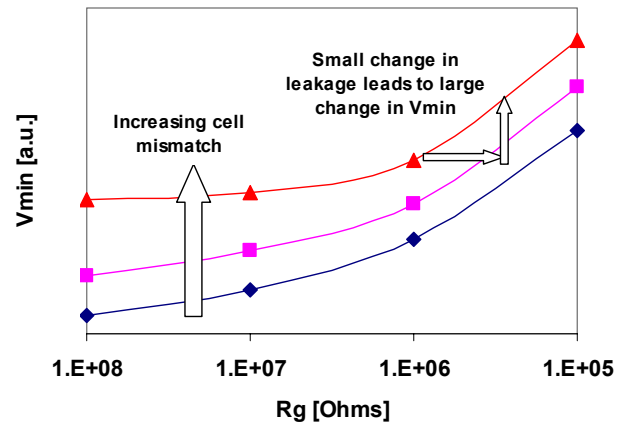

Figure 5: Simulations of cell Vmin as a function of defect leakage and pull-down asymmetry are consistent with measurements and show that the impact of small changes in gate leakage due to RTS noise can have large impacts on the Vmin of the cell.

To study the effect of the gate leakage fluctuations on Vmin of a discrete SRAM cell, an experiment was conducted to measure the Vmin of an isolated SRAM cell test structure after soft breakdown was induced on the NMOS pull-down transistor. The isolated cell test structure has all of the devices in the cell connected to pads such that a single NMOS pull-down device can be stressed independently of the other devices. The soft breakdown event was induced

using the standard technique of stressing the device with an external resistor. Once soft-breakdown was observed, the other devices in the cell were checked to ensure that they were not damaged.

The 1/f noise spectrum of the post soft breakdown current of the stressed transistor shown in Figure 6 is the same as that observed on SRAM level data and indicates that the erratic bit fluctuations are due to a soft breakdown failure model. In addition, read Vmin measurements have been conducted on the cell and show similar behavior to that of the limiting cell in the SRAM array. The single cell data shows erratic behavior and the erratic behavior increases with cell mismatch induced by degrading the PMOS device. All observed experimental behavior is consistent with the simulation results presented in figure 5.
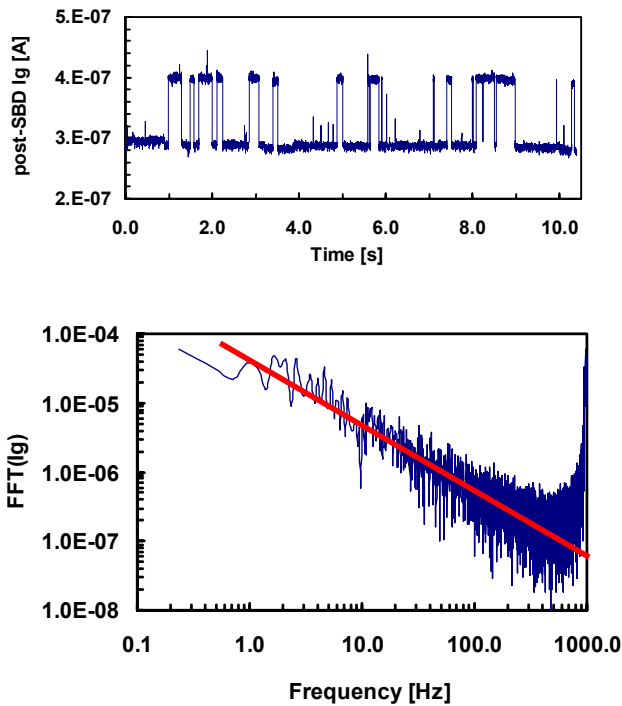
Figure 6: Time domain and spectral analysis of device level RTS noise measurement of post SBD gate current shows a 1/f type of behavior and is consistent with the unit level Vmin behavior.

In figure 7, the single cell data shows Vmin fluctuations that increase with additional sampling. The Vmin range is far above the noise of the measurement and is consistent with that observed for the SRAM array in Figure 1.
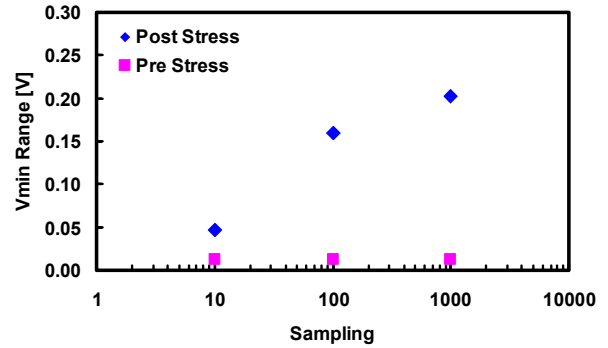
Figure 7: Single cache cell Vmin measurements show that Vmin instability can be induced by soft breakdown in the NMOS pull-down. The erratic Vmin behavior is consistent with the previously observed SRAM array behavior.

Erratic Behavior During Stress

Previously published data [1] on erratic behavior in flash cells has shown no correlation between pre and post burn-in units. Normal bits can become erratic and drop into the tail of the distribution while previously stable bits can show fluctuations. Figure 8 confirms this behavior by demonstrating that the Vmin range at time zero is not necessarily correlated to the range at any readout during burn-in stress. It is believed that the ability of bits to become more stable, after an initial period of instability, is due to a progression to a "harder" oxide breakdown mode that exhibits less gate leakage noise.
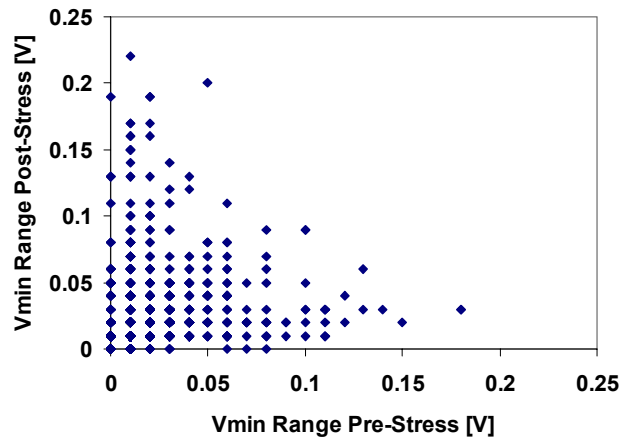
Figure 8: Post stress vs. pre-stress Vmin range data shows simi-lar behavior to that reported for flash memories. Unit instability can become better or worse during stress.

To demonstrate how the erratic behavior can worsen during stress, the pull-down NMOS and pull-up PMOS devices were stressed independently in the single cell test structure so that the effects of RTS noise induced by oxide soft breakdown and the cell imbalance caused by PMOS NBTI

could be decoupled. Figure 9 illustrates that additional PMOS stress after the soft breakdown event can create more cell imbalance by increasing the Vmin range and exaggerate the erratic effect. It is believed that the effect of PMOS degradation can cause the erratic cell behavior to increase during stress of the SRAM array.
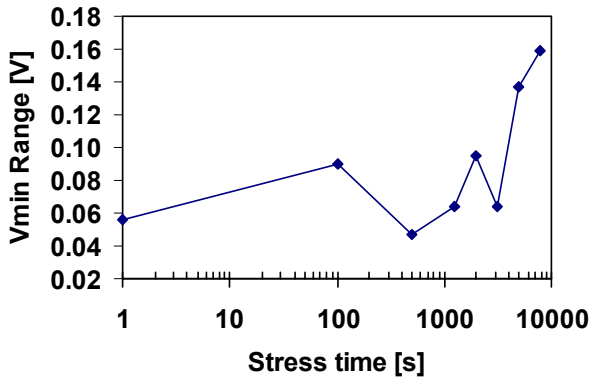

Figure 9: PMOS NBTI stress on the PMOS pull-up transistor can increase the erratic Vmin fluctuation.

Process Solution Path

Optimization of our 90nm process resulted in an elimination of the erratic Vmin behavior of SRAM cells. Two approaches were used. First, an improvement in gate oxide quality reduced the likelihood of gate oxide soft breakdown. Second, optimization of SRAM cell device strength ratios reduced the sensitivity to gate oxide soft breakdown. The results, in Figure 10, show that the Vmin range is reduced to a very low level after burn-in stress.
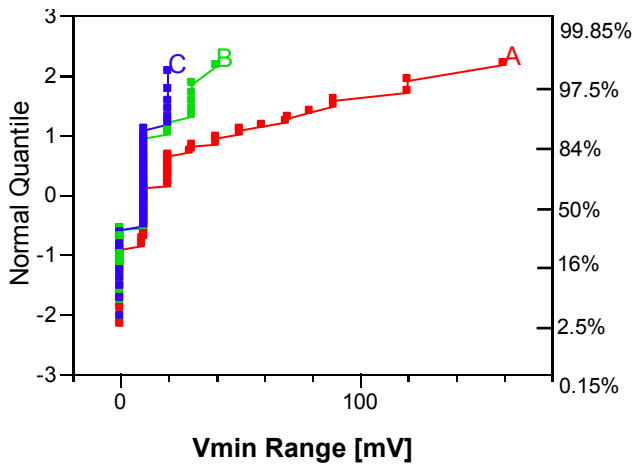

Figure 10: Process optimization improvements from case A to case C can reduce the range of Vmin fluctuations after burn-in stress. The remaining variation is within the tester repeatability.

CMOS Scaling Trends

As SRAM cell sizes are scaled, mismatch driven cell stability degrades, and the sensitivity of the cell to gate

oxide soft break-down defects is increased, as shown in Fig. 11. In addition, the larger number of SRAM cells per unit area increases the probability of incorporating an erratic bit in an SRAM array. A combination of process and circuit solutions will likely be needed to enable continued scaling of SRAM cell size and continued scaling of minimum operating voltage.
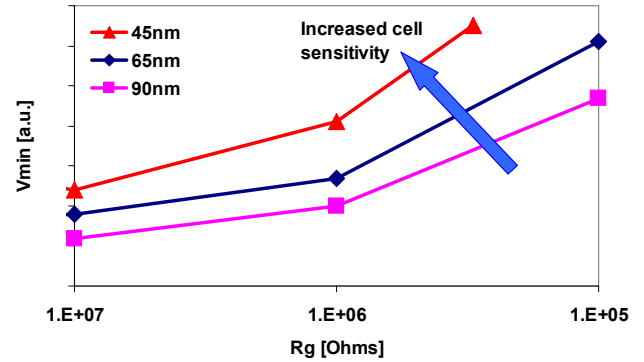

Figure 11: Scaling trend for Vmin sensitivity to gate leakage shows that the erratic fluctuation issue worsens with cell size scaling as the static noise margin decreases.

Summary

Erratic Vmin cell behavior in SRAM arrays has been studied and shown to be due to soft breakdown induced RTS noise. Cell level characterization clearly shows that the Vmin fluctuation can be worsened by PMOS NBTI degradation. Both SRAM and device level data indicate that the erratic behavior follows a 1/f noise spectral density, and SRAM sampling indicates that the amplitude of the fluctuations can increase with number of readouts. Process optimization can effectively be used to lessen the effect of RTS noise on Vmin behavior. Alternatively, the power supply could be increased to solve the problem at the expense of higher leakage and power. Future process technology development will require process and circuit solutions.

References

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