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ERRATUM

Erratum to: Design of new practical phase shaping circuit using optimal pole–zero interlacing algorithm for fractional order PID controller

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Unfortunately, the Fig. 4a, b was incorrect in the original publication of the article. The correct version of Fig. 4a, b is given here.

The original article was corrected.

The online version of the original article can be found under doi:10.1007/s10470-016-0920-0.

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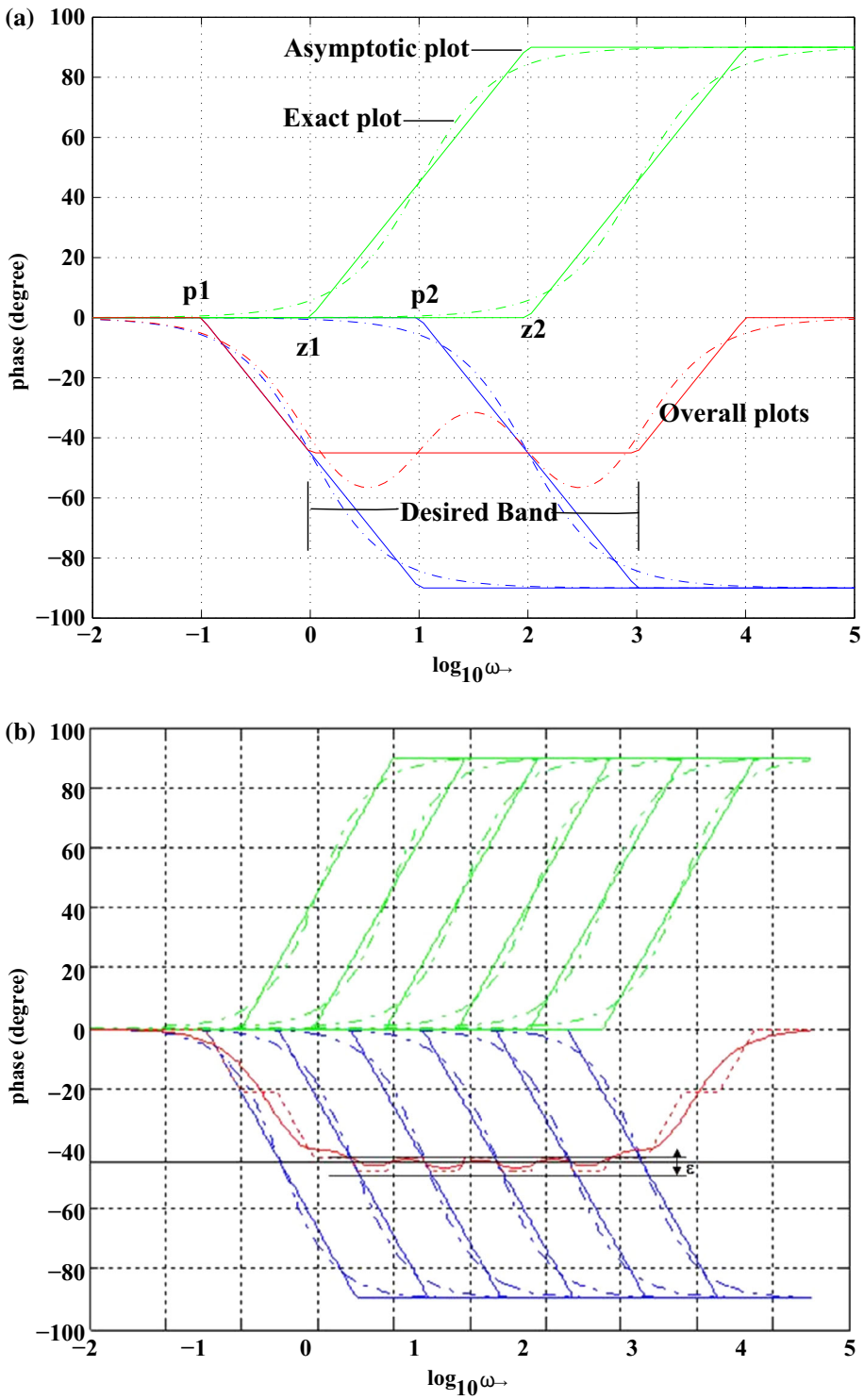

Fig. 4 **a** Asymptotic phase plot with two pole–zero pairs for $\alpha = -0.5$ ($-45°$). **b** Asymptotic phase plot with six pole–zero pair