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Erratum to: Ultrathin flexible InGaZnO transistor for implementing multiple functions with a very small circuit footprint

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Erratum to

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The article "*Ultrathin flexible InGaZnO transistor for implementing multiple functions with a very small circuit footprint*" written by Chaoqi Dai, Peiqin Chen, Shaocheng Qi, Yongbin Hu, Zhitang Song, and Mingzhi Dai, was erroneously originally published electronically on the publisher' internet portal (currently SpringerLink) on 30 September 2020 with caption of Fig. 1 and related context, and the Acknowledgements.

Instead of
Figure 1 (d) To implement an AND gate, the traditional design uses 3 transistors, the latest report uses 2 transistors [14], and the single transistor design uses 1 transistor.

It should read
Figure 1 (d) To implement an NAND gate, the traditional design uses 3 transistors, the latest report uses 2 transistors [14], and the single transistor design uses 1 transistor.

On page 2, instead of
As illustrated in Fig. 1(d), the conventional design of the AND logic gate has 3 transistors, whereas a recently-published design has two transistors [14]. The design here can implement the AND gate using only one transistor.

It should read
As illustrated in Fig. 1(d), the conventional design of the NAND logic gate has 3 transistors, whereas a recently-published design has two transistors [14]. The design here can implement the logic gates such as logic NAND gate or logic AND gate using only one transistor.

In the Acknowledgements, instead of

Acknowledgements

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It should read

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