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RICE UNIVERSITY

ESD CIRCUIT SYNTHESIS AND ANALYSIS USING TCAD AND SPICE

by

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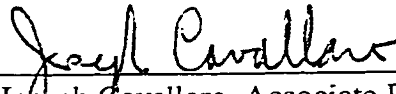

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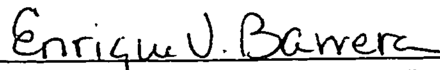

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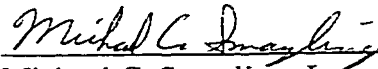

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ABSTRACT

This thesis describes the development of a SPICE sub-circuit model for an avalanche triggered SCR used for ESD protection in integrated circuits. The purpose of this work was to develop a model that accurately predicts the terminal characteristics of the SCR operating under steady state and transient conditions. Process and device simulations (using Technology Computer Aided Design tools, or TCAD tools) were used to gain insight into the dynamics of the complex SCR behavior prior to and during the latchup triggering. Test structures of the SCR, as well as its sub-components, were fabricated for characterization and modeling data collection. The TCAD results gave us access to internal physical quantities at key points along the I-V characteristics, which explicitly indicated the dynamics leading to latchup triggering. These analyses and the test structure characterization were necessary to properly formulate the SPICE model. The SPICE model development approach is presented, as well as methods to validate the model including steady state and fast rise time transient measurements on the actual ESD circuit. This is the first SPICE model presented for an avalanche triggered SCR demonstrating accurate terminal behavior under both steady state and transient triggering conditions. It is intended for use in a design environment for examining ESD circuit behavior at the chip level. The model allows a way to synthesize new circuits in a simulation environment without the need to fabricate test circuits and variations in silicon. Furthermore, the physical insight gained from the models will become more important as process technologies scale into deep submicron feature sizes.

ACKNOWLEDGMENTS

A research project leading to a dissertation is the result of hard work and the dedication of many people. There is no question that the guidance, support, and mentoring of my advisors played a tremendous part in my completion of this project. To Mike Smayling and "Dr. Bill" Wilson, I want to say "thanks" for believing in my ability and allowing me to grow, and learn, throughout the course of this project. While this dissertation contains specific details and results of my research, I believe that other, less easily observable results, are equally important. The insight I gained regarding the general scientific concepts of laboratory observations, analysis, modeling, and verification will stay with me forever. I also want to thank Mike for teaching me the value of an efficient infrastructure. In the end, the ability to obtain data, be it from a silicon wafer or from a simulation result, in an efficient and well planned manner, is what allowed me to do the analysis and obtain the results I present in these pages.

Many other individuals have been an important part of my life these past few years. Professor Richard Tapia inspired me in my undergraduate years, and I am indebted to him for all those years of mentoring and guidance. My colleagues Alister Young and Ichiro Fujii provided technical and moral support which helped me overcome seemingly "insurmountable" barriers. I want to thank my fiancee, Nubia Sanchez, for her incredible patience these past few years. I love you Nubia, and I'm looking forward to our wedding and our life together. Last but not least, I want to thank my parents, Donato and Gloria Rodriguez, for all the love and support they have provided me, my brother Miguel, and my sister Sonia.

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CHAPTER 1

INTRODUCTION

1.1 Overview

The goal of the research described in this thesis was to identify methods that can be used to systematically develop components and circuits used for the protection of integrated circuit chips against electrostatic discharge (ESD) damage. These specialized circuits tend to be a complex mixture of sub-components, some normally considered "parasitic," which are used to form a complete protection network. The circuits usually exhibit complex terminal characteristics that make it difficult to model them accurately. The sub-components themselves often are not characterized individually, and as a result, it is difficult if not impossible to quantify their effects on the overall circuit operation. This lack of analysis at the component level, as well as the circuit level, leads to ignorance of the actual circuit and its physics, which makes it impossible to quantify its behavior during an ESD event.

The results presented here demonstrate that a systematic approach of analysis and synthesis can be used to effectively develop ESD circuits and models. The emphasis will be placed on the tools and the methods that are necessary for understanding the physics and terminal characteristics of ESD circuits. Accurate models for ESD circuits add significant capability to IC designers as it allows them a way to analyze the behavior of these circuits at the chip level under normal pin operation as well as during a discharge

event. The case today is that a chip failure in some way related to ESD circuitry, whether due to a discharge or not, is not easily modeled or understood [1].

The methods presented in this thesis are intended for use in analyzing sub-component behavior and developing models that accurately quantify these individual parts as well as the overall circuit operation. In order to accomplish this, the models must be based on the physical operation of the circuit, and must fully comprehend its static and dynamic characteristics. To this end, the use of commercially available TCAD tools were coupled with measurements on actual silicon devices to confirm the physics and operation of the circuit used in this study. The simulation results are significant due to their accurate representation of the circuit operation, and most importantly, to the insight gained into the circuit operation.

A very important part of this work is based on the TCAD simulation results, but an equally important part was based on the test structures specifically designed and fabricated to characterize the different parts of the circuit. Measurements were made and data was collected for the individual components and circuits for both their static and dynamic operation characteristics. The approach and methods used for these measurements will be described in detail.

The results of this research demonstrate that the terminal characteristics of the ESD circuits can be understood explicitly, and models for circuit level simulation can be developed that accurately model the static and dynamic operation of these complex circuits. As a specific example of this work, a SPICE model for an avalanche-triggered silicon-controlled rectifier (AT-SCR) will be presented which accurately demonstrates all

of the appropriate features measured on the silicon test structures. This is the first model presented for the AT-SCR demonstrating these capabilities.

In what follows of this introductory chapter, some basic information regarding static charge phenomena will be summarized. In addition, basic protection elements for integrated circuits will be presented, including relevant literature references with a brief perspective on previous work in ESD circuit analysis and modeling.

1.2 Background and Definitions

Any separation of static charges can lead to an electrostatic discharge, commonly referred to in the electronics industry as an ESD event. ESD events are familiar to most people as the "zaps" felt occasionally when touching a doorknob or other grounded metallic ware after walking across a carpet, especially on a dry day. This phenomenon occurs when an excess charge is allowed a low resistance discharge path to ground. ESD has long been recognized as one of the biggest threats to electronics, particularly in integrated circuit form. It is a reliability issue, creating damage in the IC's due to the high discharge currents that can form, and it is also an economic threat, as damaged packaged parts means the long process of fabrication, testing, packaging and shipping has to be re-done to replace that part. In actuality, many parts are manufactured at once, but damage due to ESD means an IC that was otherwise functional and met the required specifications has to be replaced, and this leads to increased manufacturing costs and delays at the final product manufacturing line.

As a result of the impact of ESD on integrated circuits, standard procedures have been defined to help reduce the possibility of damaging integrated circuits during handling and manufacturing. Usually these employ a method of slowly releasing any excess charge to ground (through a highly resistive path), preventing the formation of high currents during handling. While this reliability problem is well understood, damage to IC's by electrostatic discharges still occurs, and is one of the primary causes of customer returns. This is because there are ways of reducing or removing excess static charge, but no perfect way of eliminating it from occurring in the first place.

The discussion that follows will discuss some basic principles of electrostatic discharge, such as how charges are created and why they can be harmful to integrated circuits. Many researchers have spent years devising ways of preventing ESD damage to IC's, particularly by designing special circuitry intended to protect the microchips during an ESD event. Some of this work will be briefly reviewed, with the intention of summarizing some of the progress made in this area. Of particular importance is the increasing use of computer models for understanding the physical effects which become important during static discharges in IC's. Standard models for ESD testing of IC products have been developed, and will also be discussed here. The emphasis in this introduction is to give insight into why ESD events occur, the origin of charges, and typical effects that can be observed in an IC as a result of static discharges.

1.3 Excess Charge Creation

One of the main points to get out of this introductory chapter is the fact that static charges are easily generated, and these exist in many of our day-to-day experiences. In the doorknob example, the person has acquired a charge due to the rubbing of his/her shoes with the carpet. When rubbed against most materials, the carpet will tend to become positively charged. Thus, the shoes gain a negative charge. This negative charge on the shoes in turn induces a net positive charge on the feet. The rest of the body, farther from the shoes, will tend to become negatively charged. This charge separation in a human body is possible due to its capacitance, ~100pF, and its ability to easily redistribute charge.

As the negatively charged hand approaches the doorknob, an electric field forms between it and the hand, and the charge on the doorknob aligns itself in response to this field. Depending on the strength of the electric field, a discharge can occur in different ways. For example, if the field is strong enough (~30KV/cm), the hand approaching the knob can cause the "breakdown" of the air dielectric, creating a path for the charge to ground through the door. More likely, the discharge will occur the moment the hand touches the doorknob. This discharge current is due to the excess electrons on the hand seeking a ground potential. Most discharges are not felt, unless they are of a high enough potential difference and occur in a very short time. Most estimates claim ~3KV as the threshold of human sensation. However, most electronic circuits are sensitive to potentials well below this level.

The rubbing of shoes (triboelectric charging) against a carpet is only one example of charge creation. Examples of other materials and how they tend to charge up can be found in Table 1, which shows the triboelectric series, a list of materials showing their tendency to become either positively charged or negatively charged due to triboelectric charging. For example, rubbing fur with silk will tend to make the fur positively charged, and the silk negatively charged, when separated. This list shows general trends, but many factors influence the final charging, including the surface smoothness, cleanliness, contact area, and speed of material separation.

Fundamentally, there are several methods of creating an excess charge distribution in materials. In addition to triboelectric charging, charge can be created by physical contact (no rubbing), induction, thermionic emission, field emission, ion/electron beams, photoelectric effects, and corona effects.

Contact charging can be understood by thinking about what happens when two dissimilar metals come in direct contact with each other. Since the Fermi energy levels are different, a transfer of electrons will take place in order to bring the system to equilibrium. Thus, the material with lower Fermi energy will tend to gain electrons and become negatively charged when separated from contact. In the case of a metal, the charge will distribute itself evenly over the surface. For an insulator, the charge tends to localize near the point of original contact, and trying to ground it will not allow the charge to "bleed" off.

Table I. The Triboelectric Series.

Tendency to become positively charged

1. Air
2. Human skin
3. Asbestos
4. Glass
5. Mica
6. Human hair
7. Nylon
8. Wool
9. Fur
10. Lead
11. Silk
12. Aluminum
13. Paper
14. Cotton
15. Wood
16. Steel
17. Sealing Wax
18. Hard rubber
19. Mylar
20. Epoxy-glass
21. Nickel, copper
22. Brass, silver
23. Gold, platinum
24. Polystyrene foam
25. Acrylic
26. Polyester
27. Celluloid
28. Orlon
29. Polyurethane foam
30. Polyethylene
31. Polypropylene
32. Polyvinylchloride (PVC)
33. Silicon
34. Teflon

Tendency to become negatively charged

Tribolectric charging is of major concern in semiconductor processing due to the many processing steps requiring the flow of gases and fluids during manufacturing. Many of these potentially could cause excess charges to be placed on the wafer surface, creating a hazard even before the chips are packaged. Static charges in processing potentially lead to other problems as well. For example, these can not only damage internal junctions and oxides, but the charge itself helps to attract other particles, creating defects. Such particles created during processing are normally airborne in the laminar flow and would not necessarily be attracted to the wafer surface.

Induction charging results from bringing a neutral object (conductor) near a charged object. The conductor will tend to redistribute its charges internally as it comes near the electrostatic field lines emanating from the charged object. This is simply because equal charges repel each other, and opposite charges will attract. As the charges re-align in response to the applied field, the initially neutral conductor has become polarized. Different effects can be observed depending on whether this polarized object is grounded or not. For example, if the conductor is grounded, excess electrons will seek the ground level, leaving behind an excess positive charge. Now, if the charged object is removed, the polarized conductor has become positively charged. If the neutral conductor was not grounded, removing the charged object will leave it back in its initial state.

If a net charge is induced on a part, this will be discharged the moment it is placed in a grounded board or socket. This is believed to be one of the most common ways integrated circuits are damaged. For example, if an IC is transported in insulating material that is exposed to an electrostatic field, the packaged part can become charged. It

is for this reason that parts are transported in conductive packages, which provides shielding, and will not allow the parts to become charged. Charging can also take place by handling and touching electronic parts or their cases with a charged hand. Standard procedures in manufacturing areas call for ESD and grounding straps to be tied on the wrist, providing a safe path to ground for any excess charges.

Thermionic emission charging results from the heating up of a material. The heat increases the energy levels of the electrons, allowing them to overcome the material's potential barrier. The result is a positively charged material. Photoelectric charging also results from increasing the electron energy level, but in this case is due to photons falling on the surface of the material. This particular type of charging can lead to parts failing if they are exposed to UV light for large periods of time.

Field emission charging results when solid or liquid particles are exposed to electric fields. The particles become polarized, and for high enough fields may be stripped of electrons, leaving them in a positively charged state. Corona charging is caused by sharply pointed objects being charged to high voltages. If the resulting electric fields are higher than the breakdown field limit for the ambient gas or air, ionization will take place resulting in charged particles. Any other particle entering this ionized region will gain the charge of the most prominent (positive or negative) ion.

Ion and electron beam charging is based on energy transfer from neutral particles with ions, electrons, and alpha particles. Air ionizers work on this principle [2]. Alpha particles are emitted into the air, and the resulting collisions with atoms strip electrons

and lead to positively charged air molecules. The excess electrons in the air also create negative ions as they join with the outer electron orbits of neutral molecules.

In summary, static charges are easily generated in work areas and testing or manufacturing lines. The most common charge threat to IC's are in the form of a charged human or machine contact. Other threats are the induction of charges via automatic assembly areas, where the movement of the parts induces static charges on the parts and subsequently discharge when they are inserted in a grounded board or socket. Charges can also be created during the fabrication process, and these can also pose serious threats to the final product yield. Air ionizers are typically used in the fab clean room areas to help neutralize static charge buildup. During handling, personnel are required to wear wrist straps to prevent them from becoming charged. The wrist strap offers a resistive path (~1Mohm) to ground, preventing fast transient discharges from occurring.

The currents created by ESD discharges can be quite high, on the order of 1A or more. Depending on the magnitude of the discharge, stressing a packaged integrated circuit can lead to thermal destruction of the silicon junctions and/or gate oxide rupture in the internal circuits, making the chip no longer operable. As stated earlier, IC's are actually susceptible to static charge damage throughout the whole manufacturing process: beginning during the wafer fabrication process, through testing, and final manufacturing line assembly. They are particularly susceptible during human handling, and this has led to the development of a standard model, known as the Human Body Model, used throughout the industry for measuring "ESD Robustness."

1.4 Human Body Model Circuit

Figure 1-1 shows a schematic of the electric circuit used to test IC's using the Human Body Model (HBM). The 1.5K-ohm resistor represents the human body resistance, and the 100pF capacitor represents a human body capacitance. Ls and Cs represent parasitic inductance and capacitance associated with the actual testers. Typical voltages used to charge the test capacitor are in the range of 2KV to 4KV. Depending on the application, this voltage may be higher or lower. For example, automotive parts require operation in much harsher environments compared to desktop applications, and they often require higher levels of protection, about 6KV to 10KV [3]. DRAM chips on the other hand are typically stressed to lower levels, on the order of 1KV. It has been noted that for most IC's, being able to pass 2KV or higher stresses leads to a reduced "fallout" during assembly and handling. For parts that are not able to pass 2KV stresses, the fallout rate increases rapidly.

There is another type of stress modeled similar to the HBM, known as the Machine Model (MM). This is for modeling discharges due to contact with machines and equipment during automated assembly, where little or no human handling occurs. The major difference between the Machine Model and the Human Body Model is the series resistance, which for the Machine Model will nominally be about 0 ohms (the body resistance no longer is part of the stress). In practical form, the resistance is about 10 to 25 ohms, and the inductance is about 2.5 micro-henrys. For this test, the discharge

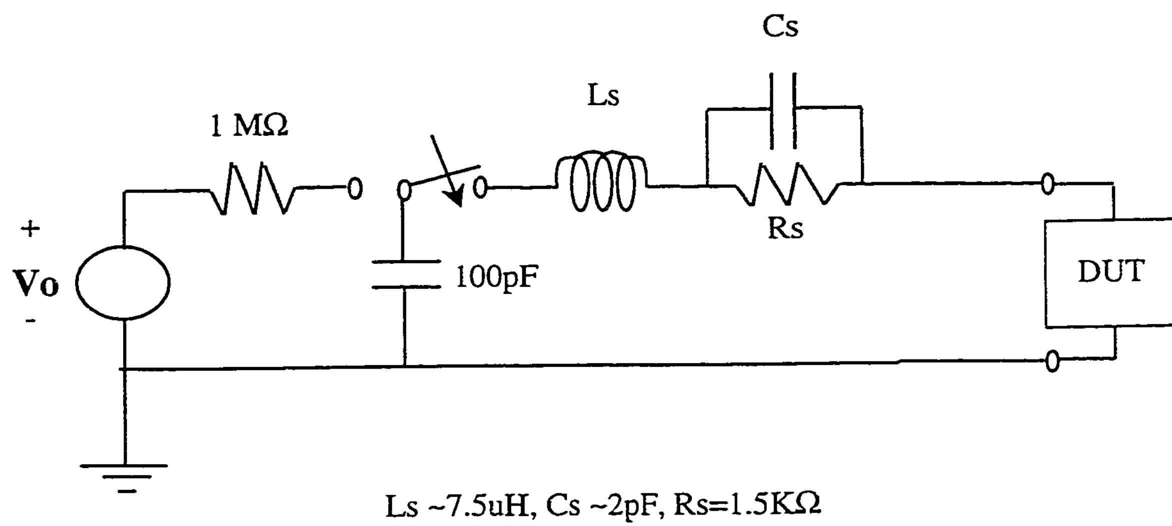


Figure 1-1. Circuit representing the Human Body Model ESD test.

capacitor is charged to 100V or 200V maximum. These parameter values are typical values used in Machine Model ESD tests, but there is no standard industry-wide machine model.

1.5 ESD Protection Circuit Constraints

The ESD circuit must not interfere with IC functions during normal operation. It must have a high impedance state during normal operating conditions, and low impedance during ESD transients. Figure 1-2 shows a scale with relative voltages to illustrate this point. The maximum voltage that the internal circuits are exposed to during a discharge must keep the electric field across the insulating gate oxide below the "breakdown" level. A higher voltage can cause the internal circuits' gate oxide to rupture or become very leaky, making the chip inoperable.

1.6 Components and Circuits for ESD Protection

1.6.1 *Resistor and Diode Combination*

One of the first protection circuits used was a resistor with diodes [4]. This is shown in Figure 1-3. The resistor helps reduce the maximum current through the circuitry, and the diodes are either forward biased, keeping the maximum voltage low, or they reach junction avalanche breakdown, keeping the internal circuits voltage below oxide breakdown. A diffused junction breakdown voltage is one of the basic parameters used to keep the maximum voltage below the gate oxide breakdown voltage. The

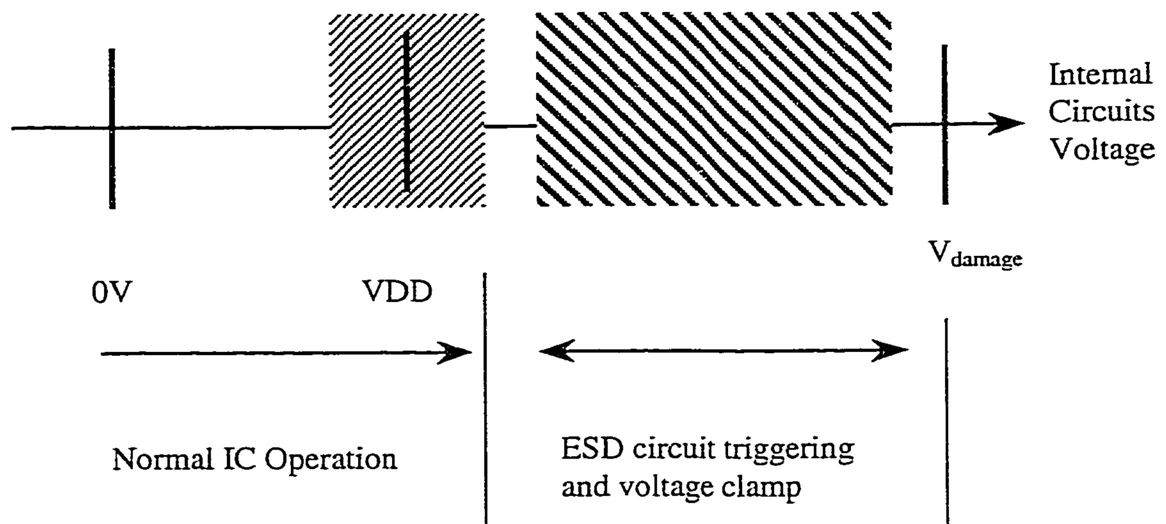


Figure 1-2. Relative voltage scale showing the range of interest for integrated circuit protection against ESD stress.

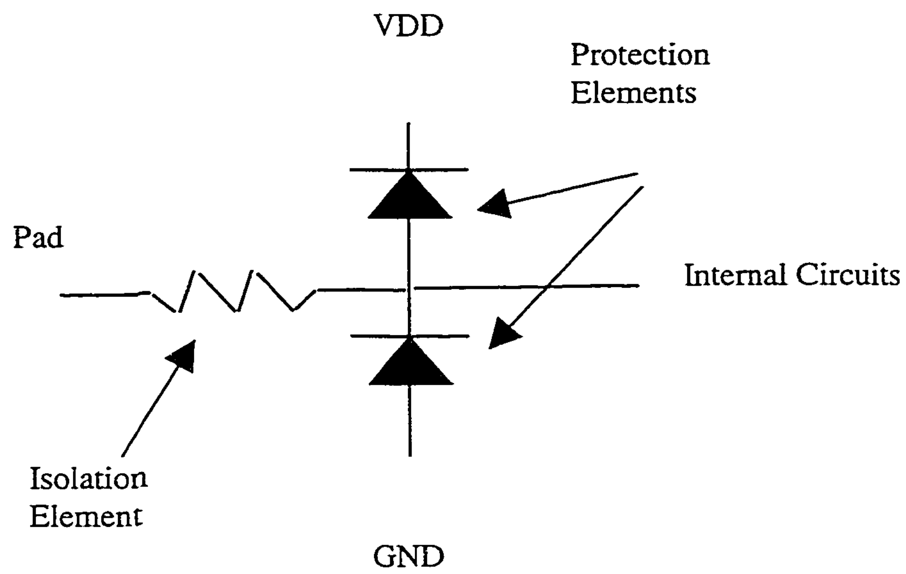


Figure 1-3. ESD protection circuit consisting of a series resistor and diodes to the ground and power supply pins.

disadvantage of the diode approach is that they will conduct and increase the power consumption during normal switching since signal overshoot can forward bias the PN junction during a low to high transition, and the NP diode can become forward biased during a high to low transition.

1.6.2 *NMOS Transistor in Parasitic Bipolar Mode*

NMOS transistors can be useful as ESD protection, if the drain-well junction breakdown is below the gate oxide breakdown. The drain junction avalanche will aid to clamp the maximum voltage, and the high currents induce a parasitic bipolar effect, which will reduce this during an ESD stress. The current source is the drain/well junction avalanche current. A schematic and transistor cross section is shown in Figure 1-4.

1.6.3 *Silicon Controlled Rectifier*

SCR's are useful, if they can be made to trigger below the damage voltage level. Once it's triggered, an SCR goes to a low voltage holding state, which gives it the high current handling capability. Figure 1-5 shows a simple schematic for an SCR. In general, the literature shows, SCR's provide the highest ESD protection levels [5] [6] [7] [8] [9] [10]. The SCR "latches" during a discharge, but it must not latchup during normal conditions. One of the drawbacks of the grounded gate NMOS approach is the relatively high holding voltage during its operation. Since this is ~10V (using the example of a 0.7um CMOS process), the I*V product will tend to be rather high [10]. Using SCR's for ESD protection can improve this, since the holding voltages can be relatively low (~2V

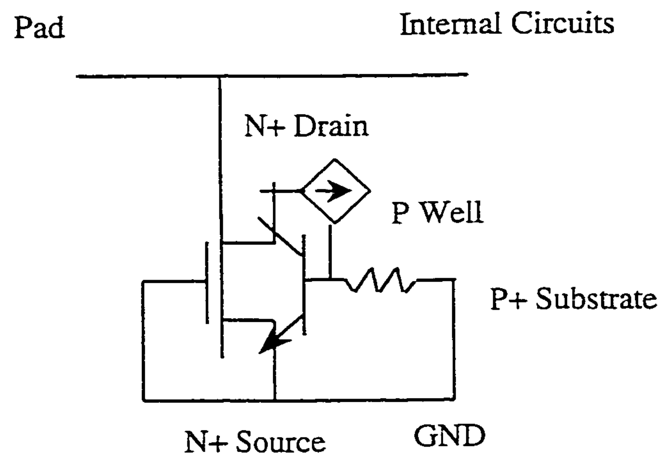


Figure 1-4. NMOS transistor used for ESD protection. The internal junctions of the MOS device behaves as bipolar transistor during the high current stress.

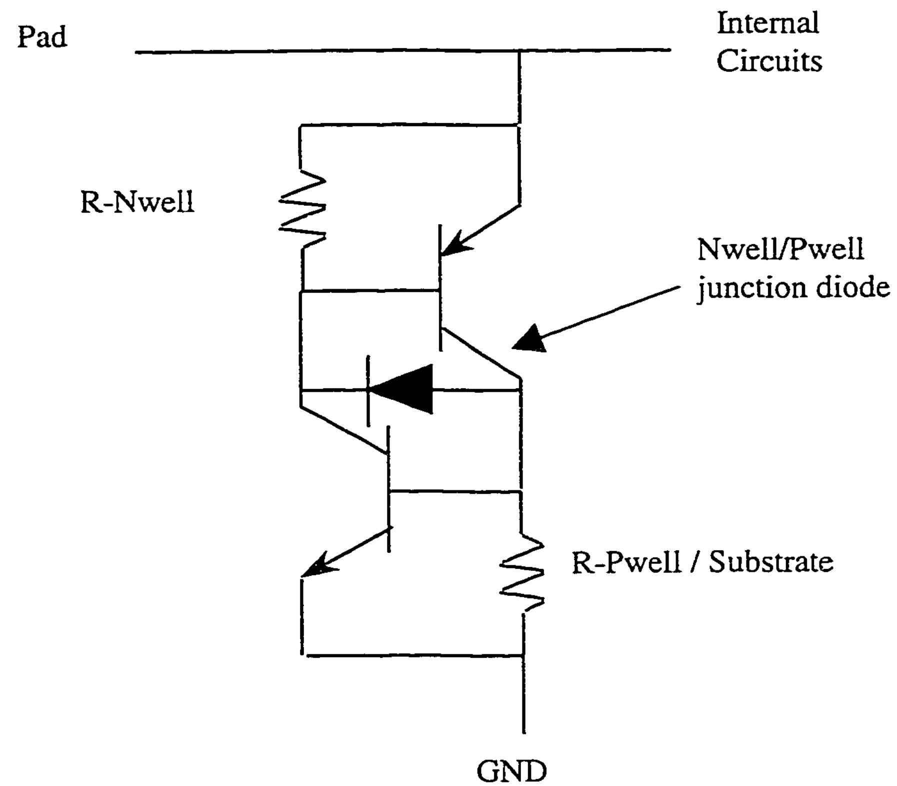


Figure 1-5. Silicon Controlled Rectifier created by parasitic bipolar devices in a CMOS process. The SCR's have a low on-resistance once they are triggered into the latchup mode, however, the latchup triggering may be difficult and require a very high voltage.

or less), thereby reducing the power dissipation in the silicon during an ESD event. Furthermore, the MOS structure is typically optimized for CMOS performance, and the fact that it may be used for ESD protection does not play a role in its development.

For example, MOS scaling for advanced CMOS processes inevitably has resulted in shallower source/drain junctions. Initially it was believed this would help improve ESD performance since the higher electric fields would aid in forcing the "snap-back" mode of operation. In fact, the opposite occurred. Several factors have been used to explain the ESD performance degradation. For example, the failures have been attributed to the reduced drain and source contact resistance due to the use of silicides; a full physical understanding of the observed degradation has not been made, and these effects are still under investigation [11].

SCR's built using parasitic PNPN structures, on the other hand, can be designed especially for the high current operation required for ESD [8] [5] [12]. This allows a more flexible consideration of parameters in designing components specifically for ESD protection. While the CMOS well profiles may not be negotiable, the structures can still be optimized to a certain extent based on layout: spacings between anode/cathode regions for example. The use of the CMOS parasitic SCR's are favorable because once the device is triggered, the well profiles are not critical because these regions become "conductivity modulated," and the high carrier concentration between the anode and cathode creates a very low resistance path for current flow.

Since the input pads are tied to input MOS transistors, one of the critical factors in ESD design is the trigger voltage and/or current required for initiating the latch-up. In general, the important parameters for an SCR include the trigger voltge/current and the holding voltage and current. The holding voltage can be optimized to a low level using appropriate anode/cathode spacings, resulting in a low "on-state" voltage drop which is desirable.

A more complex problem is that of actually triggering the thyristor. The trigger voltage needs to be high enough to avoid latchup during normal operation, but it needs to be low enough that the input gate oxides are not stressed to rupture. Typical dc operation limits the gate oxide electric field to ~10MV/cm. This translates to about 10V for a 100 angstrom gate oxide thickness.

There are several methods of triggering a thyristor. In the extreme end, the reverse-biased center junction (J2) in the pnpn diode can be made to avalanche, creating electron-hole pairs that can then initiate the self-sustaining latchup. The problem with this approach for ESD protection is the high breakdown voltage of typical CMOS Pwell/Nwell junction diodes (~40V or higher). One way to reduce this breakdown voltage is to use an N+ abutting contact at the Nwell/Pwell edge as part of the anode. This will lower the initial breakdown voltage to the N+/Pwell junction diode breakdown, which is ~ 20V or less.

Furthermore, integrated structures using series moat resistances along the input path are commonly used. These serve to help build up the pad voltage to aid in triggering

the SCR's. In general, SCR structures have been found to demonstrate fairly consistent protection over a range of process and layout differences.

1.6.4 *Multiple Stage Circuits*

Typically, several of these elements are used together to form a protection circuit [13] [7] [6] [9]. The secondary element in Figure 1-6 may be an NMOS transistor used to clamp the voltage below the gate oxide breakdown. As the current increases, the resistor allows the pad voltage to build up, eventually triggering the primary element, which is usually a silicon controlled rectifier. The primary element is there to protect the internal circuits as well as the other elements in the ESD circuit.

In this research, a type of multi-stage ESD circuit, consisting of a SCR triggered by avalanche breakdown of a junction to initiate the bipolar currents is studied in detail. The SCR consists of a diffused N+ resistor tied to the drain of an NMOS transistor. The input pad is tied directly to one end of the N+ resistor. During a stress, the pad voltage rises, eventually reaching the point of avalanche breakdown of the NMOS drain N+/P-well junction. During this avalanche, electrons are swept by the high electric field in the depletion region into the drain terminal, and holes are injected into the P-well and P-substrate, which is at ground potential. As the avalanche continues, more hole current flows into the substrate, causing the source junction of the NMOS transistor starts to become forward biased. This is due to the hole current raising the potential near the surface above ground level. As the N+/P-well source junction becomes forward biased, electrons are injected into the P-well. Some of these electrons diffuse through the P-well

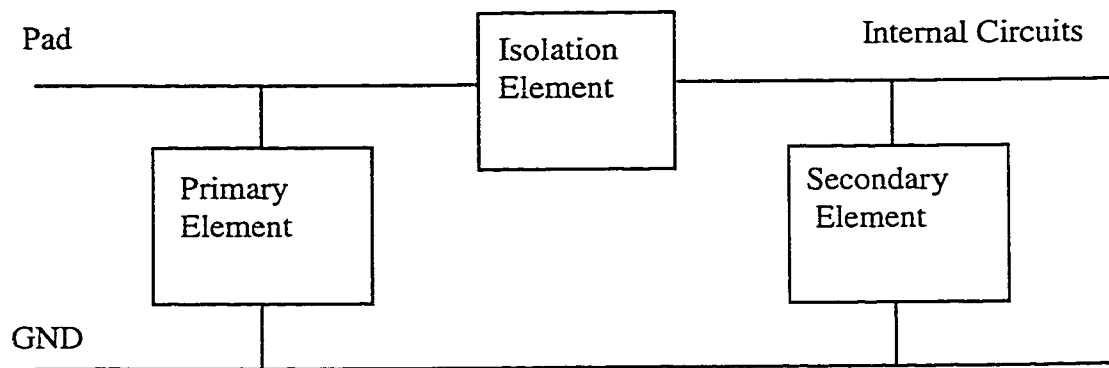


Figure 1-6. Typical ESD circuitry consisting of multiple stages and components.

(which has now become a NPN base region) and get collected by the drain (which is now behaving as a NPN collector). There are some electrons that do not diffuse across towards the drain, but instead are collected by a nearby N-well region that is tied to the input pad. This second NPN transistor forms part of the SCR. As the pad voltage continues to rise, the current through the N-well starts to forward bias a P+ junction (also in the N-well), initiating a PNP current flow. The P-substrate acts as the PNP collector. Once this current is high enough, the SCR regenerative currents increase and the structure enters into its latchup state. Detailed analysis and models for this structure will be presented later in the thesis.

IC stressing by machine and human handling both lead to similar damage, and that typically is thermal junction damage and/or filament creation across MOS structures. A third form of IC damage is seen, although not as often. This damage results in MOS transistor oxide breakdown. This failure mode was observed after protection circuits were able to protect to 2KV HBM and 200V MM type stresses. The mechanism of ESD stress in this case is believed to be the charging of a packaged IC during assembly or transport in manufacturing lines. The discharge will occur when one of its pins contacts a metal handler or is inserted into a grounded socket. Again, there is no agreed upon model, but a typical one will stress to ~1KV and the pulse duration is on the order of a few nanoseconds.

As mentioned earlier, industry standard models are available for manufacturers to test their products and verify the ESD protection level. This allows semiconductor suppliers a way of building in ESD robustness and thus improve the reliability of the

products. Adding ESD as part of the IC reliability and qualification process has led to a large amount of research towards understanding discharge effects on electronics, and ways to design special circuits intended to protect the electronic chips. Typically, empirical relationships have been combined with test chip circuit testing to help design protection structures intended to protect internal IC circuitry during an ESD event. More often than not, this approach has required several wafer fabrication cycles to complete, with continuous "tweaking" of the layout/design of the protection structures.

Recently, researchers have published work regarding the use of computer models in the design of ESD structures and for gaining physical understanding of the associated phenomena. From these efforts, it is clear that the use of computer simulation is an increasingly important method in helping to reduce the costs associated with developing integrated circuits exhibiting appropriate levels of ESD protection capability. To date, published work has shown the use of process and device numerical simulators for generating doping profiles and simulating two-dimensional structure response to high current stress pulses. The results show current densities and areas of possible current filament formation in the structure. Other researchers have described the development of electrothermal simulators for examining ESD structure behavior during a stress event [14] [15] [11] [16] [17]. The results show important factors, such as junction temperature, which can be used to compare against empirical models and determine if the "time to failure" criteria will be violated or not. These tools clearly give insight into the physics associated with ESD events, however designers do not use them since they are not

included in standard design flows. Furthermore, they stress the modeling and simulation of individual components *Vs* models for inclusion in a complete circuit simulation.

Some researchers have shown results of modeling more complete systems, including parasitic elements such as background board capacitance. The impact of these elements was shown to make a dramatic difference on the behavior of the protection circuits, and helped to pinpoint the weak areas. Thus it is clear that complete system simulation is an important capability to have. Today, most circuit design and simulation is carried out using SPICE, a simulator that does not include thermal effects.

Despite this, it is still a useful way to ascertain current and voltage characteristics of the circuits being designed. Therefore, this makes it clear that as a way to immediately impact and improve the design of circuits to account for the ESD tests, is to provide models the designers can use on a routine basis. To this end, ESD structures now take on a much more important role: they become part of the process technology supported components. This means that design community is given an ESD component to include in the layout, but it is also supported with a SPICE model, which can then be used to check the interactions with other chip circuits and parasitic elements.

This structured approach requires an understanding of the ESD physics, and how structures operate during a discharge. These structures used for protection are typically complex and are actually made up of several "sub-components." Therefore, proper characterization involves developing a sub-circuit model, which will include all of these sub-components. This requires test structures that include not only the complete ESD circuit, but access to the individual sub-components. These are then used for SPICE

model development and characterization. Model verification is accomplished by comparing measured and simulated results. Process and device simulations can be used to design the sub-components, and examine device characteristics before fabrication.

CHAPTER 2

OVERVIEW OF TOOLS AND METHODOLOGY

The research described in this thesis was carried out using many different tools including various software packages and instruments. This chapter will describe the data flow and give a general description of the methods used to do the analysis on the ESD SCR circuit and its components.

2.1 Silicon Analysis Flows

Figure 2-1 shows the general synthesis and analysis concept implemented on silicon structures as part of this research. We start with an existing layout database which has an ESD circuit of interest, which in this case is an avalanche triggered SCR. In order to implement a synthesis and analysis strategy, the circuit needs to be reduced to its basic components, which in this case consist of a N+ resistor, an NMOS transistor, a parasitic NPN transistor, and a parasitic PNP transistor. The test structures to be fabricated therefore consist of the ESD circuit itself as well as the internal components.

These types of protection circuits behave differently depending upon the spacings between different diffusion regions; as a result, the test structures are fabricated with some layout variation in order to examine the impact on ESD performance and triggering conditions. For example, the original test module contained different spacings between the N+ source diffusion and an adjacent Nwell. Some data will be presented based on

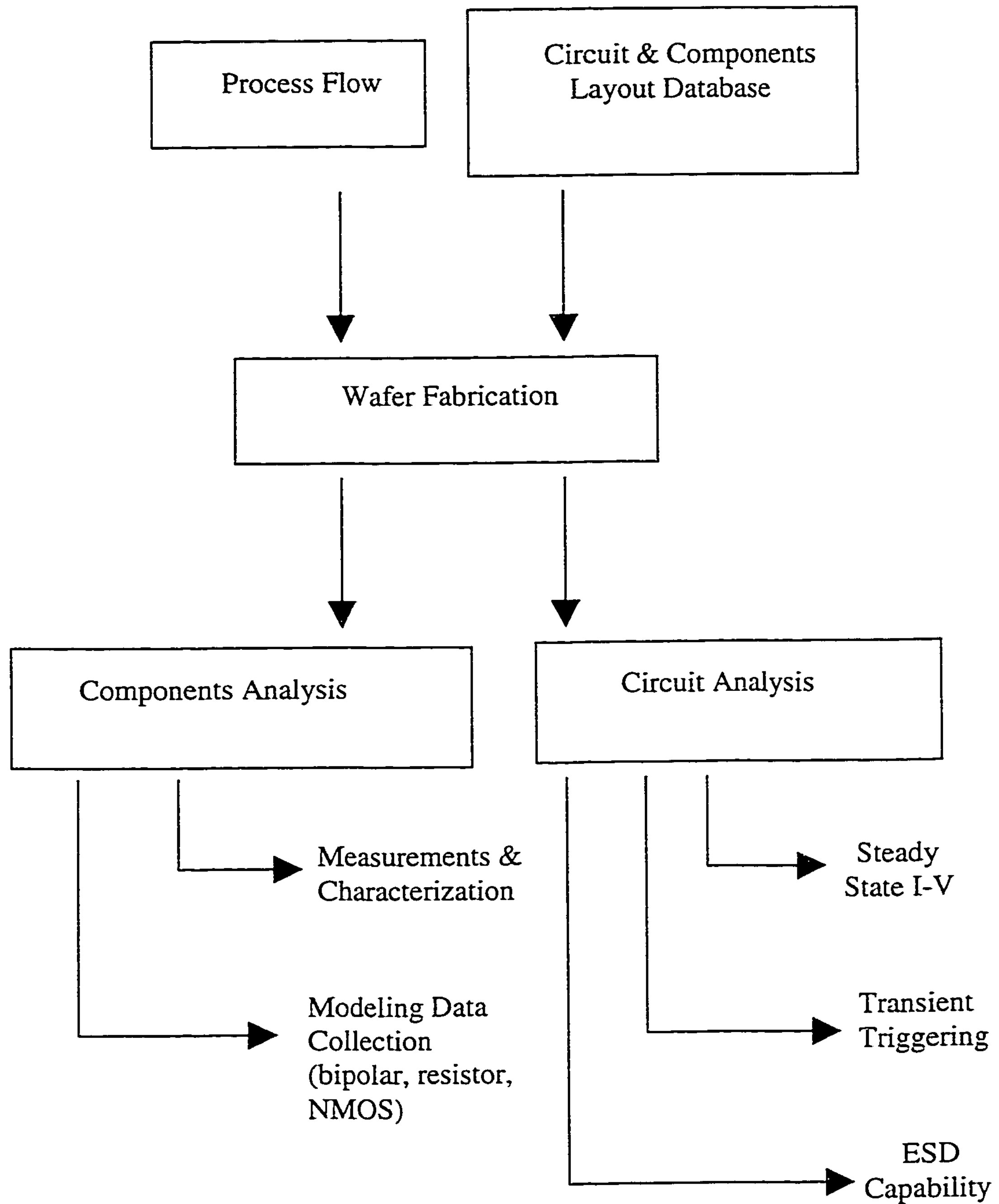


Figure 2-1. Synthesis and analysis data flow for the silicon test structures.

these original measurements. For this work, test modules were designed to study two specific values of this spacing. The NPN transistor that was affected by this variable was also fabricated and analyzed. The number of variables was minimized, since the point was to establish a correlation between silicon, TCAD, and SPICE using this approach. A reduced number of variables allow this analysis to proceed more efficiently. In addition, curve tracer analyses of structures with very wide spacings were found to have difficulty in triggering, so these wider bipolar structures were not included in the detailed analysis.

2.1.1 *Test Structure Analysis – Component Characterization & Modeling*

Once the silicon has been fabricated, analysis proceeds on the components and on the ESD circuit itself. Figure 2-2 shows the software and hardware system used for the component analysis. LabVIEW is a software package commercially available from National Instruments, which allows user programmability for measurement on standard industry equipment. The LabVIEW software allows flexibility in the data collection, since it can automatically port measured data into a database (Excel) for efficient data reduction. Network connectivity also aids in the data transport. The bipolar structures, NMOS transistor and a N+ resistor were measured with this system at Rice. The HP4145 allowed the measurement of the 3 terminal resistor I-V data, which was useful for measuring the substrate current in the breakdown region.

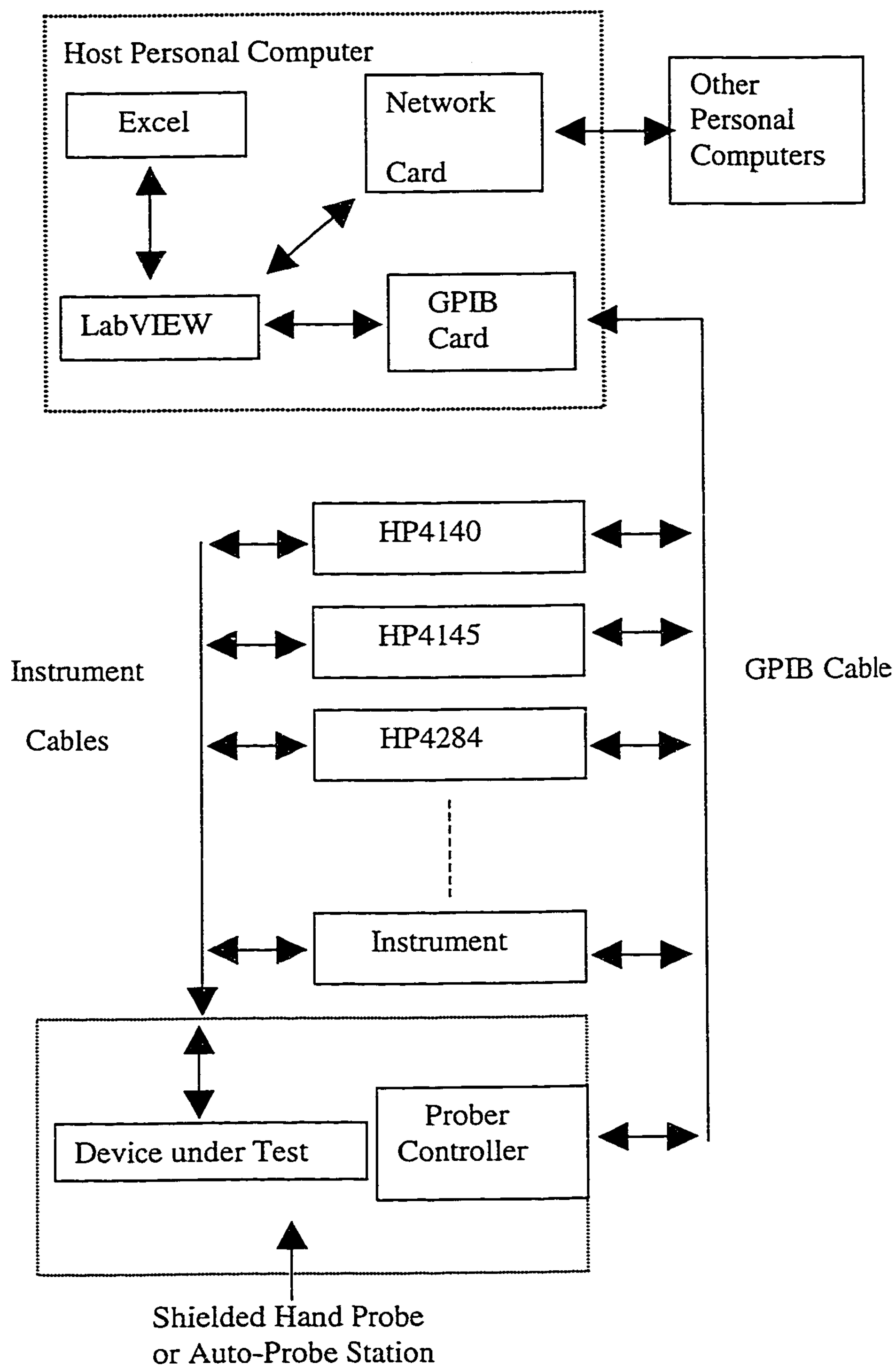


Figure 2-2. Hardware and software system for semiconductor characterization.

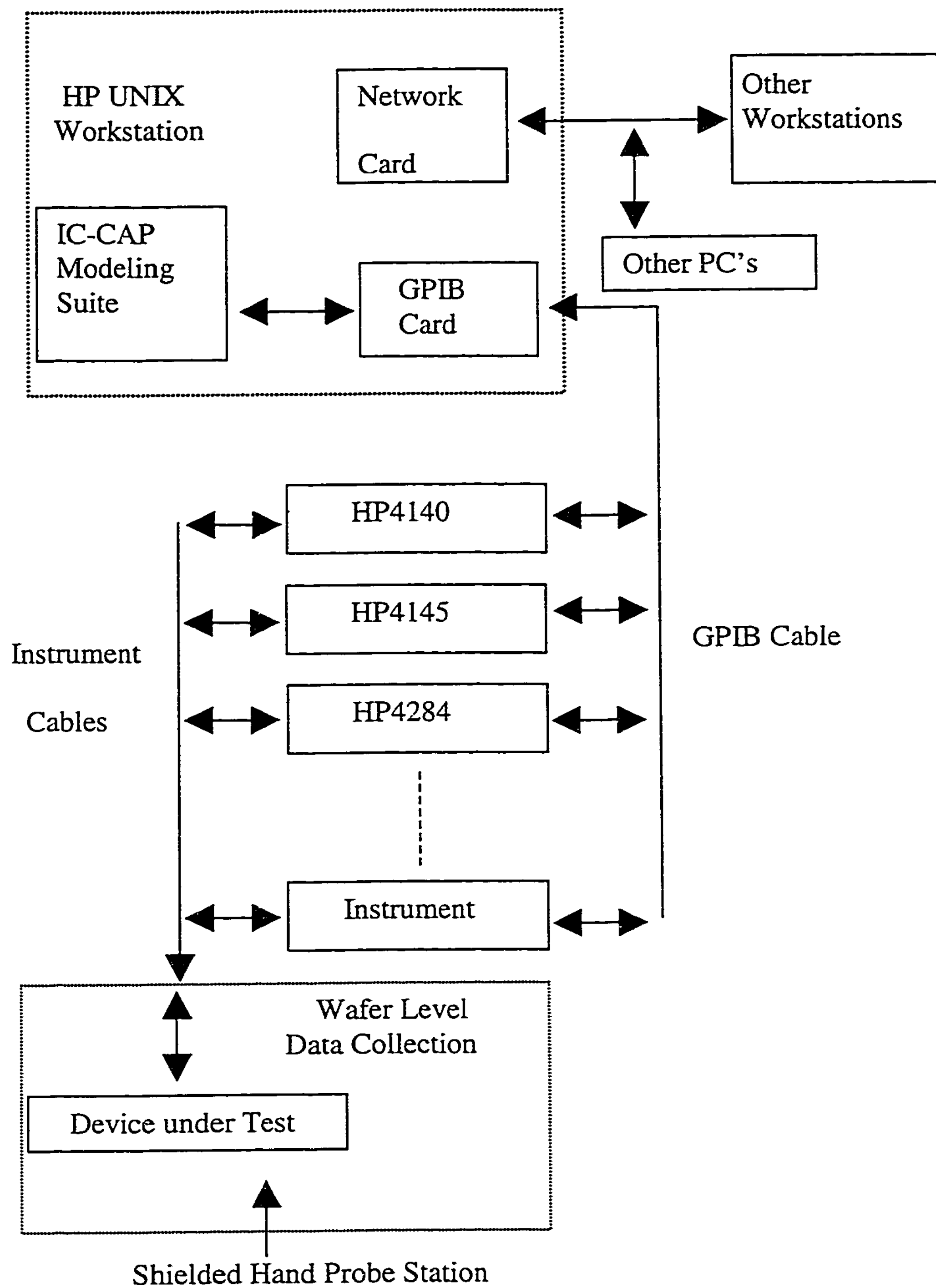


Figure 2-3. Hardware and software system for semiconductor modeling.

Figure 2-3 shows the system used for the modeling data collection. The bipolar structures were measured using the Hewlett-Packard IC-CAP software, which allows the collected data to be used for SPICE model parameter extraction and fitting. The data that was measured for the bipolar components were the forward and reverse Gummel Plot and the forward and reverse Early family of I-V. The Gummel measurement is used to measure the currents through the collector and base terminals, as the base-emitter junction is forward biased using the emitter terminal. The collector terminal is usually held at ground potential for this measurement. It is a standard measurement used for extracting basic bipolar parameters. The Early I-V data is measured by sweeping the collector terminal voltage (emitter grounded) at different base-emitter voltages or base currents. This data is useful for collector resistance extraction, as well as to extract the Early Voltage parameter. This parameter measures the impact of basewidth modulation due to an increasing reverse bias on the collector-base junction.

The IC-CAP software is also linked with the modeling suite, which includes SPICE3. The models available include the standard MOS equations, the BSIM equations, and also the industry standard Gummel-Poon bipolar model [18] [19]. The software is currently not available in a PC version, so data transfer from the Unix workstation to the PC for final summary and analysis was done via saved text files, imported into MS Excel.

The NMOS transistor is used as a bipolar device to trigger the ESD circuit. This high current I-V characteristic was measured using a TEKTRONIX 576/577 curve tracer, with a standard 177 test fixture. The N+ resistor was also measured with the curve tracer, as was the ESD SCR circuit itself.

2.1.2 *ESD Circuit Measurements*

The ESD circuit was measured using two approaches: a steady state triggering method using the curve tracer, and a transient triggering method using a fast rise time pulse excitation. The latter method will be presented later. A general schematic of the curve tracer setup is shown in Figure 2-4. A typical measurement may consist of a 25V or 75V (depending on the NPN basewidth) maximum voltage applied through a 120Ω or 500Ω series resistor. The series resistor helps to limit the maximum current through the device. This ability to "dial in" a resistor and a voltage allows a sweep to high current regions, which provides post-trigger I-V data to be sampled and recorded. This data is then useful for analyzing the SCR on-resistance as it switches from the high impedance "off state" to its low impedance "on state." In addition, the data can be quite useful for model calibration and checking. Limiting the current with the series resistor results in an intersection of the SCR response with the series load resistor, which can then be confirmed and cross-checked with SPICE. In summary, the steady state measurements, using the curve tracer, are useful for gathering on resistance data, triggering voltage and current, and also the minimum holding current just before SCR turn-off.

In addition to the critical data gathered from the curve tracer, it is important to check the transient triggering dynamics of the ESD circuits [10]. In actual operation, ESD circuits are intended to respond to a fast rise time pulse, and the time it takes to achieve triggering is an important parameter. Pulsed measurements were made on packaged SCR parts. Figure 2-5 shows a plan view of a 14 pin white ceramic package used in these

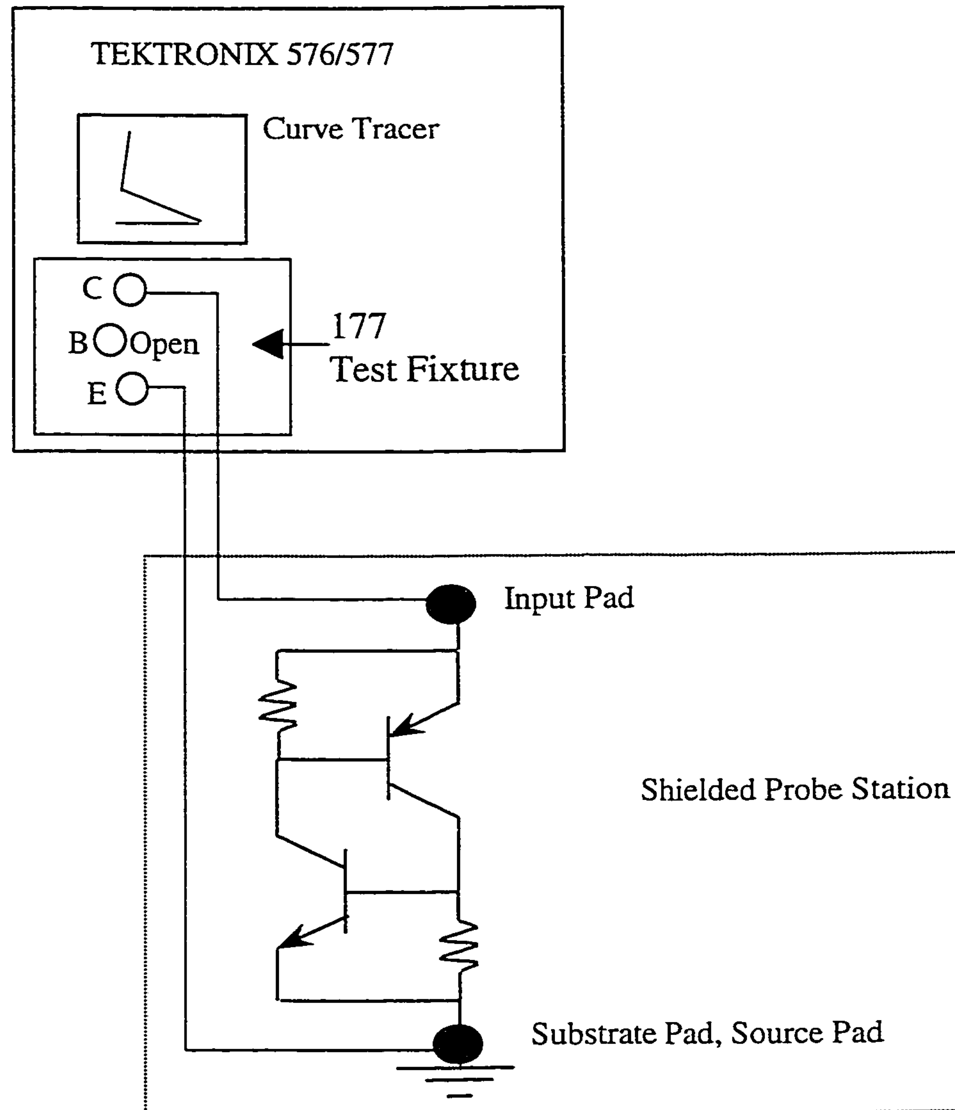


Figure 2-4. Schematic setup for the curve tracer experiments.

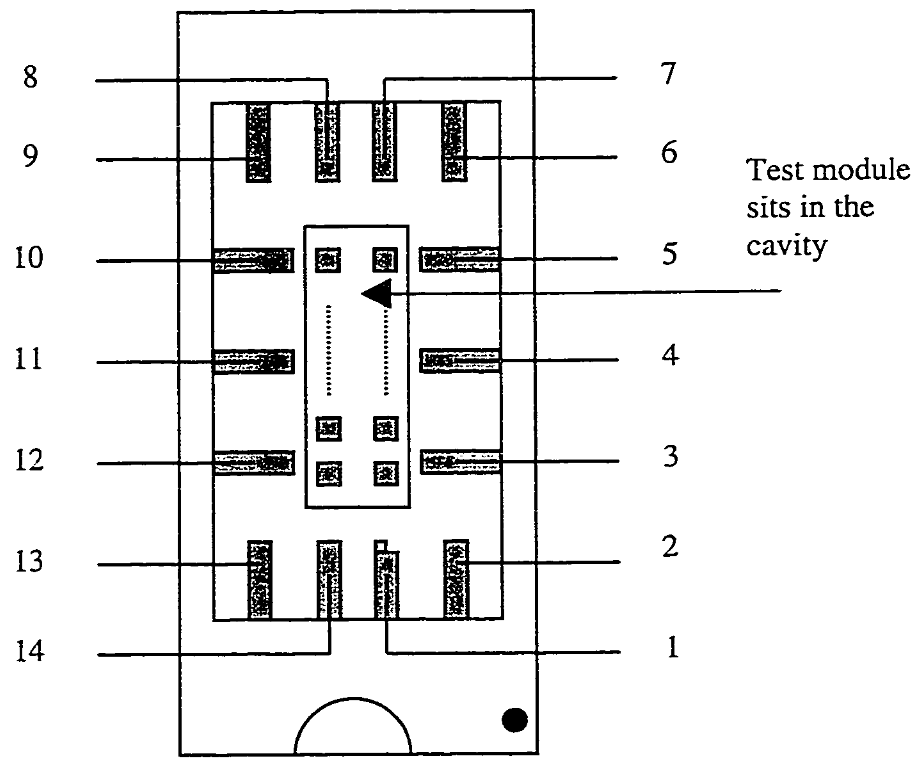


Figure 2-5. Layout of the 14 pin white ceramic package used for the pulsed, transient triggering tests.

experiments. Voltage pulses with ~15nsec rise times were applied through a load resistor to measure the transient triggering response. The schematic for this setup is shown in Figure 2-6. The measurement required a special test fixture that was designed to minimize the lead inductance and capacitance. In addition, the measurements of the input pad voltages were made using active TEKTRONIX high frequency probes. Figure 2-7 shows an example of typical transient results before and after the test procedure was improved. The data was measured using a TEKTRONIX TDS684B oscilloscope, which is a 1GHz bandwidth instrument. The oscilloscope allows saving measured data in spreadsheet format to a disk, which facilitates the data reduction and presentation. The triggering conditions could be varied using the magnitude of the input voltage pulse and/or the value of the load resistor. The active probes have a maximum voltage limitation, and this limits their use to circuits that have trigger voltages below 20V.

2.2 Process and Device Simulation Flow and Analysis

Figure 2-8 shows the flow used in the TCAD simulation environment. The layout information was transferred to the process simulator via mask files, which were then called by the process simulation deck. The key point here is that 2-dimensional structures were developed which accurately resembled the actual structures fabricated on silicon. The sub-components could be analyzed as well as the complete ESD circuit. The circuit used in this study actually has an important 3-dimensional dependency due to the layout of the N+ diffused resistor. This dependency was analyzed using the silicon test structures. A small resistor section was added in the simulation to

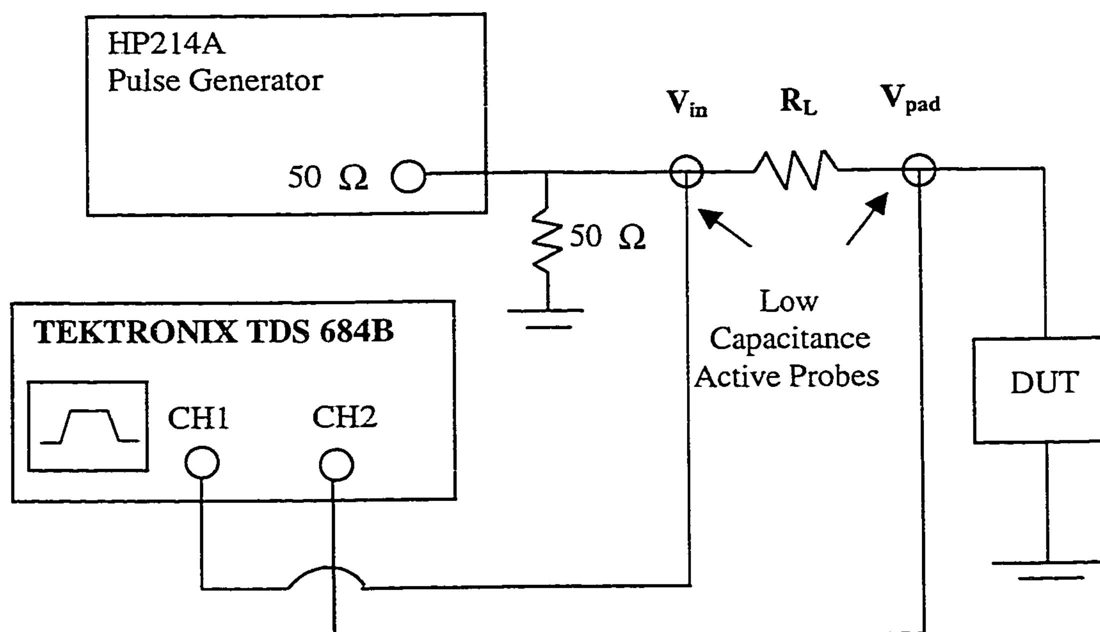
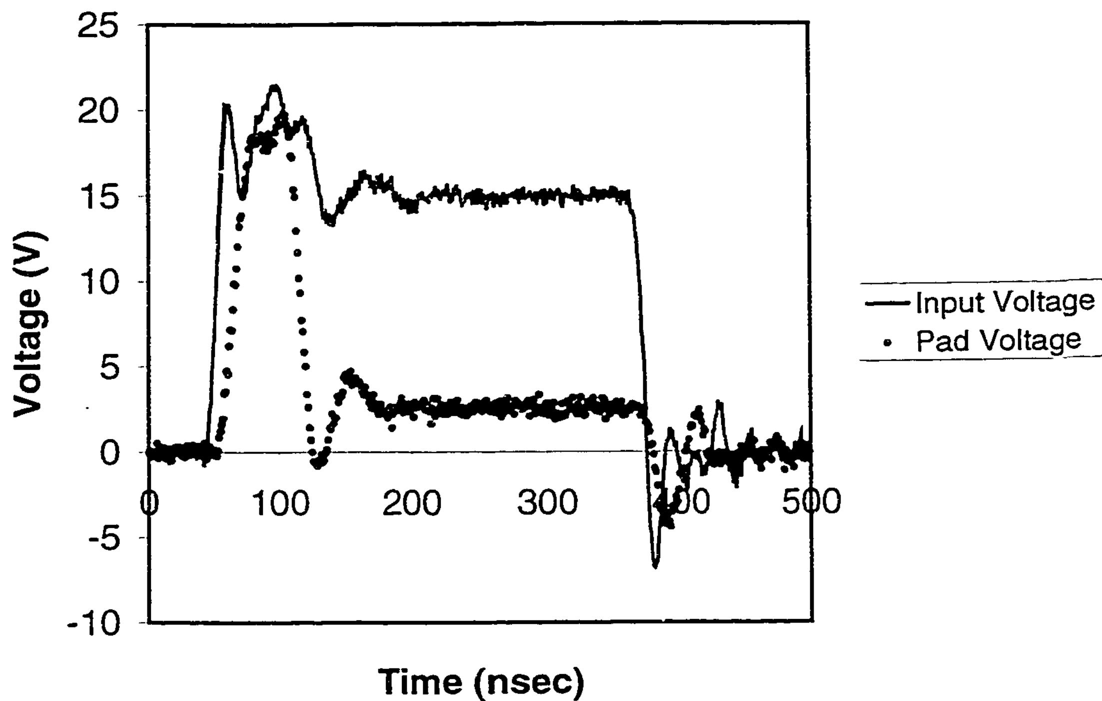


Figure 2-6. Schematic setup for the transient pulse triggering experiments.



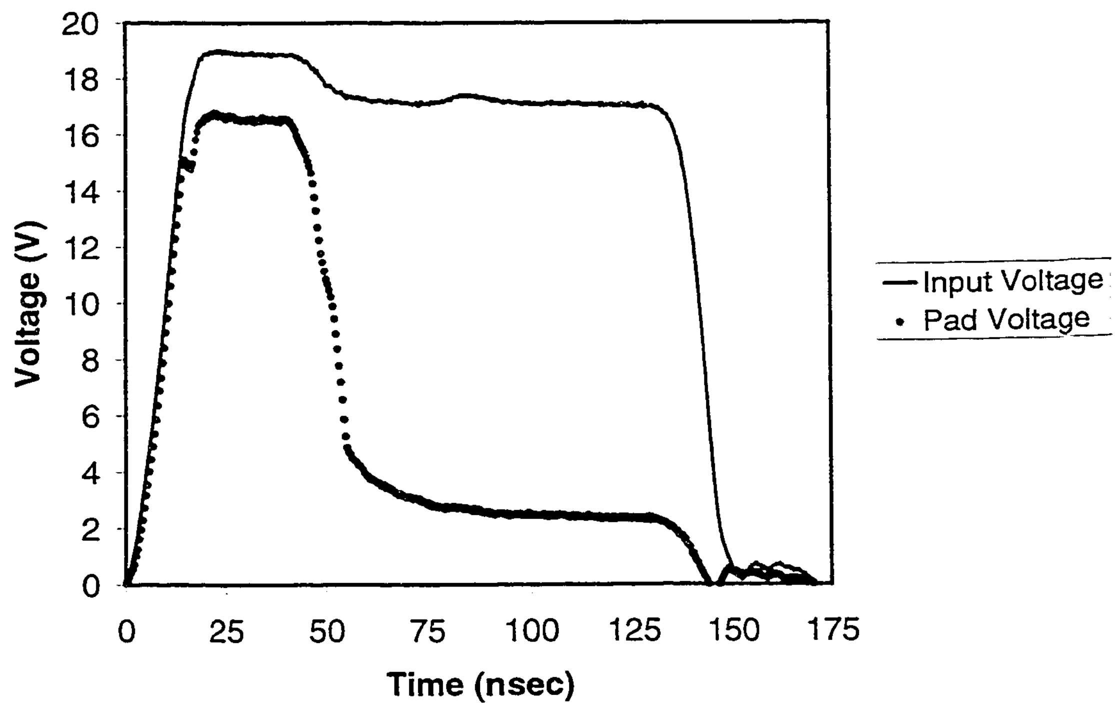


Figure 2-7. Original transient test results (top) Vs the improved data achieved using a special fixture that minimizes the lead inductance and capacitance. The coaxial cabling was eliminated, and high frequency probes were used for the measurements.

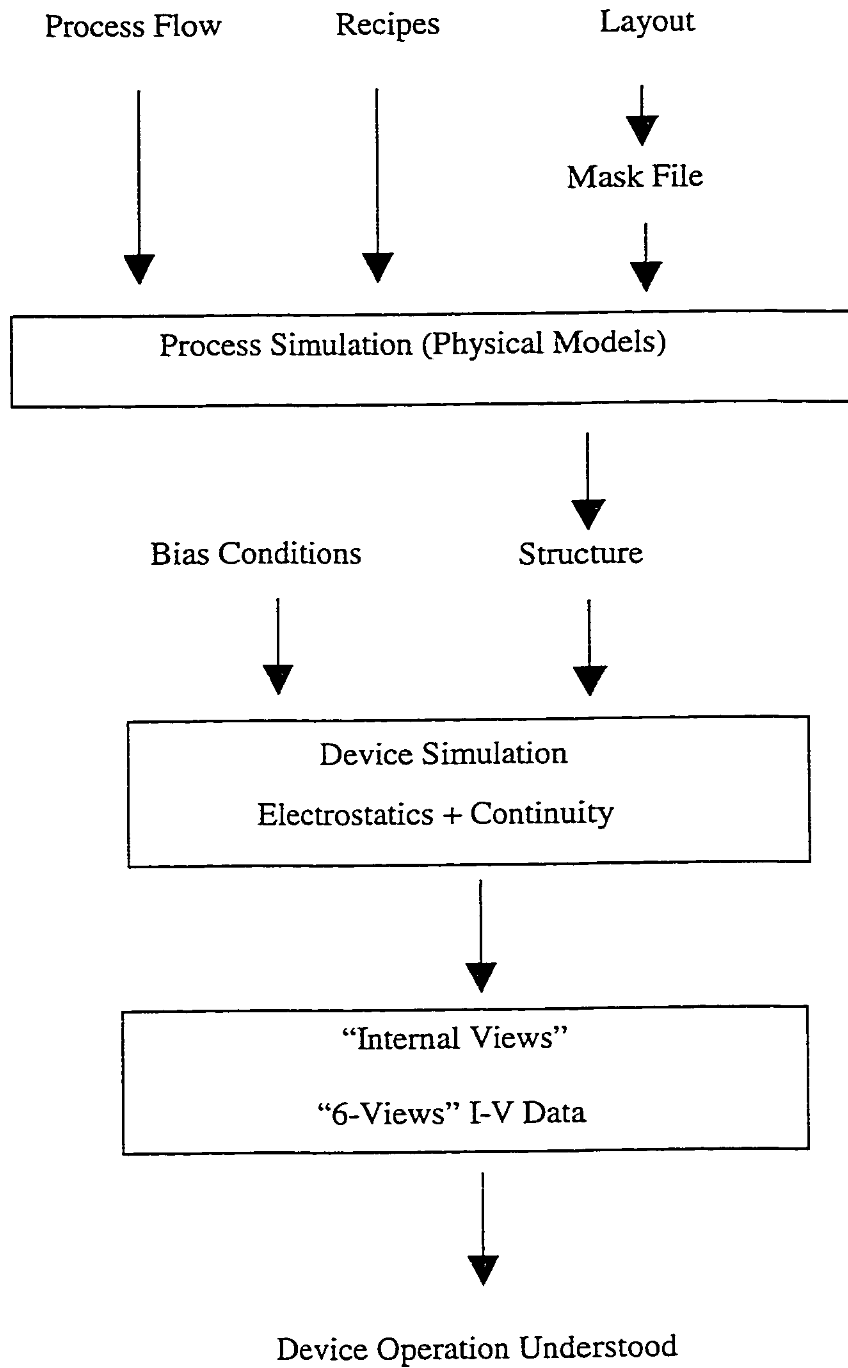


Figure 2-8. TCAD simulation flow with the input and output data.

help mimic the actual structure. A more accurate simulation would require a true 3-dimensional simulator. However, this 3-d requirement is only important in modeling the breakdown behavior of the resistor, which only occurs under rather special conditions. Despite this limitation, the quantitative aspects of the bipolar and MOS structures were in agreement with the measurements. The simulated ESD circuits behaved very similar to the measurements on the silicon structures. The lack of 3-dimensional simulation results was not a barrier to completing this study, since the final results include the consolidation of TCAD simulation results with the silicon measurements and analysis.

Once the structures were created in the process simulator, they were then transferred to the MEDICI device simulator. The simulator solved the continuity equations as well as Poisson's equation for electrostatic potentials, self-consistently. For the ESD circuit, the device simulator was used to raise the pad voltage, which allowed the device to enter avalanche breakdown and show the "snap-back" and latchup effects. This was done using a mathematical method, called the continuation method, which allowed the tracing of complex I-V curves in the simulation. This simulation resembled a steady state measurement, with the difference being that the curve tracer applied pulses that have a "turn-off" slope, whereas in the simulator we were only simulating the "turn-on" portion, by raising the voltage from 0V to some maximum value.

One of the most valuable points of the device simulator is the fact that solution files could be saved at key points along the I-V trace, which then allowed the investigation of physical properties and conditions at these points of interest on the I-V curve. This is what is meant by the "internal views." Whereas the simulated I-V data

showed a response similar to what is measured on the silicon, the internal views actually demonstrated the dynamics that were taking place inside the structure. One of the main ideas of the thesis is that the sub-circuit model presented for the avalanche triggered SCR could not have been assembled accurately without these internal views. The internal views explicitly indicated the physical phenomena in the structure as the device went from the "off" condition to the "on" condition. Particularly important was the sequence of the component participation in the dynamics. Understanding this allowed the development of an accurate sub-circuit model for SPICE.

In addition to the I-V characteristics for the circuit, the device simulator was also used to measure the individual components. The simulated data for the bipolar structures was used for comparing against measured SPICE parameters, providing a further validation of the concepts explored in this thesis. Basic I-V data, for example, the Early curves, the Gummel plot, in both forward and reverse mode, are what is meant by the "6-Views" of a transistor. These are terminal current-voltage characteristics from which basic parameters can then be extracted.

2.3 SPICE Modeling Flow and Validation

Figure 2-9 shows the flow that was used for consolidating the component SPICE models extracted from the silicon test structures, the component characterization data, and the TCAD simulation results. In this instance, all of the three approaches were necessary in order to comprehend the behavior and terminal I-V characteristics of the SCR. The TCAD results were particularly critical, since they demonstrated the physical

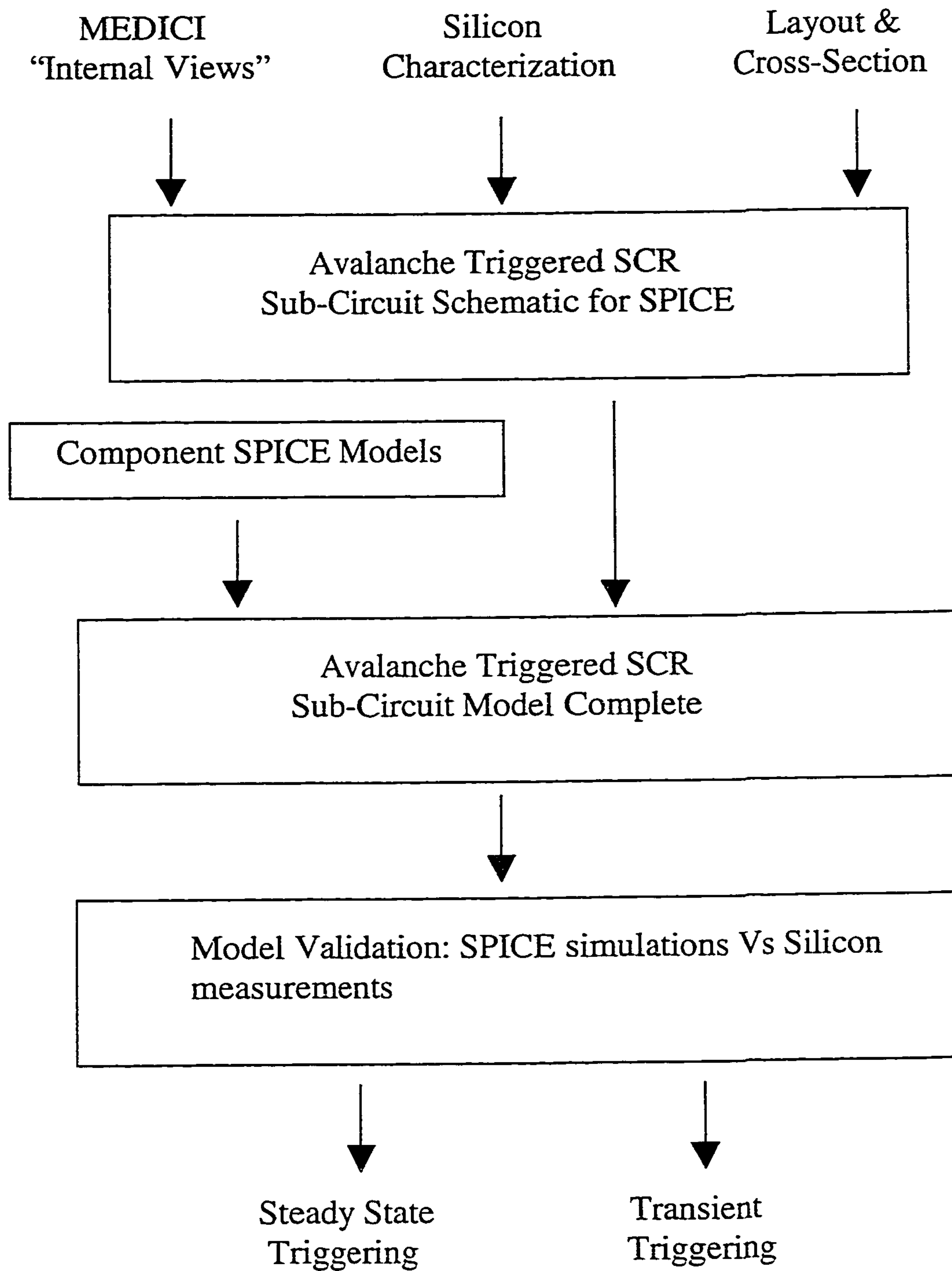


Figure 2-9. Inputs required for creating a valid SPICE sub-circuit model and method of validation using simulation results comparison against the silicon data.

operation of the circuit explicitly. The TCAD data, detailed measurements, and layout parameters allowed a physically valid sub-circuit model to be established. A valid model schematic including the models fitted and extracted using IC-CAP, allowed the SPICE simulations to be compared against the circuit measurements. The curve tracer data and the transient triggering results were used for checking the model and any final calibration. This model validation included not only the steady state and transient triggering dynamics, but the high current operation as well, which gave the on-resistance characteristics of the circuit.

Figure 2-10 shows a generic flow of the overall picture of the synthesis and analysis process implemented in this thesis, including the final expectation for the SPICE model, which is its use in a chip level examination of the circuit response to an ESD event. At the chip level, designers are able to include the routing and parasitic parameters that play an important role in the overall ESD circuit behavior. In many ways, this last flow chart represents the philosophy and the ideas presented in this thesis.

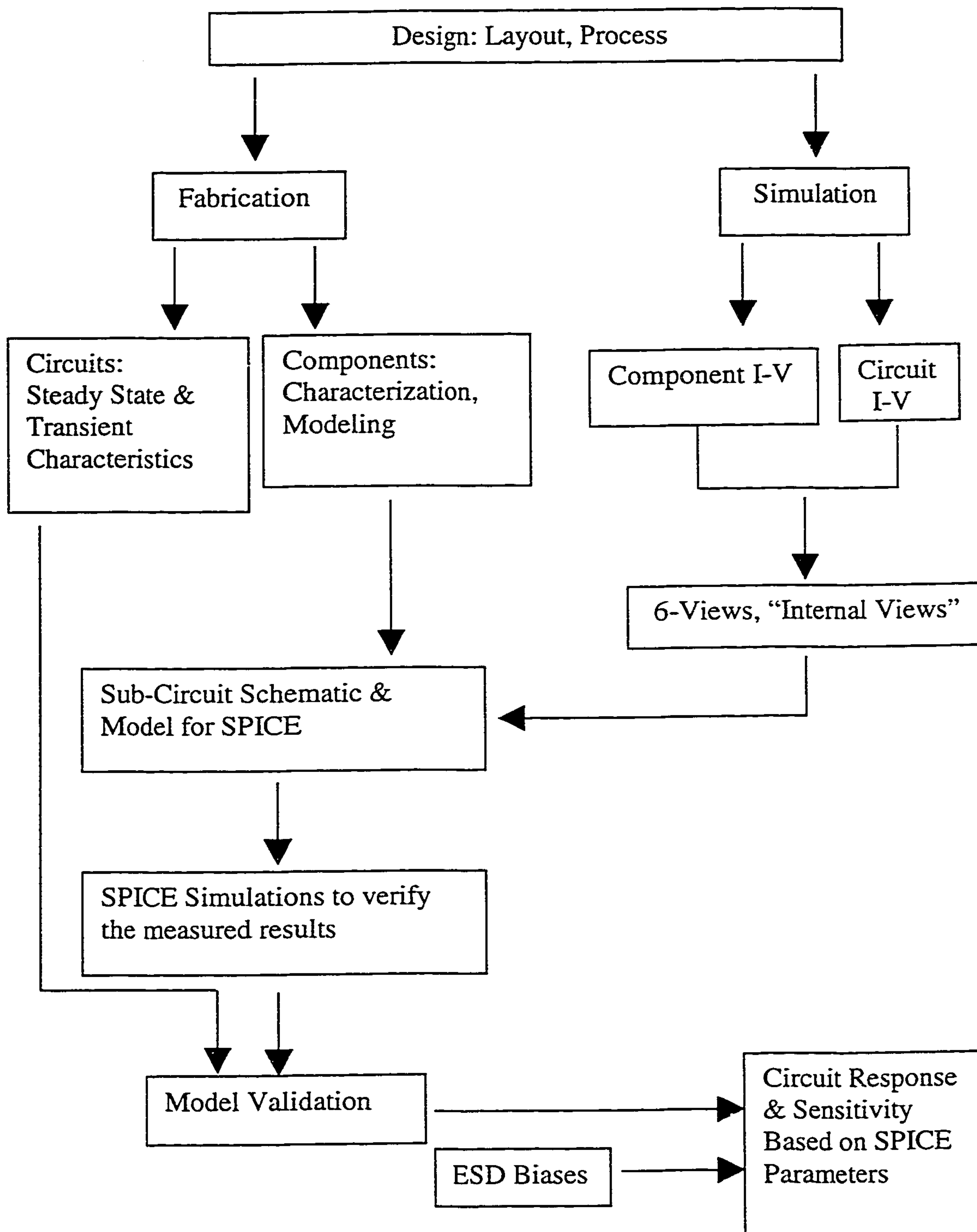


Figure 2-10. Synthesis and analysis flow for an ESD sub-circuit SPICE model. Chip level analysis and sensitivity follows the model validation.

CHAPTER 3

DESCRIPTION AND OPERATION OF THE AVALANCHE TRIGGERED SCR

This chapter will present a general description of the avalanche triggered SCR studied in this research. Layout, cross-section, and simple schematic views will be presented, followed by a brief description of how the SCR operates. Figures will be shown in cross-section format, including relevant schematic components, to show the basic features of operation. A more comprehensive and detailed analysis will be presented in later chapters. The purpose of this chapter is to introduce to the reader the structure and basic features of the SCR.

3.1 **Layout View**

Figure 3-1 shows the layout view of the avalanche triggered SCR used in this study. The input pad is connected to P+ and N+ diffusions inside a Nwell, as well as to one end of an N+ diffused resistor. The ends of the N+ diffused resistor are placed inside Nwell regions to provide protection against avalanche current damage due to high voltage transients. The Nwell diffusions raise the breakdown voltage of the resistor at these points, effectively preventing an avalanche condition. Under specific circumstances, resistor avalanche still can occur; those instances will be described in later chapters. The N+ drain of a grounded gate NMOS transistor is connected to the other end of the N+ resistor. This connection point also leads to the internal chip circuitry in the actual product design. The NMOS device protects the internal circuitry by clamping the

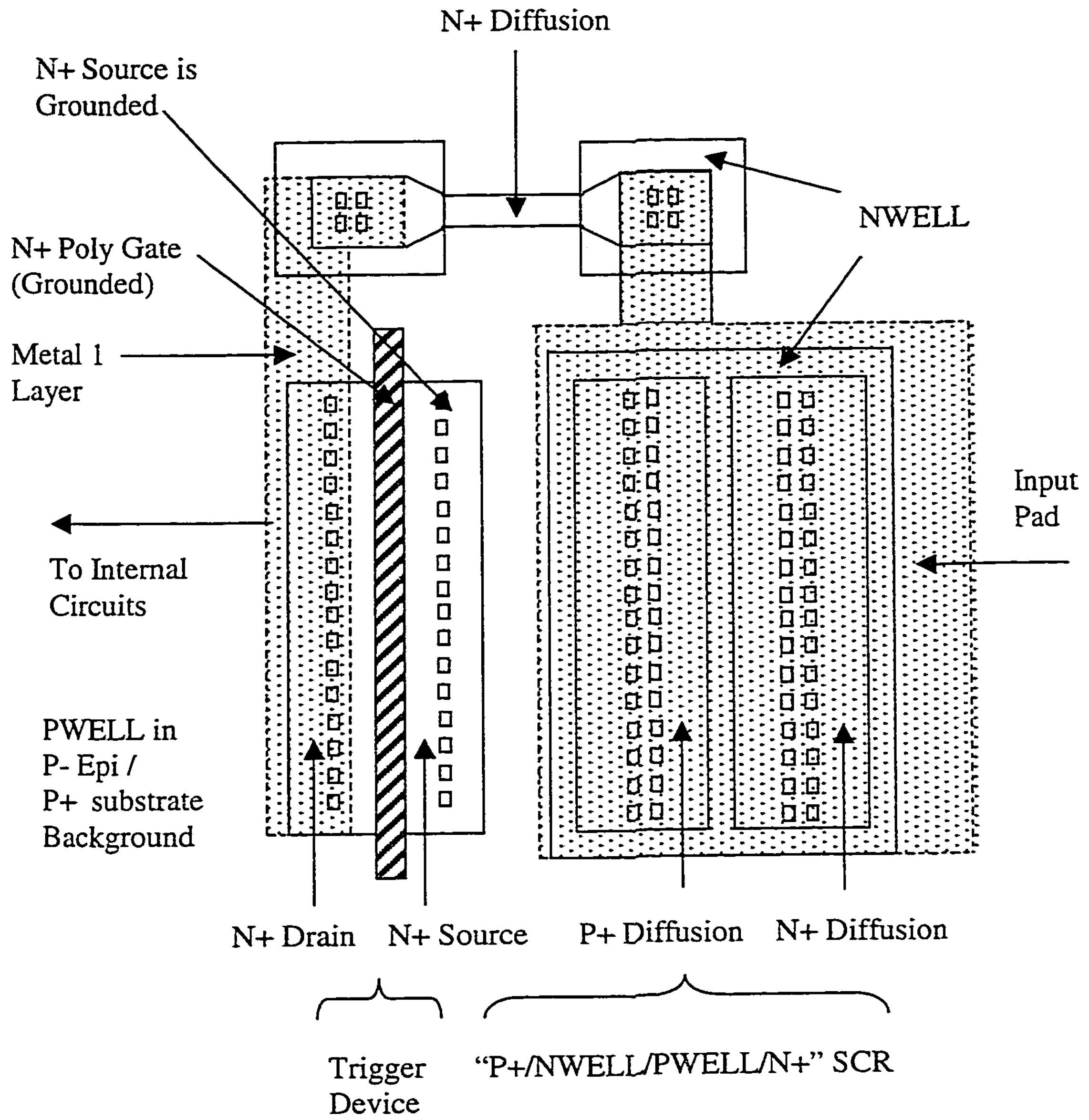


Figure 3-1. Layout view of the "avalanche triggered" SCR.

voltage to the drain breakdown level. Secondly, and just as importantly, the NMOS device acts as a trigger for the SCR. This operation will be described in the following pages. The SCR itself, once triggered, consists of the N+ NMOS source, the Pwell background doping, the Nwell doping and the P+ diffusion inside of the Nwell. This structure is created from the same steps used to fabricate a typical CMOS wafer with a P- epi on a P+ substrate. No additional process steps are required for the SCR.

3.2 Cross Section View

The cross section of the AT-SCR circuit is shown in Figure 3-2. The N+ resistor allows the internal voltage to be clamped to the drain junction breakdown level of 15V, which is sufficient to protect the gate oxide, even though the input pad voltage may continue to rise during an ESD event. The NMOS device acts as a parasitic bipolar transistor during avalanche breakdown and SCR operation. The other important parts of the structure are the lateral NPN and the PNP transistors, which form the part of the circuit that goes into latchup. Once the SCR triggers, the drain voltage drops to near 0V, reducing the stress on the NMOS trigger device.

3.3 SCR Operation

Figures 3-3 through 3-8 will be used to illustrate the generic operation of this device. As the concepts are described, components inside the structure will be added to illustrate their relative importance to the device operation. Figure 3-3 shows the pad at a low positive voltage level relative to the substrate, and the only current that flows is the

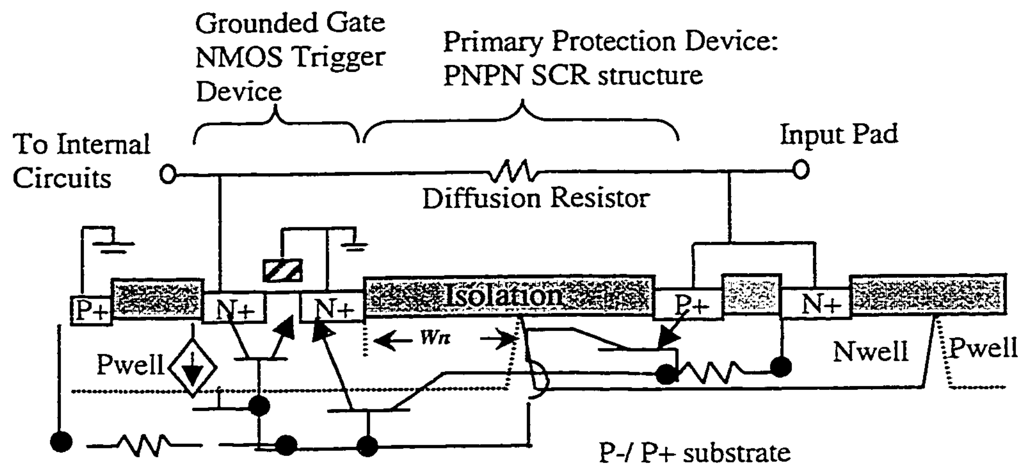


Figure 3-2. Cross-section view of the avalanche triggered SCR used in this study.

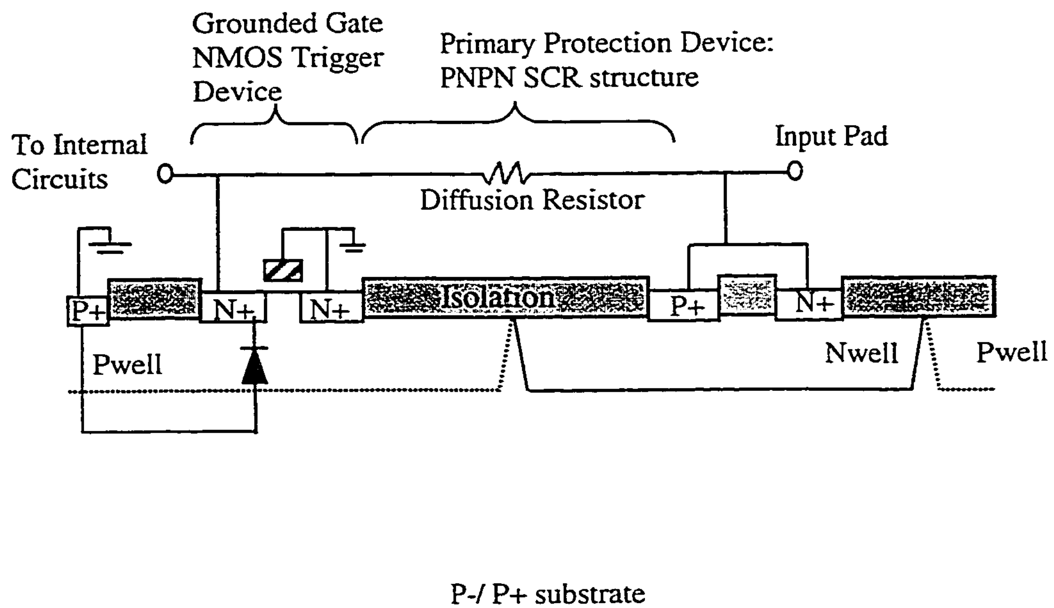


Figure 3-3. With a low voltage applied to the substrate, the NMOS drain acts as a reverse biased diode, and the only current that flows is the reverse saturation current.

reverse biased N+ drain/Pwell diode saturation current. In Figure 3-4, the pad voltage level is much higher, and the NMOS drain is in avalanche breakdown mode. As mentioned earlier, this protects the internal circuits by clamping the voltage to the junction breakdown value. The avalanche process creates electron-hole pairs at the N+ drain/Pwell junction. The excess holes are subsequently injected into the P-epi/P+ substrate region, which is at ground potential, and the excess electrons are swept into the drain by the electric field across the avalanching junction.

As shown in Figure 3-5, the hole current flowing through the finite resistance between the Pwell and the P substrate contact causes the surface potential near the NMOS channel region to rise. This potential increase creates a forward biased diode junction at the Pwell/N+ source junction. Once this happens, the MOS N+ source diffusion behaves as an electron emitter. This behavior leads to a bipolar transistor effect in the MOS device since some of these emitted electrons will drift into the drain junction, which now behaves as a NPN collector. This bipolar effect causes a "snapback" in the drain voltage, which is a condition where the drain voltage drops to a level below the avalanche limit, but the current still continues to rise sharply due to the bipolar action of the parasitic device. This "holding voltage" on the drain remains approximately constant until the SCR triggers.

As the pad voltage continues to rise, several effects can be observed, shown in Figure 3-6. First of all, the MOS drain junction potential is holding constant at its snapback voltage. Since the pad voltage is still rising, a voltage drop is appearing across the N+ diffusion resistor. Thus, the pad voltage increases and the resistor sustains the

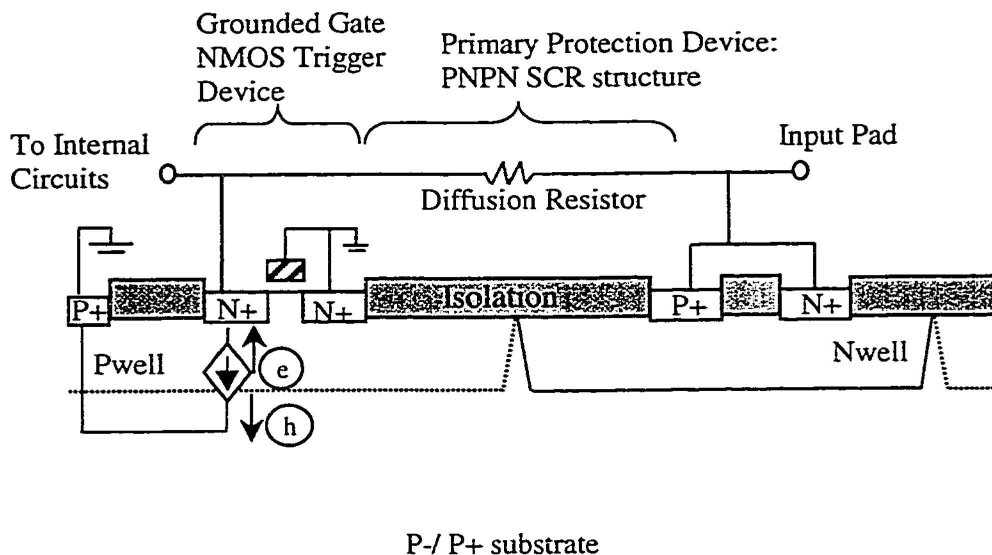


Figure 3-4. At a high enough drain voltage, the NMOS drain junction enters avalanche breakdown, creating electron-hole pairs. The junction behaves as a voltage dependent current source. Electrons are swept into the N+ drain; holes are injected into the substrate.

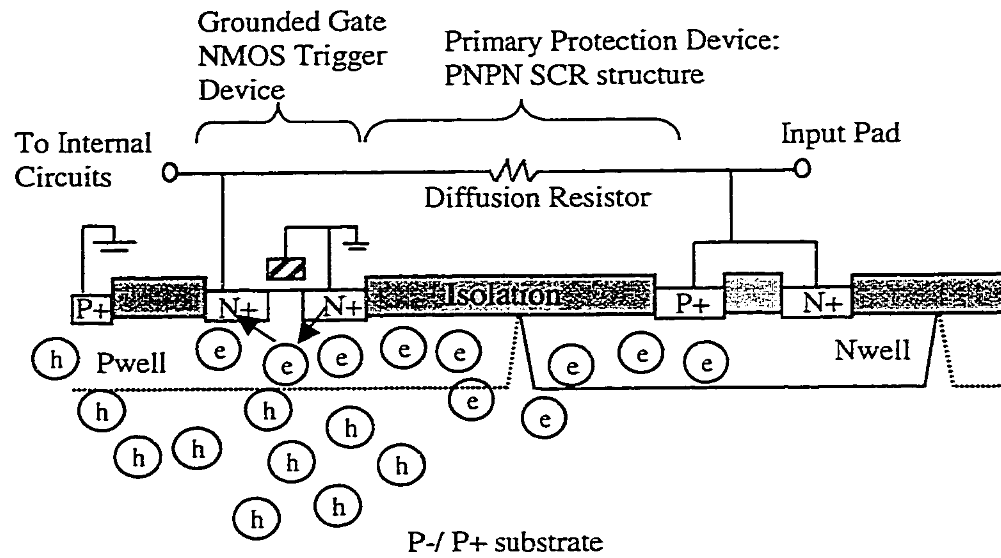


Figure 3-5. The finite resistance of the Pwell creates a potential drop, which increases the potential near the surface, allowing the N+ source junction to become an electron emitter. The reverse-biased drain junction collects some of these electrons, forming a parasitic NPN transistor (shown by the arrows). Other electrons drift through the Pwell towards the Nwell, which is also reverse biased.

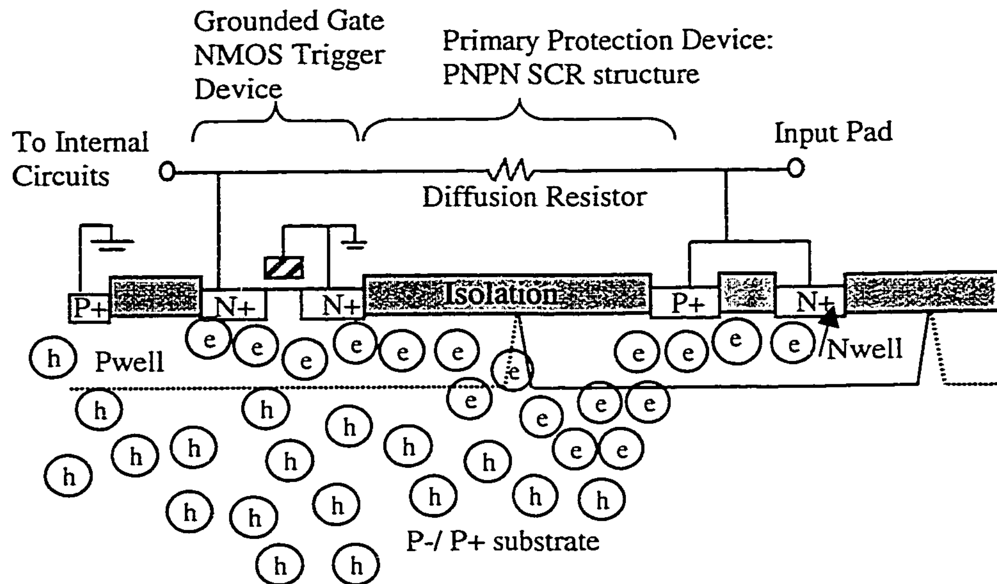


Figure 3-6. The NMOS parasitic NPN and a lateral NPN formed by the N+ source emitter, Pwell drift region as the base, and Nwell as the collector are fully conducting. The electron current in the Nwell is creating a potential drop near the P+ junction.

difference in potential between the pad voltage and the NMOS snapback voltage. Secondly, the depletion region width around the Nwell/Pwell junction increases, and this also starts to behave like a NPN collector for some of the electrons emitted by the N+ source. At this point, there are now two NPN transistors in operation: the parasitic NMOS NPN, and the lateral NPN. In addition, the N+ diffusion resistor is conducting due to the difference in potential across its two terminals.

Figure 3-7 shows what happens when the pad voltage reaches a very high level. To begin with, the NMOS drain is still in avalanche bipolar mode. This means the N+ electron emitter is still injecting electron current, and the resulting increase (due to its bipolar gain) in lateral NPN collector current creates a potential drop inside the Nwell/P+ junction due to its finite resistance. Once this junction becomes forward biased, the P+ diffusion becomes a hole emitter, and a PNP transistor consisting of the P+ emitter - Nwell base - Psubstrate is turned on.

These two parasitic bipolar transistors lead to regenerative feedback, and the classic latchup condition takes place. Figure 3-8 shows the lateral NPN and PNP transistors fully turned on and operating in the saturation mode. The Pwell/Nwell diode is forward biased and the surface under the field isolation is conductivity modulated, meaning the resistance is very low due to the large number of carriers present there. At this point, the SCR has triggered; all of the junctions are forward biased, and the voltage at the pad drops to a low level, which depends on the external load conditions.

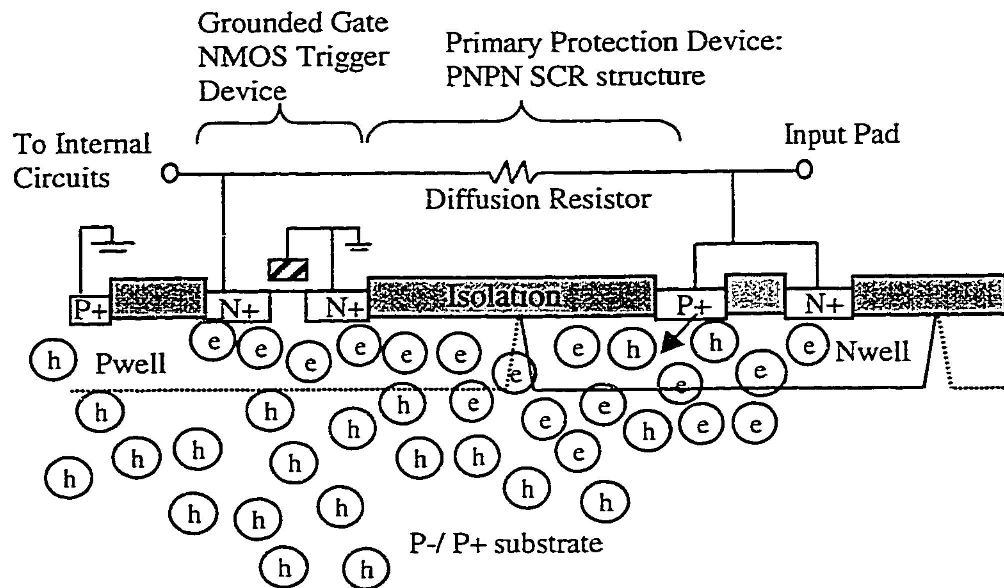


Figure 3-7. The P+ / Nwell junction is forward biased, triggering a PNP bipolar effect with the P substrate as the collector and Nwell as the base. The arrow shows the P+ diffusion emitter, injecting holes into the Nwell.

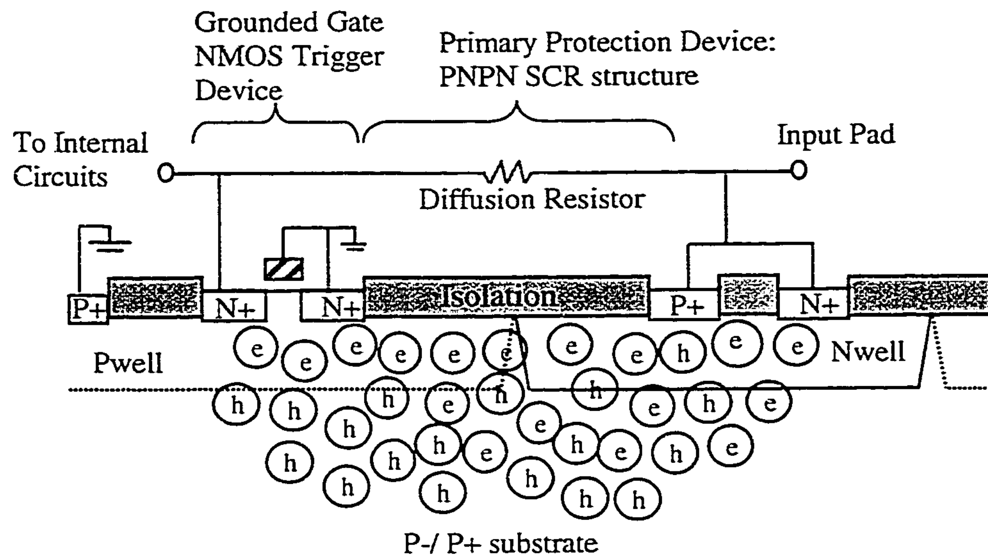


Figure 3-8. Most of the current now flows between the N+ source and P+ diffusions. The region under the isolation oxide forms a very low resistance path for current flow since all of the junctions are forward biased. This is the latchup condition. The MOS device is no longer in avalanche breakdown mode, but continues to conduct as an NPN transistor.

To review briefly, the SCR triggering and latchup dynamics follows the following sequence: At low voltages, the N+ drain and Pwell junction behaves as a reverse biased diode. As the voltage gets higher, the NMOS drain reaches the avalanche breakdown condition. The NMOS device goes into a bipolar mode, and the drain voltage is clamped at a "snapback" voltage. The N+ resistor has to sustain the difference in potential between the increasing pad voltage and the MOS snapback voltage, which may be thought of as a holding voltage. As the pad voltage increases, the lateral NPN starts to turn on. This lateral NPN current increases to a point where the P+/Nwell junction becomes forward biased, turning on the PNP transistor and leading to the latchup condition. At latchup, the MOS device is no longer in avalanche breakdown, but continues to conduct current as a bipolar transistor.

CHAPTER 4

COMPONENTS IN THE AVALANCHE TRIGGERED SCR

As described in the previous chapter, there are four basic components in the avalanche triggered SCR. These are listed below for convenience:

- N+ diffusion resistor,
- NMOS in bipolar mode,
- NPN transistor,
- PNP transistor.

This chapter will present the analysis of each of the SCR components, including layout view and structure description; TCAD simulations and measurements; SPICE model representation and SPICE results. The data was collected on silicon test structures specifically designed to analyze the SCR sub-components in detail. To do this, the SCR structures were designed and fabricated on a specific test module, and the same module contained replicas of the SCR, but with the sub-component connections separated out in order to measure those independently. This allowed the measurement of the SCR characteristics as well as the characterization of the independent pieces from the same wafer and die. This analysis was one of the keys in developing a SPICE model that accurately models the physics and dynamics of the SCR operation.

4.1 N+ Diffusion Resistor

4.1.1 *Layout and simulated cross-sections*

Figure 4-1 shows the layout view of the N+ diffusion resistor used in this SCR. The background doping is Pwell in P- epi over a P+ substrate. The ends of the resistor are in Nwell over P- epi and P+ substrate. The layout view shows that the N+ diffusion resistor is a three terminal component. A model for this resistor is not as straightforward as one might imagine when thinking of a resistor in the classical "two–terminal" sense. To understand this clearly, 2-D TCAD simulated cross-sections are shown in Figure 4-2, referring to the cut-lines in Figure 4-1. Along section A-A', the cross-section shows the Nwell profile at the ends, with a planar junction diode in the center region. Section B-B', on the other hand, shows that the edges of the N+ diffusion and isolation oxide expose a cylindrical junction, and the center region again shows a planar junction diode. An accurate TCAD simulation of this resistor will require all 3 dimensions to be included. This will be discussed further in the later section.

4.1.2 *Measurements, Simulations, and Literature Review*

Semiconductor diffused resistors show terminal I-V characteristics that are different from resistors in the classical sense. Figure 4-3 shows a plot of a SPICE simulation result of a two terminal, constant-valued (200Ω) resistor with a DC sweep from −10V to +10V. The resulting I-V curve demonstrates the classical linear response one would expect according to Ohm's Law. In contrast, Figure 4-4 shows the measured I-

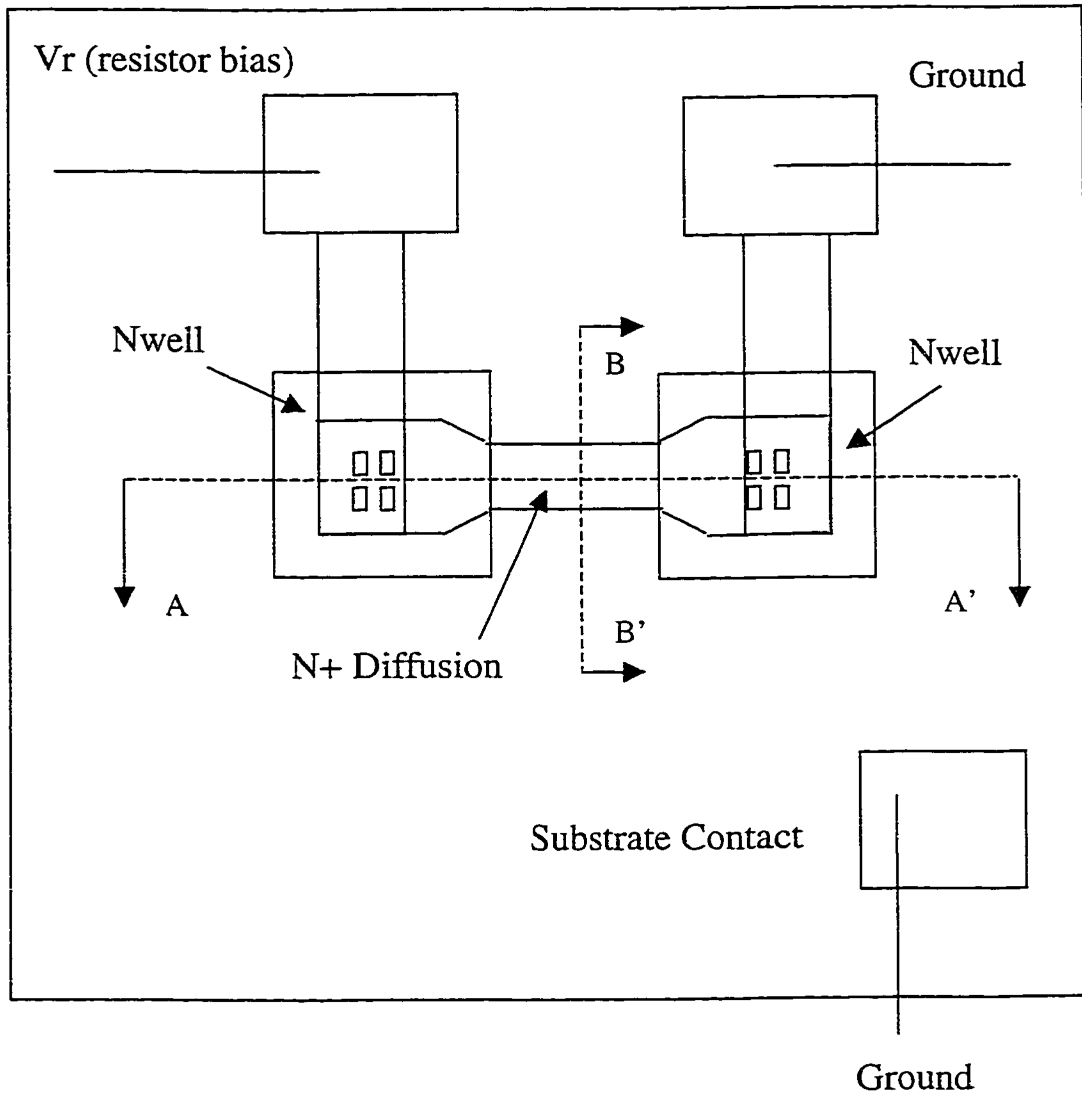


Figure 4-1. Layout view and biasing terminals of the N+ diffusion resistor.

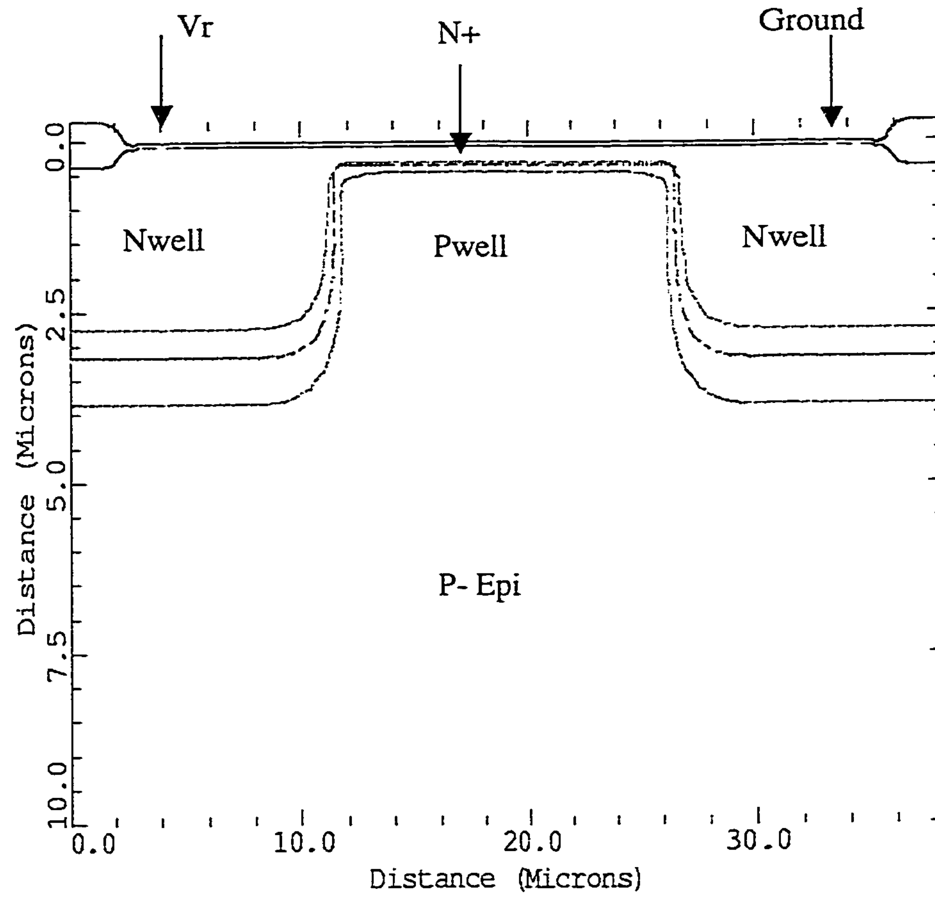


Figure 4-2A. N+ diffusion resistor simulated cross section along the A-A' direction.

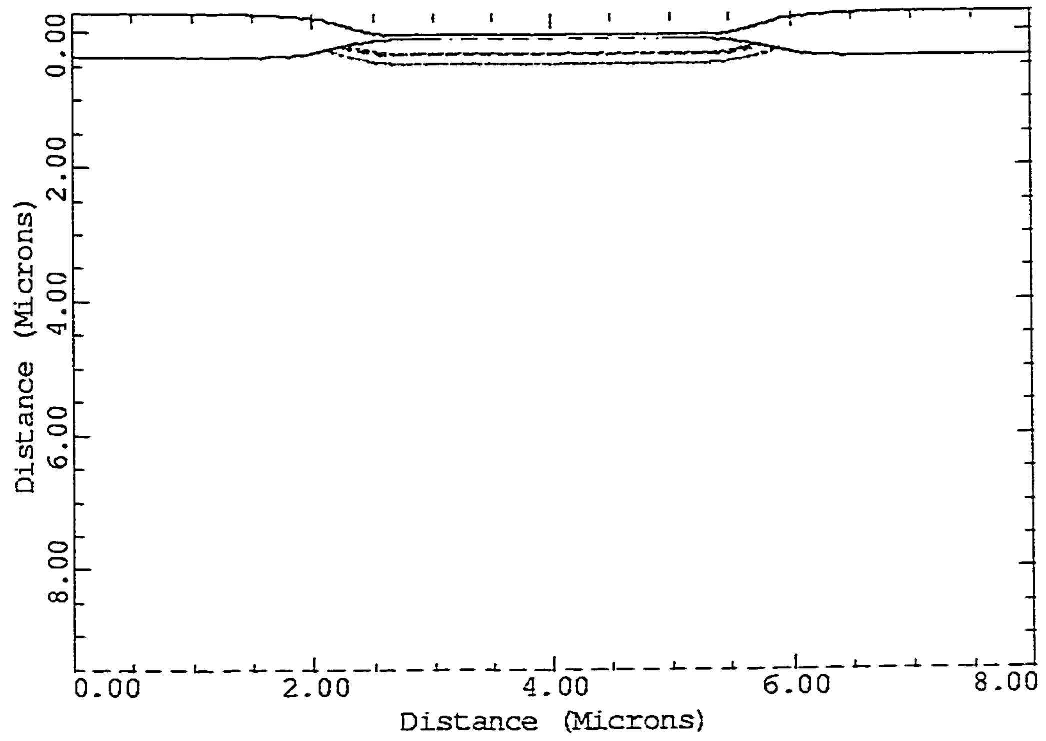


Figure 4-2B. N+ resistor cross-section along the B-B' cutline.

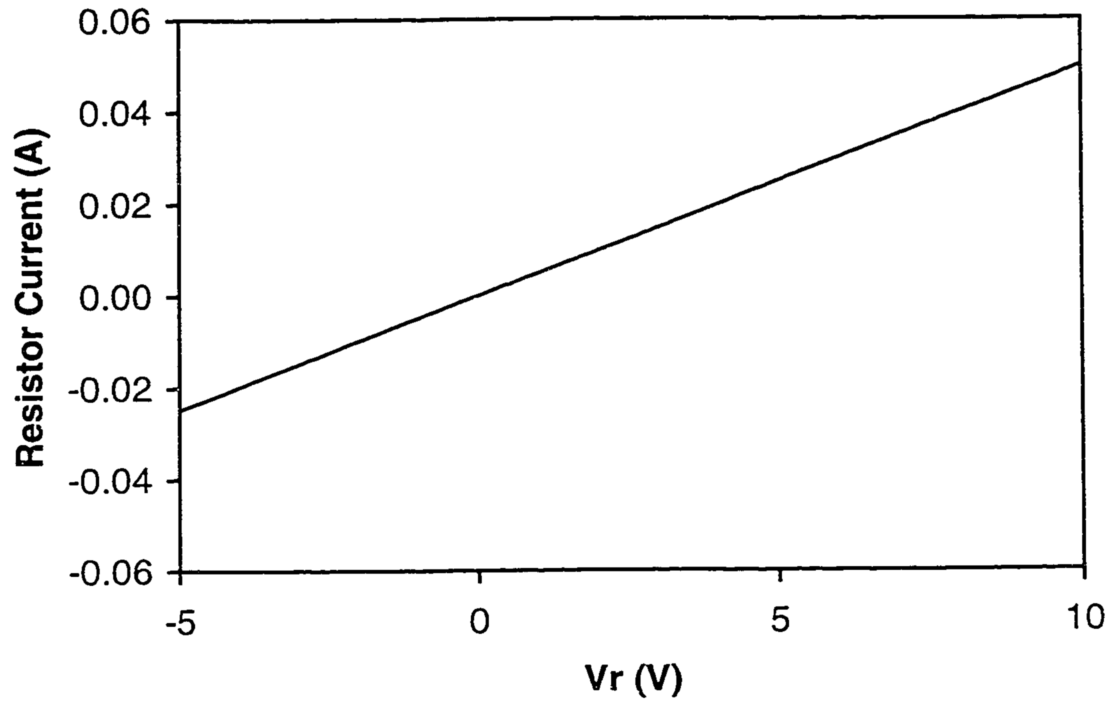


Figure 4-3. A DC sweep from –10V to +10V in SPICE applied to a 200Ω constant valued resistor.

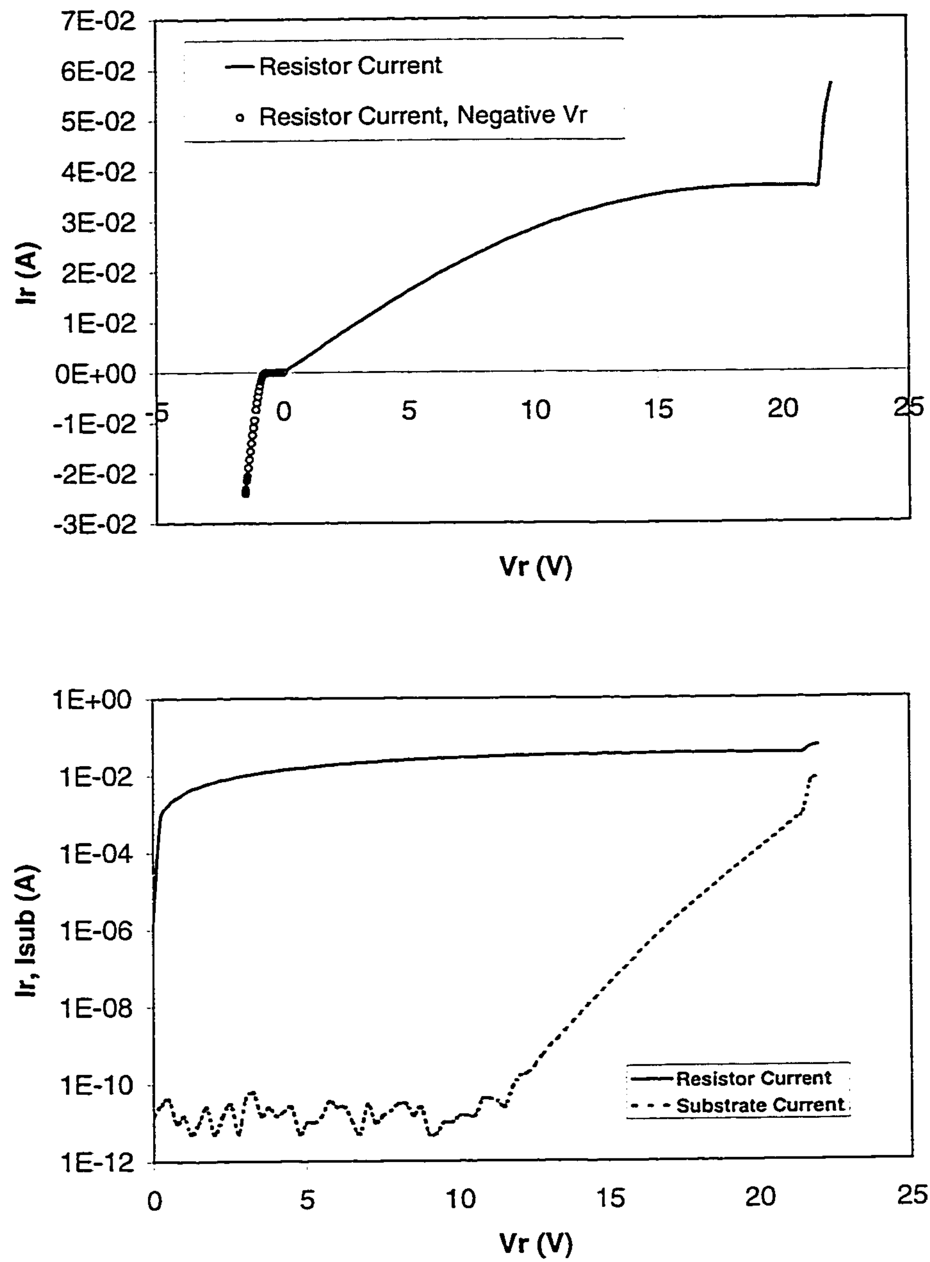
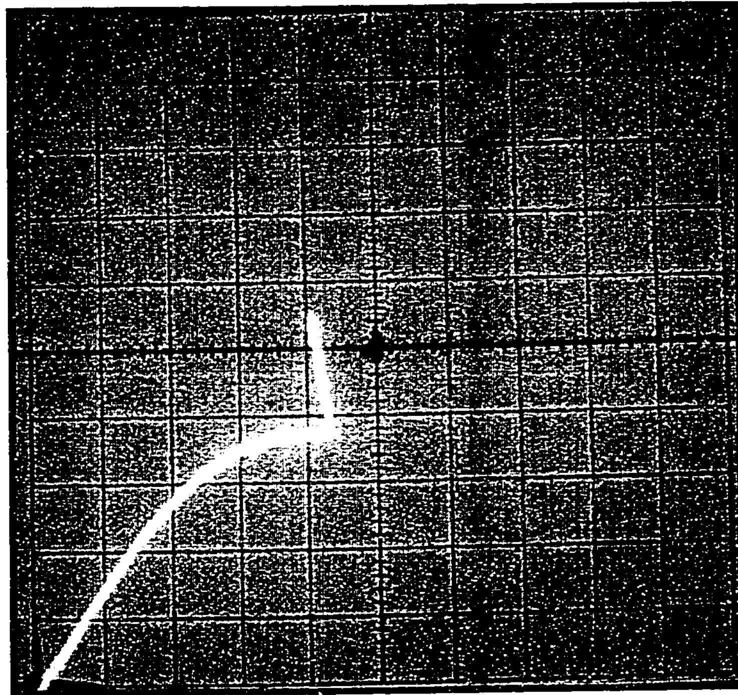


Figure 4-4. The top figure shows the negative and positive voltage sweep resistor current. The middle figure shows the log scale resistor and substrate I-V, showing the N+ / Pwell diode avalanche current starting ~12V.

V data for the N+ diffused resistor of Figure 4-1, including a sweep into the negative bias region. As can be readily observed from the data, the diffused resistor shows very different behavior from the classical resistor I-V. In the negative bias region, the resistor behaves as a forward biased diode. This is the first obvious effect of having a P substrate terminal connection at ground. In the positive bias region, the resistor demonstrates a linear region at low voltages (Vr < 5V), as would normally be expected, then a velocity saturation region (Vr > 6V), and finally an avalanche breakdown condition (Vr ~22V), again evidence of the third terminal at ground potential. Electron velocity saturation creates a non-linear increase to the resistance at higher voltages (fields), as can be seen from the data in Figure 4-4. Figure 4-5 shows the curve tracer measurement in the positive bias region, clearly depicting the avalanche breakdown mode, where the current increases dramatically.

Krieger and Niles did an extensive analysis on diffused resistors, both heavily doped (such as the N+ resistor), and lightly doped (Nwell) which was published in 1989. In their analysis, they started with a majority carrier current density equation that assumed a mobility-field relationship shown in the following equation:

$$J = q(N_o + n)\left(\frac{\mu_o E}{1+\left|\frac{E}{E_c}\right|}\right). \qquad \text{Eq. 4-1}$$



Vertical Scale: 10mA / DIV
Horizontal Scale: 5V / DIV

Figure 4-5. Typical N+ resistor curve tracer measurement.

E_c is the critical field, which is the electric field where velocity saturation starts to take effect. The low field mobility is indicated by μ_o, and N_o indicates the doping level. Their analysis indicated that for heavily doped resistors, the saturation current density should be about 5 x 10^7 A/cm^2. For the lightly doped case, the saturation current density should be about 1.6 x 10^4 A/cm^2. Their analysis agreed very well with the lightly doped diffused resistors, i.e., experimentally, they were able to measure their predicted current saturation density on Nwell resistors. Their result for the heavily doped resistors, however, was too high.

There are many examples of experimental data indicating that carrier drift velocity actually starts to saturate near or just above ~10^3 V/cm [20]. In the case of the N+ resistor studied in this work, the structure sustains an electric field (from a simple calculation, and confirmed by the MEDICI results) of about 5 x 10^3 V/cm at 15V applied bias. At a bias of 20V, the field has reached about 7 x 10^3 V/cm. These field values are well into the range at which velocity saturation is significant.

4.1.3 *N+ Resistor SPICE Model*

The measured I-V data demonstrates that a SPICE model for this resistor requires a 3-terminal model, including the diode seen in negative bias, and during avalanche breakdown. Figure 4-6 shows how circuit elements comprised of a network of discrete resistors and diode elements are used to model the resistor. The avalanche breakdown of the N+/Pwell diode will first occur in the cylindrical region just beyond the N-well profile. The measured data shows that the high end of the resistor is at about 22V before

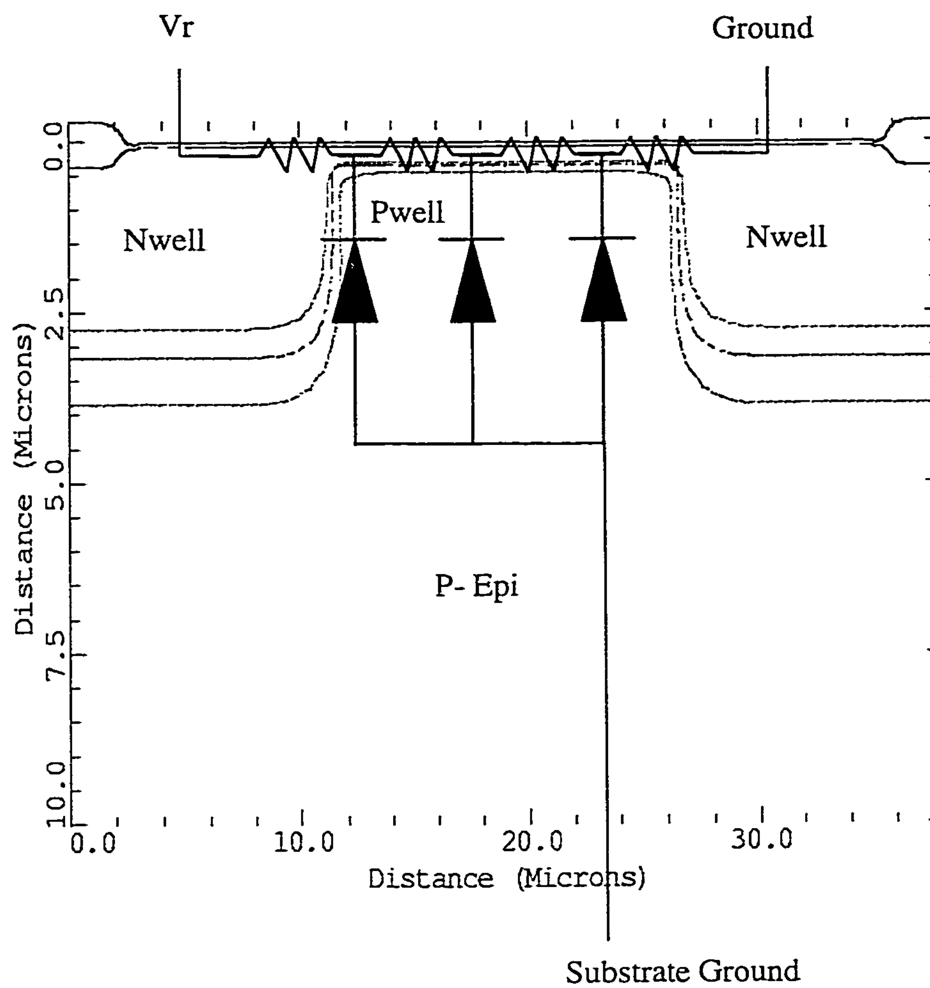


Figure 4-6. Diode and resistor network schematic for the N+ resistor.

the avalanche is fully on; since the resistance is at a high value under these conditions, the potential in the cylindrical region is actually about 16V. In order to see this breakdown effect accurately in TCAD, the simulation will have to include the three-dimensional structure in order to show the cylindrical edge in breakdown while the high end of the resistor is at about 22V. Simulating section A-A' will lead to breakdown in the planar junction case, which is near 38V. Section B-B' on the other hand, will show a 16V breakdown, which is the diode breakdown voltage for N+/P-well doping in this process technology.

Figure 4-7A shows the simplest model that can be used for SPICE simulation of a bias dependent resistor, including the substrate diode. Figure 4-7B shows the result of the SPICE simulation of this circuit. The single diode model can be used because once the avalanche breakdown starts, the maximum voltage will be "pinned" to that level, and the rest of the resistor section will not experience breakdown. There are conditions where this part of the resistor behavior is important to the SCR operation, and it will be pointed out in the discussion. The SPICE model used includes 3 resistor sections of equal value, which are bias dependent, and are implemented in a lookup table format. The diode itself is also implemented as a look up table for SPICE.

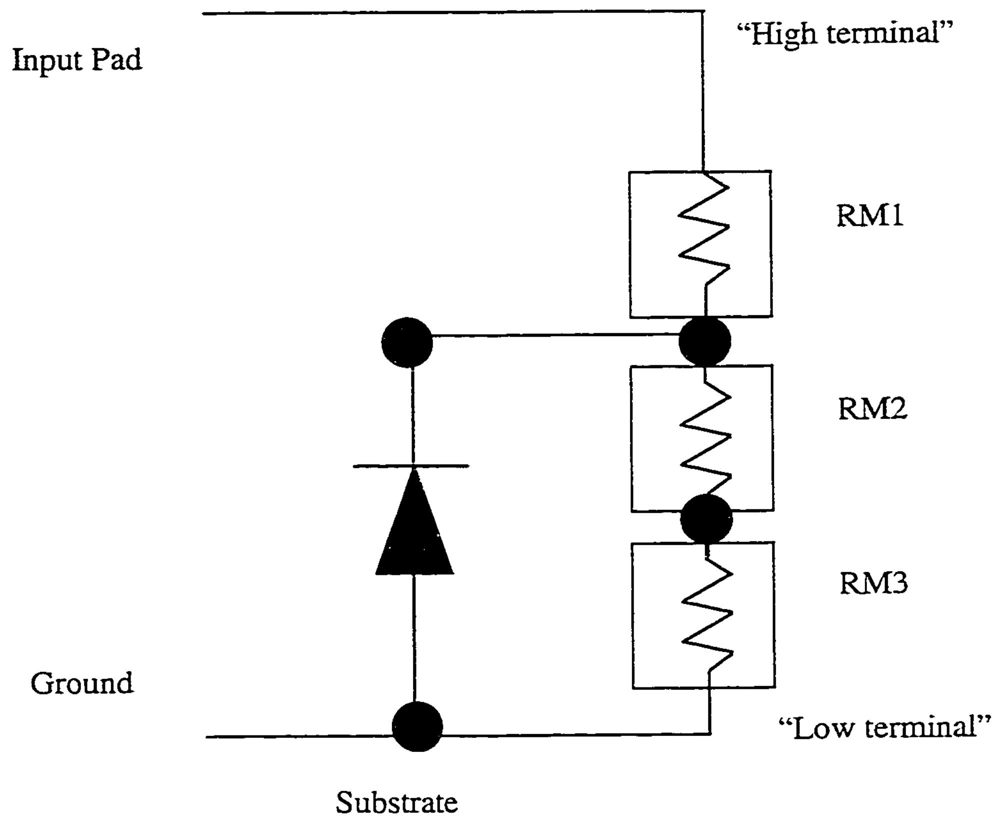
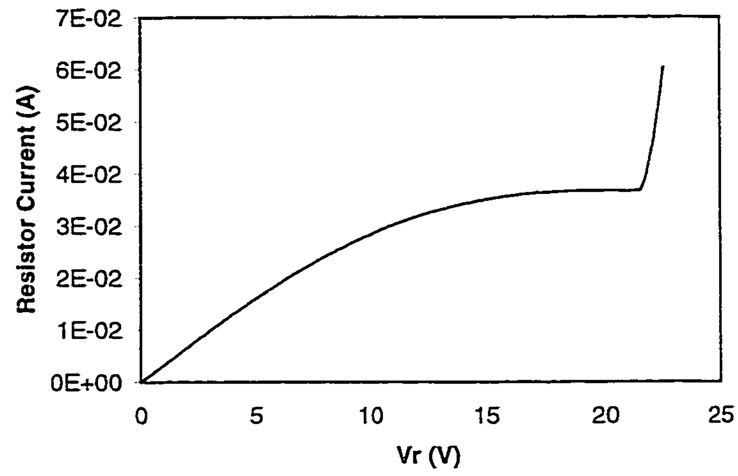


Figure 4-7A. Simple model to include bias dependent resistors in SPICE.



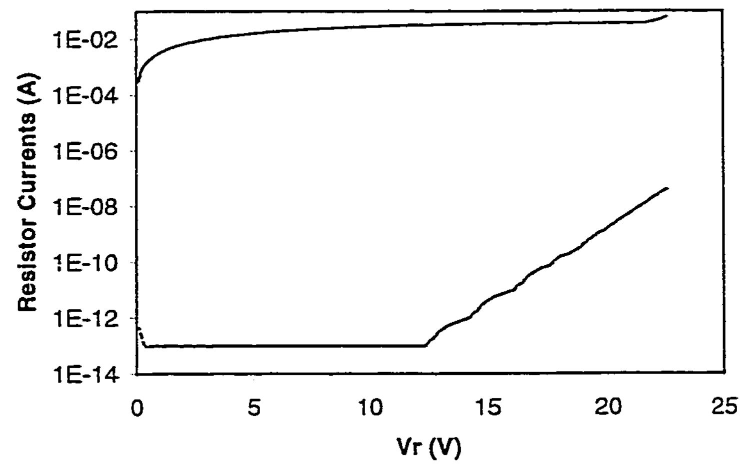


Figure 4-7B. SPICE simulation results of the N+ resistor model.

4.2 NMOS in Bipolar Mode

4.2.1 *Layout and Simulated Cross-Section*

Figure 4-8 shows the layout of the NMOS transistor used in this SCR. It is a single N+ polysilicon gate device with a N+ arsenic implant for the source/drain contact, and an N- phosphorus implant for a lightly doped drain profile adjacent to the channel. Figure 4-9 shows the simulated cross section of this transistor. The solid line in the N+ source/drain doping profile indicates the metallurgical junction, and the dashed lines indicate the zero bias depletion region edges. For this simulation, the substrate contact is made at the bottom of the structure, which is a P+ substrate. The drain contact is at the left side of the structure.

4.2.2 *Measurements, Simulations, and Literature Review*

When used as an ESD component, the NMOS transistor gate is normally tied to ground, as is the source contact, and the drain is connected to the input pad being protected [21] [22]. As the voltage rises during stress, this mode of operation resembles the "BV_{dss}" or drain-substrate junction avalanche curve (for a non-punchthrough transistor). As the transistor goes into drain avalanche, electrons are swept into the drain contact by the high electric field, and holes are injected into the substrate. This hole current has several implications. First, if the current is high enough, the Pwell resistance will raise the potential near the N+ source, effectively lowering the source/well diode barrier. This initiates electron injection into the Pwell region, where a fraction of them get

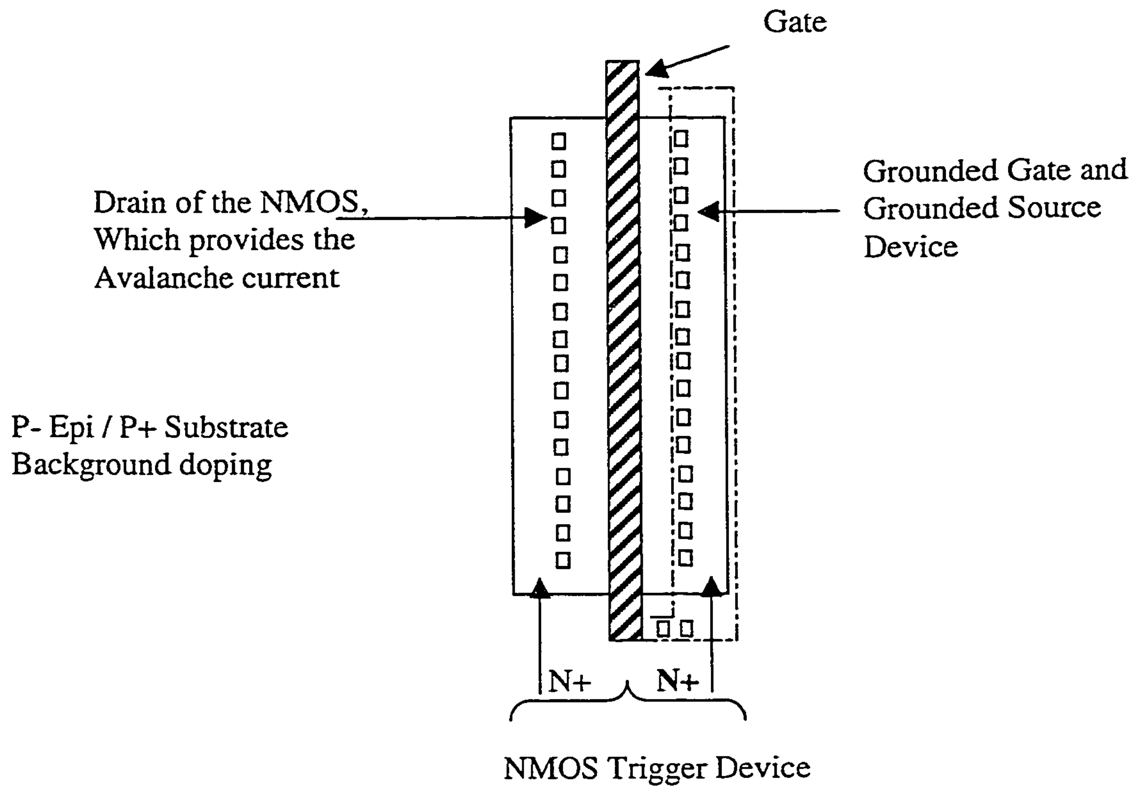


Figure 4-8. Layout of the grounded gate NMOS transistor, which serves as the trigger component for the SCR.

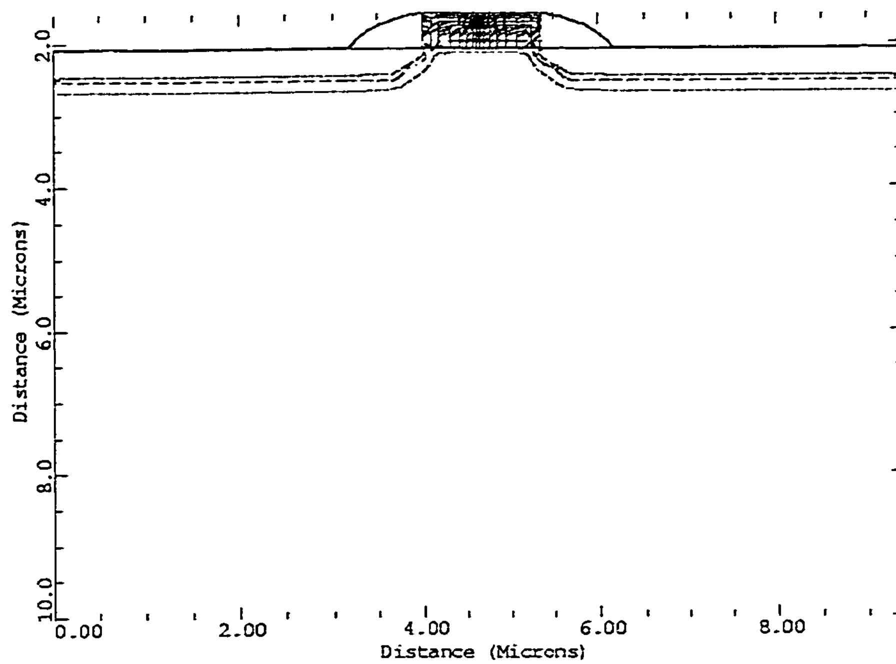
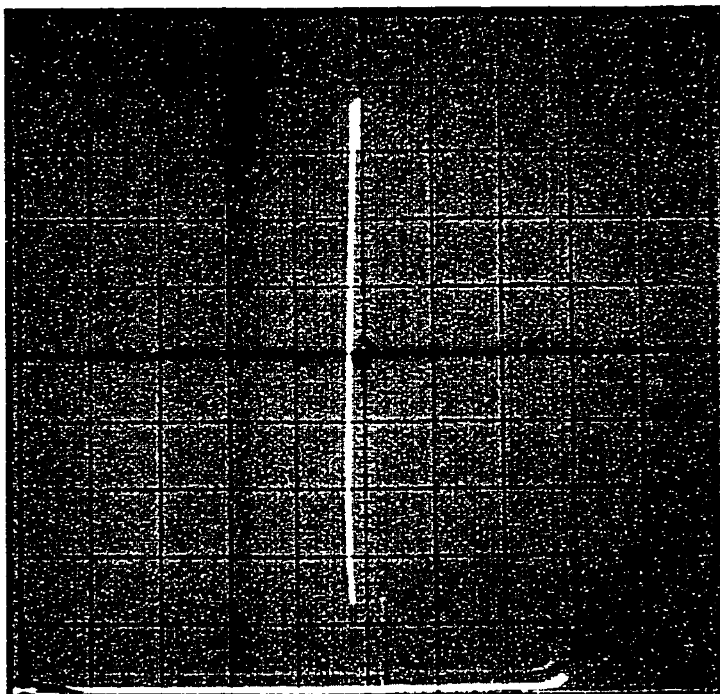


Figure 4-9. Simulated cross-section of the NMOS transistor showing the zero bias depletion regions.

collected at the drain due to its high electric field, initiating a NPN bipolar operation. Even if the P-well resistance does not create sufficient potential drop as a result of the substrate current, the hole accumulation near the source can also serve to lower the source/well diode barrier, thereby leading to bipolar operation.

When bipolar breakdown is initiated by drain avalanche (Vgs=0V), an effect known as "snapback" causes a reduction in the drain voltage, similar to the BVCEO breakdown in a NPN transistor [23] [12] [24] [25]. Figure 4-10 shows a schematic of the breakdown and "snap-back" measurement, as well as a representative curve tracer result. This bipolar effect is not only initiated by drain avalanche breakdown. Substrate currents are also created during normal operation (Vgs > 0V), and for high enough drain voltages can create enough hole accumulation and currents to cause bipolar breakdown. Figure 4-11 shows measured and simulated data of this effect. The simulation data also shows the Vgs=0V condition, or the "BVdss." These bipolar characteristics of NMOS transistors have been characterized and modeled extensively [26] [27] [28] [29] [30] [22] [31] [32] [33] [34] [35] [36] [37] [38]. Bipolar breakdown during normal transistor operation is referred to as "Bvii," and has long been recognized as an important parameter for understanding NMOS performance in an ESD protection device [27].

Other more subtle effects also play an important role in this parasitic mode of NMOS transistor operation. Muller showed the impact of the channel profile on bipolar breakdown [33]. Essentially two types of profiles were studied, 1) shallow "Vt adjust" profile, with a high resistivity well, and 2) deeper, high concentration implant with a low resistivity well. The source and drain processing were apparently held constant in this



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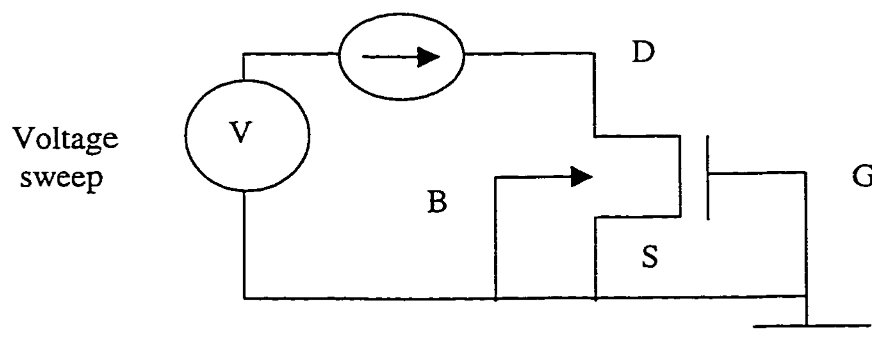


Figure 4-10. Typical curve trace result for the NMOS transistor in high current mode and schematic of the measurement.

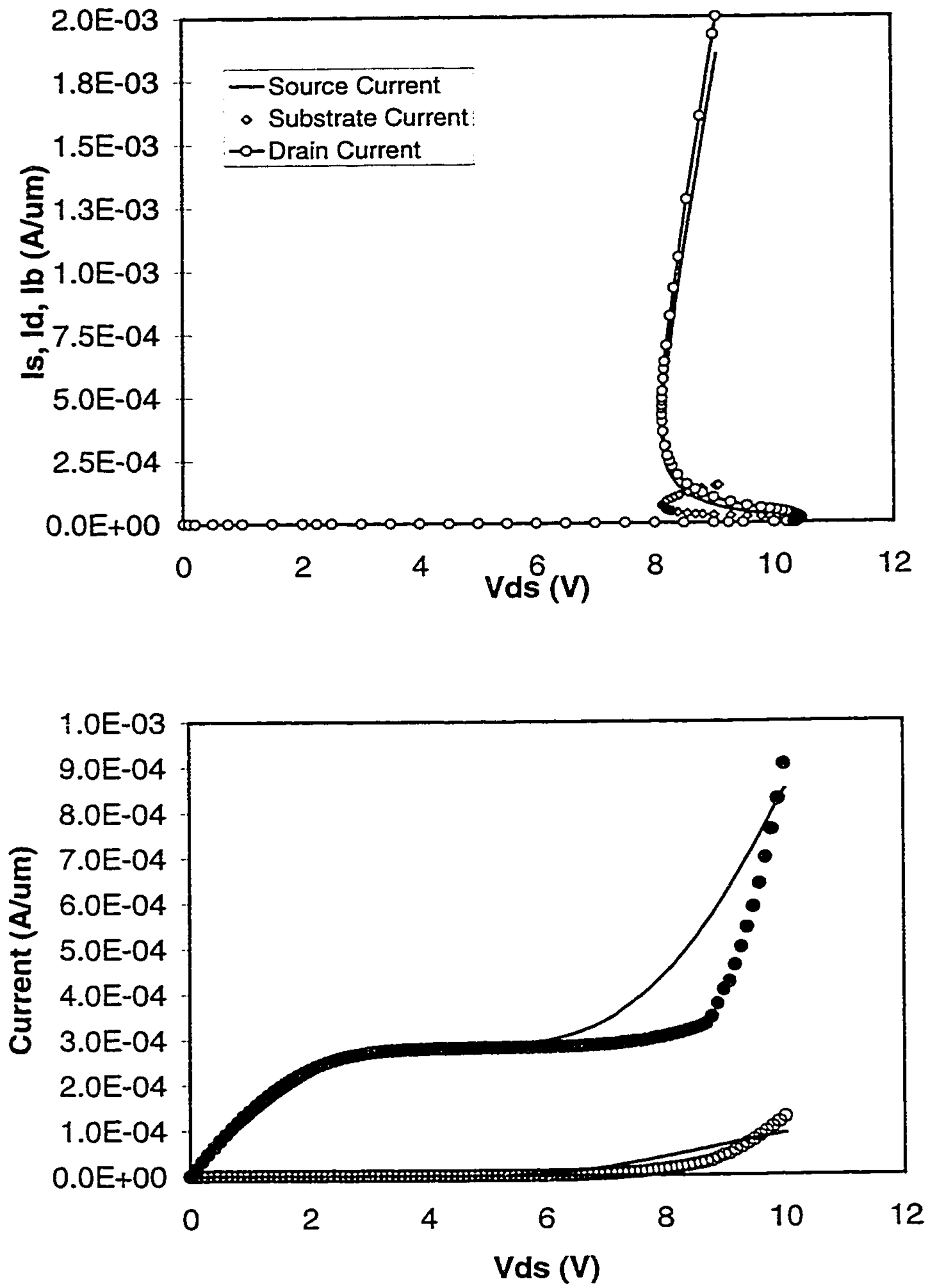


Figure 4-11. MEDICI simulation of the "BV_{dss}" (Vgs=0V) NMOS transistor drain sweep including avalanche and bipolar breakdown (top) and the "BV_{ii}" (bottom) where the transistor is on and enters the bipolar mode due to the avalanche created by the substrate current. In the bottom plot, the measured data is in the circles, the simulated data is the straight line.

study. The conclusions were that type 1 profiles resulted in source/well junction barrier lowering by hole accumulation near the source region. Type 2 profiles were shown to be more "robust" in that bipolar breakdown could be increased ~1V or more compared to type 1 profiles. The bipolar breakdown in this second case was apparently initiated by the increase of the well potential near the surface.

The paper did not describe the effects of "cross terms" in their experiments. For example, transistors with shallow implant and low resistivity wells were created, as well as deeper implants with high resistance wells, but the results were not presented. There were also other discrepancies that were not fully accounted for. For example, the threshold voltages with backgate bias (as expected) were quite different, and this resulted in significant differences in the drain current. For type 1 transistors, the drain current was ~60% higher compared to type 2 transistors. A more careful study would consider the impact of the ionization rate, for example, the ratio of drain current to substrate current for different biases, and the substrate current characteristics as a function of drain and gate bias for all cases.

In addition to the channel profile, the source/drain profiles also influence the parasitic bipolar effects. Chen published a report regarding the impact of the source/drain process on bipolar breakdown and ESD protection [27]. Essentially what he found was that LDD junctions exhibited higher snapback voltages compared to graded junctions and double diffused junctions. The graded junctions were phosphorus only junctions. The double diffused junctions in his study were composed of a shallow arsenic component and a deeper (both lateral and vertical) phosphorus implant. The lightly doped drain has

both arsenic and phosphorus, with a shallow lightly doped region next to the channel. His results showed that ESD performance degrades as the snapback voltage increases. Therefore, for ESD protection, the double diffused junction provided the most reliable performance. The impact of channel profile was not included in this report.

Other authors have published similar studies. Duvvury showed that shallow arsenic doping with phosphorus double diffused profile resulted in a good compromise between hot carrier effects and ESD performance [21]. Similarly to Chen, Duvvury concluded that lower snapback voltage transistors yielded more robust ESD protection. Wei did another extensive study of source/drain profile types. Similarly to Chen, Wei concluded that LDD transistors resulted in poor ESD performance, while DDD and MDD profiles resulted in better protection. MDD profiles were described to be implants of either arsenic or phosphorus following a phosphorus LDD implant before spacer formation [39]. In both cases the MDD profiles were slightly deeper, and with more lateral overlap of gate, than the phosphorus LDD profile. The double diffused profile was phosphorus, and was much deeper than the MDD profiles. Also, this double diffused profile was implanted after sidewall spacer formation. In all cases, an arsenic shallow implant was done after the spacer formation. Phosphorus MDD and DDD profiles had good ESD performance, while the arsenic MDD yielded transistors with very high substrate currents. The conclusion was that phosphorus MDD transistors offered a good trade-off between hot carrier effects, ESD protection and breakdown voltage.

What these researchers have shown consistently is that deeper diffused junctions with phosphorus have resulted in the transistors that offer a compromise between hot carrier immunity and ESD performance. Clearly, the source/drain formation together with channel profile has strong implications for device scaling, both from a typical operation point of view and from a "building in reliability" view.

4.2.3 *Bipolar Mode SPICE Model*

As the literature review and published data indicate, the NMOS high current bipolar mode of operation is useful for dissipating the ESD energy. As a result, many models have been presented over the years to account for the bipolar physics as part of the MOS equations. Models for simulating these effects in SPICE that have recently been published are rapidly becoming part of the standard simulation capabilities in university and industry software [38] [9] [40] [41]. Figure 4-12 shows the cross-section example and Figure 4-13 shows the equivalent circuit of a SPICE sub-circuit model representation of the NMOS transistor with the parasitic bipolar components. The SPICE model requires the usual MOS parameters; additionally, the following equations are calculated with the user supplied values for the following variables in order to model the bipolar effects: Ioe, Ioc, AI, and BI.

The equations calculated in SPICE are:

$$I_c = I_{oc}\left[\exp(\frac{V_{be}}{V_T}) - \exp(\frac{V_{bc}}{V_T})\right] \quad \text{Eq. 4-2}$$

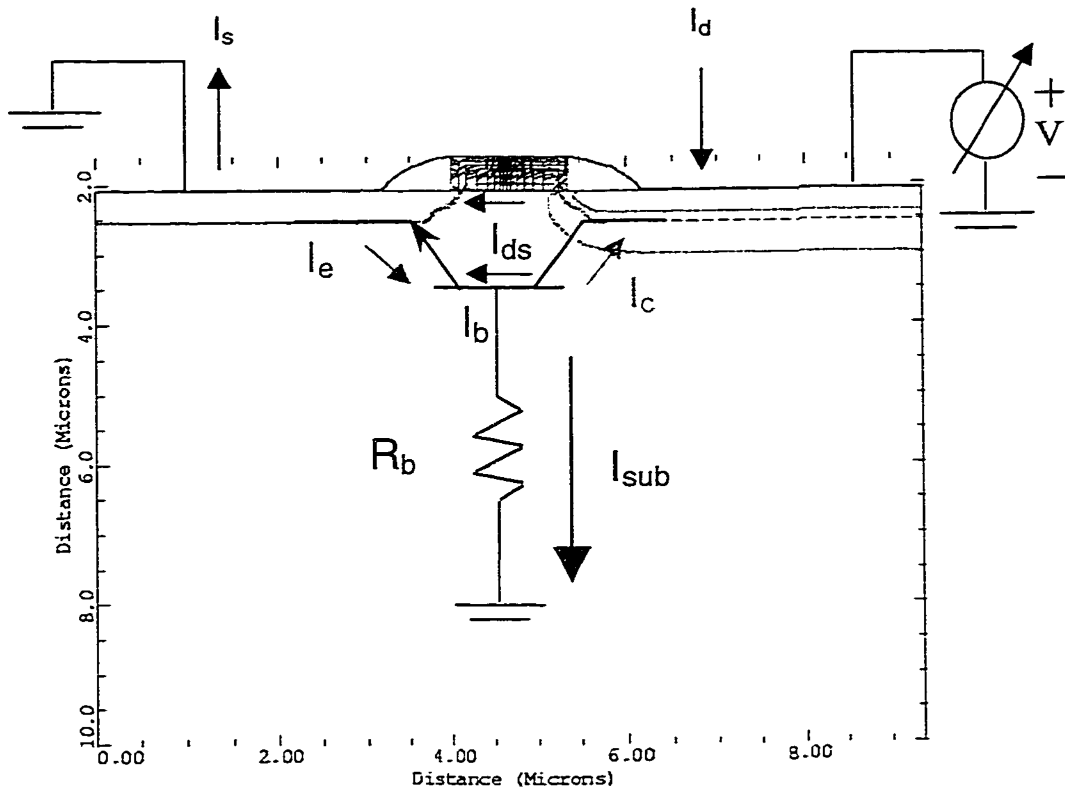


Figure 4-12. NMOS transistor cross-section and its bipolar elements under a high current avalanche condition.

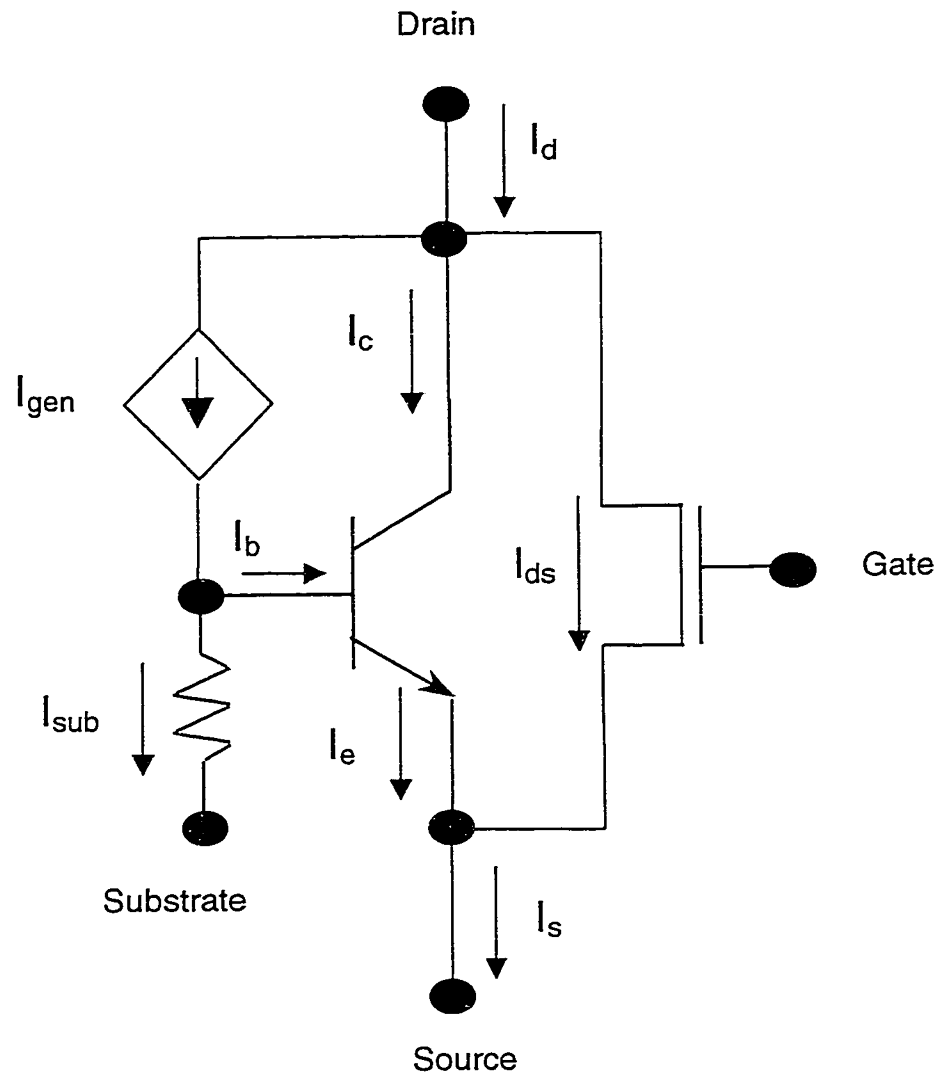


Figure 4-13. Equivalent circuit diagram of the MOS model including avalanche and parasitic bipolar effects.

$$I_B = I_{oe}\left[\exp(V_{be}/V_T) - 1\right] \quad \text{Eq. 4-3}$$

$$R_{sub} = V_{be_on} / I_{sub} \quad \text{Eq. 4-4}$$

$$I_{gen} = (M - 1)(I_{ds} + I_c) \quad \text{Eq. 4-5}$$

$$M = \frac{1}{1 - A_i \exp(\frac{-B_i}{V_{ds} - V_{dsat}})} \quad \text{Eq. 4-6}$$

Examples of ways to extract some of the parameters include the relationship between breakdown voltage and the ionization coefficients, A_i and B_i,

$$A_i = \exp(\frac{B_i}{BV}), \quad \text{Eq. 4-7}$$

where BV is the avalanche breakdown voltage for the NMOS transistor. Recent research activity at Stanford University and University of Illinois shows a wide acceptance for this bipolar model [40] [41] [9]. The research at Stanford is aimed at improving the numerical stability of the model equations and they are also investigating ways of improving the modeling of the substrate resistance.

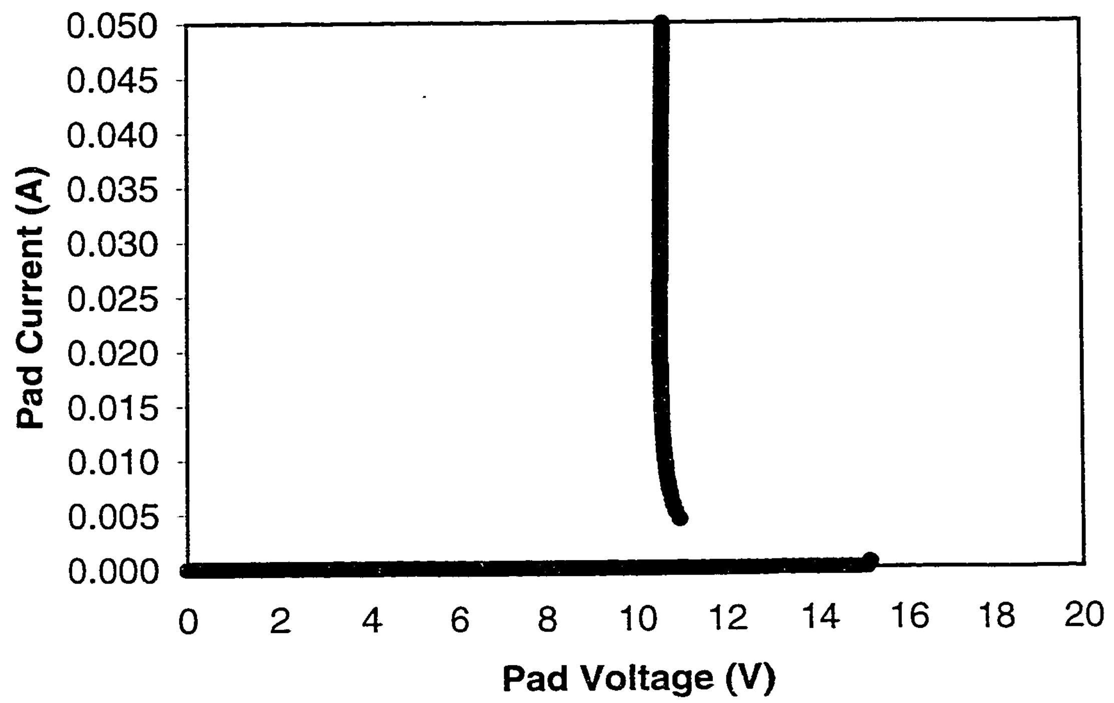


Figure 4-14. SPICE simulation of the NMOS transistor including bipolar breakdown mode.

The data was fitted to the NMOS transistor data in the high current regime, using the suggested avalanche breakdown parameter extraction, and keeping the bipolar leakage currents near their default value. Figure 4-14 shows the SPICE model fit to the measured data shown in Figure 4-10. The substrate resistance is calculated at the point where the bipolar transistor turns on, with a value of about 1KΩ. I_{oc} represents the bipolar collector saturation current, which is normally fit using

$$I_{oc} = \frac{I_d / M - I_{ds}}{\exp(V_{be_on} / V_T)} . \qquad \text{Eq. 4-8}$$

I_{oe} can be extracted from (where K is a fitting parameter)

$$I_{oe} = I_{oc}(M-1)/K . \qquad \text{Eq. 4-9}$$

4.3 NPN Transistor (4.5μm basewidth)

4.3.1 *Layout and Simulated Cross-Section*

Figure 4-15 shows the layout of the NPN transistor. This consists of the N+ source diffusion as the emitter, the Pwell isolation region as the base, and the N+/Nwell region as the collector. The base contact is the P+ substrate contact. Figure 4-16 shows a simulated cross section, with the solid line around the Nwell showing the metallurgical junction and the depletion edges indicated by the dashed lines. These are the solution for the zero bias result. This cross section clearly shows the effects of the doping profile on the junction capacitance. At the bottom of the Nwell is the P- epi layer, which is very

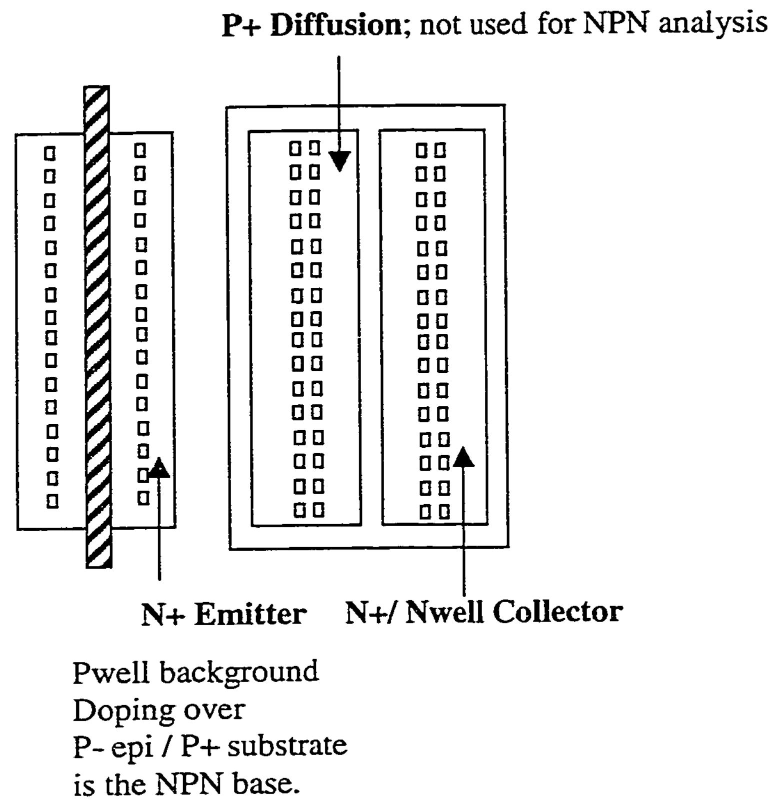


Figure 4-15. Layout of the NPN transistor. The P+ and N+ diffusions inside the Nwell were separated out to have access to the individual bipolar structures. The N+ NMOS source is the NPN emitter.

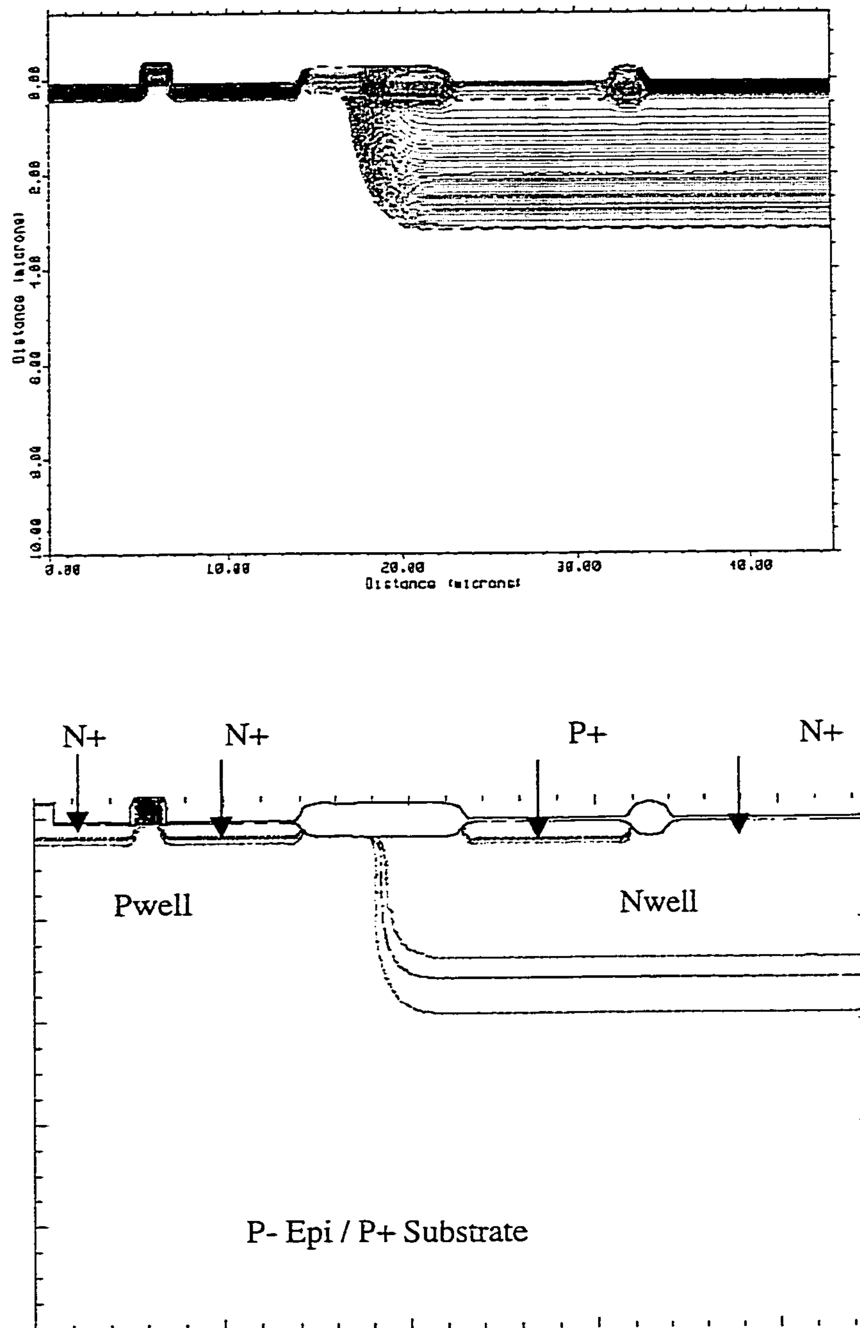


Figure 4-16. Simulated cross sections. The top structure is the TSUPREM4 structure, showing the doping contours. The bottom structure shows the result of a zero bias solution in MEDICI, with the depletion edges indicated at the junctions.

lightly doped, with a boron concentration of ~1E15 ions per cubic cm. At the left edge of the Nwell is the Pwell doping, which is about 50x higher in concentration than the epi layer. The difference in capacitance can be seen by the extent of the depletion edges, with the sidewall capacitance effectively an order of magnitude higher than the bottom junction capacitance. As can be seen from the cross section, this NPN device is a parasitic element created by the isolation region and adjacent diffusions. In other words, it is a device that is not designed by the process for specific characteristics. Instead, it exists due to the combination of diffusions and geometry made possible by the CMOS process. In addition, process technologies are developed specifically to prevent these parasitic elements from forming part of the circuit elements.

4.3.2 *NPN Transistor Measurements and Simulations*

Even though these parasitic components are not intended to be used in active circuitry, they are often used in ESD circuit design, since they do not add cost to a typical manufacturing process; i.e., there are no additional implants, mask steps, or diffusions required to create these structures. On the other hand, these elements are typically not modeled and their behavior in an ESD circuit is not quantified. In this work, models for these devices are considered important as we aim to understand the behavior of the ESD circuitry using SPICE.

Two of the most important bipolar measurements are the Gummel plot and the Early curves characterization. These data can be used for fitting one of the most widely used bipolar models, the Gummel-Poon model, which is included in the SPICE software.

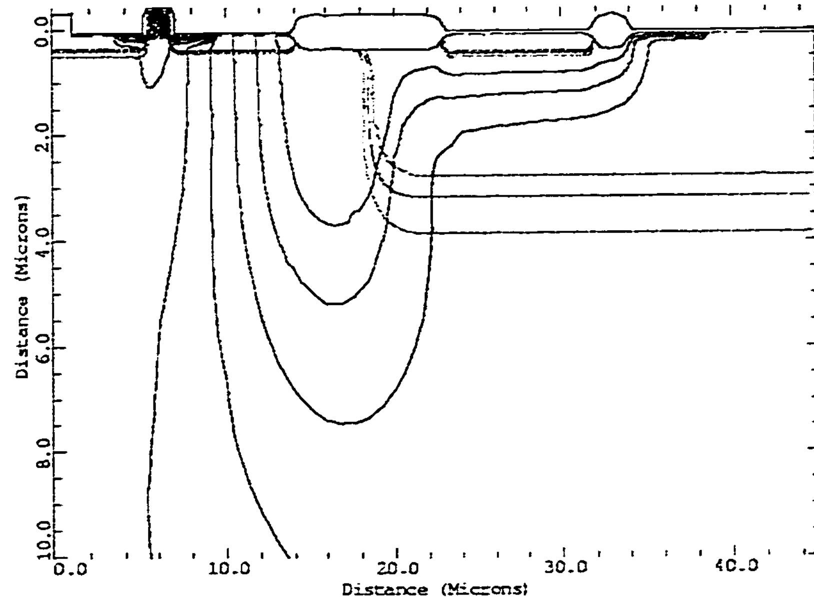
Figure 4-17 shows simulated cross-sections of the Forward Gummel simulation results, where the emitter is raised to a negative voltage to forward bias the base-emitter junction. The two plots show the current density flow lines at mid-injection and high injection. The collector-base junction is held at 0V. The DC bipolar gain can be extracted from this data defined as the ratio of the Ic and Ib values as a function of the emitter forward bias.

Of special importance are the methods in which the resistances are fit by the software, particularly in the high injection regime. Other parameters to be concerned with include the BVCEO, which is the collector – emitter breakdown with the base terminal open. In this case, the breakdown is very high, about 50V, as shown by the measured data in Figure 4-18. This is beyond the values we encounter for the NPN and the SCR.

4.3.3 *NPN Transistor SPICE Model*

The model used for the bipolar components is the industry standard Gummel-Poon model. Other bipolar models, which can be used in most circuit analysis programs, are various versions of the Ebers-Moll equations. The EM1 model is for DC analysis only. The EM2 model includes the EM1 plus some non-linear charge storage effects and ohmic resistances. The EM3 and Gummel-Poon models are similar; the difference is that the GP treatment accounts for beta roll-off at high currents, basewidth modulation and base transit time effects in a more unified manner.

In the GP model, the minority carrier current through the base is calculated using the following equation,



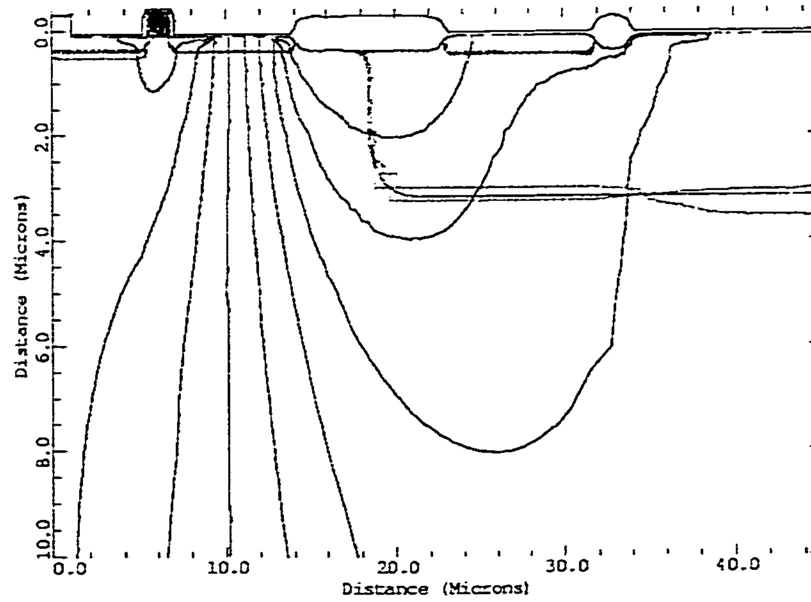


Figure 4-17. Simulated mid-injection (top) and high injection bipolar currents for the 4.5um wide base NPN transistor.

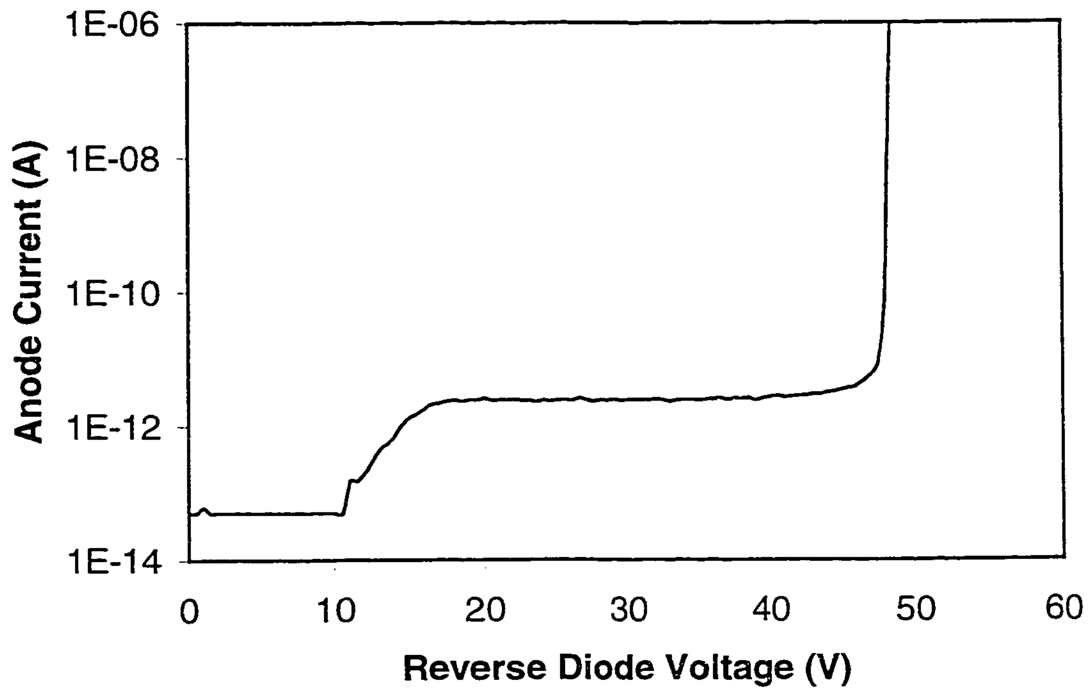


Figure 4-18. Nwell to Pwell diode avalanche breakdown. The breakdown voltage is beyond the interest for this work.

$$I_c = Is\left[\exp\left(\frac{V_{be}}{N_F V_T}\right) - \exp\left(\frac{V_{bc}}{N_R V_T}\right)\right] \quad \text{Eq. 4-10}$$

I_s the saturation current and is normally extracted from the Forward Gummel data. The non-ideality factors, N_F and N_R, are extracted from the slope of the forward and reverse Gummel data, in the regions below high injection. Other important parameters include the "knee current," which is the collector current value on the Gummel Plot at which the slope changes from about 1 to about ½. Most of the forward characteristic parameters can be fitted or extracted using the Gummel Plot data and the Forward Early data.

The SPICE model data for the Forward Early fitting is shown in Figure 4-19. Due to the wide base of these transistors, the data and the model show that the Early Effect, the modulation of the collector current due by the collector-base voltage, is almost non-existent. The extracted Early Voltage for these devices was on the order of 100V. Figure 4-20 shows the Forward Gummel Plot results, and Figure 4-21 shows bipolar gain resulting from the measured data and the model. Particular attention was paid to how to do the fitting in the high current region, where the internal resistances start to make an impact on the device behavior. In general, however, the key to getting a good result for the complex structure was found to be the region of the I-V near the base-emitter forward biasing potential, which is where the bipolars turn on. Getting this region accurate ensures that the SCR will trigger at the appropriate biases and currents. Figure 4-22 shows some of the procedures that were followed in fitting the bipolar parameters.

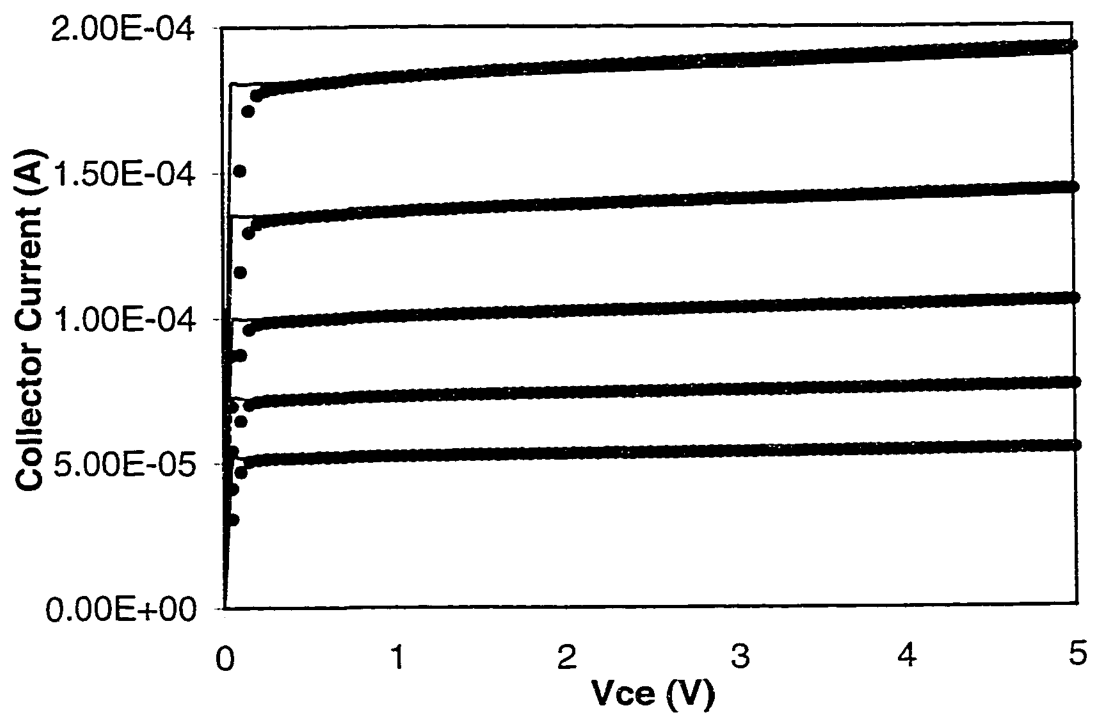


Figure 4-19. Measured and SPICE simulated Forward Early characteristics for the 4.5um wide base NPN transistor.

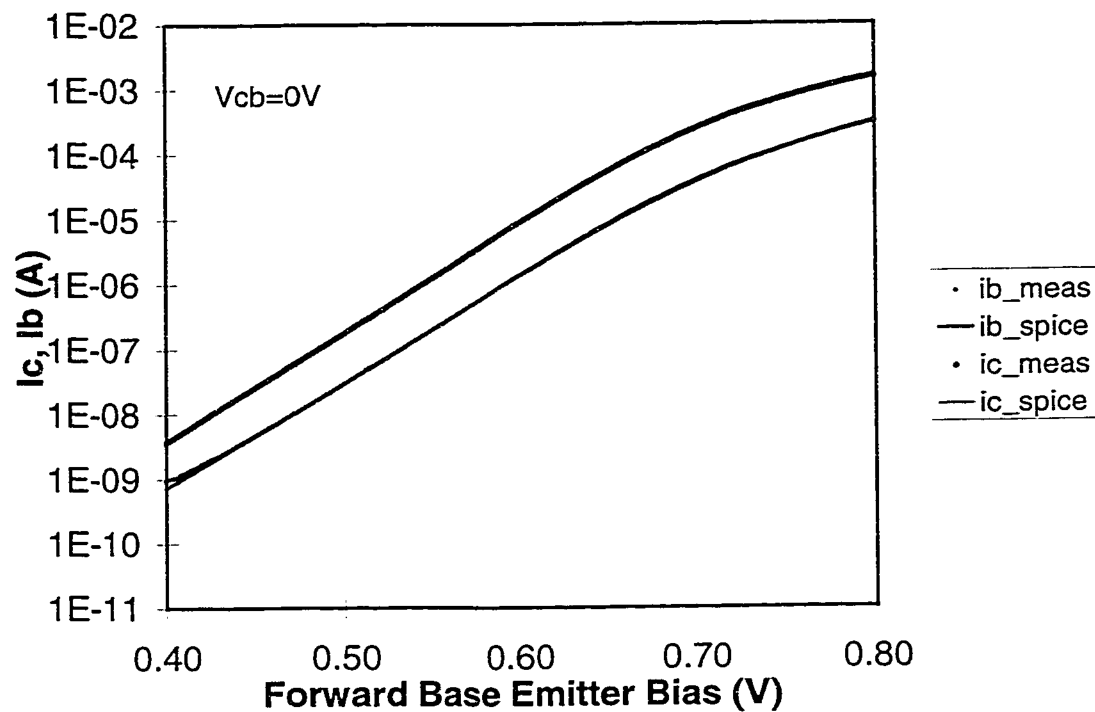


Figure 4-20. Measured and simulated Forward Gummel Plot for the 4.5um wide base NPN transistor.

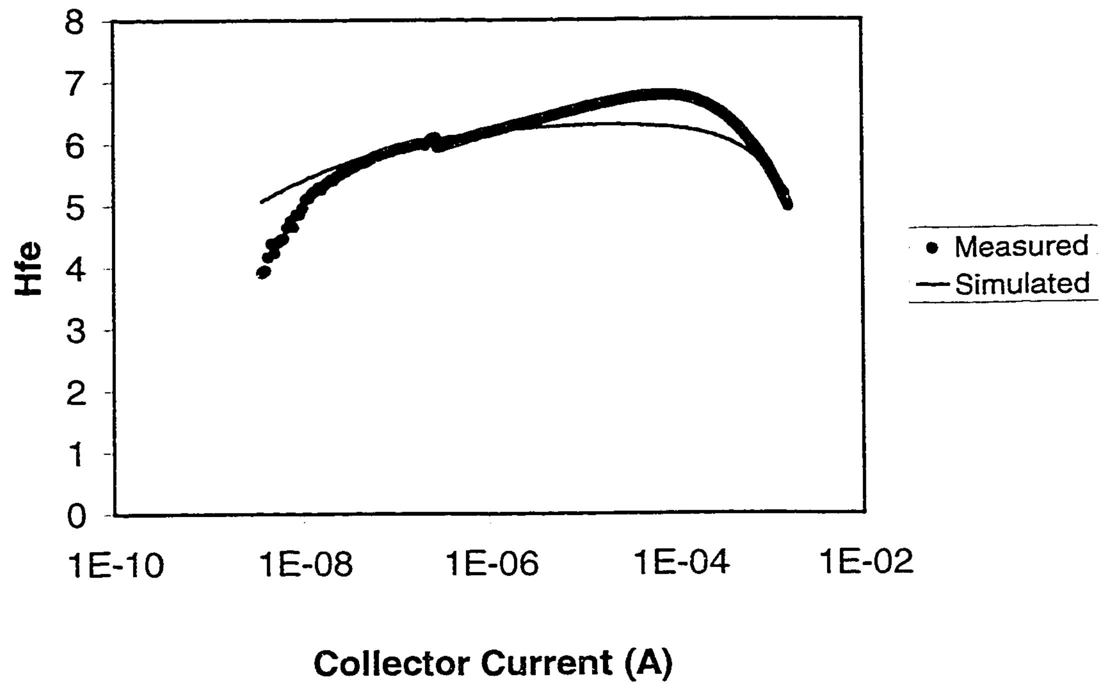
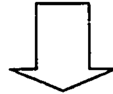


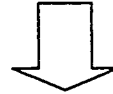
Figure 4-21. The measured and simulated current gain for the 4.5um wide base NPN transistor.

Gummel-Poon Bipolar Modeling Flow, DC Forward I-V

Measure Forward Gummel and Early I-V from test structure using IC-CAP



Using Low to Mid-Injection region on Gummel Plot, match Ic & Ib data with IS, BF, NF, NE, C2 (or ISE). (NF ~1; BF should be pinned to max. measured gain; RC, RE, RB, RBM, & IRB should be ~0; IKF ~∞)



Using the High-Injection region, fit the measured Ic and Ib data using RE, RB, RBM; IKF & IRB can be balanced to accurately model both Ib & Ic in high current regions. VAF and Rc can be fit using the Forward Early I-V.

Figure 4-22. Flow used for modeling the bipolar structures in this work.

4.4 NPN Transistor (9μm basewidth)

4.4.1 *Layout and Simulated Cross-Section*

Figure 4-23 shows the simulated cross-section of this transistor. The layout is exactly the same as the 4.5μm NPN, except that the spacing between its N+ emitter and the Nwell collector was extended out to 9μm. As was mentioned before, two different SCR's based on this basewidth were studied as part of this research.

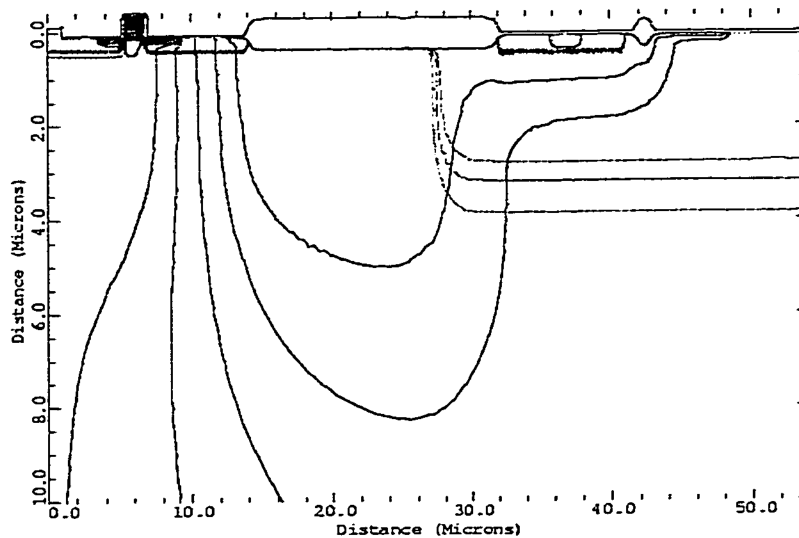
4.4.2 *Transistor Measurements and Simulations*

Basically, all of the bipolar structures were measured and analyzed in the same way. Forward and reverse Early and Gummel data were taken for parameter extraction. This was the primary method of obtaining the SPICE parameters. TCAD simulations were performed to demonstrate the ability of the TCAD models, and to confirm the measured results from the silicon. Figure 4-24 shows the mid-injection and high-injection current densities from the Forward Gummel simulations. Comparison with Figure 4-17 shows that the two NPN transistors behave in a similar manner, except that the wider base device has a lower current gain.

4.4.3 *9μm Wide Basewidth NPN SPICE Model*

Figures 4-25 through 4-27 show the Forward Early, the Forward Gummel, and the DC current gain capability of this SPICE model. Many devices were measured for

Figure 4-23. Simulated cross-section of the 9um wide base NPN transistor.



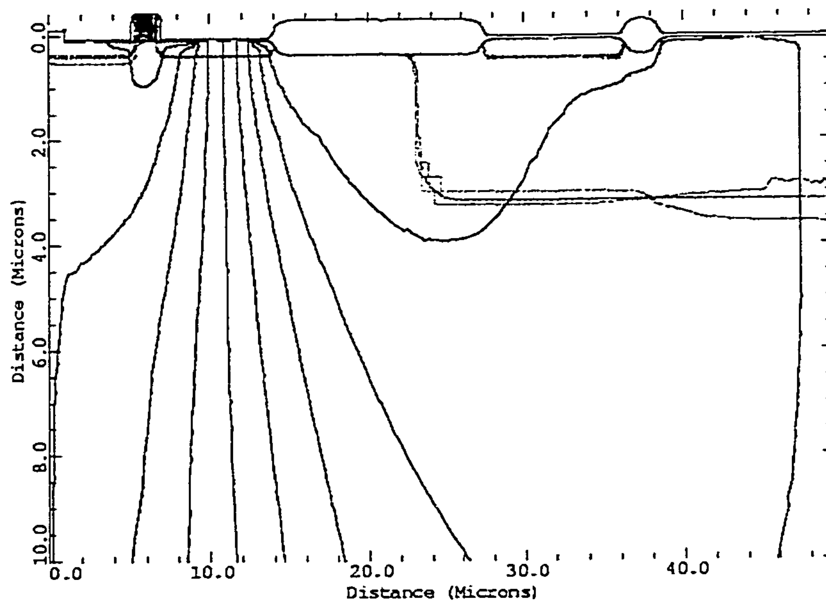


Figure 4-24. 9um NPN transistor current flow at the middle-gain region (top) and at high injection region (bottom). The NMOS drain also behaves like a collector under these conditions.

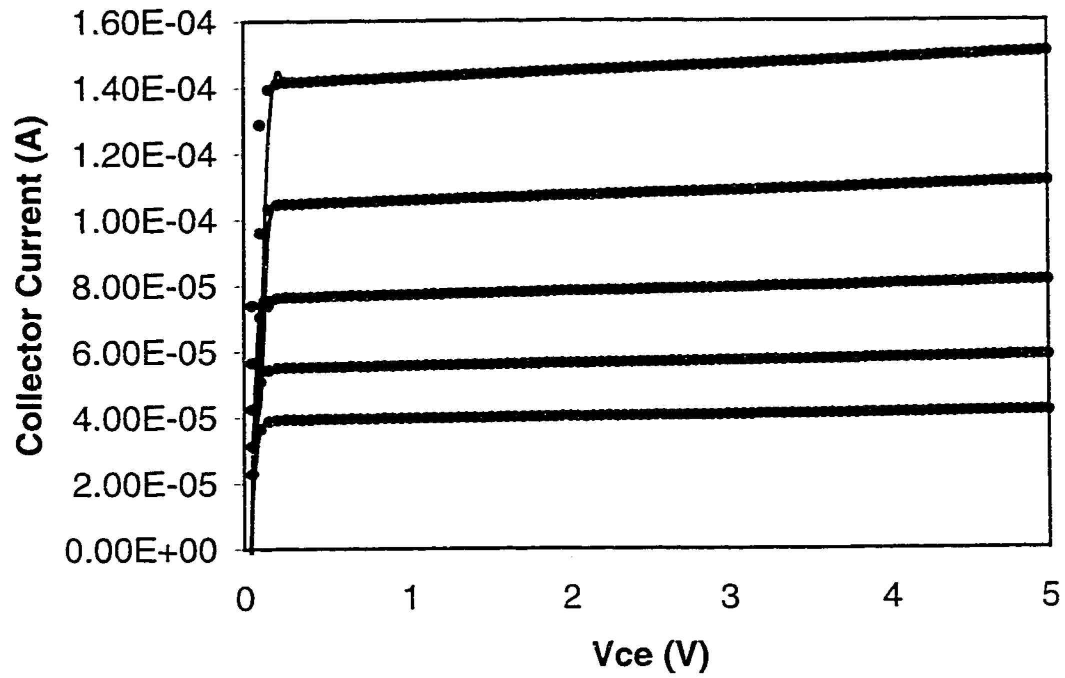


Figure 4-25. Measured (dotted) and simulated (straight line) Forward Early curves for the 9um wide base NPN transistor.

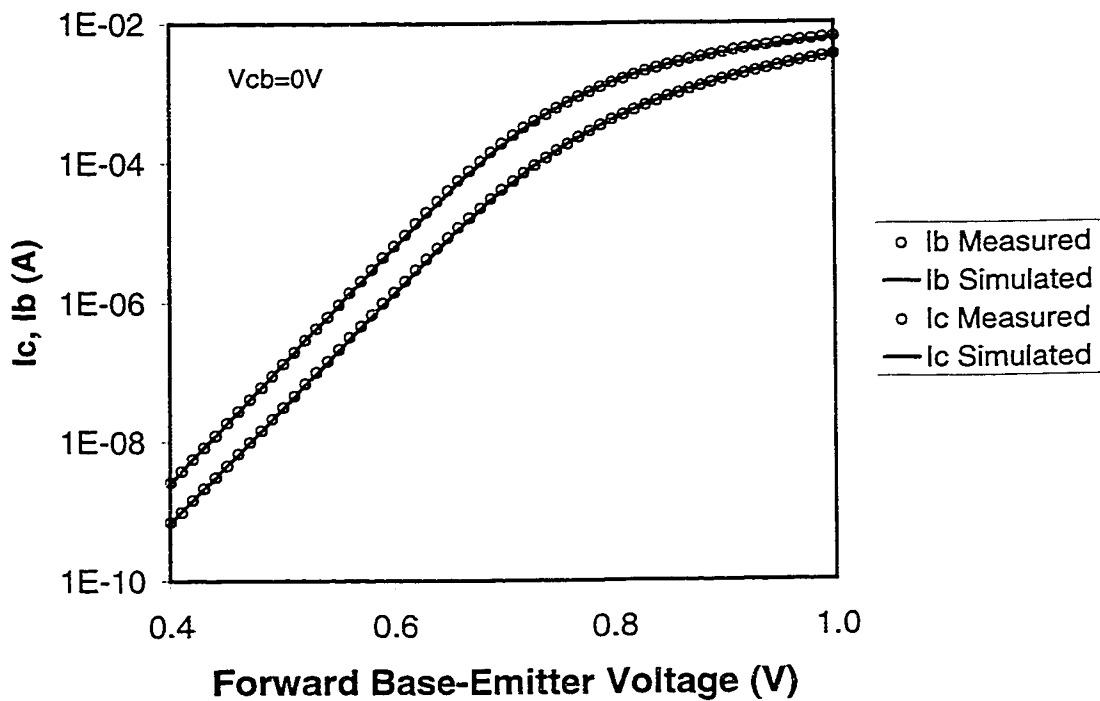


Figure 4-26. Measured and simulated Forward Gummel Plot for the 9um wide base NPN transistor.

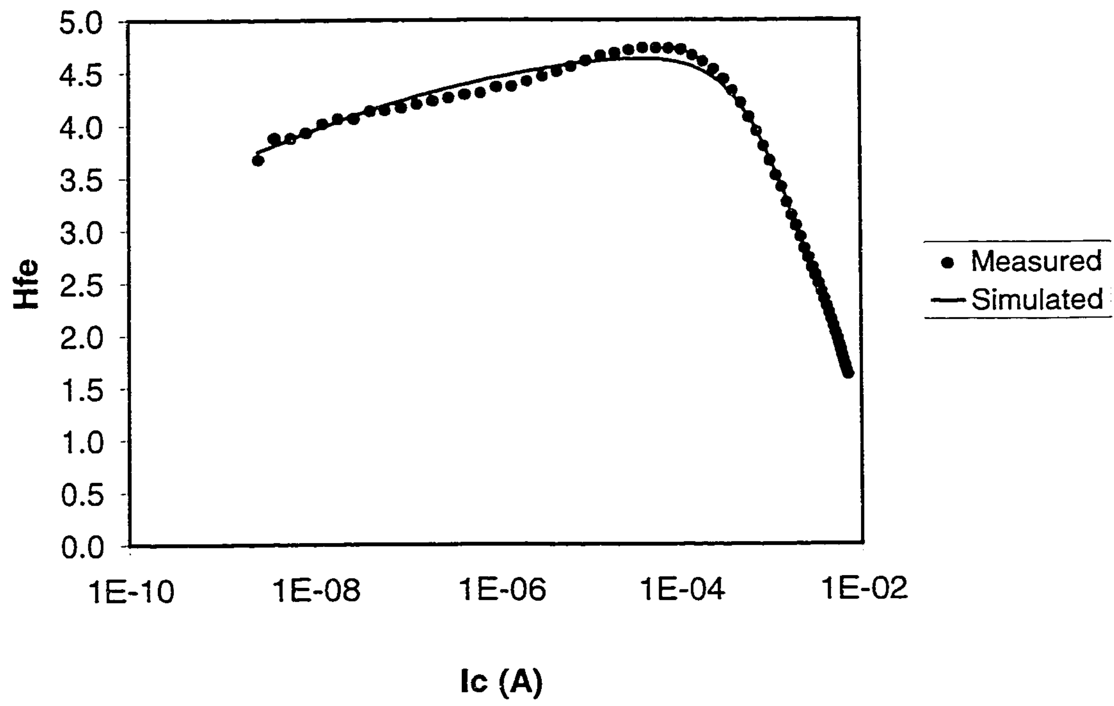


Figure 4-27. Measured and simulated DC current gain, Hfe, for the 9um wide NPN transistor.

comparison against different wafers, and this data will be presented at the end of this chapter.

4.5 **PNP Transistor**

4.5.1 *Layout and Simulated Cross-Section*

Figure 4-28 shows the PNP transistor layout, and Figure 4-29 shows the simulated cross section. This transistor is also a parasitic device, as it is created from default processing conditions and a layout that purposely contains the required doping regions. The P+ diffusion serves as the emitter, the Nwell is the base, and the P substrate is the collector.

In many SCR structures, the P+ diffusion and the N+ diffusion inside of the Nwell are shorted together to reduce layout space. The standard form of the SCR we used in this study contained this type of layout. However, to properly characterize the PNP transistor, a layout with non-abutting, but adjacent, P+ and N+ regions separated was created. This allowed us to separate the emitter and base terminal connections in the test module in order to access the PNP transistor. SCR's were also created with this layout, in order to ensure one-to-one correspondence between the bipolar structures and the integrated SCR circuit. A minimum spacing of about 2.2um was used for this separation, and it adds a very small amount of NPN collector resistance (about 2.5%) compared to the original structure. As the sensitivity results will show later, this difference is negligible in the SCR operation.

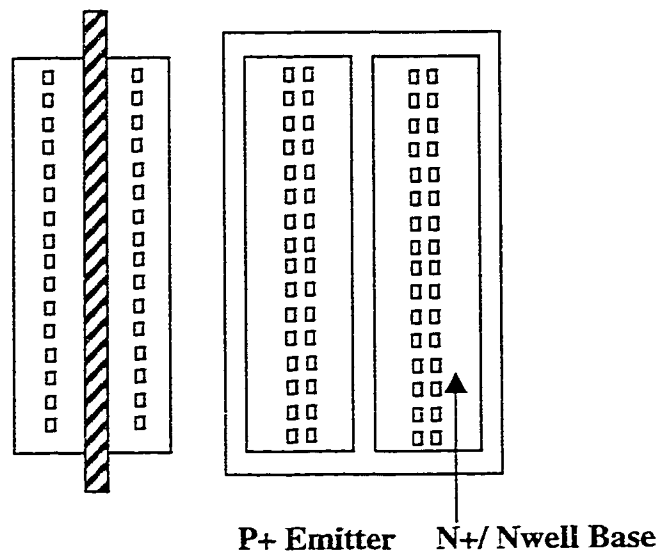


Figure 4-28. Layout of the PNP transistor. The P+ diffusion inside the Nwell is the Emitter. The background (P substrate) is the collector.

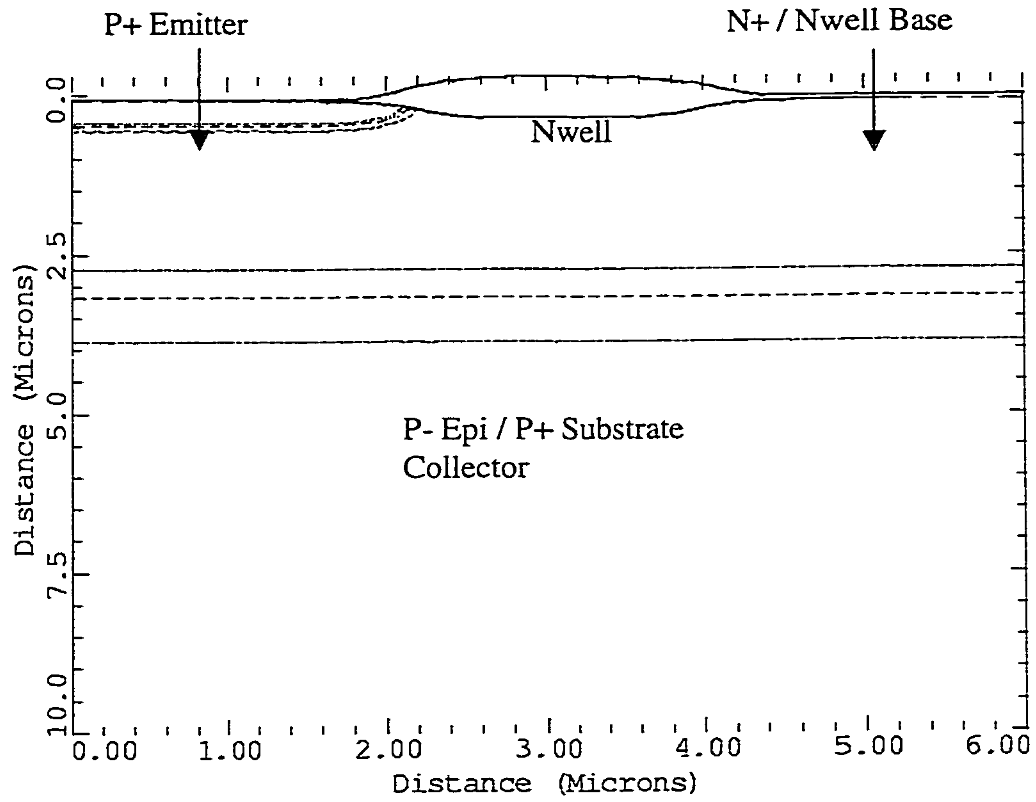


Figure 4-29. Simulated cross-section of the PNP transistor.

4.5.2 *PNP Transistor Measurements and Simulations*

Figure 4-30 shows the simulated mid and high injection currents in this transistor. One of the interesting points about this PNP device is that the gain is much higher than the NPN transistors. The primary reason for this is the smaller effective basewidth of this transistor, compared to the NPN devices.

4.5.3 *PNP Transistor SPICE Model*

The SPICE model results, also fitted using the IC-CAP software, are shown in Figures 4-31 through 4-33. Again, very reasonable results can be observed from the data. Of particular importance were getting the mid-injection regions accurate, since this is point where the PNP transistor turns on strongly and leads to latchup in this SCR circuit.

4.6 **Summary and Conclusions**

Extensive data was taken on the individual components used in this SCR circuit. In addition to the data, TCAD simulations were run as a crosscheck of basic parameters and to gain insight into the device characteristics. Table II shows a summary of some of the basic simulated and measured data. Figure 4-34 shows an example of the parameter distribution for the bipolar devices across a wafer. Figure 4-35 shows the results for a second wafer, from a different lot, which demonstrate the parameter stability expected from a mature production process.

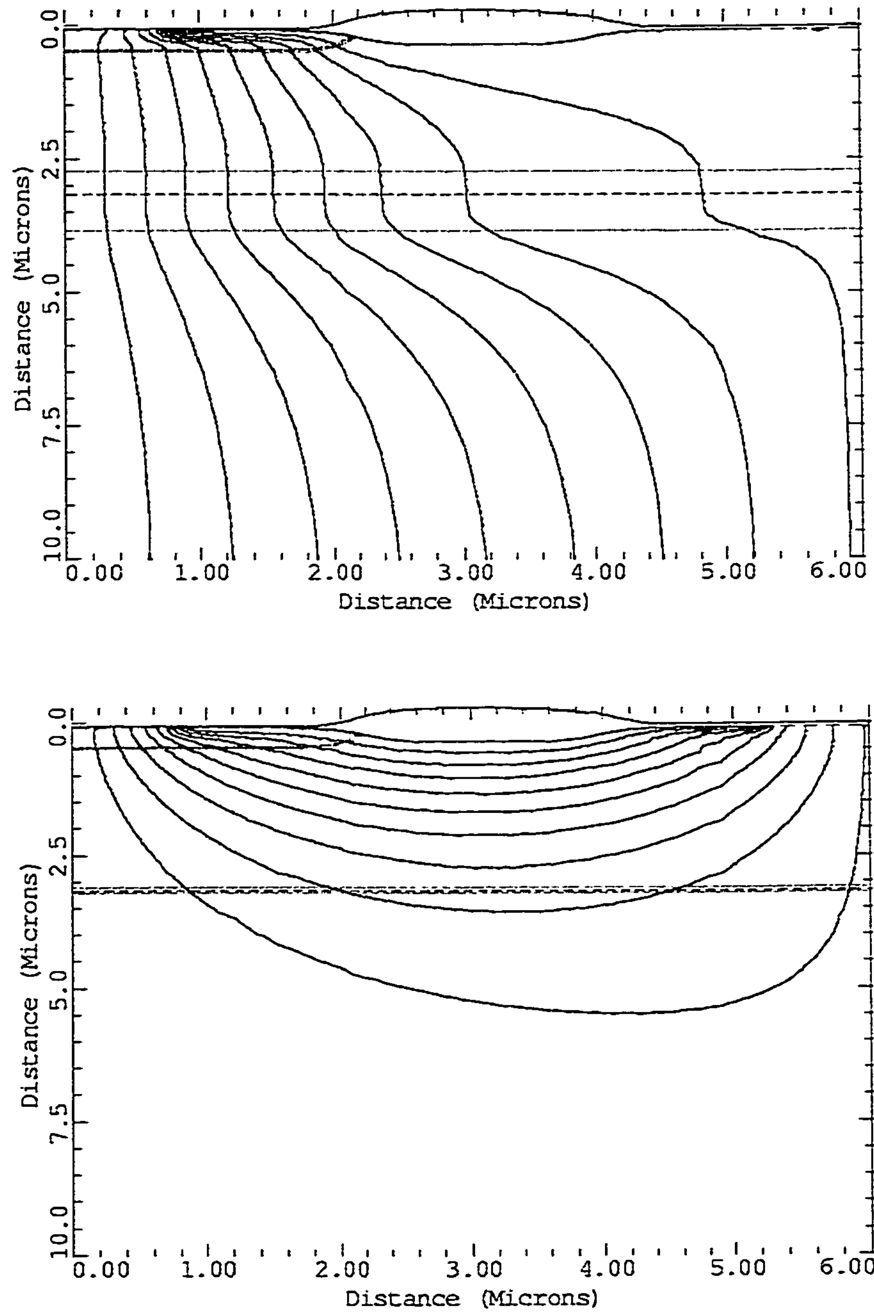


Figure 4-30. Mid injection (top) and high injection current flow for the PNP transistor.

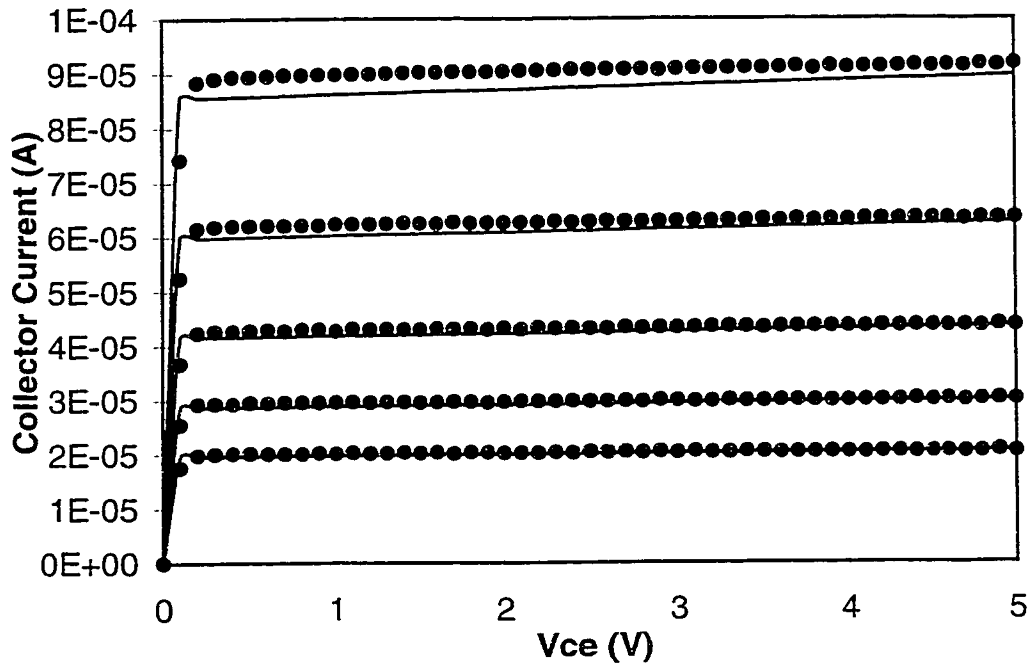


Figure 4-31. Measured and SPICE simulation of the Forward Early characteristics for the PNP transistor.

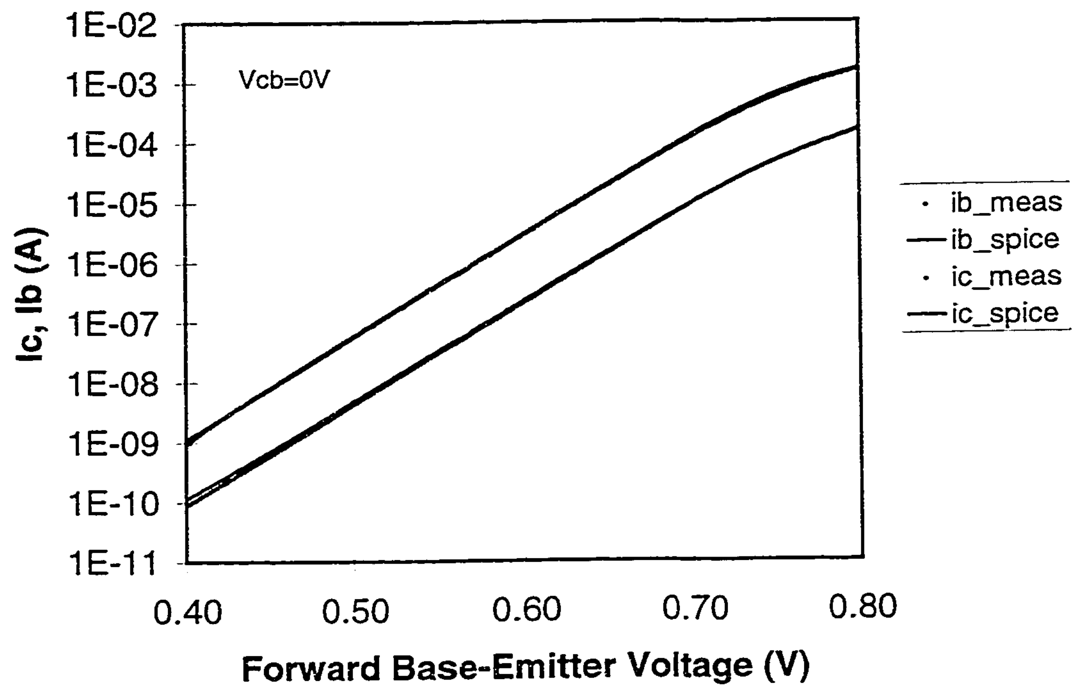


Figure 4-32. Measured and simulated Forward Gummel data for the PNP transistor.

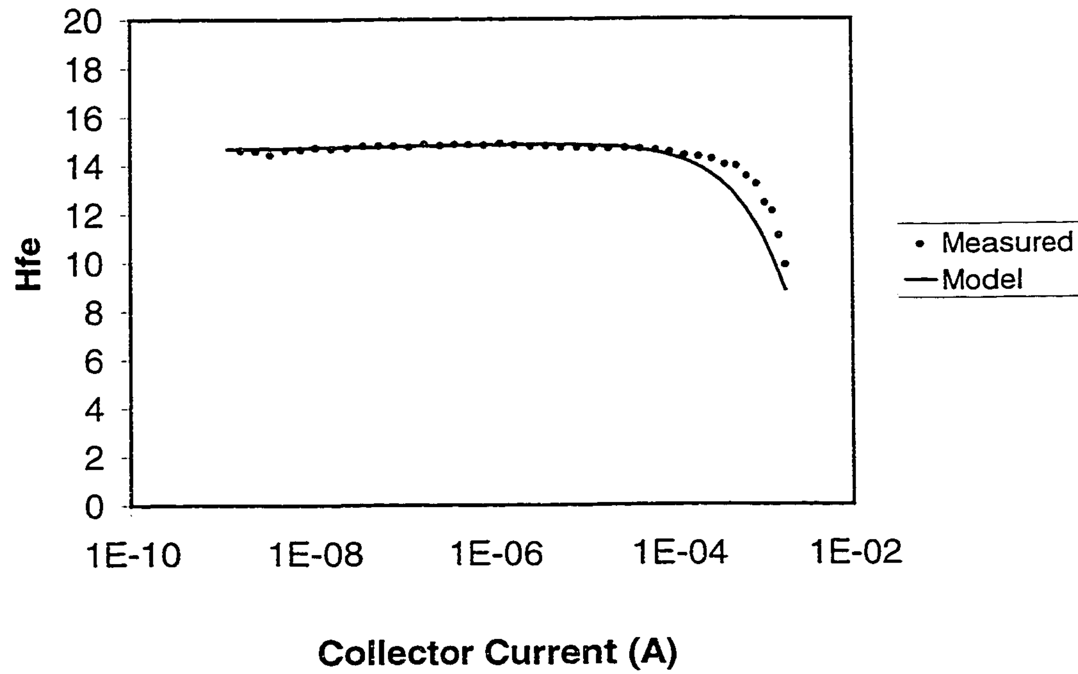


Figure 4-33. Measured and simulated DC current gain for the PNP transistor.

Table II. Summary of Measured and Simulated Results.

Component, Parameter	Measured	Simulated
SCR PNP, H_{fe}	14 +/- 2	11
SCR 4.5um NPN, H_{fe}	6.5 +/- 1	6.5
SCR 9um NPN, H_{fe}	4.5 +/- 1	3.5
NMOS BV	12 +/- 2	11
NMOS BVii	9 +/- 1	8

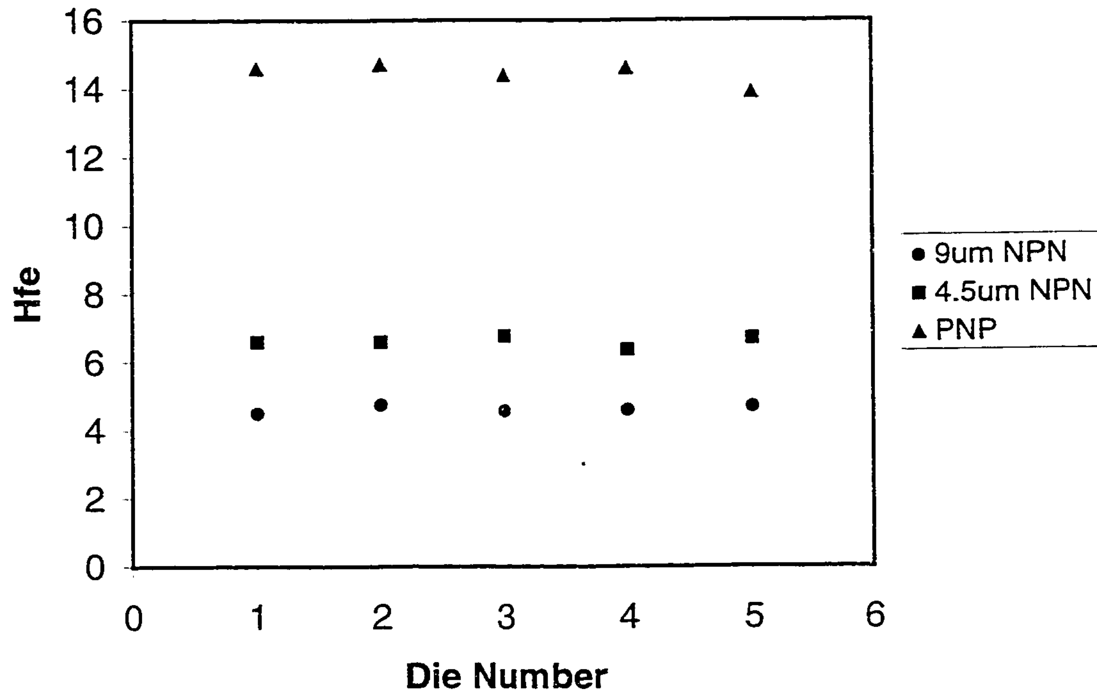


Figure 4-34. Measured data from one of the wafers studied in this research. The five dies were located in the bottom, left, center, right and top of the wafer.

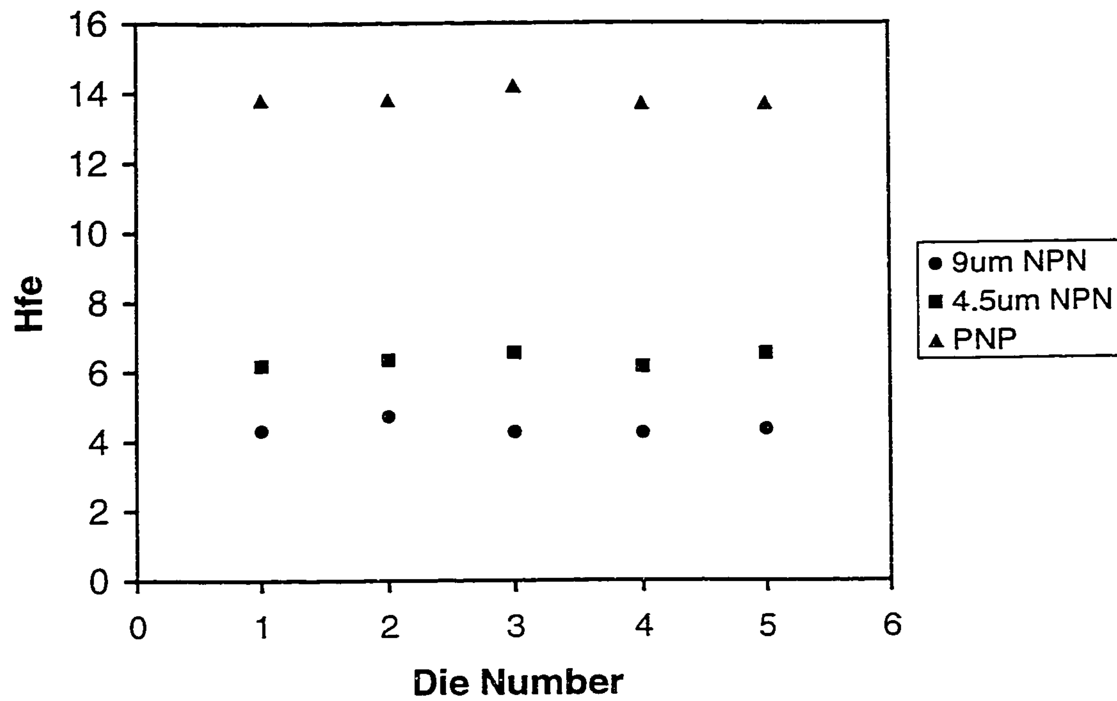


Figure 4-35. Hfe distribution for a second wafer used in this study.

CHAPTER 5

STEADY STATE OPERATION OF THE AVALANCHE TRIGGERED SCR

This chapter will describe in detail the steady state operation of the avalanche triggered SCR. The physical operation of the device will be reviewed, including the TCAD results used to describe the various phenomena that are occurring in the device prior to and after latchup triggering. The TCAD simulation results are the key to understanding how the device operates, and these results played a major role in developing the SPICE sub-circuit model of the structure. The SPICE representation of this circuit will be presented, including the comparison of the model to the silicon measurements under steady state conditions.

5.1 **Avalanche Triggered SCR Description**

5.1.1 *Layout and simulated cross-section*

Figure 5-1 shows the layout view of the SCR used in this study. The background doping is Pwell in P- epi over a P+ substrate. The SCR consists of an input pad contacting P+ and N+ diffusions inside a Nwell. This input connection also contacts one end of the N+ diffusion resistor. The other end of the resistor leads to the internal circuitry, as well as to the drain of a grounded gate NMOS transistor. This is the structure that represents the ESD protection circuitry. The SCR triggers to protect the internal circuitry from high voltage damage or stress. Under normal operating conditions the circuit is in a high impedance state. Figure 5-2 shows the cross-section of the device. One

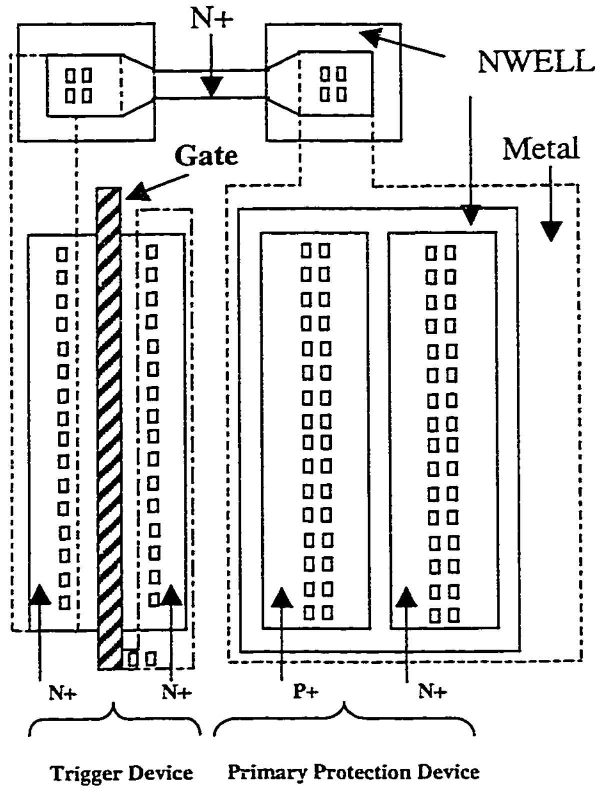


Figure 5-1. Layout view of the avalanche triggered SCR.

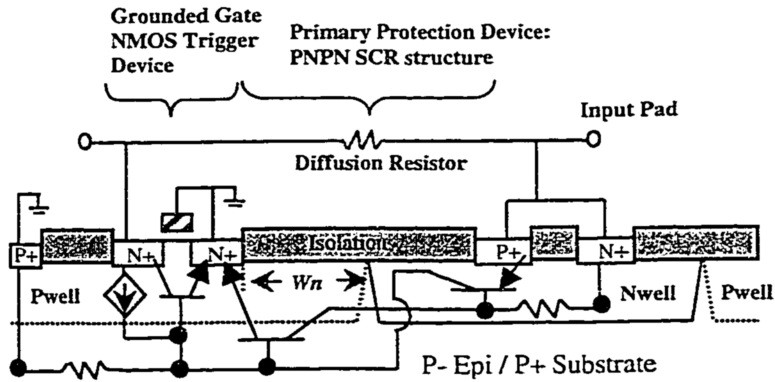


Figure 5-2. Cross-section view of the avalanche triggered SCR.

of the variables often considered is the spacing between the N+ emitter and the Nwell, which is the lateral NPN metallurgical basewidth. The effect of this spacing on the SCR characteristics will be summarized in this chapter. Figure 5-3 shows a 3-dimensional plot of the doping inside of the SCR structure.

5.2 SCR Curve Tracer Measurements

Figure 5-4 shows typical curve tracer results for avalanche triggered SCR's with different NPN basewidths. The drawn dimensions were 5, 10, 15, and 20μm with a 90% shrink applied at the actual mask pattern generation. The data were taken with the TEKTRONIX 577 curve tracer, with usually 25V or 100V maximum DC power supply and a load resistance of 120Ω or 500Ω.

Figure 5-5 shows an example of the most general I-V curve measured, with 7 regions of interest labeled A-G. The last region, G, is the point where the SCR turn-off occurs as the applied sweep voltage goes to 0V. Regions A-D and F can be observed clearly with the TCAD simulation results. With the smaller NPN basewidth structures, region E is not always observed. Essentially what happens is that the SCR has trouble reaching the trigger condition, and the I-V curve reaches the N+ resistor breakdown. From the discussion in Chapter 4, the NMOS portion of the structure has a stable holding point at about 10V. The resistor itself will typically start to enter avalanche breakdown when the high side terminal is at about 22V with respect to ground. These two curves are shown in Figure 5-6 for convenience. Referring back to Figure 5-5, it can be inferred by superposition that region E is due to this resistor breakdown. For shorter NPN

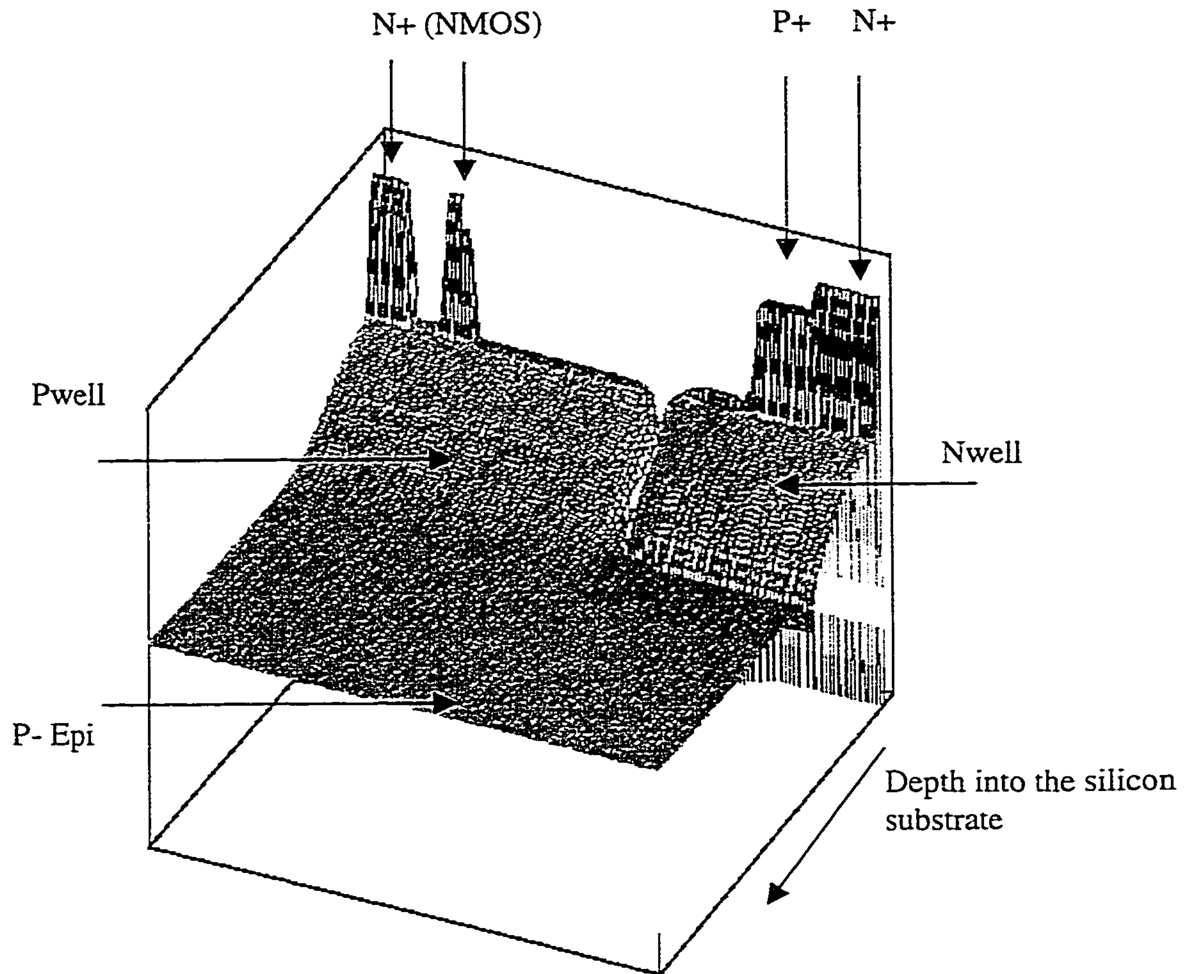
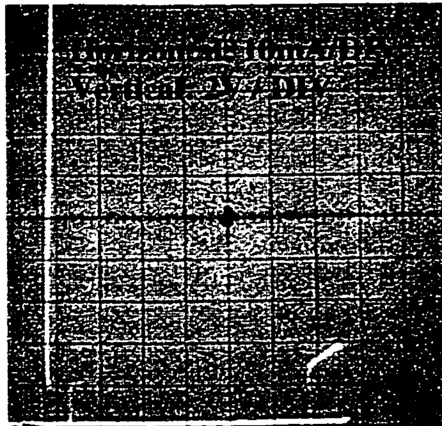
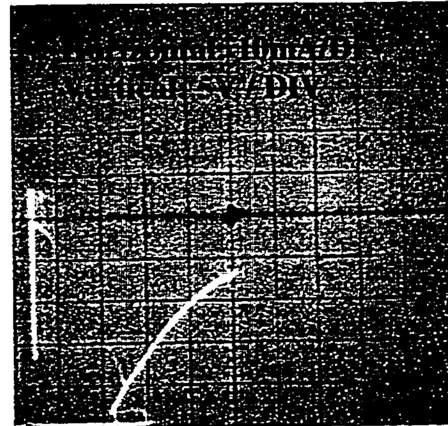


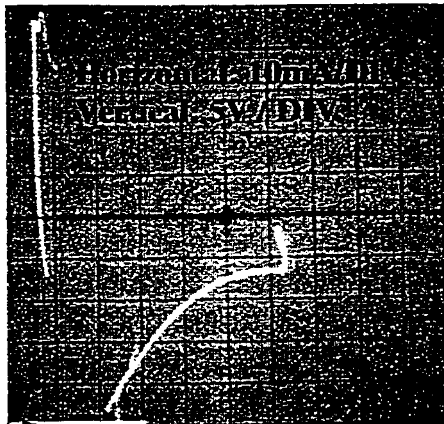
Figure 5-3. Doping profiles of the SCR, excluding the N+ resistor.



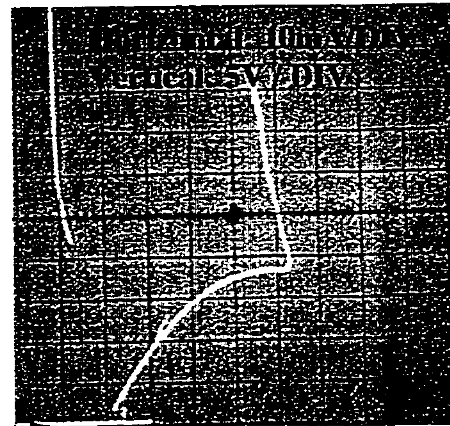
A. SCR_A: NPN BW=4.5um



B. SCR_B: NPN BW=9um



C. NPN BW=13.5um



D. NPN BW=18um

Figure 5-4. Avalanche triggered SCR characteristics for 4 different NPN basewidths. SPICE models for SCR_A and SCR_B above are the focus of this thesis.

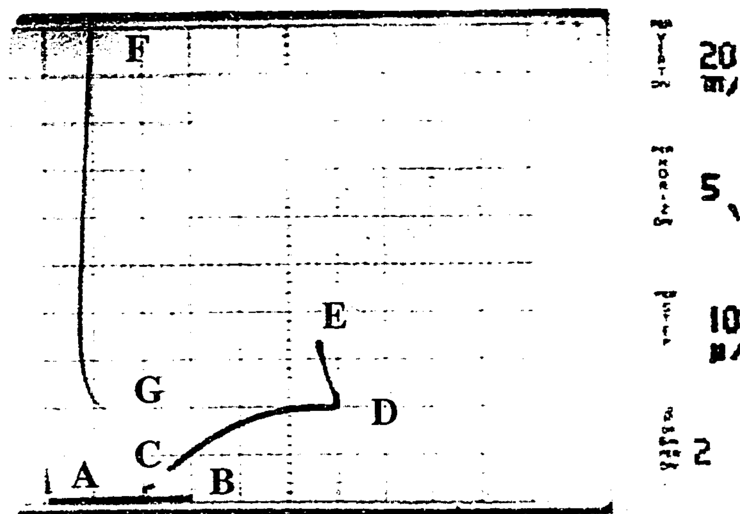
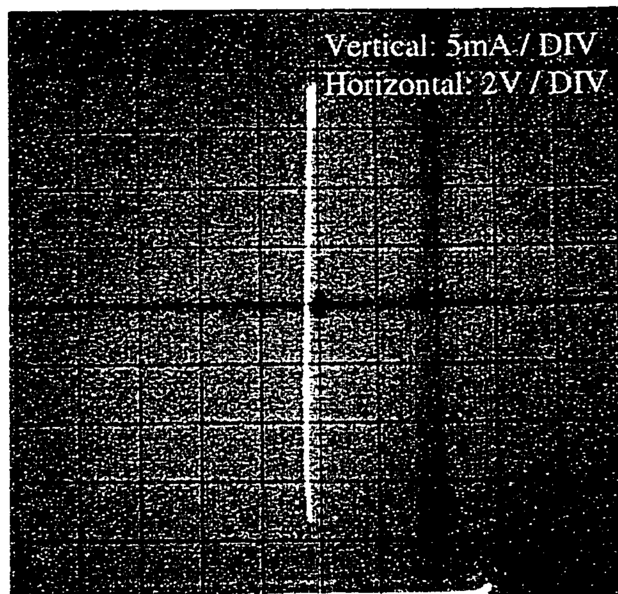
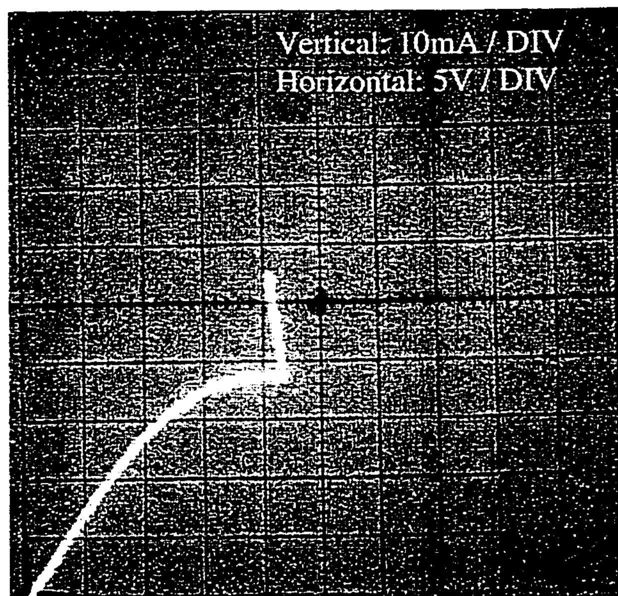


Figure 5-5. A general I-V curve for the avalanche triggered SCR, indicating the points of interest.



A. NMOS transistor high current I-V including snapack.



B. N+ Resistor I-V showing current saturation and avalanche breakdown.

Figure 5-6. High current characteristics of the NMOS transistor and the N+ resistor.

basewidths, the emitter injection efficiency for the lateral NPN is higher and the feedback mechanism leading to SCR triggering is more easily obtained. As the NPN basewidth increases, this feedback mechanism is less efficient, and it becomes more difficult to trigger the SCR. This "increasing difficulty" for triggering can be observed from the data by referring again to Figure 5-4. For NPN basewidths above 9µm, the resistor enters avalanche breakdown, increasing the majority carrier concentration in the P-well and substrate, initiating the latchup trigger. In addition, the data shows that the N+ resistor breakdown limits the maximum voltage seen by the input pad and input diffusions.

It should be pointed out that the original test module for these structures did not contain the isolated components; therefore, the different triggering characteristics observed between the structures with different NPN basewidths were not readily explainable. This simple example demonstrates the importance of having access to the circuit sub-components for measurement and analysis. In this case, having access to the individual bipolar structures and the N+ resistor made a big difference in understanding the measured SCR I-V data.

5.3 TCAD Simulation Results of the SCR and Physics Review

In Chapter 3, a generic discussion was presented giving an overview of the SCR operation. This section will present these details as gathered from the simulation results. Particular focus will be made on regions B-D and F, which are readily observable from the 2-dimensional simulation results. A more accurate simulation, in 3-dimensions, could demonstrate the avalanche breakdown effect observed for wide NPN basewidth

structures. As was seen in the previous section, that particular SCR did not trigger without observing N+ resistor breakdown. The 2-dimensional simulations will show that the wide basewidth structures indeed do not trigger.

In order to simulate the complex I-V behavior, the device simulation in MEDICI needs to include the use of a numerical method known as the "continuation" method, which allows MEDICI to trace difficult I-V characteristics, for example, negative resistance regions. As it is tracing through these portions of the I-V curve, it is continually adjusting a load resistor in the simulation. Because of this, and the fact that the N+ resistor is only approximated in this structure, the match with the silicon values are not perfect; however, despite an imperfect match, the simulator does trace out all of the key points on the SCR I-V curve. This allows us to understand the complex I-V behavior by studying the "internal views," that is, key physical parameters such as potentials and current density, at the different stages of the solution.

Figures 5-7 through 5-9 show the simulated I-V curves for 3 different SCR structures, identified by the NPN basewidth. The two smaller basewidths (4.5μm and 9μm) clearly show SCR triggering while the 13.5μm wide device does not trigger. It should be emphasized that this is consistent with the measurements, since the 13.5μm basewidth structure did not trigger until after the N+ resistor entered avalanche breakdown. This behavior is not observed in MEDICI since this would require a 3-dimensional simulation, of which MEDICI is not capable.

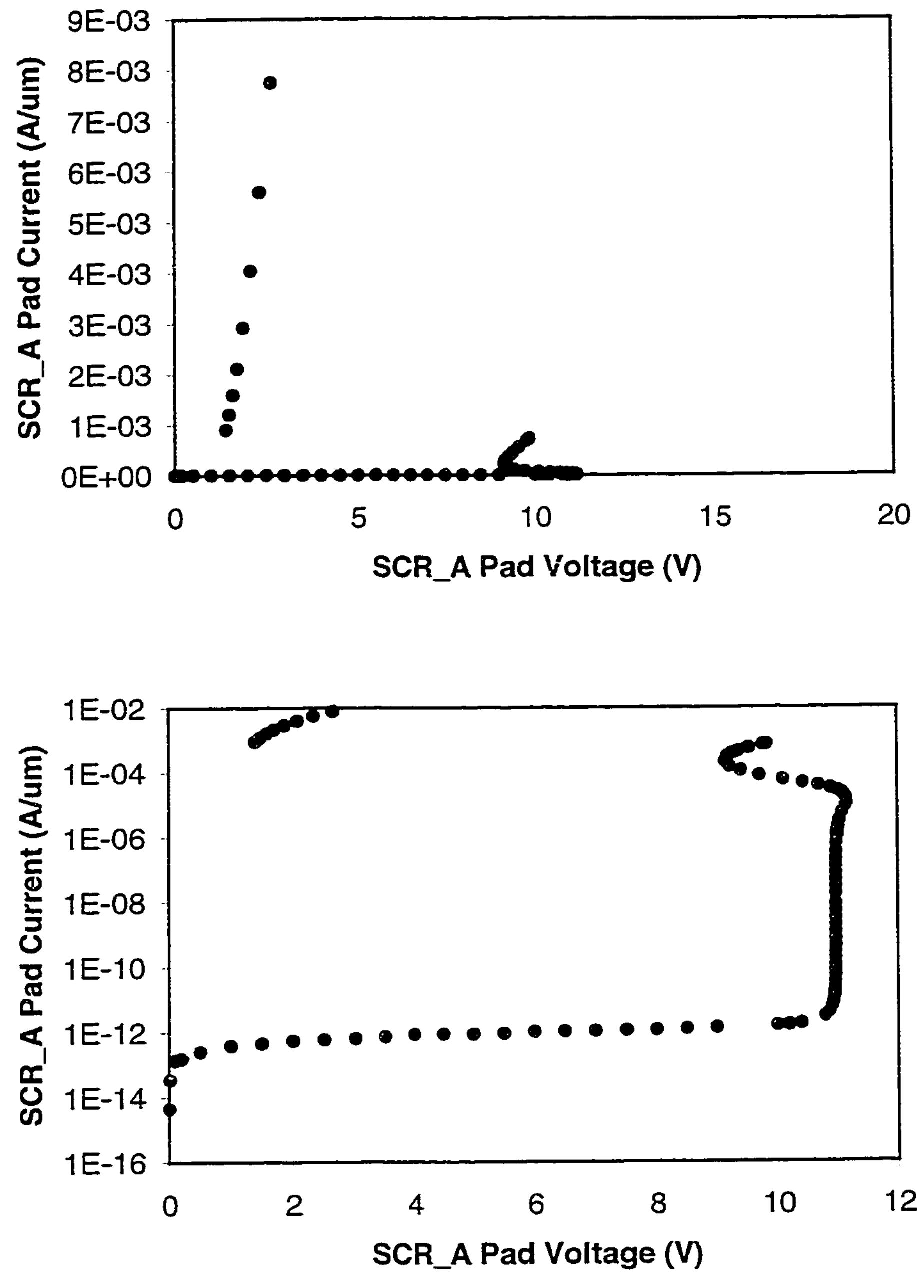


Figure 5-7. Linear and log scale MEDICI I-V simulation results for SCR_A.

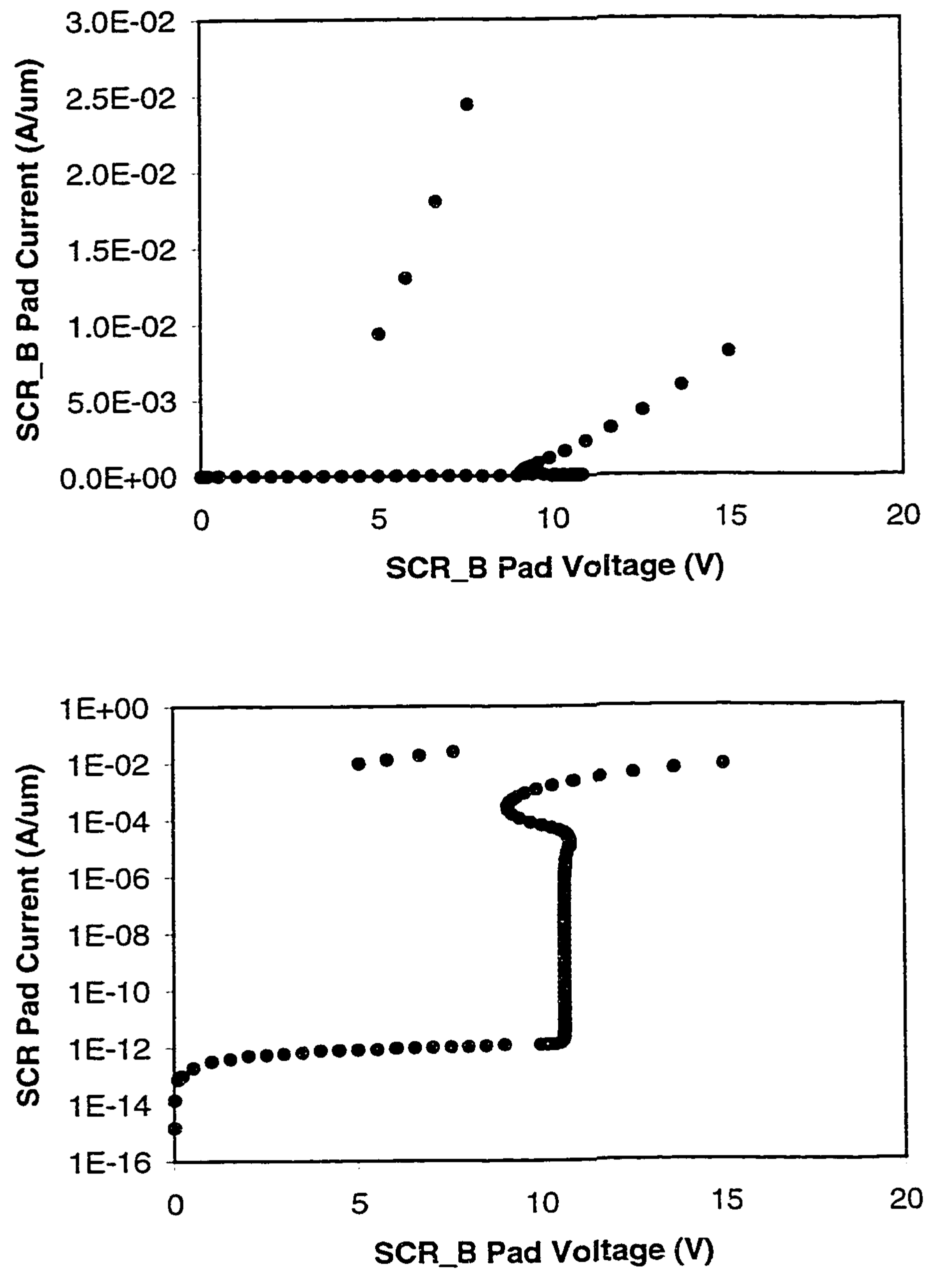
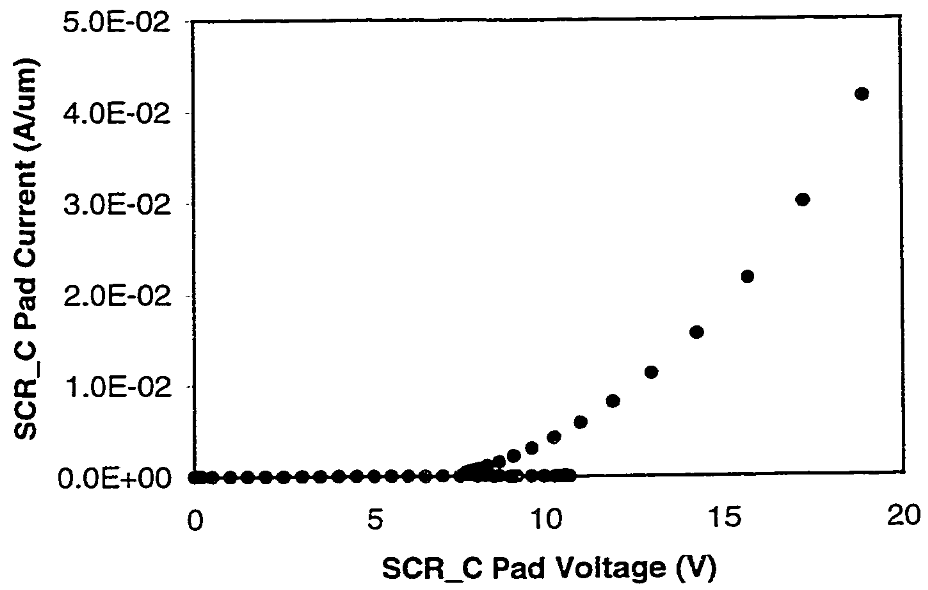


Figure 5-8. Linear and log scale MEDICI I-V simulation results for SCR_B.



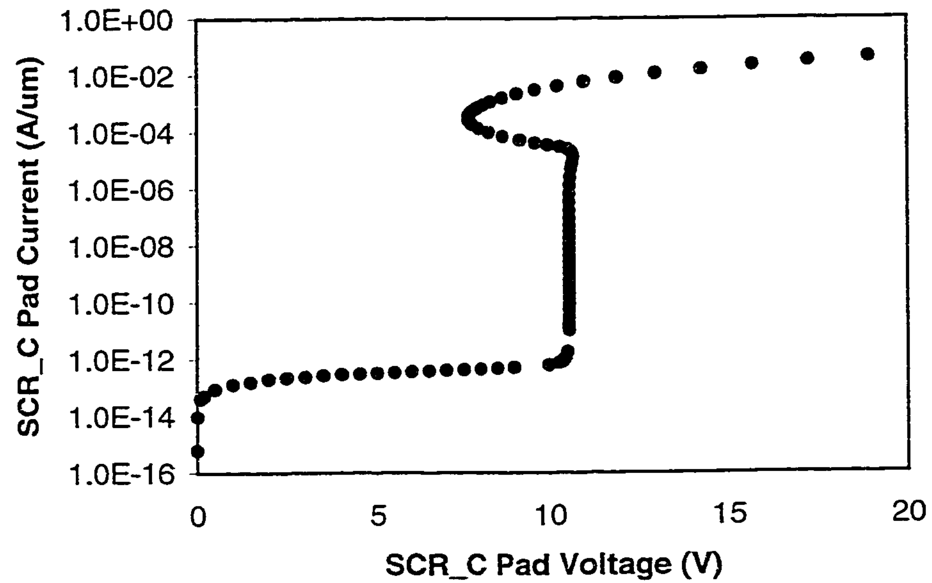


Figure 5-9. Linear and log scale MEDICI I-V simulation results for SCR_C, the SCR with 13.5um basewidth NPN.

As explained earlier, point A is where the SCR is completely in the "off" state and very little is happening in the structure. All of the diffused regions are basically behaving as reverse biased diodes at this point. Point B is where the NMOS enters the avalanche mode and physical quantities, such as the electric field and ionization rates, start to change dramatically. The following figures will show physical parameters of interest at each of the I-V points labeled B-D and F.

As a starting point, Figure 5-10 shows the potential distribution inside of the SCR structure as the DC sweep voltage is applied. The maximum potential on the scale is 20V in all cases. At point B, the NMOS device is in avalanche condition, and as a result, the potential gets pinned to about 10.5V while the current rises sharply. At C, the NMOS device is in the "snap-back" holding point; the potential at the input increases since there is a diffused resistor allowing the terminal potential to increase, even though the NMOS drain potential is held approximately constant. At point D, the PNP transistor is turning on, and the potential begins to drop to a low holding point, representing the latchup-state. This is shown on the plot representing point F.

Figure 5-11 shows the electric field, on a logarithmic scale, for these same four regions on the I-V curve. The electric field plots demonstrate the impact of the doping level on the field magnitude. For example, at point B of the I-V curve the potential is at 10V on both sides of the structure. Yet, the electric field is much higher on the left, since the field is dropped across a very small depletion region at the NMOS N+ drain/Pwell junction. On the right side of the structure, the 10V potential is dropped across the

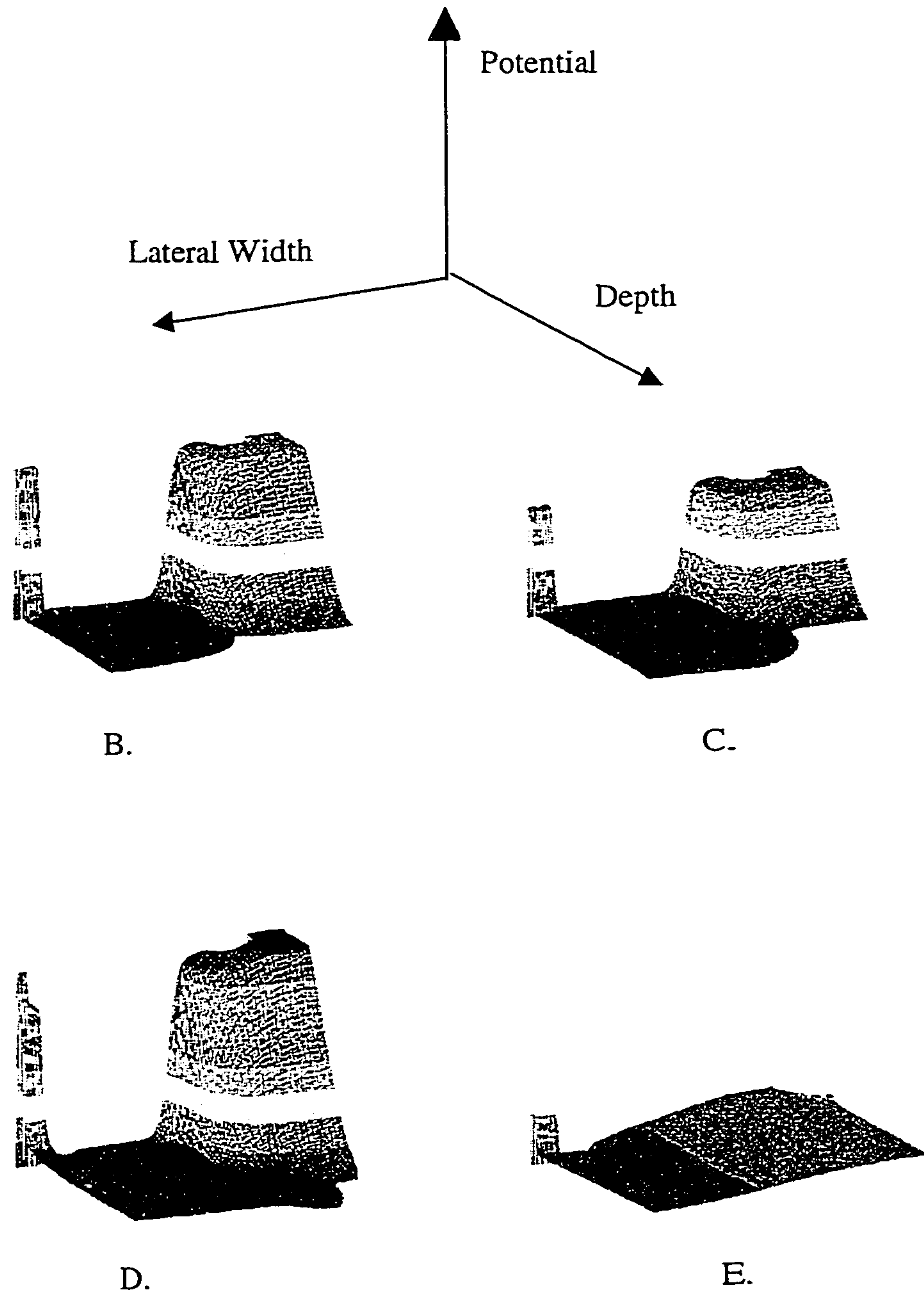


Figure 5-10. Relative potential distribution for the avalanche triggered SCR at key "turn-points" of the I-V characteristics, referenced by the letters under each plot.

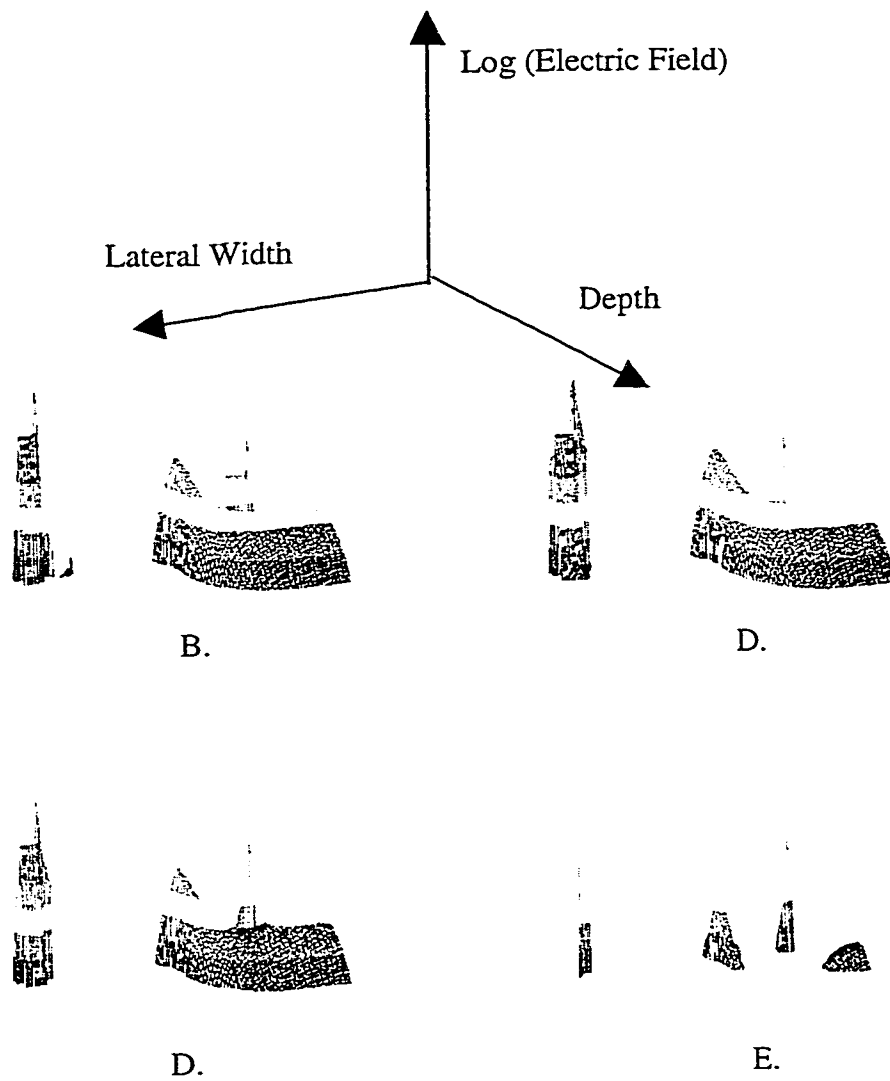


Figure 5-11. Electric field for the avalanche triggered SCR at the points of interest: B-E. The center junction gets forward biased as the device enters the latchup mode, reducing the electric field dramatically.

Nwell/Pwell junction. The lower doping levels in the wells lead to the reduced electric field.

The electron and hole generation rates, G_n and G_p, respectively, are calculated in MEDICI by the following equations,

$$G_n = \alpha_n \exp(-\frac{b_n}{E}) \qquad \text{Eq. 5-1}$$

$$G_p = \alpha_p \exp(-\frac{b_p}{E}) \qquad \text{Eq. 5-2}$$

where the calculated values represent the number of electron-hole pairs created due to impact ionization; α_n and α_p are the electron and hole ionization coefficients, respectively, in units of pairs per cm. Figure 5-12 shows the carrier generation rates due to impact ionization on a logarithmic scale. Clearly, the drain avalanche creates most of the excess carriers at point B on the I-V curve. The Pwell/Nwell junction shows some excess carrier generation, but at about two orders of magnitude below the drain.

Figure 5-13 shows the electron current density as the I-V curve traces through the different points of interest. This is perhaps one of the most important series of plots. Clearly, as the device reaches the NMOS snapback point, the lateral NPN transistor is also taking part in the conduction. It will be shown later that the PNP transistor in region C and C-D is not conducting yet. This information is critical for setting up the SPICE

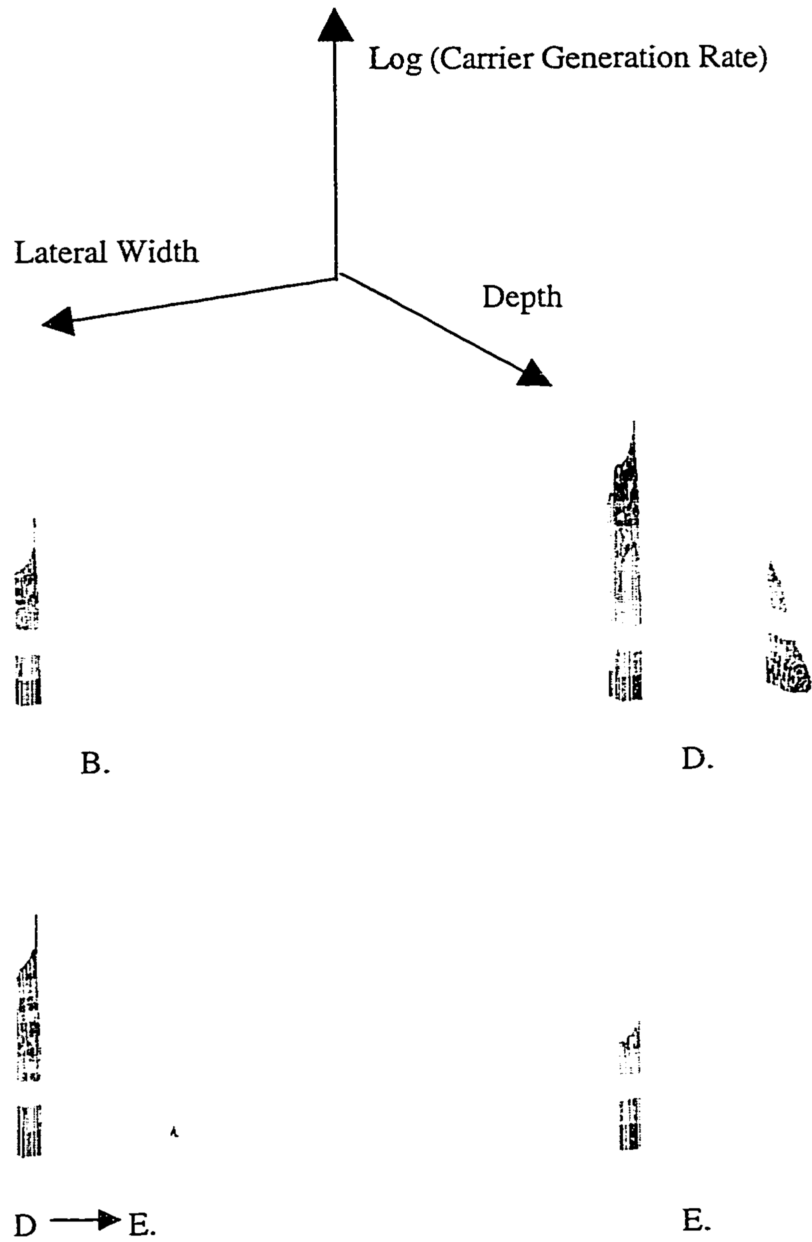


Figure 5-12. Carrier generation rates due to impact ionization for the avalanche triggered SCR at the points of interest: B-E.

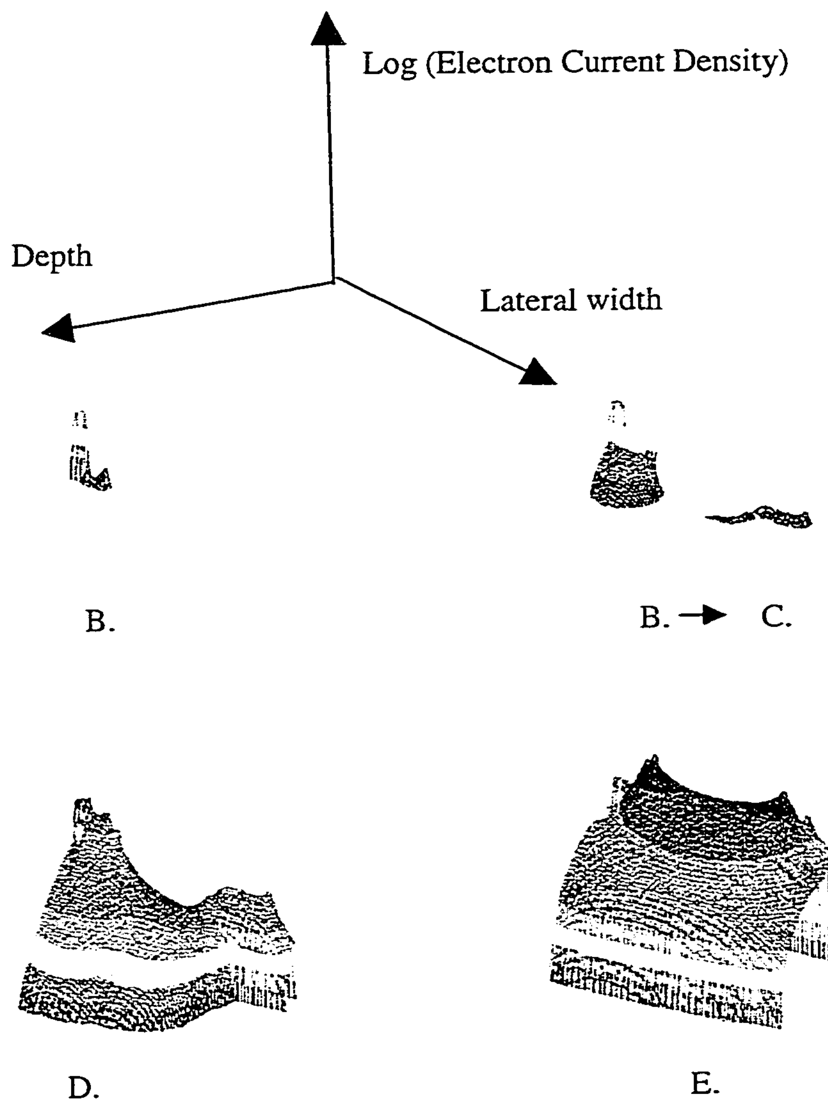


Figure 5-13. Electron current density for the avalanche triggered SCR showing the evolution of the electron current flow as the SCR transitions from snapback to latchup.

sub-circuit model correctly. The lateral NPN transistor starts to turn on as a result of the NMOS bipolar effect, since the NMOS N+ source diffusion starts to behave as an electron emitter for the lateral NPN transistor. This makes sense from Figure 5-11 and Figure 5-12, which show that at point C, there is a high reverse bias on the Nwell/Pwell junction, and therefore an electric field capable of sweeping any electrons near that junction into the Nwell region. The reverse biased Nwell/Pwell junction is behaving as an NPN collector-base junction, encouraging the lateral bipolar behavior, causing a portion of the emitted electrons to drift into the N+/Nwell contact.

Figure 5-14 shows the hole current density. It clearly shows that the PNP transistor does not turn on until the SCR reaches point D in the I-V curve, just prior to latchup triggering. This series of simulated results therefore explicitly indicate the SCR triggering dynamics. The NMOS transistor reaches avalanche breakdown, and starts to enter a parasitic bipolar mode. Under these conditions, the NMOS source diffusion behaves as an electron emitter and some of these electrons drift across the Nwell/Pwell junction, which has a reverse bias and therefore acts as a NPN collector. This lateral NPN current flow forward biases the Nwell/P+ junction, triggering the PNP transistor to turn on, and leading to regenerative feedback, which causes the latchup-state.

Figure 5-15 shows the electron concentration and the different I-V points, and Figure 5-16 shows the hole concentration. These last two series of plots show that indeed, regenerative feedback is occurring, allowing the carrier concentrations to increase above the background level. This condition is known as conductivity modulation since the substrate contains equal amounts of excess electron and hole concentrations.

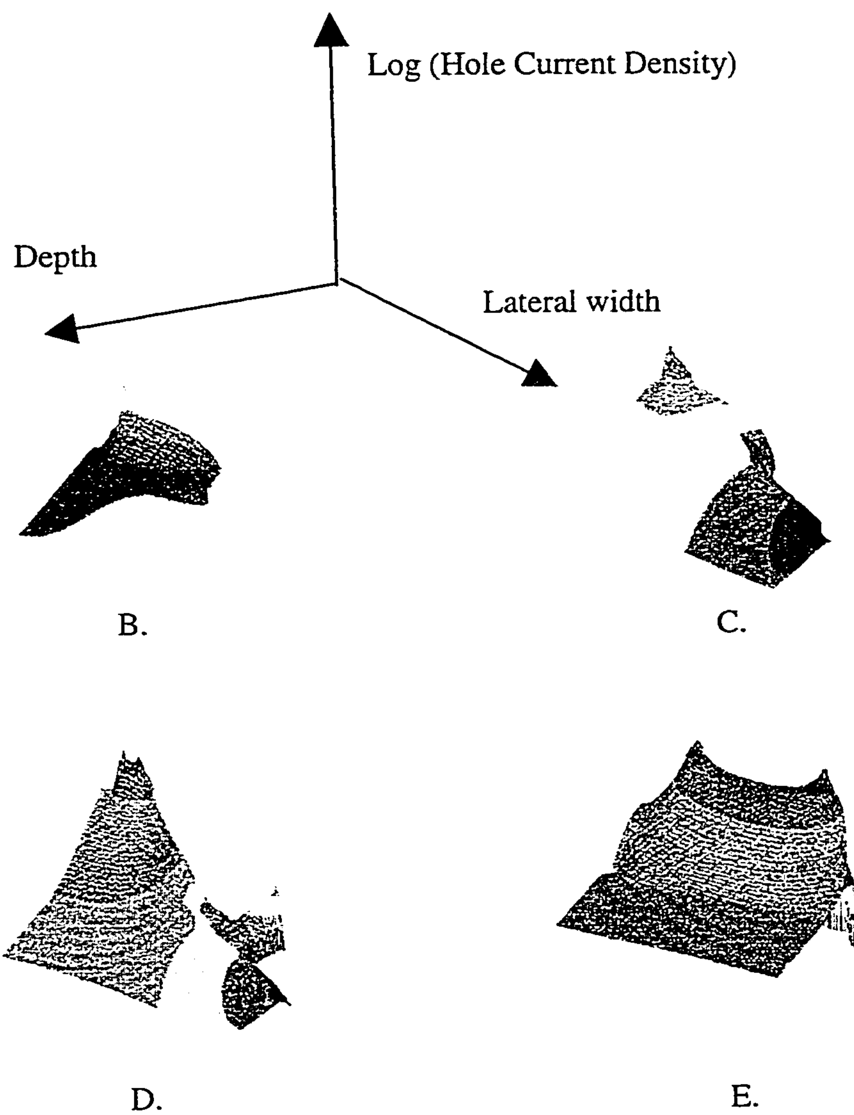


Figure 5-14. Hole current density showing the PNP transistor is the last component to "turn-on," triggering the SCR latchup.

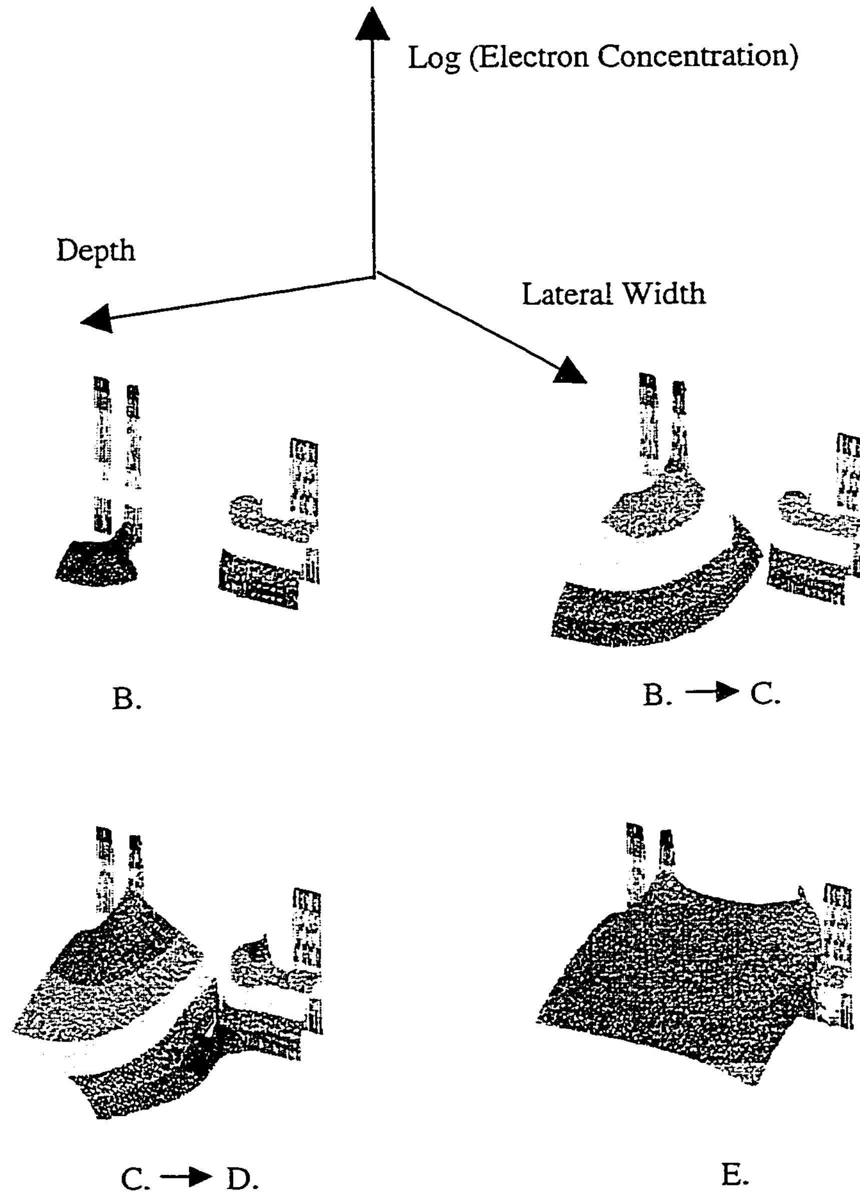


Figure 5-15. Electron concentration for the avalanche triggered SCR at the points of interest: B-E.

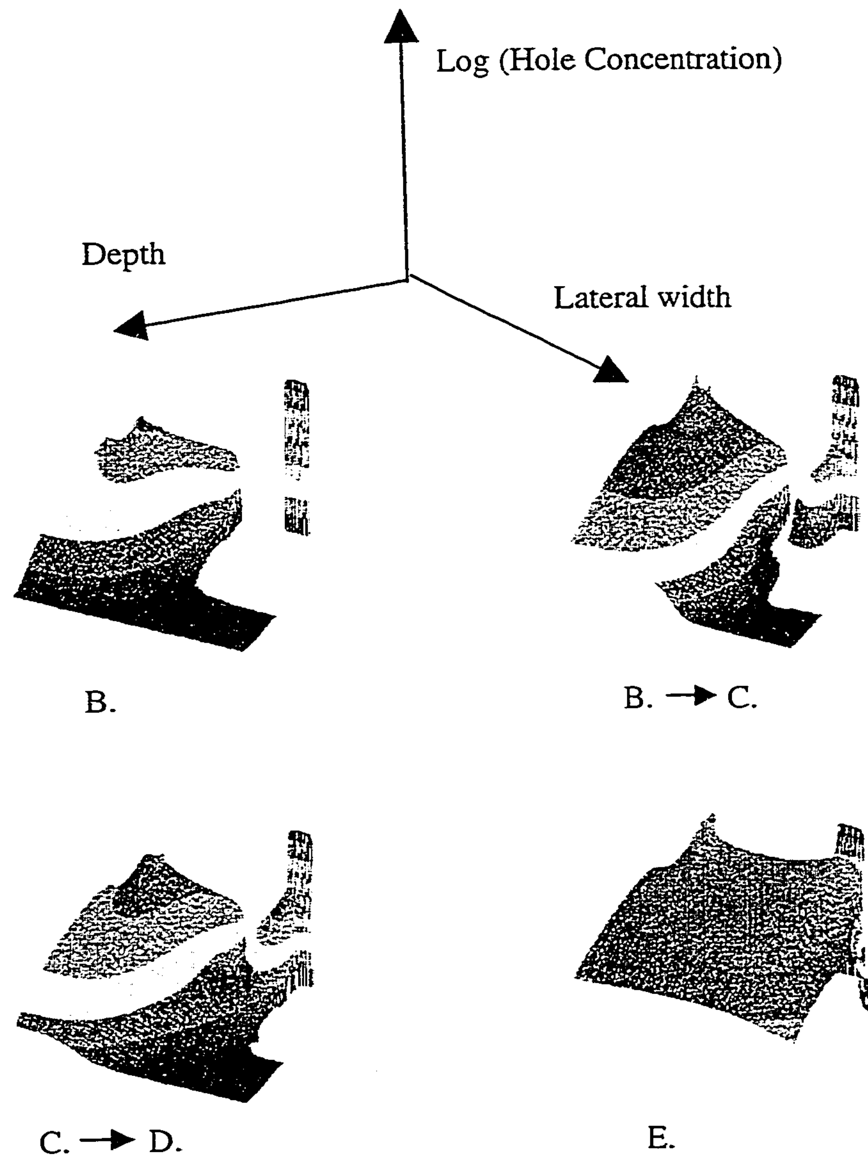


Figure 5-16. Hole concentration plots at key stages in the I-V simulation.

These results demonstrate the intrinsic value of the simulations. First of all, the simulated DC sweep contains all of the points of interest on the I-V results as was measured on actual devices with a curve tracer. This is possible because we are able to solve for the avalanche breakdown of the NMOS transistor, and with the use of the continuation numerical method, can observe the parasitic bipolar effect in the MOS device. The diffusion resistor added to simulate part of the N+ resistor in the actual structure allows the potential to increase while the NMOS drain is at its stable bipolar holding point. Most importantly of all, the I-V sweep demonstrates that at some high potential above the MOS holding point, the structure can enter into the latchup mode.

By examining the regions of interest using the simulation solutions, we are able to explicitly understand the SCR behavior leading to latchup triggering. These results were extremely important for setting up the SPICE sub-circuit model. In order for the SPICE model to be accurate, it needs to demonstrate the same triggering dynamics observed in the TCAD results: the NMOS enters avalanche and bipolar mode – the lateral NPN turns on – the PNP turns on – leading to regenerative bipolar feedback and latchup.

For further comparison, Figures 5-17, 5-18, and 5-19 show the current densities, carrier concentrations, electric field, and potential distribution for the case in which latchup does not occur. As can be clearly seen, even though the NMOS is in bipolar mode, the lateral NPN is conducting, and the PNP is turned on, the center junction remains reverse biased and therefore latchup does not occur. This is consistent with literature references demonstrating that while both bipolar devices conducting is a necessary condition for latchup, it is not a sufficient condition [42] [43]. The condition

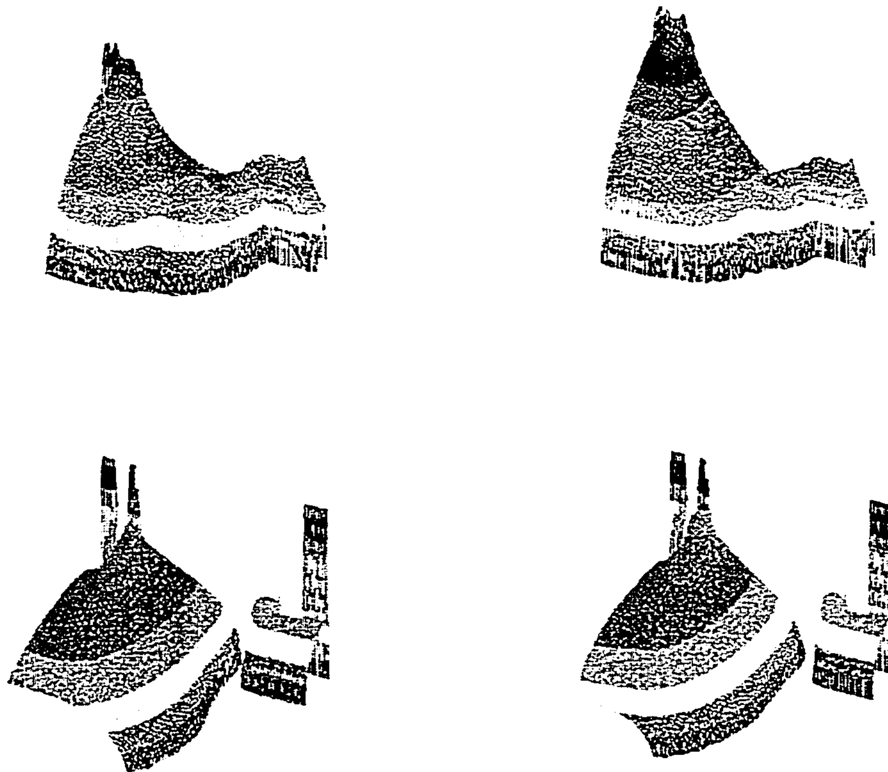


Figure 5-17. Electron current density (top) and excess electron concentration for SCR_C at high pad voltage conditions. This SCR did not trigger into the latchup state.

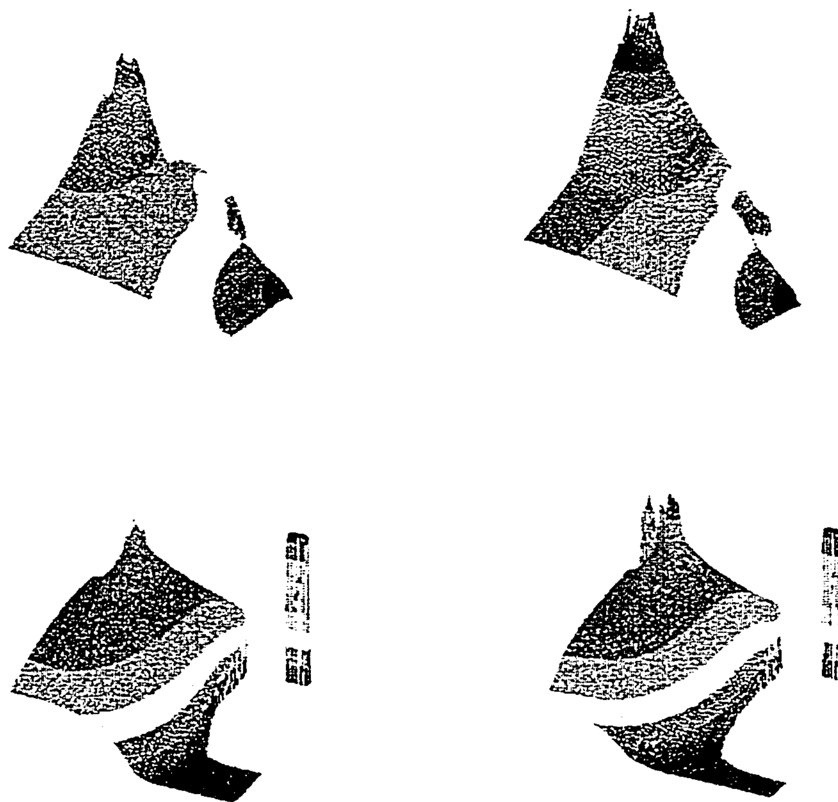


Figure 5-18. Hole current density (top) and hole concentration at high pad voltages for SCR_C, which did not trigger into latchup.

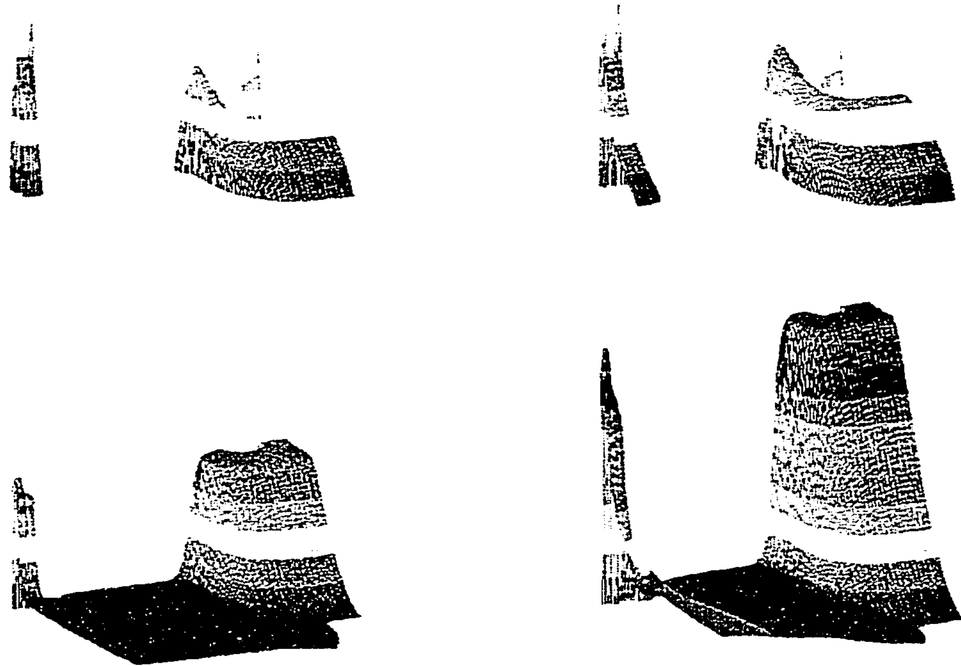


Figure 5-19. Electric field (top) and potential distribution for SCR_C, at high pad voltage levels, showing the middle junction is still reverse biased, therefore latchup does not occur.

that must be met for latchup to occur is that the current through the structure must reach the switching current value.

The effect of the NPN basewidth can also be viewed from the basic transistor parameters. The classical latchup condition is that the sum of the PNP and NPN alpha parameters be equal to or greater than one. For an SCR, the anode (pad) current can be derived as

$$I_A = \frac{I_S}{1-\alpha_{npn} - a_{pnp}}, \qquad \text{Eq. 5-3}$$

where I_s refers to the reverse biased diode leakage current due to the center reverse biased junction. The effect of the NPN basewidth on the common base current gain, α, is easily obtained from the Gummel plot data. Figure 5-20 shows the current gain of the 3 NPN transistors as a function of basewidth. Clearly, the 13.5μm basewidth NPN transistor has a very low gain at high injection, and its ability to create regenerative bipolar feedback is poor.

5.4 Avalanche-Triggered SCR SPICE Sub-Circuit Model and Simulation Results

The TCAD results demonstrated qualitatively how the avalanche triggered SCR device operates. All of the features of the SCR terminal characteristics were obtained by the TCAD simulations: NMOS avalanche, bipolar mode, and finally, the pad voltage increase until latchup was triggered in the structure. From the "internal views," we were

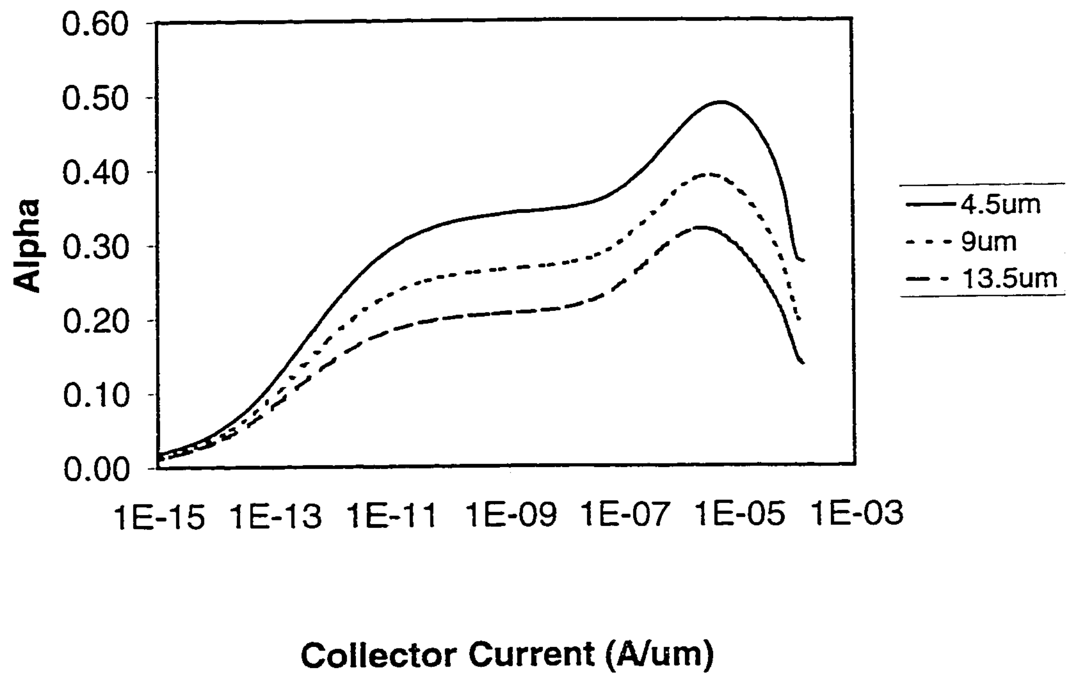


Figure 5-20. Common base current gain for the 3 different NPN transistors.

able to explicitly comprehend the contribution of each of the individual components to the overall SCR operation.

Additionally, the special structures designed to characterize and analyze the individual components on silicon were also helpful. For example, we were able to characterize the N+ resistor structure and see how its terminal behavior impacted the SCR. By having access to silicon structures, we were able to understand the components' terminal I-V behavior and their role in the SCR operation. The effects of the resistor, including saturation and breakdown, would have been visible in a 3-dimensional simulation.

Figure 5-21 shows the SPICE sub-circuit model for this structure. It should be noted that this representation has gone through several iterations. For example, initially the N+ resistor was included as a constant value (which was determined by the geometry), and there was no avalanche diode associated with it. Later, an avalanche diode was included, but it still was considered a constant valued resistor. This final schematic came after considering the 3-d effects associated with this resistor, and its current saturation effect.

The resistor "R" in the model is included to help model the bias dependent resistance observed from the measurements. Other researchers have used a similar resistor, but it has been considered a constant previously. The base resistor, "RB," was extracted from fitting done on the NMOS breakdown and snapback model. The collector resistance, "RC," was calculated using the Nwell sheet resistance. For example, the dimensions of that particular resistor are W ~ 90um and L ~ 12um. This gives a L/W

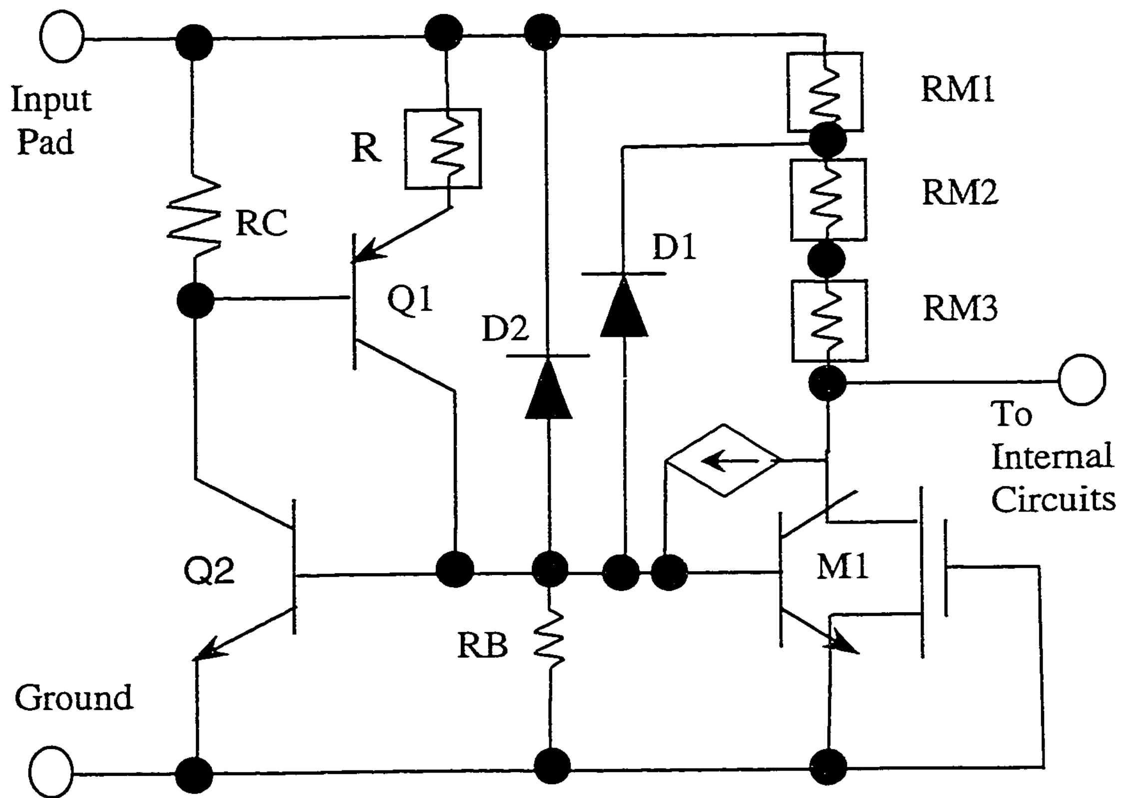


Figure 5-21. The SPICE sub-circuit model for the avalanche triggered SCR.

value (number of squares for a diffused resistor) of ~0.1333. The typical N-well sheet resistance is ~800 Ω/square, giving a typical value for Rc of about 110Ω. This parameter has an important impact on the SCR triggering characteristics, as will be shown later.

5.4.1 *SPICE Simulation of the SCR Steady State Triggering Characteristics*

The SPICE simulations were run to mimic the data measured with the curve tracer. Figure 5-22 shows the circuit that was simulated in SPICE. Simulating the SCR triggering with a trapezoidal pulse allows us to see important characteristics such as the triggering current and voltage, the maximum current allowed by the series resistor and the SCR turn-off characteristics such as the minimum holding voltage and current, which are important parameters. The SCR "holding characteristics" would not be observable from a DC sweep that ramps from 0V to some maximum value.

Figure 5-23 shows the simulation result for SCR_A, which has the NPN with the 4.5um basewidth. This can be compared to the data shown in Figure 5-4A. Figure 5-24 shows the result for the 9um basewidth NPN structure. Again, refer to Figure 5-4B for comparison with the measurement. These simulation results show excellent agreement with the measurements. The pulses applied in the simulation were on the order of milliseconds, with microsecond rise times. Figure 5-25 shows some overall SPICE model performance, namely the trigger current, against typical measured data from different wafers. In general, the SPICE results are within the distribution of several devices. The triggering voltage result against measured data is shown in Figure 5-26. SCR_B is

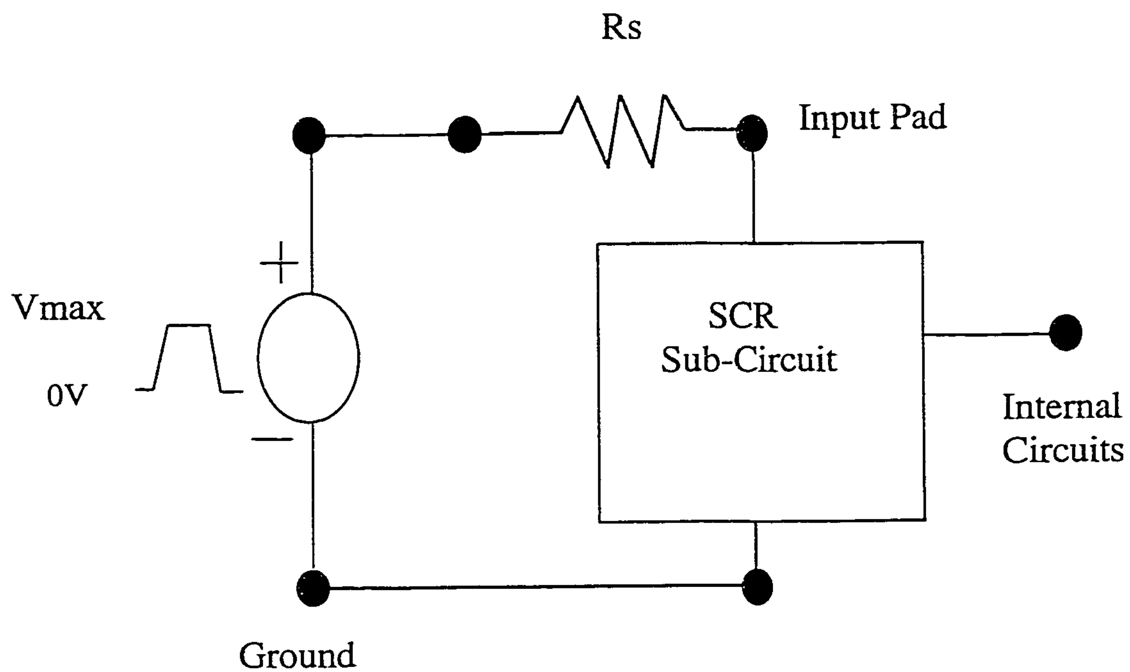


Figure 5-22. SPICE circuit used to simulate the steady state triggering characteristics of the SCR.

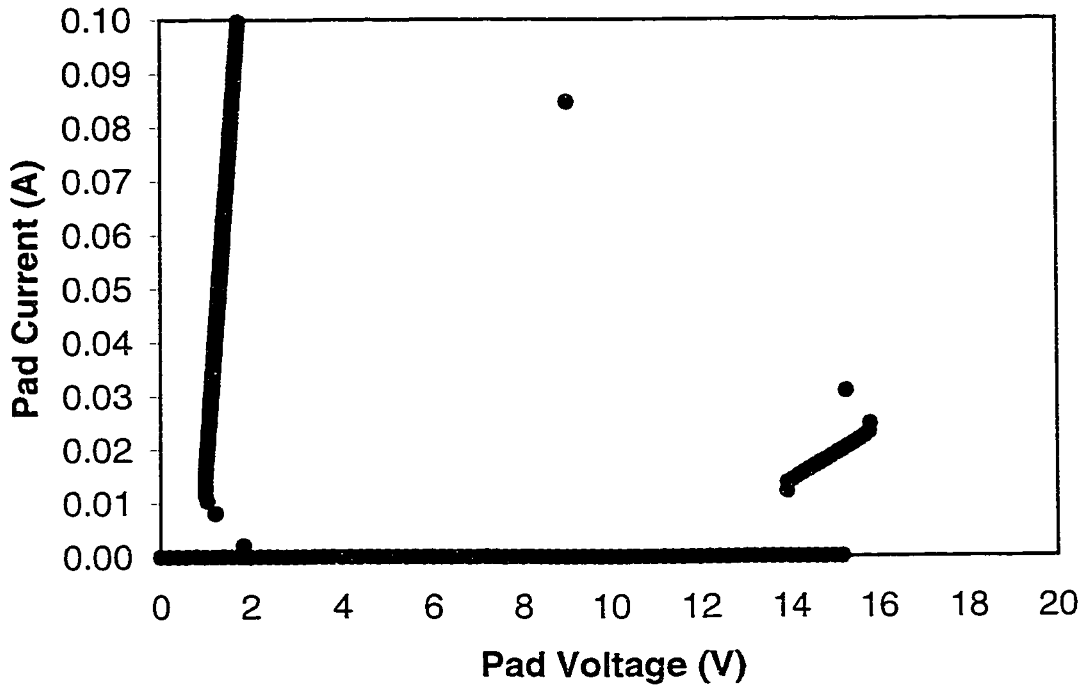


Figure 5-23. SPICE steady state triggering simulation of SCR_A, with NPN basewidth=4.5μm.

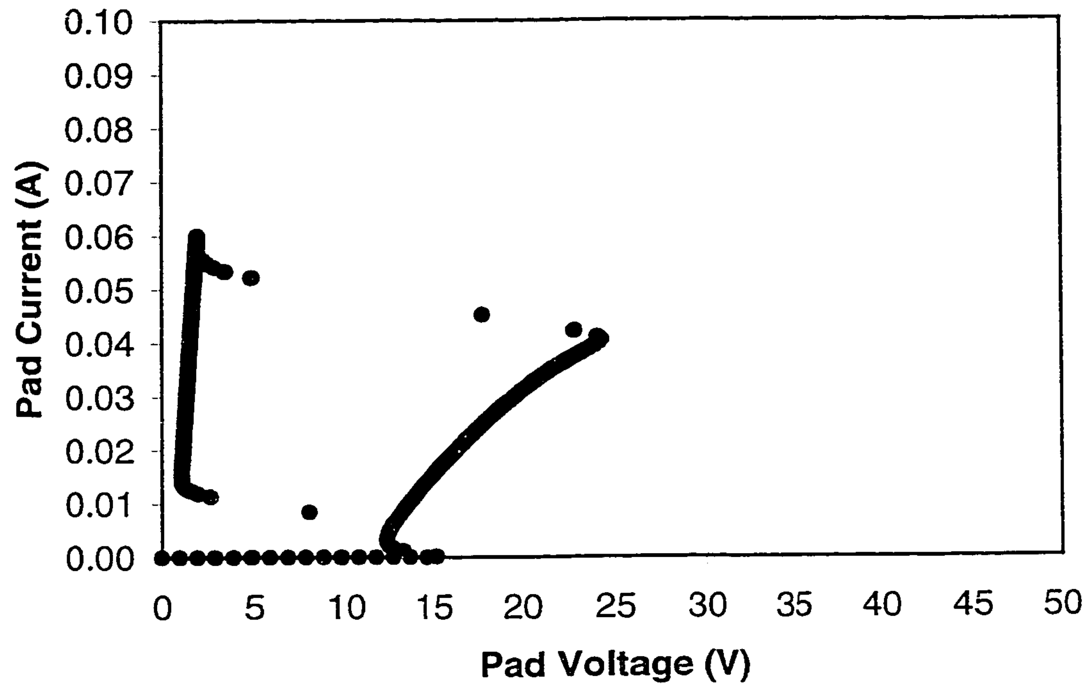


Figure 5-24. SPICE steady state triggering simulation of SCR_B (NPN basewidth=9μm).

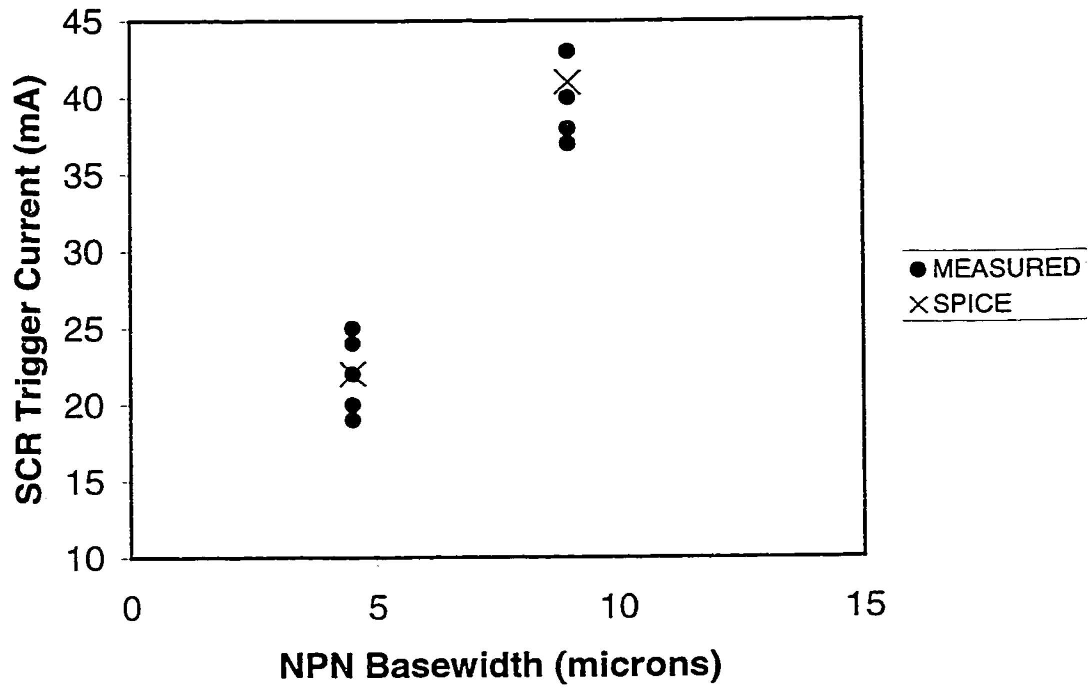


Figure 5-25. Simulated triggering currents compared against typical measured data.

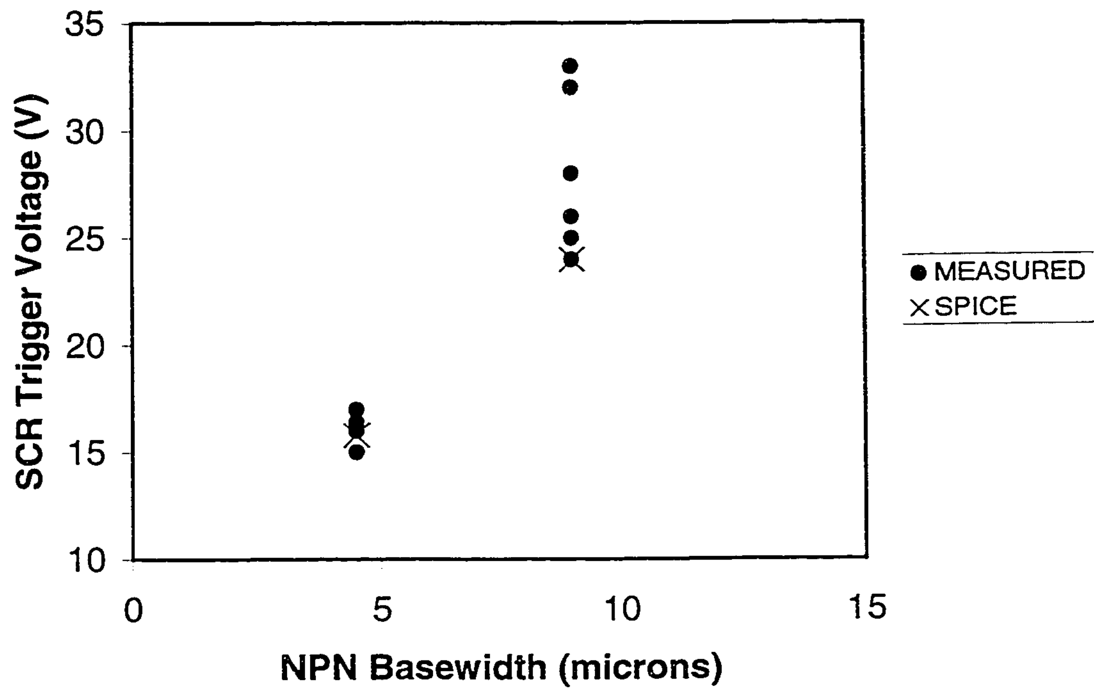


Figure 5-26. Simulated triggering voltage compared with typical measured data.

towards the bottom of the triggering voltage distribution, while SCR_A is near the middle of the data.

5.4.2 *Sensitivity Analysis*

SCR_A and SCR_B SPICE simulations were further run with some intentional variations on the RB and RC values in the model. Each of the two resistor nominal model values was varied by +/- 20% while the other remained constant. Both were also allowed to be at +20%, both were allowed to be at –20%, and finally, one set of runs was for the case of an essentially infinite RB value, for example, a floating substrate. Figure 5-27 shows the impact of these simulations on the triggering current. One of the conclusions is that the RC value seems to swing the current more than RB. For example, the higher trigger currents are due to low RC values, whereas the lowest triggering currents tend to be for the case of high RC.

Figure 5-28 shows the same set of experiment results on the trigger voltage. The first thing that is clear is that the wider base NPN device is much more sensitive to changes in the resistor values than the smaller device. Secondly, most of the variation is again dictated primarily by the RC value. Higher RC leads to a lower triggering voltage, while a lower RC leads to a higher triggering voltage. These simulation results show good consistency with the measured data, since the wider base device tended to have more spread in the trigger voltage than did the smaller device.

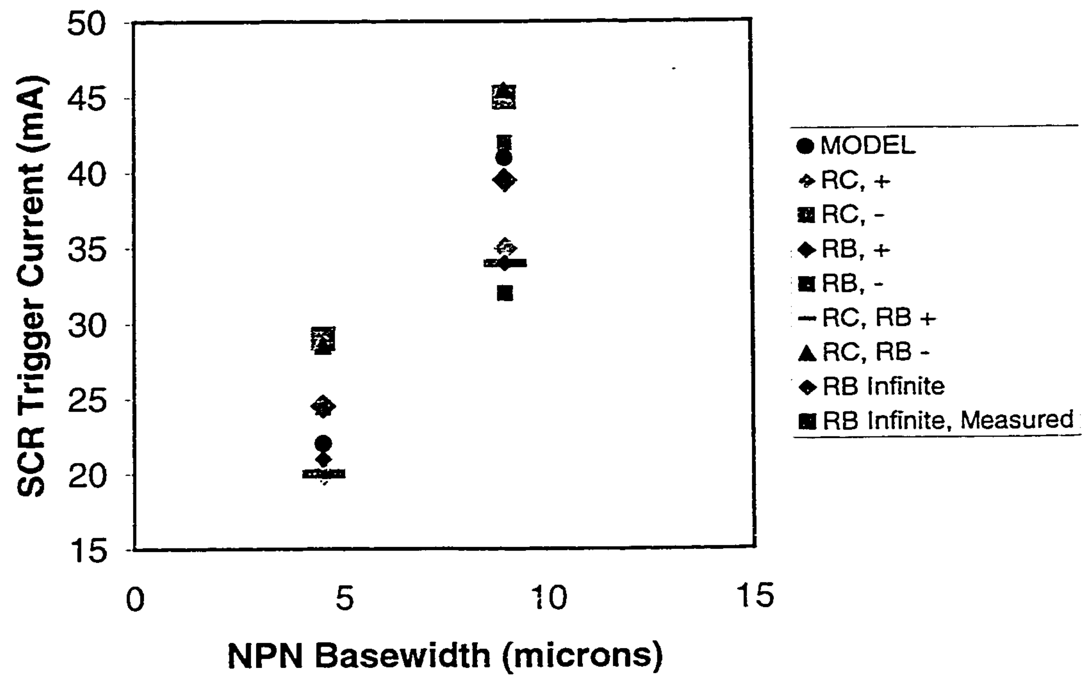


Figure 5-27. Sensitivity analysis shows the impact of 20% change of RC or RB on the triggering current value.

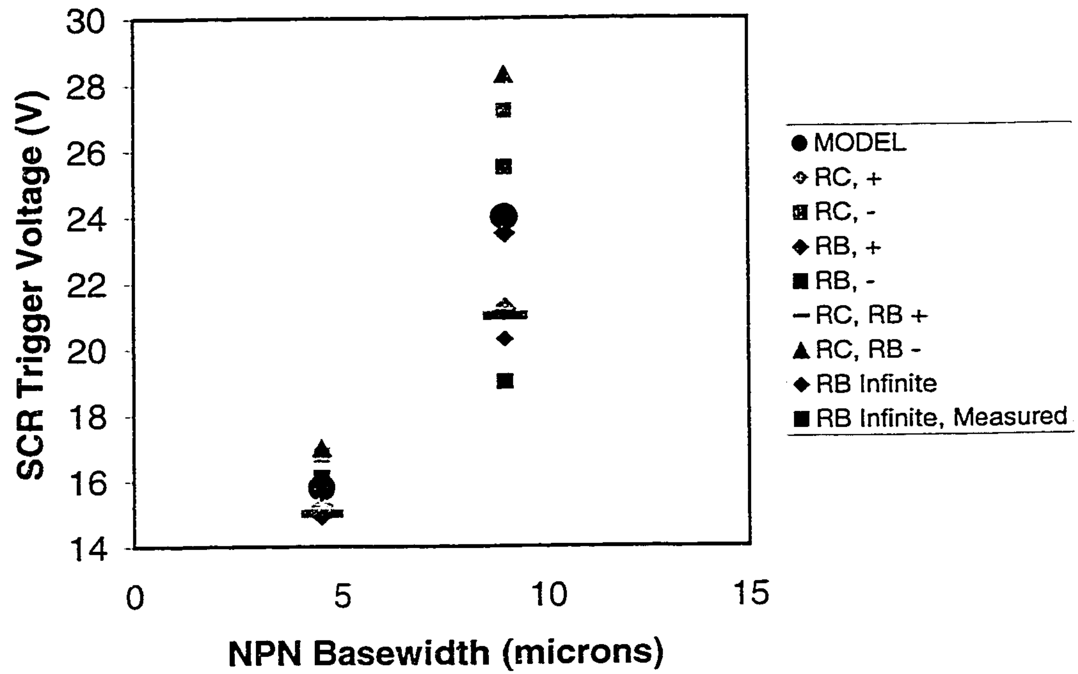


Figure 5-28. Sensitivity analysis shows the impact of 20% change in RC or RB on the triggering voltage. The small basewidth SCR triggering voltage is much less sensitive than the large basewidth SCR.

5.4.3 *High Current Characteristics*

DC simulations were run of SCR_A to generate the high current I-V characteristic, and compare it to measured results, both steady state and transient. Figure 5-29 shows the high current behavior, including a plot showing the resistance of the SCR as it transitions from the low current to high current state. This "on-resistance" clearly has a bias dependence, and it is for this reason that the resistor R, which approximates this value in the model, is modeled with a bias dependence. This bias dependence is not unreasonable. As the SCR enters into a high current state, the substrate gets more heavily conductivity modulated, meaning that the excess carrier concentration continues to increase, and this leads to a lower resistance. The value saturates due to the series resistance present in the test structure (metal pads and metal routing).

5.5 **Summary and Conclusions**

In this chapter, all of the important pieces needed to understand the avalanche triggered SCR operation have been reviewed. First and foremost, the TCAD data provided insight that could not be obtained by any other method. There were some limitations in SCR data that could be extracted from TCAD due to the 3-dimensional effects. However, including some resistance in the input pad of the drain structure resulted in terminal characteristics that contained all of the features we measured on the silicon structures.

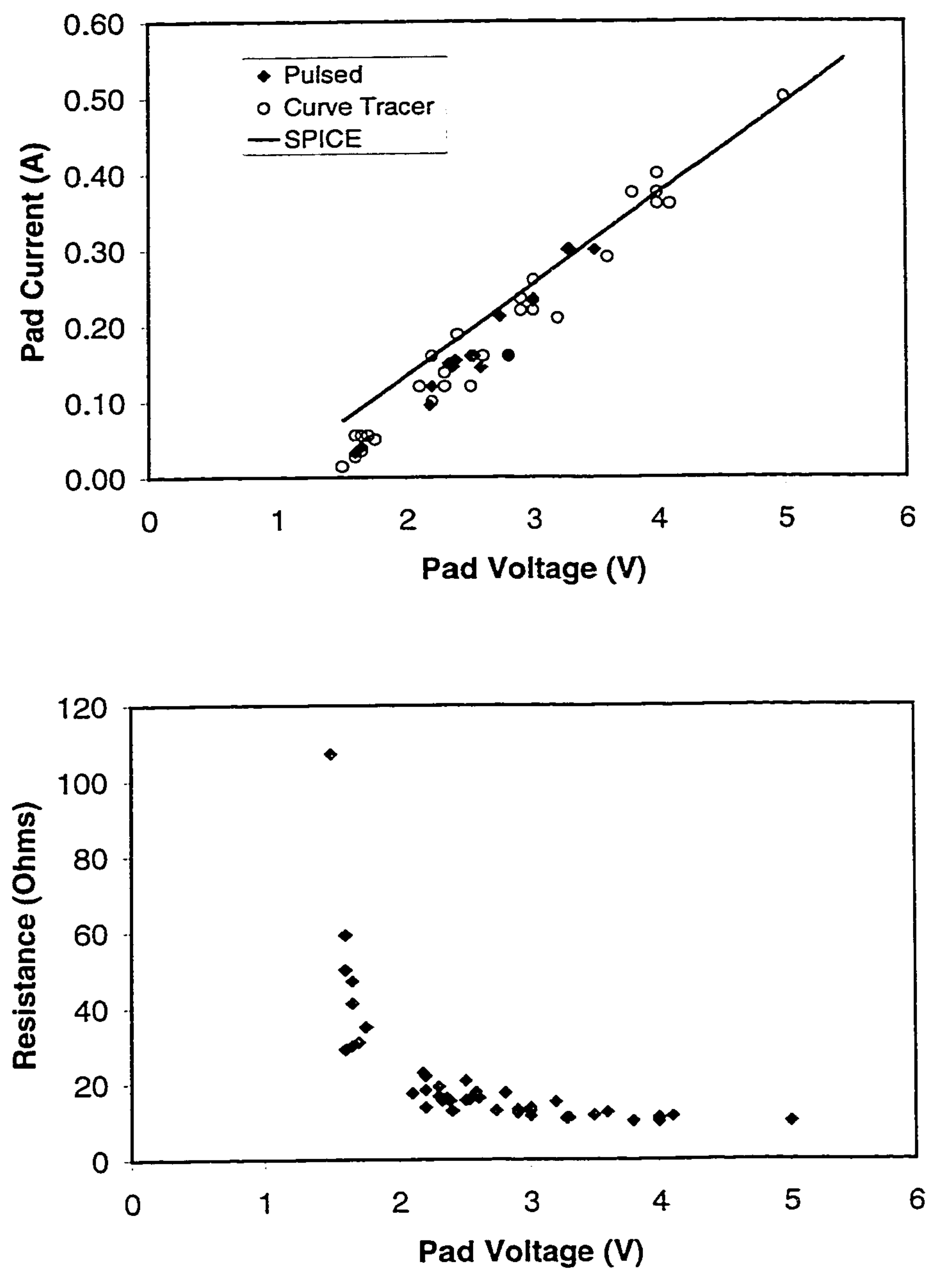


Figure 5-29. The high current characteristics of the SCR. The bias dependent on resistance saturates near 8Ω at very high currents.

Secondly, the internal component simulations gave good results, since the TCAD results showed that the widest structure, the one with the 13.5um wide base, would not trigger due to the low common base gain of that NPN transistor. The curve tracer measurements showed that indeed, that structure does not trigger, and it requires the "aid" of the N+ resistor entering the avalanche breakdown mode in order to trigger. In this mode, excess holes are being injected into the P-substrate providing more current for the PNP transistor, allowing the switching current necessary for latchup to be reached.

The TCAD tools indicated which structures could trigger into latchup, and which ones could not. Finally, for the structures that did trigger, the "internal views," which are the physical parameters such as current density and carrier concentration obtained from the simulated solutions, gave insight as to which components were participating in the conduction at strategic points along the I-V characteristics. These internal views showed explicitly what devices were being "turned-on" as the voltage was raised. This information helped in setting up the sub-circuit model pieces needed for SPICE. In addition to the TCAD, the bench measurements were critical, as in the example of the N+ resistor, for comprehending all of the circuit elements correctly in the SPICE sub-circuit model.

The SPICE results for the steady state operation of the SCR show that the model accurately gives the terminal characteristics observed in the measurements. The results for both NPN structures are in very good agreement with typical measured data.

CHAPTER 6

TRANSIENT OPERATION OF THE AVALANCHE TRIGGERED SCR

The previous chapter presented the sub-circuit model for the avalanche triggered SCR. As was shown in the previous chapters, the final version of the SPICE model required detailed analysis at the component level. The analysis was completed using both TCAD simulations and detailed measurements on specially designed silicon test structures. The SPICE model proposed for the structure demonstrated very accurate steady state triggering and latchup behavior. This chapter will present the application of the model to the transient excitation case.

6.1 Motivation

The main purpose of this research is to provide an approach for accurately modeling the circuit level response of an ESD circuit at the chip level. The actual discharges that need to be suppressed by the protection circuit have a rise time on the order of 10 nanoseconds. A good model should therefore have accurate prediction in the fast rise time triggering domain. Particularly important are the confirmation of the physics and the model capability on these short time scales. Ultimately, however, the steady state conditions are also very important, since once the SCR triggers into latchup the I-V characteristic resembles the steady state condition. The approach being proposed in this thesis is that the steady state triggering and transient triggering are two important

ways of validating a SPICE model for a complex circuit such as the avalanche triggered SCR.

6.1.1 *Preparing for the transient measurements*

Before any experiments were carried out, several things had to occur. First of all, transient tests are carried out with packaged units due to the hardware involved in carrying out the experiments. Figure 6-1 shows the characterization effort that was necessary in order to get the parts packaged. Essentially, the packaged parts had to have known characteristics in order to compare to models and simulations later. In addition to the detailed wafer level analysis, a mapping from wafer level test pads to the pins on the package had to be provided and documented for later use.

6.1.2 *Transient Measurements Setup*

In order to validate the model under very short time scales, transient measurements were made using a HP pulse generator (HP214A) capable of providing 10 nanosecond scale rise time pulses. The schematic for these experiments was presented in Chapter 2, Figure 2-6. As was pointed out in that chapter, the experimental setup required a special test fixture that reduced stray capacitance and inductance to a minimum. The fixture was designed to provide easy access to the pads under test. Initially, 10X probes were used for some measurements, but these did not provide enough bandwidth for clean data collection. Eventually, Tektronix active probes model P6245 with less than 1pF capacitance allowing ~1.5GHz bandwidth was used for the

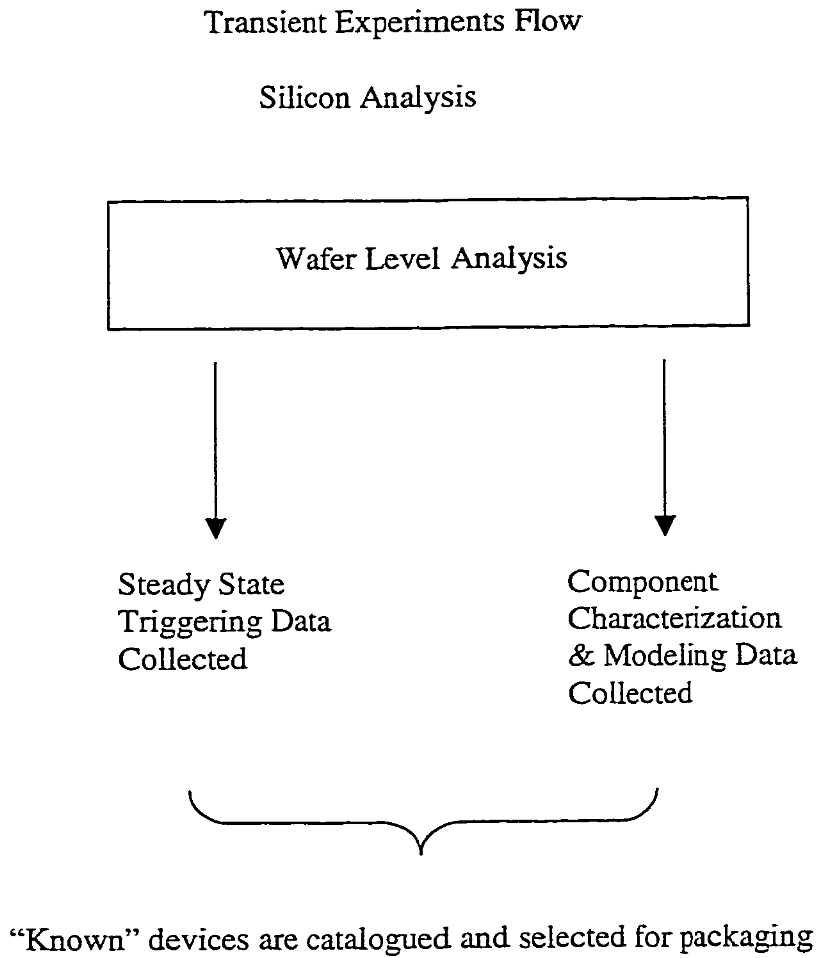


Figure 6-1. Detailed wafer level analysis was done before any parts were packaged for the transient triggering experiments.

measurements. The disadvantage of these probes is that there is a limitation on the maximum voltage one can measure, and this limited the probe use to the ~16V triggered SCR. It was not possible to obtain good measurements on the high voltage triggered devices (SCR_B).

6.2 Transient Triggering Measurements and Simulations for SCR_A

Figure 6-2 shows an example of a typical transient measurement on SCR_A and the simulation of the experiment using the actual input voltage pulse data in SPICE. The first step to confirm the validity of the data is to examine the pad current magnitude before the SCR triggers into latchup. This data and the SPICE result are shown in Figure 6-3. The I-V data is shown in Figure 6-4. These characteristics are somewhat different data, but all of the basic features are there. For clarity, the I-V data is labeled with the points A-F, as was done on the curve tracer data presented in Chapter 5. One difference is that the turn-off time for these pulses was on the order of about 15 nanoseconds, which didn't allow the SCR to turn-off the same way it does on a longer time scale. More will be said about this in the next chapter.

6.3 Transient Triggering Simulations for SCR_B

Figure 6-5 shows the SPICE simulation result for SCR_B, which has the higher triggering voltage. As was noted earlier, its high voltage triggering did not easily allow its properties to be measured on this time scale. Figure 6-6 shows the current characteristics,

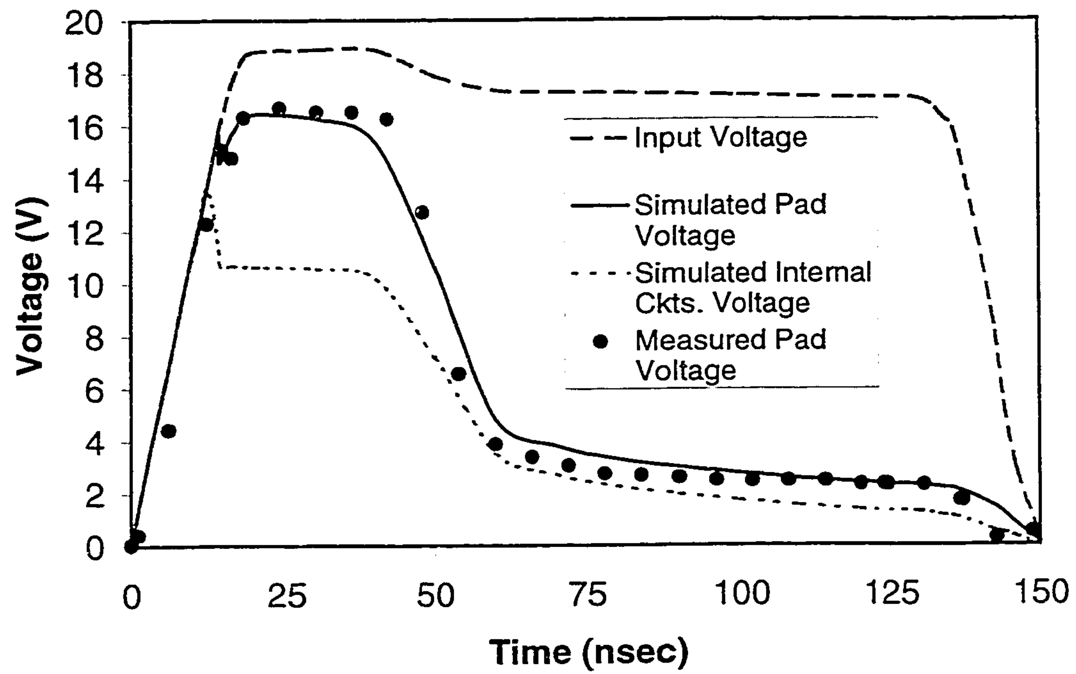


Figure 6-2. Measured and simulated voltages of SCR_A under a low voltage transient trigger condition.

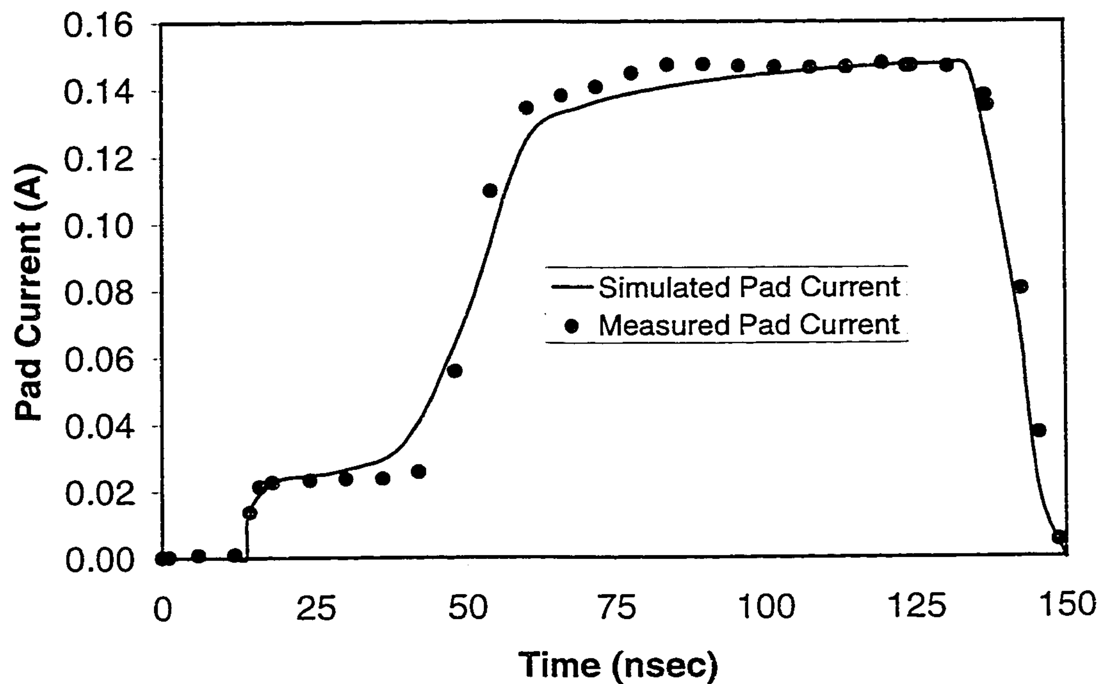


Figure 6-3. Measured and simulated pad currents for the low voltage transient trigger voltage of Figure 6-2.

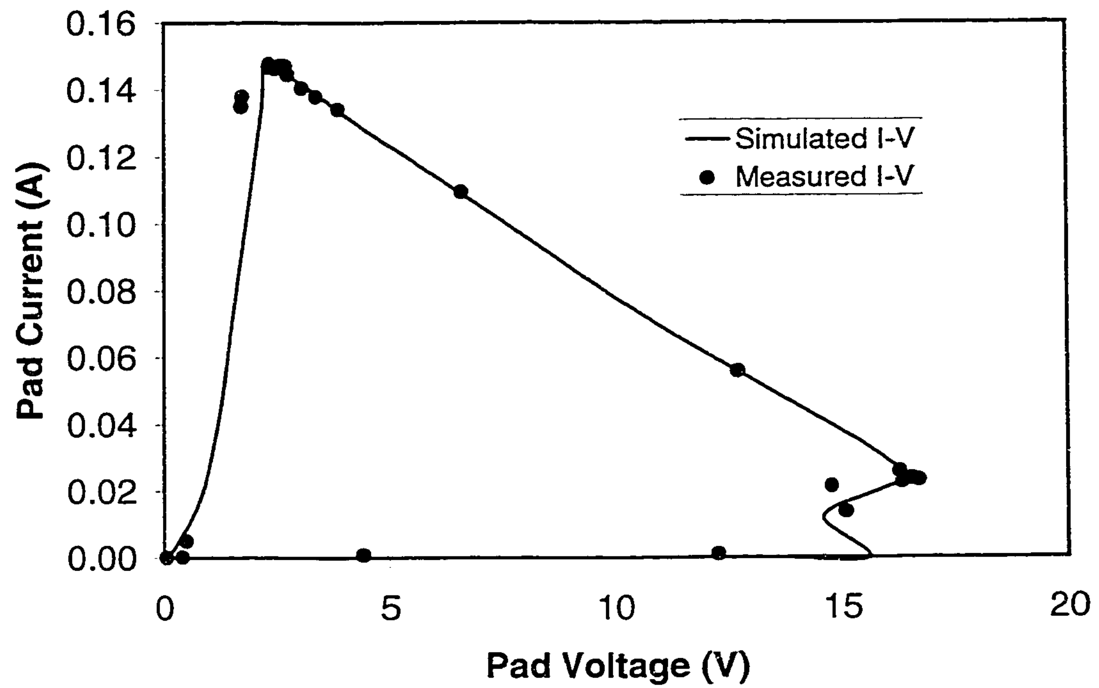


Figure 6-4. I-V characteristics for the measured and simulated low voltage transient trigger case.

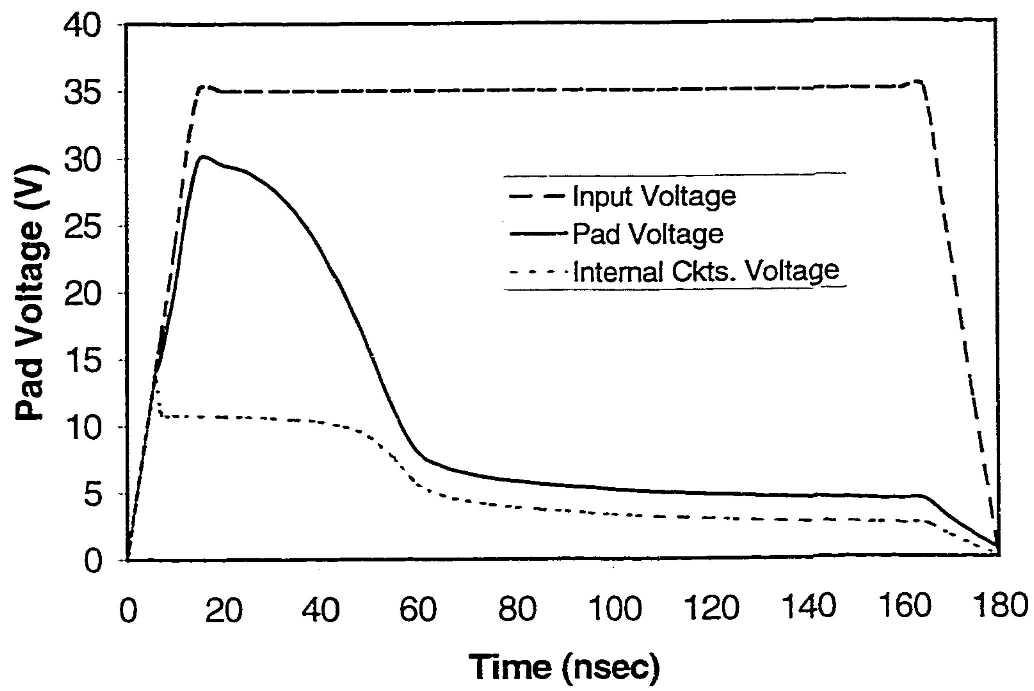


Figure 6-5. SCR_B simulated voltages for a 35V input trigger pulse.

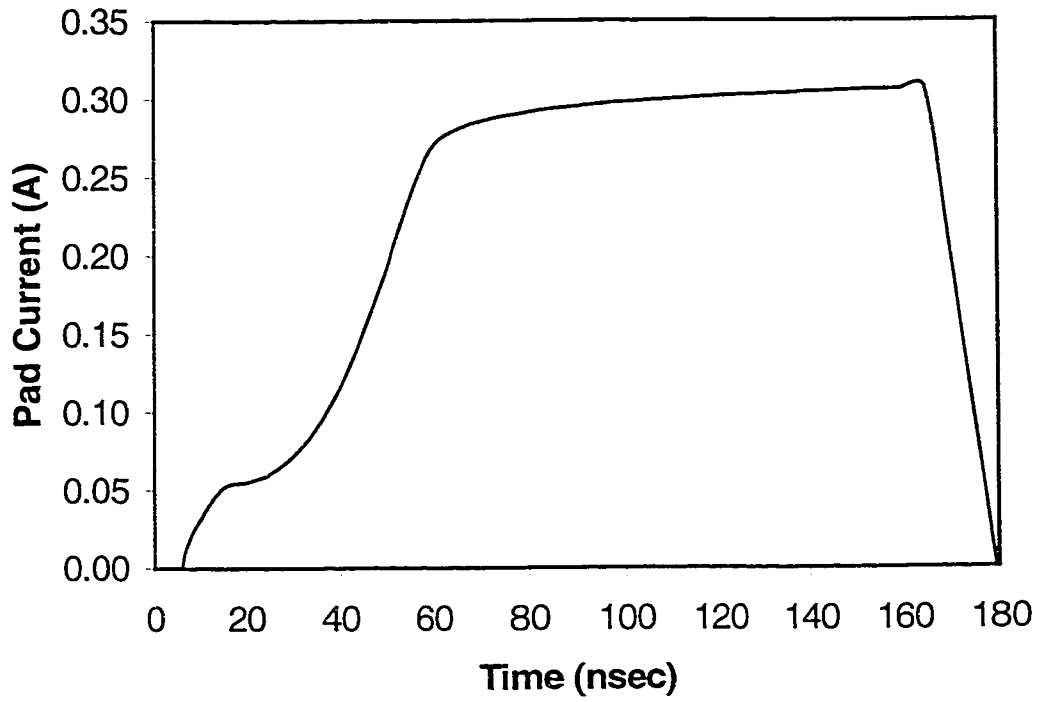


Figure 6-6. Current for SCR_B subject to a 35V square pulse trigger signal.

and Figure 6-7 shows I-V data. This last plot shows that in general, most of the characteristics are similar as to what were measured and simulated in the steady state. The I-V data are presented with the time steps indicated to show how quickly the device goes from a high voltage to the low voltage latchup condition. This fast response is the reason we are not able to capture that part of the data with the curve tracer, which operates on the microsecond time scale.

6.4 Conclusions and Summary

The data presented in this chapter demonstrate that the model is accurate for steady state simulation and transient triggering. In general, the transient case agrees well with the steady state case, although the data presentation makes it look a little bit different. The correlation between the transient testing and the steady state triggering is strong, since, even on a short time scale of about 50 nanoseconds, the measurements and the simulations demonstrate that the pad voltages agree with the steady state data. This method provides an additional data set for validating an ESD circuit SPICE model, but it requires devices that have sub-20V triggering. For deep submicron type technologies, this approach appears to be very useful. The main point is that the data can be collected in a semiconductor characterization lab without the use of ESD testers or without having to resort to ESD stress tests.

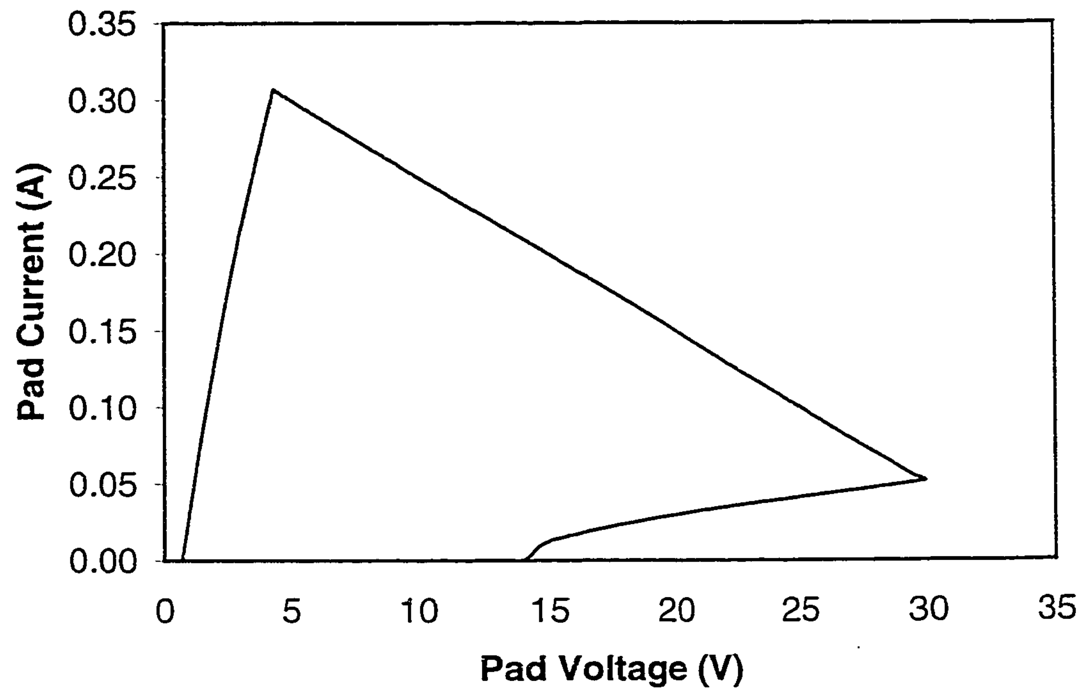


Figure 6-7. I-V characteristics of SCR_B subject to a 35V square pulse excitation.

CHAPTER 7

ESD SIMULATIONS, FURTHER ANALYSIS, AND CONCLUSIONS

The SPICE model developed in this work is valid over a wide range of triggering conditions, from steady state to nanosecond scale voltage pulses. The main purpose of this work is to understand how ESD circuits behave when subjected to an electro-static discharge event. One important result from this thesis is that there are ways to validate the model using standard characterization equipment. Data presented in the previous chapters show excellent correlation between the silicon measurements and the SPICE simulations. Analysis of the results leads to insight into how the device operates and what characteristics are important. In this chapter, representative discharge simulations will help shed more light on how these complex circuits operate. Some examples of how the devices fail will be presented, followed by some conclusions.

7.1 Human Body Model SPICE Simulations

HBM simulations on SCR_A were run at different stress levels to compare the results as the stress level rises. The circuit used to simulate the ESD events is as shown in Figure 1-1, in Chapter 1, with the discharge capacitor biased using the FORCE statement in SPICE. The important and relevant features obtained from the simulations are the pad I-V data, as well as the internal circuits' voltage. Figure 7-1 shows the SPICE result from a 100V HBM discharge simulation. The data shows that in this case, the internal voltage remains below the oxide damage threshold of 15V. The simulated currents are shown in

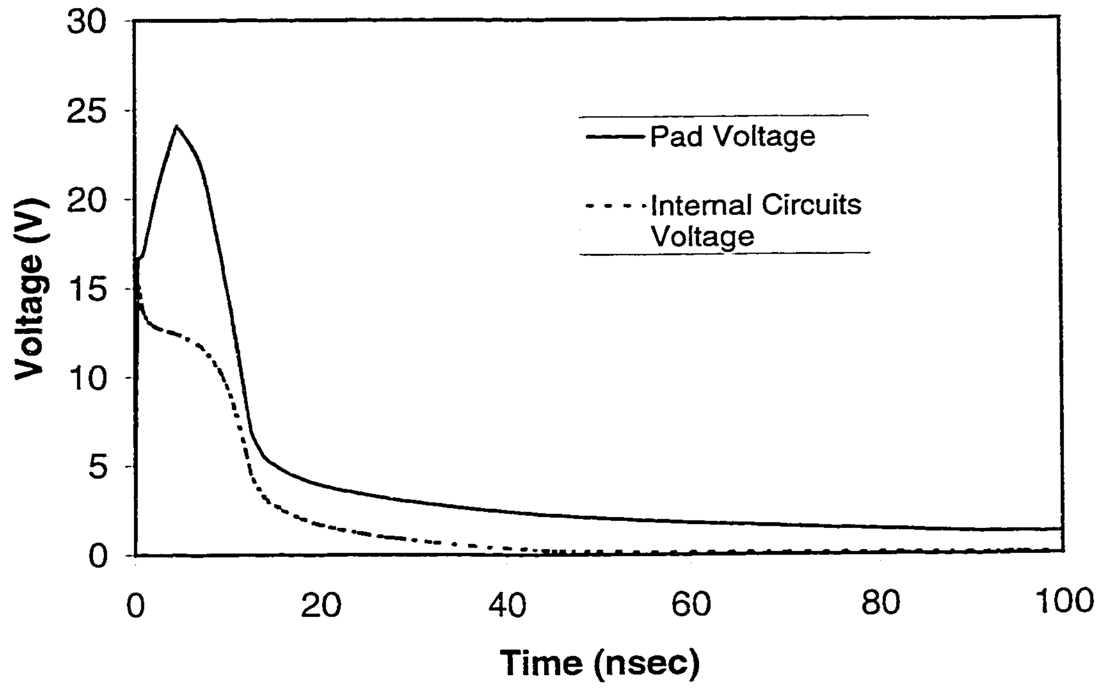


Figure 7-1. Voltages of interest for SCR_A under a 100V Human Body Model stress.

Figure 7-2. The pad I-V data is shown in Figure 7-3. The points are showing the 0.5 nanosecond timesteps used in the simulation. It is important to note that for the case of a 100V HBM stress, the absolute maximum current is limited to about a V/R value of $100/(1.5 \times 10^3)$ which is 66mA, close to the resulting maximum current simulated.

Figures 7-4 through 7-6 show simulation results for a 2KV HBM discharge. In this case, the pad voltage rises very fast to a high voltage, but is finally limited by the N+ resistor breakdown. In general, for very high voltage stresses, the maximum voltage on the pad reached about 35V; as explained earlier, the N+ resistor starts to avalanche at ~22V, and with the NMOS drain voltage holding somewhere about 10V, the maximum voltage will reach about 32V. This is consistent with the measurements on the silicon test structures, which showed that even for the SCR's that had difficulty triggering (due to their very wide base NPN) the maximum voltage an SCR allowed on the pad was 33V.

Figure 7-7 shows a summary of the results obtained from ESD simulations in SPICE. The results show that for stresses above 2KV, there is a potential for the circuit not to protect properly since the internal voltage is rising above 15V, the damage threshold voltage. This internal voltage does not remain at such a high level for very long, just a matter of nanoseconds, but these results indicate that perhaps there is a susceptibility to damage. Thus, even though the SCR itself is able to withstand a 6KV stress without damage, it is quite possible that it can still fail to protect the internal circuits at stresses above 2KV.

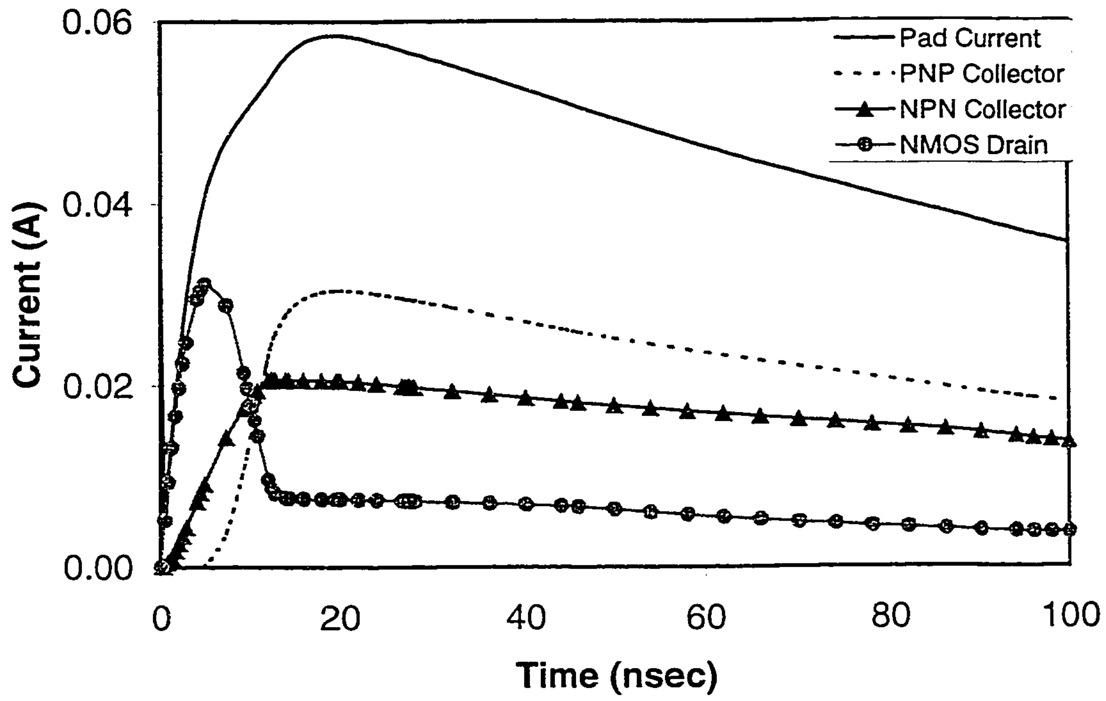


Figure 7-2. Currents for SCR_A under 100V Human Body Model stress condition.

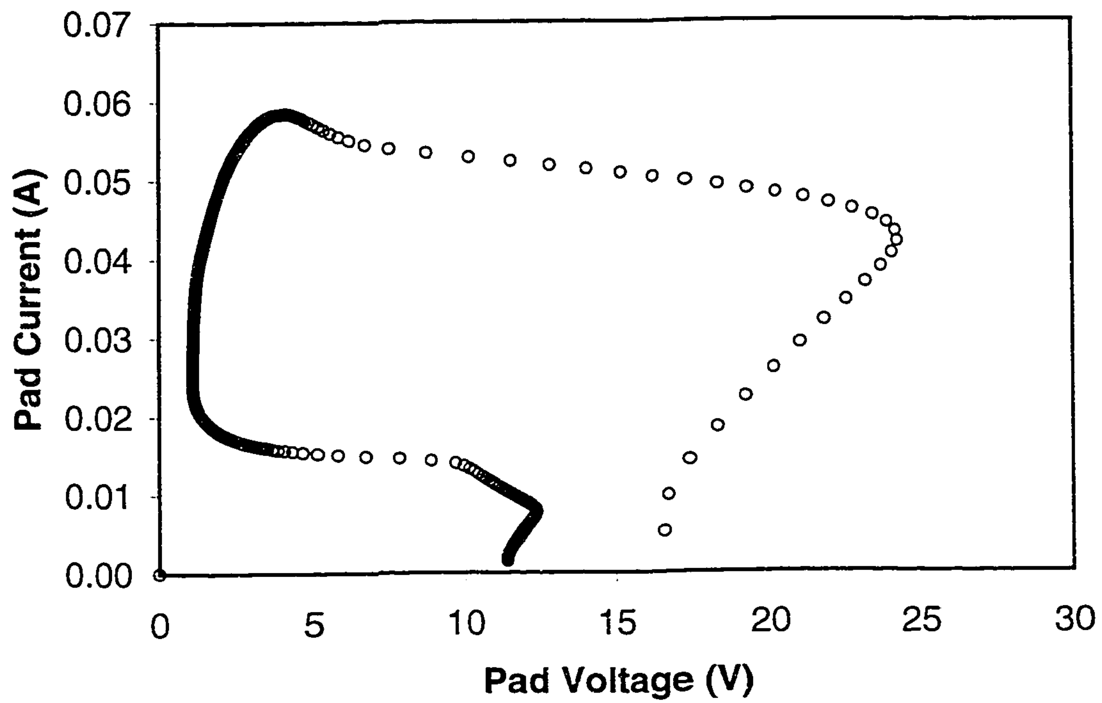


Figure 7-3. The I-V curve for SCR_A under 100V Human Body Model stress condition.

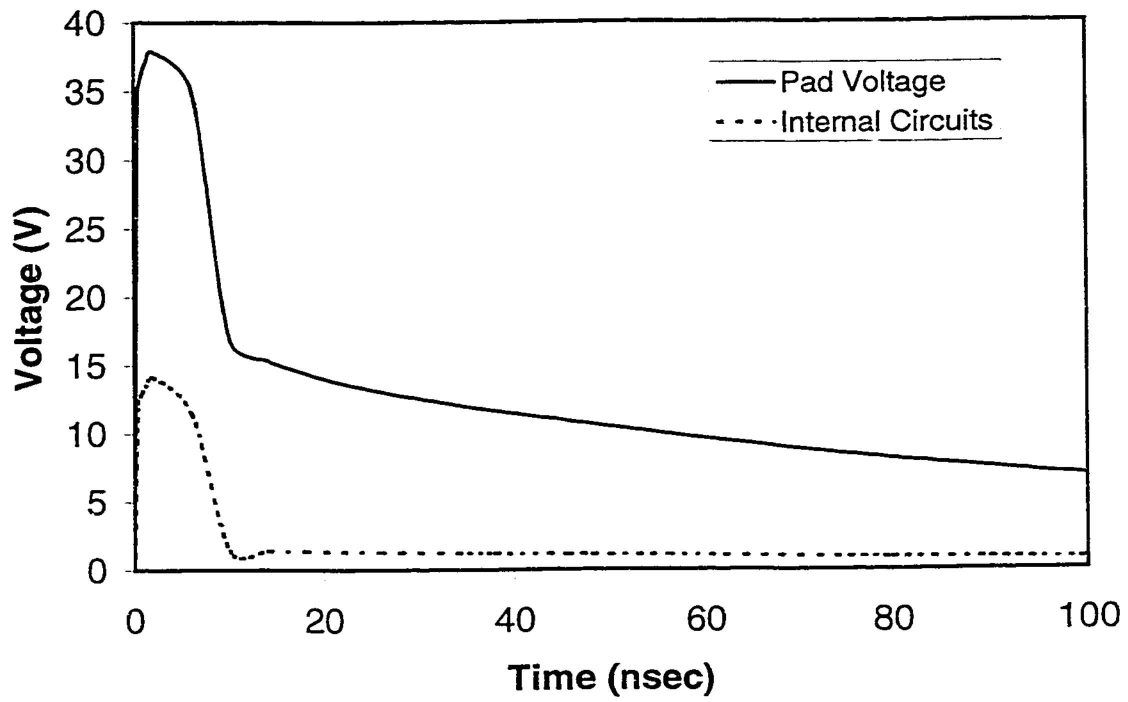


Figure 7-4. Voltages for SCR_A under a 2KV HBM stress condition.

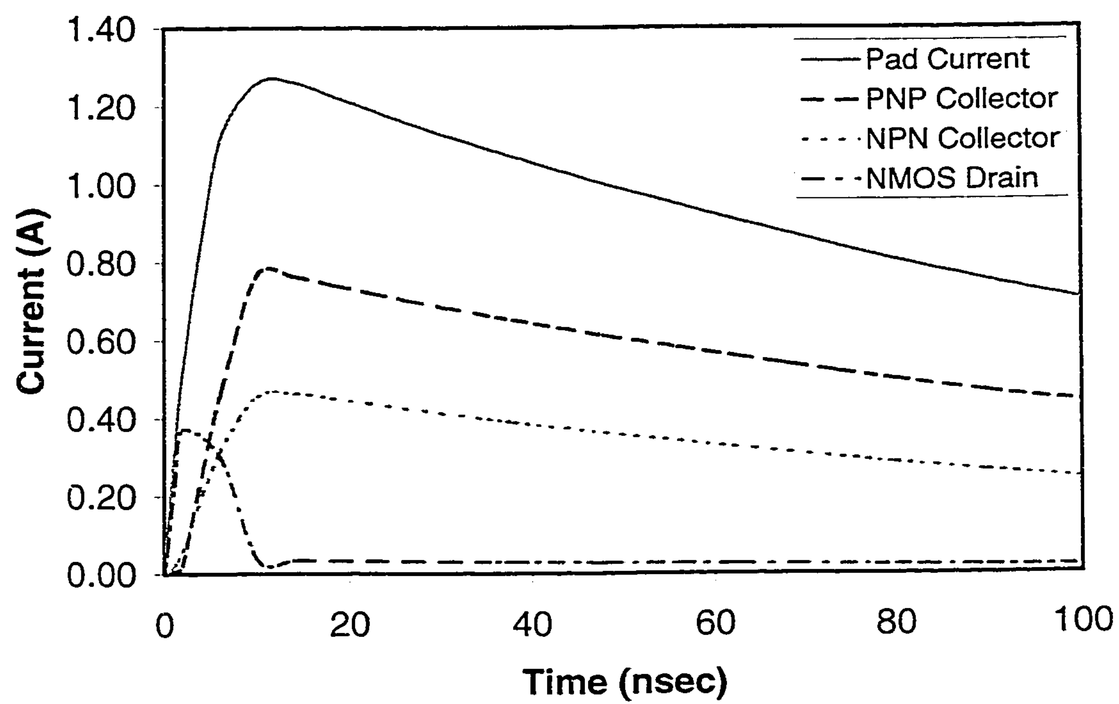


Figure 7-5. Currents for SCR_A under a 2KV HBM stress condition.

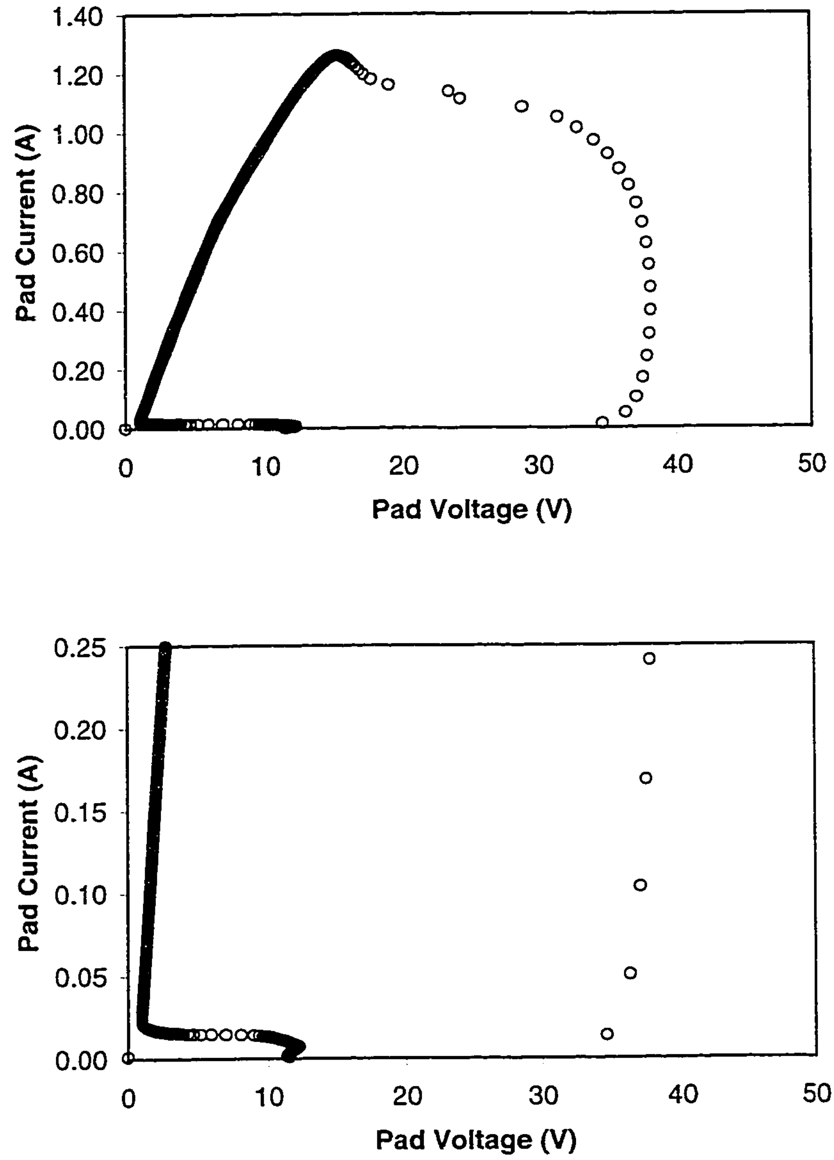


Figure 7-6. I-V characteristics for SCR_A under a 2KV HBM stress condition. The top plot shows the full I-V data. Each point refers to a 0.4nsec time step. The bottom plot shows a close up of the triggering region and the turn off region.

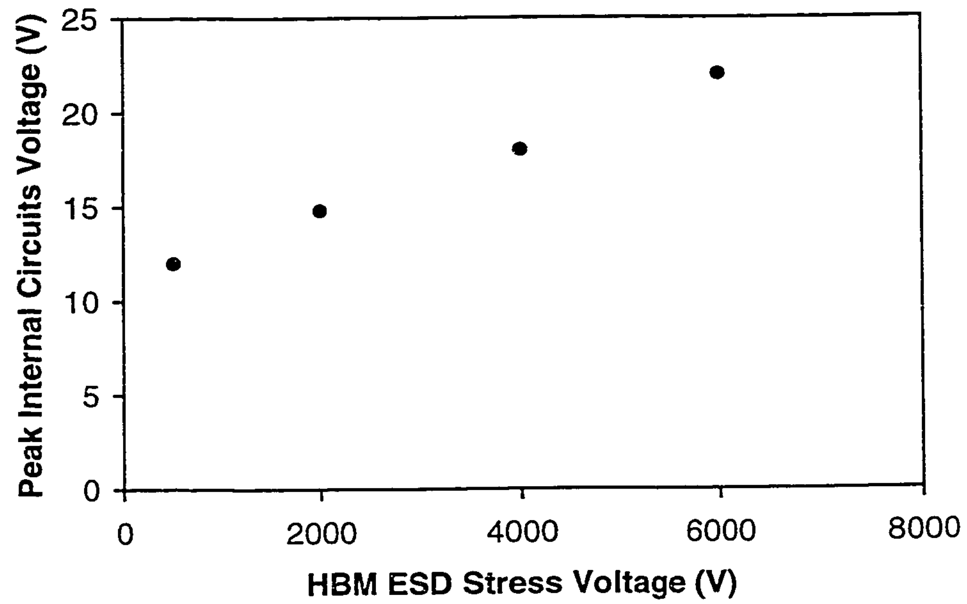


Figure 7-7. Simulated Peak Internal Circuits Voltage Vs the HBM stress level. The internal circuits are protected very well up to 2KV.

7.2 **Further Analysis**

The simulation results just presented show another interesting effect: as the discharge slowly drops towards 0V, the SCR is allowed to enter the off state. This is particularly obvious from the simulated data shown in Figure 7-3. One way to understand this turn off effect is to note that the current is not yet at 0 amps. This means that the SCR is still conducting, and it is slowly turning off, along with the stress. If you recall from Chapter 5, one of the important criteria for an accurate model is the high current resistance matching. A model was presented for the on-resistance of the SCR as it entered the latchup state. While the SCR is turning on, the resistance is dropping until it enters the full latchup state and the substrate is fully conductivity modulated. As the SCR is turning off, the current remains about constant, but the voltage is rising. One way to think about it is that the resistance is increasing; essentially, the SCR is re-tracing its on-resistance characteristic, but going the other way around: from the "on state" to the "off state." Physically, this makes sense since when it is in the off state, the SCR has very high (infinite) impedance.

The ESD simulations have shown that for very high stresses, the pad voltage is allowed to rise to what the N+ resistor can sustain. Under these conditions, the N+ resistor is forced into avalanche breakdown until the pad voltage can drop due to the SCR triggering into latchup. While this mode of operation is useful for limiting the maximum voltage, it also is a source of very high stress for the N+ resistor. During this research, this resistor was found to be the most susceptible to damage and SCR failure. Figure 7-8 shows an SEM photo of one of the SCR's which failed during lab measurements. This

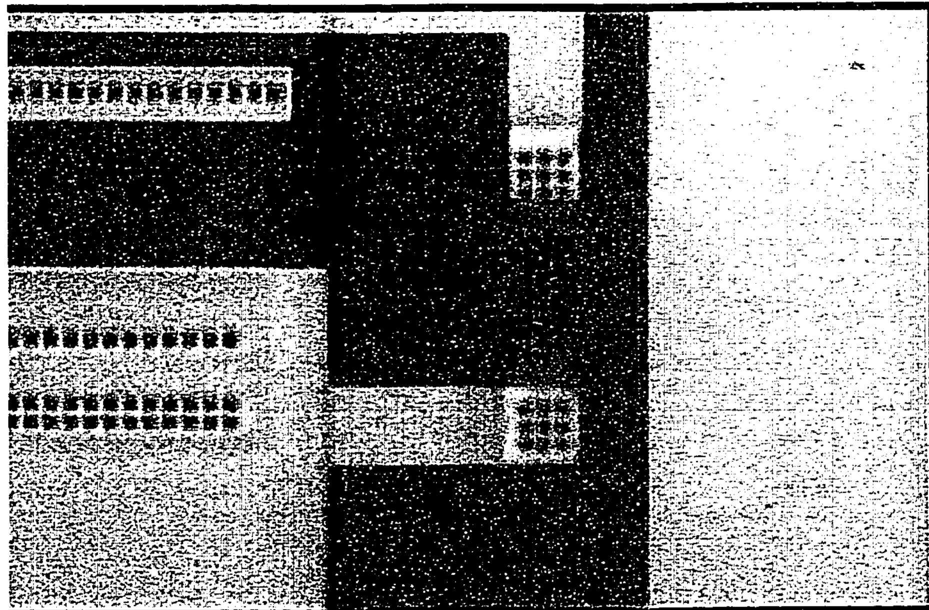


Figure 7-8. Example of a failure site for a wide (NPN) basewidth SCR. The SCR had difficulty triggering, causing the N+ resistor to enter the avalanche breakdown condition. The SCR was not able to trigger, causing the resistor to enter thermal breakdown.

particular example had difficulty triggering due to the wide NPN basewidth. As the resistor was conducting in the avalanche mode, the SCR could not trigger, and the increasing voltage forced thermal breakdown on the resistor. One obvious change to this SCR could be to have the N+ resistor completely in a Nwell, so that it would never break down. This change, however, will mean that the maximum limit on the pad voltage will be the 50V Nwell to P substrate breakdown. So, the SCR will have to be carefully designed in order to trigger below that maximum level. The work presented here gives a way to experiment with the ESD circuit design, since all of the components have been characterized and modeled.

7.3 Conclusions

A sub-circuit model for an avalanche triggered SCR used in ESD protection circuits has been presented. A methodology was prescribed which allowed this complex circuit to be reduced to its basic components. The combined efforts of silicon characterization as well as TCAD simulations allowed the circuit operation and characteristics to be understood explicitly. This in turn allowed the development of a physically based SPICE model for the SCR. The model was validated using steady state and transient triggering measurements and SPICE simulations. This is the first model presented for an avalanche triggered SCR which demonstrates this capability. The SCR itself was found to be able to sustain a very high ESD stress, higher than 6KV for the Human Body Model stress. The SPICE simulations, however, indicated that the internal circuits might not be protected fully past 2KV of HBM stress. This points the way to an

improvement in the test structures. Connecting a transistor gate to this terminal could monitor the internal circuits' point; this would allow the possibility of monitoring the test transistor currents and oxide reliability during the stressing of the ESD circuit.

APPENDIX A

SPICE MODELS AND EXAMPLE DECK FOR STEADY STATE SIMULATION OF SCR_A

N+ Resistor Model

```
.MODEL MOATRB PWL(1) SYMMETRY NO SOURCE CARDS
+ DATA
+ 98.76 0.0001
+ 98.76 0.0833
+ 98.91 0.1667
+ 99.03 0.25
+ 99.14 0.3333
+ 99.26 0.4167
+ 99.4 0.5
+ 99.53 0.5833
+ 99.69 0.6667
+ 99.89 0.75
+ 100.12 0.8333
+ 100.35 0.9167
+ 100.62 1
+ 100.92 1.0833
+ 101.19 1.1667
+ 101.5 1.25
+ 101.86 1.3333
+ 102.25 1.4167
+ 102.63 1.5
+ 103.01 1.5833
+ 103.49 1.6667
+ 103.95 1.75
+ 104.43 1.8333
+ 104.94 1.9167
+ 105.46 2
+ 106.02 2.0833
+ 106.6 2.1667
+ 107.21 2.25
+ 107.85 2.3333
+ 108.49 2.4167
+ 109.17 2.5
+ 109.86 2.5833
+ 110.6 2.6667
+ 111.38 2.75
+ 112.14 2.8333
+ 112.96 2.9167
+ 113.8 3
+ 114.69 3.0833
+ 115.57 3.1667
+ 116.49 3.25
+ 117.43 3.3333
+ 118.41 3.4167
+ 119.41 3.5
+ 120.45 3.5833
+ 121.53 3.6667
+ 122.63 3.75
+ 123.76 3.8333
+ 124.89 3.9167
+ 126.08 4
+ 127.29 4.0833
+ 128.54 4.1667
+ 129.81 4.25
+ 131.11 4.3333
+ 132.45 4.4167
+ 133.81 4.5
+ 135.22 4.5833
+ 136.65 4.6667
+ 138.12 4.75
+ 139.61 4.8333
+ 141.14 4.9167
+ 142.69 5
+ 144.31 5.0833
+ 145.93 5.1667
+ 147.6 5.25
+ 149.31 5.3333
+ 151.03 5.4167
+ 152.79 5.5
+ 154.62 5.5833
+ 156.47 5.6667
+ 158.33 5.75
+ 160.26 5.8333
+ 162.21 5.9167
+ 164.2 6
+ 166.24 6.0833
+ 168.3 6.1667
+ 170.42 6.25
+ 172.55 6.3333
+ 174.72 6.4167
+ 176.94 6.5
+ 179.21 6.5833
+ 181.5 6.6667
+ 183.79 6.75
+ 186.12 6.8333
+ 188.33 6.9167
+ 190.67 7
+ 193 7.0833
+ 194.67 7.1667
+ 144.67 7.25
+ 129.33 7.3333
```

Diode Model for the N+ Resistor: forward and reverse I-V

.MODEL DNRES D
.MODEL DNRES PWL(1) SYMMETRY NO SOURCE CARDS
+ DATA

+	2.41E-02	1.5	+	7.40E-03	1.08
+	2.37E-02	1.49	+	7.06E-03	1.07
+	2.32E-02	1.48	+	6.73E-03	1.06
+	2.28E-02	1.47	+	6.41E-03	1.05
+	2.24E-02	1.46	+	6.08E-03	1.04
+	2.19E-02	1.45	+	5.76E-03	1.03
+	2.15E-02	1.44	+	5.45E-03	1.02
+	2.11E-02	1.43	+	5.14E-03	1.01
+	2.07E-02	1.42	+	4.84E-03	1
+	2.02E-02	1.41	+	4.54E-03	0.99
+	1.98E-02	1.4	+	4.26E-03	0.98
+	1.94E-02	1.39	+	3.97E-03	0.97
+	1.90E-02	1.38	+	3.70E-03	0.96
+	1.86E-02	1.37	+	3.44E-03	0.95
+	1.81E-02	1.36	+	3.18E-03	0.94
+	1.77E-02	1.35	+	2.93E-03	0.93
+	1.73E-02	1.34	+	2.69E-03	0.92
+	1.69E-02	1.33	+	2.46E-03	0.91
+	1.65E-02	1.32	+	2.24E-03	0.9
+	1.61E-02	1.31	+	2.03E-03	0.89
+	1.57E-02	1.3	+	1.82E-03	0.88
+	1.53E-02	1.29	+	1.64E-03	0.87
+	1.49E-02	1.28	+	1.46E-03	0.86
+	1.45E-02	1.27	+	1.30E-03	0.85
+	1.41E-02	1.26	+	1.14E-03	0.84
+	1.37E-02	1.25	+	1.00E-03	0.83
+	1.33E-02	1.24	+	8.74E-04	0.82
+	1.29E-02	1.23	+	7.56E-04	0.81
+	1.25E-02	1.22	+	6.50E-04	0.8
+	1.21E-02	1.21	+	5.58E-04	0.79
+	1.17E-02	1.2	+	4.74E-04	0.78
+	1.14E-02	1.19	+	4.00E-04	0.77
+	1.10E-02	1.18	+	3.36E-04	0.76
+	1.06E-02	1.17	+	2.80E-04	0.75
+	1.02E-02	1.16	+	2.32E-04	0.74
+	9.88E-03	1.15	+	1.92E-04	0.73
+	9.51E-03	1.14	+	1.57E-04	0.72
+	9.15E-03	1.13	+	1.27E-04	0.71
+	8.79E-03	1.12	+	1.03E-04	0.7

Diode Model for the N+ Resistor: forward and reverse I-V, cont'd

+	4.02E-05	0.66	+	8.60E-12	0.24
+	3.10E-05	0.65	+	7.00E-12	0.23
+	2.37E-05	0.64	+	6.00E-12	0.22
+	1.79E-05	0.63	+	5.50E-12	0.21
+	1.34E-05	0.62	+	5.50E-12	0.2
+	9.86E-06	0.61	+	4.50E-12	0.19
+	7.28E-06	0.6	+	4.50E-12	0.18
+	5.25E-06	0.59	+	4.00E-12	0.17
+	3.75E-06	0.58	+	4.00E-12	0.16
+	2.67E-06	0.57	+	4.00E-12	0.15
+	1.87E-06	0.56	+	2.00E-12	0.14
+	1.30E-06	0.55	+	1.45E-12	0.13
+	9.08E-07	0.54	+	1.45E-12	0.12
+	6.27E-07	0.53	+	1.45E-12	0.11
+	4.30E-07	0.52	+	1.45E-12	0.1
+	2.92E-07	0.51	+	1.35E-12	0.09
+	1.99E-07	0.5	+	1.35E-12	0.08
+	1.35E-07	0.49	+	1.35E-12	0.07
+	9.11E-08	0.48	+	1.35E-12	0.06
+	6.23E-08	0.47	+	1.35E-12	0.05
+	4.22E-08	0.46	+	1.35E-12	0.04
+	2.86E-08	0.45	+	1.35E-12	0.03
+	1.94E-08	0.44	+	1.25E-12	0.02
+	1.31E-08	0.43	+	1.25E-12	0.01
+	9.01E-09	0.42	+	1.05E-12	0
+	6.09E-09	0.41	+	-1.00E-13	-0.25
+	4.11E-09	0.4	+	-1.00E-13	-0.5
+	2.78E-09	0.39	+	-1.00E-13	-0.75
+	1.87E-09	0.38	+	-1.00E-13	-1
+	1.27E-09	0.37	+	-1.00E-13	-1.25
+	8.55E-10	0.36	+	-1.00E-13	-1.5
+	5.78E-10	0.35	+	-1.00E-13	-1.75
+	3.95E-10	0.34	+	-1.00E-13	-2
+	2.65E-10	0.33	+	-1.00E-13	-2.25
+	1.81E-10	0.32	+	-1.00E-13	-2.5
+	1.22E-10	0.31	+	-1.00E-13	-2.75
+	8.22E-11	0.3	+	-1.00E-13	-3
+	5.64E-11	0.29	+	-1.00E-13	-3.25
+	3.71E-11	0.28	+	-1.00E-13	-3.5
+	2.67E-11	0.27	+	-1.00E-13	-3.75
+	1.66E-11	0.26	+	-1.00E-13	-4
+	1.17E-11	0.25	+	-1.00E-13	-4.25

Diode Model for the N+ Resistor: forward and reverse I-V, cont'd

+	-1.00E-13	-4.5	+	-3.94E-08	-15
+	-1.00E-13	-4.75	+	-6.20E-08	-15.25
+	-1.00E-13	-5	+	-9.67E-08	-15.5
+	-1.00E-13	-5.25	+	-1.50E-07	-15.75
+	-1.00E-13	-5.5	+	-2.30E-07	-16
+	-1.00E-13	-5.75	+	-3.52E-07	-16.25
+	-1.00E-13	-6	+	-5.35E-07	-16.5
+	-1.00E-13	-6.25	+	-8.08E-07	-16.75
+	-1.00E-13	-6.5	+	-1.22E-06	-17
+	-1.00E-13	-6.75	+	-1.81E-06	-17.25
+	-1.00E-13	-7	+	-2.69E-06	-17.5
+	-1.00E-13	-7.25	+	-3.97E-06	-17.75
+	-1.00E-13	-7.5	+	-5.82E-06	-18
+	-1.00E-13	-7.75	+	-8.48E-06	-18.25
+	-1.00E-13	-8	+	-1.23E-05	-18.5
+	-1.00E-13	-8.25	+	-1.78E-05	-18.75
+	-2.00E-13	-8.5	+	-2.56E-05	-19
+	-4.00E-13	-8.75	+	-3.68E-05	-19.25
+	-6.00E-13	-9	+	-5.25E-05	-19.5
+	-8.00E-13	-9.25	+	-7.49E-05	-19.75
+	-1.00E-12	-9.5	+	-1.07E-04	-20
+	-2.00E-12	-9.75	+	-1.52E-04	-20.25
+	-4.00E-12	-10	+	-2.18E-04	-20.5
+	-6.00E-12	-10.25	+	-3.14E-04	-20.75
+	-8.00E-12	-10.5	+	-4.58E-04	-21
+	-1.00E-11	-10.75	+	-6.79E-04	-21.25
+	-2.00E-11	-11	+	-1.01E-03	-21.5
+	-4.00E-11	-11.25	+	-6.18E-03	-21.75
+	-6.00E-11	-11.5	+	-8.69E-03	-22
+	-8.00E-11	-11.75			
+	-1.55E-10	-12			
+	-1.90E-10	-12.25			
+	-2.95E-10	-12.5			
+	-5.45E-10	-12.75			
+	-9.35E-10	-13			
+	-1.43E-09	-13.25			
+	-2.33E-09	-13.5			
+	-3.81E-09	-13.75			
+	-6.13E-09	-14			
+	-9.86E-09	-14.25			
+	-1.57E-08	-14.5			
+	-2.50E-08	-14.75			

Diode model for the Nwell-Pwell Diode, forward & reverse I-V

```
.MODEL DNWPW D
.MODEL DNWPW PWL(1) SYMMETRY NO SOURCE CARDS
+ DATA
+    1.33E-02    1.50E+00    +    5.33E-03    1.08E+00
+    1.31E-02    1.49E+00    +    5.14E-03    1.07E+00
+    1.29E-02    1.48E+00    +    4.96E-03    1.06E+00
+    1.27E-02    1.47E+00    +    4.79E-03    1.05E+00
+    1.25E-02    1.46E+00    +    4.60E-03    1.04E+00
+    1.23E-02    1.45E+00    +    4.42E-03    1.03E+00
+    1.21E-02    1.44E+00    +    4.24E-03    1.02E+00
+    1.19E-02    1.43E+00    +    4.07E-03    1.01E+00
+    1.17E-02    1.42E+00    +    3.89E-03    1.00E+00
+    1.15E-02    1.41E+00    +    3.71E-03    9.90E-01
+    1.14E-02    1.40E+00    +    3.54E-03    9.80E-01
+    1.12E-02    1.39E+00    +    3.36E-03    9.70E-01
+    1.10E-02    1.38E+00    +    3.19E-03    9.60E-01
+    1.08E-02    1.37E+00    +    3.02E-03    9.50E-01
+    1.06E-02    1.36E+00    +    2.85E-03    9.40E-01
+    1.04E-02    1.35E+00    +    2.68E-03    9.30E-01
+    1.02E-02    1.34E+00    +    2.52E-03    9.20E-01
+    1.00E-02    1.33E+00    +    2.36E-03    9.10E-01
+    9.83E-03    1.32E+00    +    2.20E-03    9.00E-01
+    9.63E-03    1.31E+00    +    2.04E-03    8.90E-01
+    9.45E-03    1.30E+00    +    1.88E-03    8.80E-01
+    9.26E-03    1.29E+00    +    1.73E-03    8.70E-01
+    9.06E-03    1.28E+00    +    1.59E-03    8.60E-01
+    8.87E-03    1.27E+00    +    1.45E-03    8.50E-01
+    8.68E-03    1.26E+00    +    1.31E-03    8.40E-01
+    8.49E-03    1.25E+00    +    1.18E-03    8.30E-01
+    8.31E-03    1.24E+00    +    1.06E-03    8.20E-01
+    8.11E-03    1.23E+00    +    9.44E-04    8.10E-01
+    7.93E-03    1.22E+00    +    8.33E-04    8.00E-01
+    7.74E-03    1.21E+00    +    7.32E-04    7.90E-01
+    7.55E-03    1.20E+00    +    6.36E-04    7.80E-01
+    7.36E-03    1.19E+00    +    5.47E-04    7.70E-01
+    7.17E-03    1.18E+00    +    4.67E-04    7.60E-01
+    6.99E-03    1.17E+00    +    3.94E-04    7.50E-01
+    6.80E-03    1.16E+00    +    3.30E-04    7.40E-01
+    6.62E-03    1.15E+00    +    2.74E-04    7.30E-01
+    6.43E-03    1.14E+00    +    2.25E-04    7.20E-01
+    6.24E-03    1.13E+00    +    1.83E-04    7.10E-01
+    6.06E-03    1.12E+00    +    1.47E-04    7.00E-01
```

Diode model for the Nwell-Pwell Diode, forward & reverse I-V, cont'd

+	5.88E-03	1.11E+00	+	1.17E-04	6.90E-01
+	5.69E-03	1.10E+00	+	9.35E-05	6.80E-01
+	5.51E-03	1.09E+00	+	7.28E-05	6.70E-01
+	5.68E-05	6.60E-01	+	1.23E-11	2.40E-01
+	4.35E-05	6.50E-01	+	8.35E-12	2.30E-01
+	3.30E-05	6.40E-01	+	5.70E-12	2.20E-01
+	2.48E-05	6.30E-01	+	4.30E-12	2.10E-01
+	1.84E-05	6.20E-01	+	3.40E-12	2.00E-01
+	1.36E-05	6.10E-01	+	2.50E-12	1.90E-01
+	9.98E-06	6.00E-01	+	1.65E-12	1.80E-01
+	7.17E-06	5.90E-01	+	1.15E-12	1.70E-01
+	5.13E-06	5.80E-01	+	9.00E-13	1.60E-01
+	3.64E-06	5.70E-01	+	5.50E-13	1.50E-01
+	2.55E-06	5.60E-01	+	4.00E-13	1.40E-01
+	1.78E-06	5.50E-01	+	3.00E-13	1.30E-01
+	1.23E-06	5.40E-01	+	2.00E-13	1.20E-01
+	8.61E-07	5.30E-01	+	1.00E-13	1.10E-01
+	5.90E-07	5.20E-01	+	9.00E-14	1.00E-01
+	4.01E-07	5.10E-01	+	6.00E-14	9.00E-02
+	2.74E-07	5.00E-01	+	5.50E-14	8.00E-02
+	1.86E-07	4.90E-01	+	5.00E-14	7.00E-02
+	1.26E-07	4.80E-01	+	5.00E-14	6.00E-02
+	8.65E-08	4.70E-01	+	5.00E-14	5.00E-02
+	5.87E-08	4.60E-01	+	5.00E-14	4.00E-02
+	3.96E-08	4.50E-01	+	5.00E-14	3.00E-02
+	2.71E-08	4.40E-01	+	5.00E-14	2.00E-02
+	1.83E-08	4.30E-01	+	5.00E-14	1.00E-02
+	1.24E-08	4.20E-01	+	5.00E-14	0.00E+00
+	8.56E-09	4.10E-01	+	-5.00E-14	-5.00E-01
+	5.79E-09	4.00E-01	+	-5.00E-14	-1.00E+00
+	3.92E-09	3.90E-01	+	-5.00E-14	-1.50E+00
+	2.65E-09	3.80E-01	+	-5.00E-14	-2.00E+00
+	1.79E-09	3.70E-01	+	-5.00E-14	-2.50E+00
+	1.22E-09	3.60E-01	+	-5.00E-14	-3.00E+00
+	8.24E-10	3.50E-01	+	-5.00E-14	-3.50E+00
+	5.65E-10	3.40E-01	+	-5.00E-14	-4.00E+00
+	3.82E-10	3.30E-01	+	-5.00E-14	-4.50E+00
+	2.59E-10	3.20E-01	+	-5.00E-14	-5.00E+00
+	1.77E-10	3.10E-01	+	-5.00E-14	-5.50E+00
+	1.20E-10	3.00E-01	+	-5.00E-14	-6.00E+00
+	8.12E-11	2.90E-01	+	-5.00E-14	-6.50E+00
+	5.58E-11	2.80E-01	+	-5.00E-14	-7.00E+00

Diode model for the Nwell-Pwell Diode, forward & reverse I-V, cont'd

+	3.80E-11	2.70E-01	+	-5.00E-14	-7.50E+00
+	2.58E-11	2.60E-01	+	-5.00E-14	-8.00E+00
+	1.79E-11	2.50E-01	+	-5.00E-14	-8.50E+00
+	-5.00E-14	-9.00E+00	+	-2.45E-12	-3.00E+01
+	-5.00E-14	-9.50E+00	+	-2.45E-12	-3.05E+01
+	-5.00E-14	-1.00E+01	+	-2.45E-12	-3.10E+01
+	-5.00E-14	-1.05E+01	+	-2.45E-12	-3.15E+01
+	-1.50E-13	-1.10E+01	+	-2.45E-12	-3.20E+01
+	-1.50E-13	-1.15E+01	+	-2.45E-12	-3.25E+01
+	-1.50E-13	-1.20E+01	+	-2.45E-12	-3.30E+01
+	-1.50E-13	-1.25E+01	+	-2.45E-12	-3.35E+01
+	-1.50E-13	-1.30E+01	+	-2.45E-12	-3.40E+01
+	-1.50E-13	-1.35E+01	+	-2.45E-12	-3.45E+01
+	-1.50E-13	-1.40E+01	+	-2.45E-12	-3.50E+01
+	-1.05E-12	-1.45E+01	+	-2.50E-12	-3.55E+01
+	-1.05E-12	-1.50E+01	+	-2.50E-12	-3.60E+01
+	-1.05E-12	-1.55E+01	+	-2.50E-12	-3.65E+01
+	-1.05E-12	-1.60E+01	+	-2.50E-12	-3.70E+01
+	-1.05E-12	-1.65E+01	+	-2.55E-12	-3.75E+01
+	-1.05E-12	-1.70E+01	+	-2.55E-12	-3.80E+01
+	-1.05E-12	-1.75E+01	+	-2.55E-12	-3.85E+01
+	-1.05E-12	-1.80E+01	+	-2.55E-12	-3.90E+01
+	-2.35E-12	-1.85E+01	+	-2.60E-12	-3.95E+01
+	-2.35E-12	-1.90E+01	+	-2.70E-12	-4.00E+01
+	-2.35E-12	-1.95E+01	+	-2.80E-12	-4.05E+01
+	-2.35E-12	-2.00E+01	+	-2.85E-12	-4.10E+01
+	-2.35E-12	-2.05E+01	+	-2.95E-12	-4.15E+01
+	-2.35E-12	-2.10E+01	+	-2.95E-12	-4.20E+01
+	-2.35E-12	-2.15E+01	+	-2.98E-12	-4.25E+01
+	-2.35E-12	-2.20E+01	+	-3.00E-12	-4.30E+01
+	-2.40E-12	-2.25E+01	+	-3.00E-12	-4.35E+01
+	-2.40E-12	-2.30E+01	+	-3.15E-12	-4.40E+01
+	-2.40E-12	-2.35E+01	+	-3.25E-12	-4.45E+01
+	-2.40E-12	-2.40E+01	+	-3.50E-12	-4.50E+01
+	-2.40E-12	-2.45E+01	+	-3.70E-12	-4.55E+01
+	-2.40E-12	-2.50E+01	+	-3.90E-12	-4.60E+01
+	-2.40E-12	-2.55E+01	+	-4.60E-12	-4.65E+01
+	-2.40E-12	-2.60E+01	+	-5.75E-12	-4.70E+01
+	-2.40E-12	-2.65E+01	+	-8.20E-12	-4.75E+01
+	-2.40E-12	-2.70E+01	+	-6.09E-11	-4.80E+01
+	-2.40E-12	-2.75E+01	+	-9.94E-07	-4.85E+01
+	-2.45E-12	-2.80E+01	+	-9.98E-07	-4.90E+01

Diode model for the Nwell-Pwell Diode, forward & reverse I-V, cont'd

+	-2.45E-12	-2.85E+01	+	-9.99E-07	-4.95E+01
+	-2.45E-12	-2.90E+01	+	-1.00E-06	-5.00E+01
+	-2.45E-12	-2.95E+01			

SCR Model for the On - Resistance Vs Anode Voltage

```
.MODEL RF PWL(1) SYMMETRY NO SOURCE CARDS
+ DATA
+       6.5     1.50
+       6.45    1.60
+       6.4     1.70
+       6.35    1.80
+       6.3     1.90
+       6.25    2.00
+       6.2     2.10
+       6.15    2.20
+       6.1     2.30
+       6.05    2.40
+       6.0     2.50
+       5.95    2.60
+       5.90    2.70
+       5.85    2.80
+       5.8     2.90
```

SPICE Model for NMOS transistor, including ESD parameters

```
.MODEL NCH NMOS
+ WMIN = 1.08 WMAX = 100.0
+ LMIN = 0.7 LMAX = 10.0
+ TEMPMIN = -40 TEMPMAX = 150
+ VGSMAX = 6.0 VDSMAX = 600.0
+     KP= 55.80E-06      WR= 0.0000000      LR=   0.05000
+     KPS= 1.000E-09      N= 1.300E+16      NG=      0.8
+     VTO=  0.59000    VTOW=       0    VTOL= 0.0090604
+     BE=  0.72145     BEW=       0     BEL=  -0.16883
+   ALPHA=        1  ALPHAW= 0.067317  ALPHAL=  0.03698
+   THETA= 0.0027742  THETAW=  0.263785  THETAL= 0.348745
+  LAMBDA=        0 LAMBDAW= 0.053158 LAMBDAL=  0.02635
+   GAMMA= 0.037649  GAMMAW= 0.059212  GAMMAL= 0.080103
+     DE=       0     DEW=       0     DEL=       0
+     CF= 0.0015738    CFW=       0    CFL= 0.048875
+     COX= 2.301E-15    TLD=  0.0649   TLDAC=   0.212
+     CJO= 4.603E-16      M=  389.0m
+    CJOS= 6.688E-16     MS=  271.2m
+     VBI= 808.7m     TCKP=  -1.11578
+    VBIS= 564.8m      TCVT=-0.00119494
+  THETAC=        2      NS= 2.600E+16
+   TPOLY=     0.45
+      IS= 5.000E-19
+ ESDP0 = 0.7
+ ESDIOC  = 1E-18
+ ESDIOE  = 1.4E-18
+ ESDAI = 2.1
+ ESDBI = 11.25
```

Gummel-Poon model for the Vertical PNP

```
.MODEL  VPNP PNP
+ IS   = 0.18f
+ BF   = 13
+ NF   = 0.987
+ VAF = 100
+ IKF  = 200m
+ ISE  = 0.001f
+ NE   = 1.32
+ BR   = 0.5
+ NR   = 1.4
+ VAR= 50
+ IKR  = 1m
+ ISC  = 0.02f
+ NC   = 1.5
+ RB   = 1.1
+ IRB  = 1n
+ RBM = 1
+ RE   = 1
+ RC   = 1
+ XTB = 2.102
+ EG   = 1.110
+ XTI  = 1.690
+ CJE  = 639.45f
+ VJE  = 0.871
+ MJE  = 0.431
+ TF   = 14.7n
+ XTF = 5.00
+ VTF  = 713.0m
+ ITF  = 4.50m
+ PTF  = 0.000
+ CJC  = 8.465f
+ VJC  = 0.561
+ MJC  = 0.329
+ XCJC = 380.0m
+ TR   = 769.0p
+ FC   = 800.0m
+ TNOM = 27
```

Gummel-Poon Bipolar Model for the 4.5um Basewidth NPN

```
.MODEL  LNPN NPNA
+ IS   = 0.657f
+ BF   = 7
+ NF   = 0.992
+ VAF = 100
+ IKF  = 100m
+ ISE  = 4f
+ NE   = 1.45
+ BR   = 1
+ NR   = 1.09
+ VAR= 7.9
+ IKR  = 1m
+ ISC  = 0.6f
+ NC   = 1.1
+ RB   = 1.1
+ IRB  = 1n
+ RBM = 1
+ RE   = 1
+ RC   = 1
+ XTB = 2.102
+ EG   = 1.110
+ XTI  = 1.690
+ CJE  = 639.45f
+ VJE  = 0.808
+ MJE  = 0.689
+ TF   = 0.05n
+ XTF = 5.00
+ VTF  = 713.0m
+ ITF  = 4.50m
+ PTF  = 0.000
+ CJC  = 8.465f
+ VJC  = 0.561
+ MJC  = 0.329
+ XCJC = 380.0m
+ TR   = 769.0p
+ FC   = 800.0m
+ TNOM = 27
```

Gummel-Poon Model for the 9um Basewidth NPN

```
.MODEL  LNPNB NPN
+ IS   = 0.365f
+ BF   = 3.5
+ NF   = 0.978
+ VAF = 75
+ IKF  = 100m
+ ISE  = 0.115f
+ NE   = 1.063
+ BR   = 0.8
+ NR   = 0.9774
+ VAR= 40
+ IKR  = 6.407m
+ ISC  = 1.321f
+ NC   = 1.041
+ RB   = 1.1
+ IRB  = 1n
+ RBM = 1
+ RE   = 1
+ RC   = 1
+ XTB = 2.102
+ EG   = 1.110
+ XTI  = 1.690
+ CJE  = 437.64f
+ VJE  = 0.808
+ MJE  = 0.689
+ TF   = 1n
+ XTF = 5.00
+ VTF  = 713.0m
+ ITF  = 4.50m
+ PTF  = 0.000
+ CJC  = 8.465f
+ VJC  = 0.561
+ MJC  = 0.329
+ XCJC = 380.0m
+ TR   = 769.0p
+ FC   = 800.0m
+ TNOM = 27
```

SUB-CIRCUIT MODEL FOR SCRA

```
.SUBCKT SCRA ANODE CATHODE SUBSTRATE
RG    ANODE 11 PWL(1) ANODE 11 RF 1
RM1   ANODE 3 PWL(1) ANODE 3 MOATRB 1
D1    10 3 DNRES
RM2   3 4 PWL(1) 3 4 MOATRB 1
RM3   4 5 PWL(1) 4 5 MOATRB 1
D2    10 ANODE DNWPW
RC    ANODE 6 110
RB    10 SUBSTRATE 1K
M1 5 0 CATHODE 10 NCH  W=90.0 L=1.35 ESDMOD RSS=3 RDD=3
Q1 10 6 11 VPNP
Q2 6 10 CATHODE LNPNA
.ENDS SCRA
```

SUB-CIRCUIT MODEL FOR SCRB

```
.SUBCKT SCRB ANODE CATHODE SUBSTRATE
RG   ANODE 11 PWL(1) ANODE 11 RF 1
RM1  ANODE 3 PWL(1) ANODE 3 MOATRB 1
D1   10 3 DNRES
RM2  3 4 PWL(1) 3 4 MOATRB 1
RM3  4 5 PWL(1) 4 5 MOATRB 1
D2   10 ANODE DNWPW
RC   ANODE 6 110
RB   10 SUBSTRATE 1K
M1 5 0 CATHODE 10 NCH  W=90.0 L=1.35 ESDMOD RSS=3 RDD=3
Q1 10 6 11 VPNP
Q2 6 10 CATHODE LNPNB
.ENDS SCRB
```

SPICE DECK FOR SIMULATING SCR STEADY STATE CHARACTERISTICS

```
.WIDTH OUT=256
.TEMP 27
.LIB dsn=.models

**Apply a 25V Trapezoidal Pulse with 2.5 microsecond rise time, 5 microsecond
** duration, and a 5 microsecond fall time
VIN   1 0 PULSE 0 25 0 2500E-9 5000e-9 5000E-9 50E-6

** The circuit consists of a series resistor tied to the SCR input pad; the SCR is a 3
** terminal device
RS   1 2 120
Xscra 2 0 0 SCRA

** Simulate using 5 nanosecond time steps, over the duration of the pulse; write the
** data at 20 nanosecond intervals
.TR TSTEP=20E-9 TSTOP=12550E-9 TMAX=5E-9

** Print out the input voltage, the SCR pad voltage, series resistor current, bipolar
** collector currents, and the NMOS drain current
.PRINT TR V(1) V(2) I(RS) I(Xscra.Q1,C) I(Xscra.Q2,C) I(Xscra.M1,D)

.PUNCH TR V(1) V(2) I(RS) I(Xscra.Q1,C) I(Xscra.Q2,C) I(Xscra.M1,D)

.END
```

REFERENCES

1. C. C. Johnson, T. J. Maloney, and S. Qawami, "Two Unusual HBM ESD Failure Mechanisms on a Mature CMOS Process," presented at EOS/ESD Symposium, 1993.

2. A. Steinman, "Static Charge: It's a Killer!" in *Semiconductor International*, 1994, pp. 73-75.

3. M. Corsi, R. Nimmo, and F. Fattori, "ESD Protection of BiCMOS Integrated Circuits which need to operate in the Harsh Environments of Automotive or Industrial," presented at EOS/ESD Symposium, 1993.

4. T. N. Bhar and E. J. McMahon, *Electrostatic Discharge Control.* Rochelle Park: Hayden Book Company, Inc., 1983.

5. A. Chatterjee and T. Polgreen, "A Low-Voltage Triggering SCR for On-Chip ESD Protection at Output and Input Pads," *IEEE Electron Device Letters*, vol. 12, pp. 21-22, 1991.

6. M. D. Ker, "Lateral SCR Devices with Low-Voltage High-Current Triggering Characteristics for Output ESD Protection in Submicron CMOS Technology," *IEEE Transactions on Electron Devices*, vol. 45, pp. 849-860, 1998.

7. M. D. Ker and C. Y. Wu, "CMOS On-Chip Electrostatic Discharge Protection Circuit Using Four-SCR Structures With Low ESD-Trigger Voltage," *Solid State Electronics*, vol. 37, pp. 17-26, 1994.

8. L. R. Avery, "Using SCR's As Transient Protection Structures in Integrated Circuits," presented at EOS/ESD Symposium, Las Vegas, Nevada, 1983.

9. T. Li, D. Suh, S. Ramaswamy, P. Bendix, E. Rosenbaum, A. Kapoor, and S. M. Kang, "Study of a CMOS I/O Protection Circuit Using Circuit-Level Simulation," presented at International Reliability Physics Symposium, 1997.

10. J. T. Watt and A. J. Walker, "A Hot-Carrier Triggered SCR for Smart Power Bus ESD Protection," presented at International Electron Devices Meeting, Washington, DC, 1995.

11. C. H. Diaz, S. M. Kang, and C. Duvvury, *Modeling of Electrical Overstress in Integrated Circuits*. Boston: Kluwer Academic Publishers, 1995.

12. B. J. Baliga, *Power Semiconductor Devices*. Boston: PWS Publishing Company, 1996.

13. C. Duvvury and A. Amerasekera, "ESD: A Pervasive Reliability Concern for IC Technologies," *Proceedings of the IEEE*, vol. 81, pp. 690-702, 1993.

14. C. H. Diaz and S. M. Kang, "New Algorithms for Circuit Simulation of Device Breakdown," *IEEE Transactions on Computer Aided Design*, vol. 11, pp. 1344-1354, 1992.

15. C. H. Diaz, S. M. Kang, and C. Duvvury, "Circuit-Level Electrothermal Simulation of Electrical Overstress Failures in Advanced MOS I/O Protection Devices," *IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems*, vol. 13, pp. 482-493, 1994.

16. A. Amerasekera, A. Chatterjee, and M. C. Chang, "Prediction of ESD Robustness in a Process Using 2-D Device Simulations," presented at International Reliability Physics Symposium, 1993.

17. K. Kurimoto and e. al., "An Electrothermal Circuit Simulation using An Equivalent Thermal Network for Electrostatic Discharge (ESD)," presented at Symposium on VLSI Technology, 1994.

18. H. K. Gummel and H. C. Poon, "An integral charge-control model of bipolar transistors," *Bell Systems Technical Journal*, pp. 827, 1970.

19. I. E. Getreu, *Modeling the Bipolar Transistor*, vol. 1. New York: Elsevier Scientific Publishing Company, 1978.

20. A. S. Grove, *Physics and Technology of Semiconductor Devices*. New York: John Wiley & Sons, 1967.

21. C. Duvvury, R. N. Rountree, H. J. Stiegler, T. Polgreen, and D. Corum, "ESD Phenomena in Graded Junction Devices," presented at International Reliability Physics Symposium, 1989.

22. G. Meneghesso, J. R. M. Luchies, F. G. Kuper, and A. J. Mouthaan, "Turn-On Speed of Grounded Gate NMOS ESD Protection Transistors," *Microelectronics Reliability*, vol. 36, pp. 1735-1738, 1996.

23. S. K. Ghandi, *Semiconductor Power Devices*. New York: John Wiley & Sons, 1977.

24. D. J. Roulston, *Bipolar Semiconductor Devices*. New York: McGraw-Hill Publishing Company, 1990.

25. G. Krieger, "The Dynamics of Electrostatic Discharge Prior to Bipolar Action Related Snap-Back," presented at EOS/ESD Symposium, 1989.

26. A. Amerasekera, L. V. Roozendaal, J. Bruines, and F. Kuper, "Characterization and Modeling of Second Breakdown in NMOST's for the Extraction of ESD-Related Process and Design Parameters," *IEEE Transactions on Electron Devices*, vol. 38, pp. 2161-2168, 1991.

27. K.L. Chen, "Effects of Interconnect Process and Snapback Voltage on the ESD Failure Threshold of NMOS Transistors," presented at EOS/ESD Symposium, 1988.

28. M.M.S. Hassan and H. Domingos, "The Double Graded Transistor and its Beneficial Effect on Resistance to Current Mode Second Breakdown," presented at EOS/ESD Symposium, 1989.

29. F. C. Hsu, P. K. Ko, S. Tam, C. Hu, and R. S. Muller, "An Analytical Breakdown Model for Short-Channel MOSFET's," *IEEE Transactions on Electron Devices*, vol. 29, pp. 1735-1740, 1982.

30. S. E. Laux and F. H. Gaensslen, "A Study of Channel Avalanche Breakdown in Scaled n-MOSFET's," *IEEE Transactions on Electron Devices*, vol. 34, pp. 1066-1073, 1987.

31. J. R. M. Luchies, C. G. C. M. d. Kort, and J. F. Verweij, "Fast turn-on of an NMOS ESD protection transistor; measurements and simulations," presented at EOS/ESD Symposium, 1994.

32. J. C. Mitros, "Empirical Model of MOSFET Breakdown Voltages," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 12, pp. 511-515, 1993.

33. W. Muller, L. Risch, and A. Schutz, "Short-Channel MOS Transistors in the Avalanche-Multiplication Regime," *IEEE Transactions on Electron Devices*, vol. 29, pp. 1778-1784, 1982.

34. T. Polgreen and A. Chatterjee, "Improving the ESD Failure Threshold of Silicided nMOS Output Transistors by Ensuring Uniform Current Flow," presented at EOS/ESD Symposium, 1989.

35. A. Schutz, S. Selberherr, and H. W. Potzl, "A Two-Dimensional Model of the Avalanche Effect in MOS Transistors," *Solid State Electronics*, vol. 25, pp. 177-183, 1982.

36. E. Sun, J. Moll, J. Berger, and B. Alders, "Breakdown Mechanism in Short-Channel MOS Transistors," presented at International Electron Devices Meeting, 1978.

37. H. Wong, "Modeling of the Parasitic Transistor-Induced Drain Breakdown in MOSFET's," *IEEE Transactions on Electron Devices*, vol. 43, pp. 2190-2196, 1996.

38. A. Amerasekera, S. Ramaswamy, M. C. Chang, and C. Duvvury, "Modeling MOS Snapback and Parasitic Bipolar Action for Circuit-Level ESD and High Current Simulations," presented at International Reliability Physics Symposium, 1996.

39. Y. Wei, Y. Loh, C. Wang, and C. Hu, "MOSFET Drain Engineering for ESD Performance," presented at EOS/ESD Symposium, 1992.

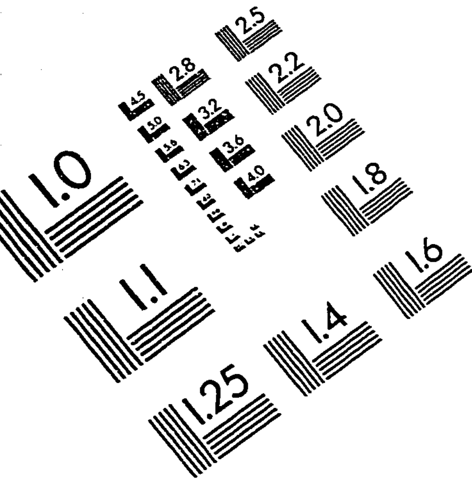
40. S. L. Lim, X. Y. Zhang, Z. Yu, S. Beebe, and R. W. Dutton, "A Computationally Stable Quasi-Empirical Compact Model for the Simulation of MOS Breakdown in ESD-Protection Circuit Design," presented at SISPAD, 1997.

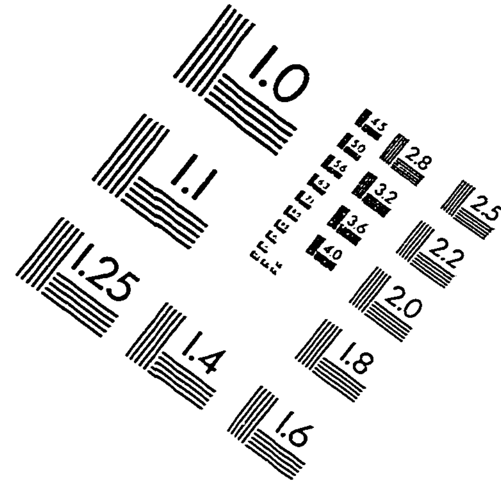
41. X. Y. Zhang, Z. Yu, S. Beebe, and R. W. Duttton, "Substrate Resistance Model for Simulating MOSFET Breakdown in ESD Protection," presented at TECHON, 1998.

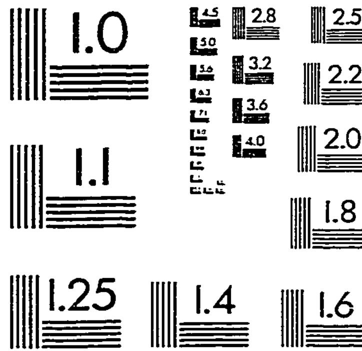
42. R. R. Troutman and H. P. Zappe, "A Transient Analysis of Latchup in Bulk CMOS," *IEEE Transactions on Electron Devices*, vol. 30, pp. 170-179, 1983.

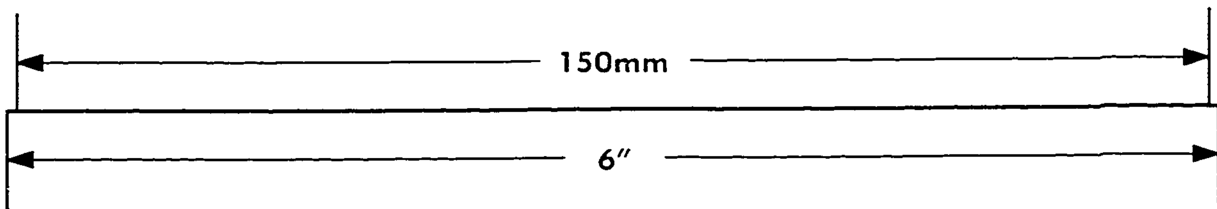
43. R. R. Troutman, *Latchup in CMOS Technology*. Boston: Kluwer Academic Publishers, 1986.

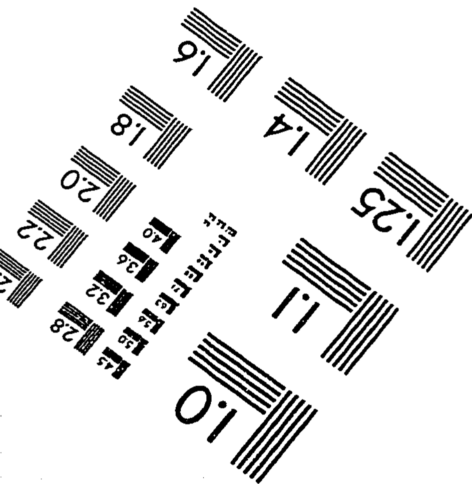
IMAGE EVALUATION TEST TARGET (QA-3)











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