ESD Design for Analog Circuits

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Springer

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ISBN 978-1-4419-6564-6 e-ISBN 978-1-4419-6565-3
DOI 10.1007/978-1-4419-6565-3
Springer New York Dordrecht Heidelberg London

Library of Congress Control Number: 2010929991

To our families

Preface

This Book and Simulation Software Bundle Project

Dear Reader, this book project brings to you a unique study tool for ESD protection solutions used in analog-integrated circuit (IC) design. Quick-start learning is combined with in-depth understanding for the whole spectrum of cross-disciplinary knowledge required to excel in the ESD field. The chapters cover technical material from elementary semiconductor structure and device levels up to complex analog circuit design examples and case studies.

The book project provides two different options for learning the material. The printed material can be studied as any regular technical textbook. At the same time, another option adds parallel exercise using the trial version of a complementary commercial simulation tool with prepared simulation examples.

Combination of the textbook material with numerical simulation experience presents a unique opportunity to gain a level of expertise that is hard to achieve otherwise. The book is bundled with simplified trial version of commercial mixed-mode simulation software from Angstrom Design Automation. The DECIMM^{TM} (Device Circuit Mixed-Mode) simulator tool and complementary to the book simulation examples can be downloaded from www.analogesd.com. The simulation examples prepared by the authors support the specific examples discussed across the book chapters.

A key idea behind this project is to provide an opportunity to not only study the book material but also gain a much deeper understanding of the subject by direct experience through practical simulation examples.

Each section of the book is accompanied by a set of simulation examples directly related to the main topics addressed in the section.

The examples are not just snapshots of the simulation results. Instead the reader has an option to use real simulation software tool. This allows the reader a practical opportunity to understand the ESD simulation examples by interactively studying the simulation results and changing simulation parameters within the limits of the trial version.

At the same time, the simulator software does not require any advanced skills in the technology computer sided design (TCAD) area. The authors of this book

and DECIMM^{TM} simulation tool developers believe that interactive features of the new tool will allow any electrical engineer or circuit designer to run the simulations successfully.

Although the free version of the simulation has some limitations compared to the full version, functionality of the free version is more than sufficient for it to be an indispensable tool in mastering of the subject of this book.

Nevertheless, the readers who do not want to take an advantage of the simulation or prefer to postpone the experience can read the textbook as any regular technical textbook.

The body of the book is prepared absolutely independent from the simulation examples, which are referred to only at the end of each chapter.

Subject and Purpose of This Book

ESD design for analog circuits is a very diverse and cross-disciplinary field. It involves an understanding of semiconductor device physics in strong non-linear operation regime deep knowledge of modern CMOS, BICMOS, and BCD process technologies, expertise in analog circuit design mixed with understanding of the product application conditions and specs, and even trends in marketing for analog integrated components.

Therefore, one of the major challenges accepted by the authors of this book consists in selection of an appropriate depth of material that will provide practical help in successful ESD design and can still be accessible enough to be used by a broad audience. This challenge requires both an appropriate simplification to fit the material within the limits of a single textbook and a new methodology to present the material. The methodology is based on combining the phenomenological approach and simulation results.

The book is organized in a hierarchy from the semiconductor device level to the product circuit level. In theory, each chapter can be studied independently. The seven chapters of the book address the following hierarchical levels:

I. Semiconductor Structures
II. Integrated Standard and ESD Devices
III. ESD Clamp Design Principles
IV. ESD Protection Network Design Principles
V. Protection of Signal Path Analog Integrated Circuits
VI. Protection of Power Management Analog Integrated Circuits
VII. System Level and Discrete Component ESD

This book targets all major aspects of ESD protection: device, network, and circuit design levels, mainly focusing on modern integrated components. System level and discrete component's ESD protection is addressed too in the last chapter.

This hierarchy is established in order to enable both sequential and independent study of the material depending of specific reader expertise and preference.

The authors expect that ESD engineers as well as students would appreciate a systematic representation of the material in increasing level of complexity. This approach covers the major background knowledge required for understanding the material.

Professionals already working in this field with engineering background expertise in device design may find it useful to skip the device chapters and proceed to the ESD network and analog circuit design material, while experts in circuit design may benefit from the device physics material that covers physical principles of conductivity modulation in semiconductor structures.

The authors believe that an option to interactively study the simulation examples will greatly benefit all readers.

The overall purpose of this book is to help professionals in the field to deal with the *Analog ESD Design* issues in their everyday professional work, attacking problems at all hierarchical levels starting from the device ESD level up to an implementation of integrated self-protecting solutions. The book is supposed to "arm" readers not only with important practical and technical knowledge, but also to add a complementary simulation experience that can be further developed with the light version of new industrial mixed mode simulation software DECIMM^{TM} from Angstrom Design Automation.

The Book Structure

The book is organized in increasing complexity of the discussed ESD subjects. This is not complexity in terms of understanding, since that will depend on the level of expertise – circuit or device design – with which an engineering professional is approaching this book. Thus, the level of complexity of the material across the chapters for circuit designers will perhaps be opposite to the level of complexity for device engineers.

The *Chapter 1* to the book below represents a short review of background material relevant to the ESD field, describing the authors' understanding of the field itself, ESD pulse specification and several other general aspects. At the same time, the introduction mainly refers the readers to other previously published books in the field, in order to maximize the space in the current book for material pertaining to the goal above. As well, the introduction establishes important definitions necessary for understanding the presented material.

Chapter 2 presents introductory material to the device design field. It provides a fundamental knowledge of conductivity modulation processes in the elementary semiconductor structures: p-n, p-i-n, n-p-n, p-n-p, p-n-p-n. The physical processes in these structures are described on a simplified phenomenological level that is easy to understand and further supported by rather simple independent simulation examples.

The material presented in *Chapter 2* about conductivity modulation in the elementary structures provides a necessary fundamental background both for understanding pulsed safe operating area (SOA) of the standard devices and for the snapback mode operation of the ESD devices. Chapter 3 covers both these aspects. It presents pulsed SOA for most typical integrated components in CMOS, BiCMOS, BCD, SOI, and SiGe process technologies, highlighting the parasitic devices formed in their structures. Pulsed SOA understanding is critical for the so-called ESD protection window realized for given circuit pins.

In parallel to each standard device, *Chapter 3* deals with most typical basic ESD protection devices that could be developed as "free" components in the given process technology. The important point of low-cost ESD design methodology is the creation of such "free" ESD devices. In case of "free" devices, it is assumed that the device can be obtained using only the available mask layers without violation of the minimum design rules exceeding physical capability of the process tools. Moreover, the "free" approach challenges self-aligned solutions and solutions that are closely based upon supported standard devices. In this case, reliability of the ESD devices can be linked to the corresponding supported device characteristics.

Chapter 4 targets the ESD clamp level using the ESD devices described in *Chapter 3* as building blocks for the variety of ESD protection clamps with desired characteristics according to pin functionality.

Chapter 5 presents a summary of ESD network design. It explores ways to apply different ESD clamp solutions to "assemble" an embedded ESD power circuit across all integrated circuit pins. The ESD network provides an ESD current path between different pin combinations that, in the case of analog circuits, may involve not only the ESD pad ring components but the internal functional circuit components as well. This chapter is a major reference point for practical ESD design of analog circuits that is further expanded on in *Chapters 6* and *7*, covering signal path and power analog circuits.

Chapter 6 is focused on ESD protection for signal path analog applications. It contains condensed introductory material that highlights design aspects specific to the ESD on a sub-block level. Signal path circuits and products are mainly represented in this chapter by high speed, precision and audio amplifiers, interface application, and digital–analog converters.

The scope of *Chapter 7* lies within different power management products. Analog ESD circuit design is discussed with the examples of dc–dc converters with integrated power devices, controllers, light management units, and LED drivers.

The final *Chapter 8* is focused on the system level of ESD design and ESD for discrete components. The goal of this chapter is not to describe the system itself, but instead the integrated components with pins interfacing directly with the system terminals. The major aspects are realization of the system level ESD protection on chip. Due to this being a relatively new topic for ESD design, this chapter contains a much more comprehensive introductory portion in comparison with the well described across literature sources introduction to ESD in *Chapter 2*.

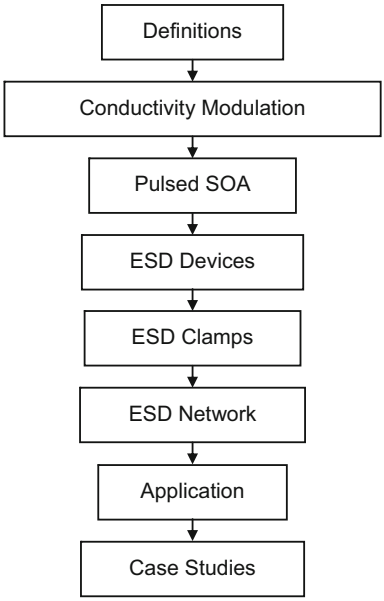

Fig. 1 Roadmap for the book composition

Finally, the last section of each Chapter provide a brief description of the simulation examples directly relevant to the material described in the Chapter. The examples are available for download from http://www.analogesd.com

Acknowledgments

The authors would like to acknowledge all their colleagues in the field who directly or indirectly helped with this book.

Vladislav Vashchenko would like to gratefully recognize his closest colleague and friend Ann Concannon from National Semiconductor for the many years of close collaboration in the ESD field that directly impacted and contributed to the creation of this book.

He would also like to acknowledge the contributions of his colleagues Alan Segerval, Donald Archer, Peter Hopper, Philippe Lindorfer, Alexei Sadovnikov, Lihui Wang, and David Lafonteese, as well as the many lead circuit designers and product engineers across the National Semiconductor Corporation with whom he worked on ESD projects with during the last decade. He is also deeply thankful for the multiple discussions of ESD subjects during the past 10 years with his colleagues in the field: Prof. Gaudenzio Meneghesso from the University of Padova, Prof. Elyse Rosenbaum from the University of Illinois, Robert Gauthier from IBM, Gianluca Boselli from Texas Instruments, Vesselin Vassilev from Novorel, Prof. Juin Lion from the University of Central Florida, Markus Mergens from QPX GmbH, Prof. Marise Bafleur from LAAS, Theo Smedes from NXP, Kai Goebel from AMES NASA, and many other colleagues and professional friends from the ESD Association and Industry. In particular, Vladislav considerably appreciates the many contributions and support of his current and past direct researcher collaborators and co-authors Dimitri Linten Mirko Scholz, Philippe Jansen, and Steven Thijs from IMEC, as well as PhD students Nicholas Olson, James Di Sarro, and Blerina Alija. He is also appreciative of his former mentors Prof. Vladimir Sinkevitch from Pulsar, Slava Osipov from AMES NASA and Boris Kerner from Daimler AG.

Andrei Shibkov would like to acknowledge many of his former colleagues from PDF solutions, in particular Carlo Guardiani.

The authors are grateful for analog design expert Vladislav Potanin, National Semiconductor, who reviewed Chapters 6 and 7 and provided very valuable comments to the material.

The authors greatly value the support and understanding provided by their families during the time devoted to this book project.

Finally, both authors would like to emphasize a critical contribution to this book by Yana Vashchenko, a first-year UCLA student, who spent many days during the

summer of 2009 performing a complete language and style edition for the whole book. They hope this practice will help her to become a better bioengineer in the future.

Contents

Chapter 1
Introduction

Readers proficient in the ESD field may decide to skip this introductory section. The section briefly summarizes the background directly relevant to the ESD field. This is done to facilitate the study of the following chapters for those who are not directly involved in the field or want to refresh the most important aspects of the knowledge. A broader spectrum of ESD background material is brilliantly covered in many books and reviews [1–7] written in the field, as well as in EOS/ESD Symposium Proceedings [8]. The purpose of this section is to summarize the general ESD approach to integrated components design and provide condensed reference material related to the ESD pulse specification, and standards. Finally, the most important definitions used across this book are established.

1.1 Analog and Digital in Prism of ESD Design

Historically, integrated circuits can be roughly subdivided into analog and digital categories. These classifications are currently used in the industry and are based upon functionality and design principles of ICs. Even in the case of complex mixed-signal circuits, different analog and digital domains can be identified and corresponding ESD methodology specific to either analog or digital circuits can be applied for each specific domain. The book title emphasizes "analog" as a major focus of the presented material due to several reasons. However, practically the material can be treated as universal ESD design guidelines for mixed-signal circuits, perhaps excluding practical examples of the most scaled down digital CMOS processes of 90–32 nm. At the same time, the digital domains in analog IC components built using 0.13–1 μm process technologies are well covered in Chapters 4 and 5 by active clamp solutions. These circuit blocks represent digital interface, digital control pins, and digital domains.

From an ESD design point of view, the digital circuits and digital circuit domains in mixed-mode circuits are different from analog circuits. The most straightforward way to identify the type of circuit is by the type of signal transferred through the circuit pins.

V.A. Vashchenko, A. Shibkov, *ESD Design for Analog Circuits*,
DOI 10.1007/978-1-4419-6565-3_1, © Springer Science+Business Media, LLC 2010

From the practical ESD design point of view, the difference between analog and digital designs is often reflected in the ESD pad ring circuit block. In case of the fully digital circuit, ESD protection is usually designed in the pad I/O (input/output) and power domains. In this case, the periphery of the digital circuit is expected to be practically fully isolated from the internal circuit.

When I/O and ESD library is designed and validated it can support wide variety of internal digital blocks with different functionalities. In this case, beyond the ESD/IO library creation itself, the major focus of ESD chip design is to ensure proper pad ring layout design that accounts for the voltage drop on metallization busses, number of clamps, and RC timers and make sure that current path for every pin-to-pin combination is addressed. As well, at appropriate voltage limitation, the current path is always expected to be confined within the ESD pad ring network. In the case of high-pin count digital ICs the problem complexity requires automated tools in form of ESD rule checkers.

The above is not intended to trivialize digital ESD design. Digital ESD design has its own complexity. For example, one of the most significant challenges is covering the specifics of high-pin count digital IC products, especially in the case of CMOS processes scaled down to 90–32 nm gate dimension. In this case, one of the major challenges is CDM (charged device model) pulse protection of the large form factor packages. There are many challenges in protection of high-speed and RF I/O pins, as well as system-level protection.

However, in the case of widely used analog 0.5 μm process technologies the digital pin protection hardly presents any real challenge. The methodologies for such protection are very well established.

The major reason for discussion of digital vs. analog circuitry is to emphasize the specific of ESD protection approach and solutions.

In the case of digital design, one can expect that the ESD network building blocks in pad ring design will typically provide only a single connection to the internal circuit. This connection can be relatively easy to analyze in the ESD current path analysis. At the same time, latch-up isolation is automatically provided by ESD library solutions with no or minimized interaction of the ESD and I/O circuit with other circuit nodes due to appropriately designed guard rings.

In opposite, analog ESD design guarantees no such condition. In general, the analog ESD protection design can be expected to account for the fact that the analog pad might have multiple connections to the internal circuit node. The connections can be realized both directly and indirectly by the coupling through the power components, for example, large drain–gate capacitance of multimillimeter width NLDMOS power array.

Moreover, most of these internal circuit nodes will generally have an unknown transient bias and current conditions for different pin-to-pin zap combinations. This makes it rather difficult to guess at what point of safe operating area the active device connected to the pin is. During ESD pulse, power components of the analog circuit may switch to on-state during ESD event and conduct a substantial amount of current during a part of the ESD pulse. A “sneak” current path can be formed

between the ESD clamp and internal circuit components depending on the layout of the circuit, especially in case of high-voltage device.

We would like to use this type of differentiation to underscore the essence of separation between the digital and the analog *ESD designs*. The fact that a substantial amount of analog products can contain digital interface pins and domains does not change this approach to ESD design principles.

Thus, in the case of *digital ESD design*, the ESD approach can be unified and formalized to be somewhat independent from the internal circuit blocks as long as their type is identified and appropriate ESD or ESD/IO library cells selected with ESD pad ring and created in accordance with the library guidelines. In opposite, in the case of *analog ESD design*, a practical ESD design should often be customized for new circuit changes, taking into account possible alternative scenarios for ESD current conduction through the internal circuit. These potentially new scenarios should be then taken into account for both ESD network design and ESD clamp choice.

Thus, one of the most critical features of the analog vs. digital designs is the ESD protection network and the internal circuit in general cannot be separated. This creates a need for the ESD engineer to understand the analog circuit at much greater depth.

Another important distinct feature from ESD perspective is the product pin count. Digital products often have hundreds of pins, while some small form factor analog products might have as few as three to five pins. This fact automatically brings into consideration the critical issue of the space used on the chip for ESD protection.

In the case of digital circuit with a high pin count, the chip periphery is relatively large and a distributed active clamp solution is relatively spatially optimal, usually requiring space, the size of one pad at each pad. Therefore, perhaps over 90% of the digital circuits are protected by the distributed active clamp solution.

A different situation can be often found in case of analog circuits. There are many examples of small-pin-count analog ICs where over 50% of the silicon die space is taken up by ESD clamps. In this case, space saving and small footprint solutions can provide a major impact on the product cost.

At the same time, the voltage tolerance for the ESD clamps that corresponds to the digital signal levels is rather low. In the case of mature process technologies, this makes even the local protection option relatively easy to address. The opposite situation is found in case of high-voltage analog products where an optimal high-voltage solution might be rather hard to find without changes to process technology.

The purpose of this book is to help professionals in the field to deal with the *analog ESD design* issues in their everyday professional work, attacking problems at all hierarchical levels starting from the device ESD level up to an implementation of integrated self-protecting solutions. The book is supposed to "arm" readers not only with important practical and technical knowledge but also to add a complementary simulation experience that can be further developed with the new mixed-mode simulation software DECIMM^{TM} from Angstrom Design Automation.

1.2 Important Definitions

1.2.1 ESD Protection Network

Practically every book written in the ESD field well describes the nature of phenomena behind ESD charge accumulation and the discharge events [1–4]. Over time the specs created for industrial application move further away from real events that may cause charging or the objects that can provide discharge through IC pins.

Therefore, to avoid redundancy and save space in this book, the starting point for the ESD subject is presented from a slightly different angle.

Without loss of generality, we will assume the following approach to the subject. An integrated circuit represents an object that contains both internal circuitry components and external pads. A discrete component can be treated as a particular case of IC where internal circuitry is represented by a single or few devices packaged together. Similarly a system can be considered as a combination of circuit blocks that contain mounted, integrated, and discrete components with external terminals.

The pads are bonded to package and pins. The pins could be package pins, system socket connectors, or device leads.

The ESD protection task will be further treated simply as an added ability to the integrated components or systems, or discrete components to withstand certain ESD pulse specification.

In this case, the ESD protection capability is treated as a part ICs or system specification similar to other normal specification parameters for the internal circuit performance and reliability.

In most practical cases of analog integrated components design, this added ability to withstand certain level of ESD pulse spec is achieved through a co-design of the internal circuitry and the ESD protection network. Therefore, an idea of separation between the ESD network and internal circuitry as well as corresponding requirements for non-conflicting existence of the ESD protection solution with the circuit performance is perhaps irrelevant.

Nevertheless, the ESD co-design goal is to minimize the impact of the ESD network components on the ideal circuit performance that could have been accomplished if ESD performance was not specified.

Similar reasoning is relevant for system-level ESD where normal product operation during ESD and electrical overstress (EOS) events may be required. System-level ESD protection is presented in Chapter 8.

Thus, a problem of ESD development can be formulated as the implementation of an embedded capability of integrated products toward withstanding standard ESD tests according to defined specification.

From a circuit design point of view, this essentially means an extra functionality of the integrated product circuit at some specific high-current pulse conditions in addition to normal operation specification targets.

There are several ways to realize such capability. One of the major principles is to implement additional peripheral ESD protection networks connected in parallel with the original functional circuit blocks. However, analog ESD design often relies

on the self-protection capability of the internal components. The self-protection of the internal components can be exploited both up to the level of the full ESD current conduction and using much smaller current levels through the internal circuit to enable a two-stage protection. In principle, a pin-specific combination of the above measures is usually used.

Thus, in general, the product can be considered as a superposition of internal functional circuit blocks and additional pulsed power circuit dealing with ESD current. This circuit can partly use the components of the functional circuit blocks. This pulsed power circuit can further be understood as the *ESD protection network*.

The major functionality of the ESD protection network is to provide a high-current path with appropriate voltage limitation in case of ESD discharge applied for every pin-to-pin combination. Under the appropriate voltage limitation requirements, a limitation of the voltage in the ESD time domain below the pulsed safe-operating area (SOA) is understood for the device. Thus, the ESD protection network should not only provide the ESD current path but also limit the voltage below absolute maximum rating conditions realized at each pin. The pulsed absolute maximum rating provided by the circuit at each pin is rather complex figure of merit that depends on time domain, rise time, maximum ratings of the devices connected to the pin, coupling of their control electrodes, and other factors that could be related to a parasitic current path realized in the actual layout.

Thus, the task can be converged into co-design and embedding of the ESD network. ESD network design principles are discussed in Chapter 5.

As has been already mentioned, this network can partly be realized using the self-protection capability of the active circuit components. However, major building blocks are the *ESD protection clamps,* connected by an appropriate metallization routing for given pulsed current level.

An ESD protection clamp usually presents itself as self-triggered in the high-current state. The self-turn-off event of clamps usually occurs due to discharge of the ESD pulse. There are two major categories of ESD protection clamps. The first uses the RC network to control on and off state conditions for the active devices. In this case, the high-current device is fully controlled in high-current mode and can be turned off by the RC network.

Another major class of *ESD clamps* is based upon avalanche breakdown and snapback *ESD devices* that involve different conductivity modulation mechanisms in order to achieve high-current conditions. Unlike active clamps, the turn-off of ESD devices with conductivity modulation usually cannot be practically controlled by a driver circuitry. The ESD device operates in the conductivity modulation mode up until the voltage conditions are changed simply due to the end of the ESD discharge, or the voltage level will be naturally reduced below the holding voltage of the snapback components or below the breakdown voltage.

The major principles for ESD clamps design are discussed in Chapter 4. The ESD devices are presented in Chapter 3. The principles of conductivity modulation are presented in Chapter 2.

1.2.2 ESD Clamps

The building blocks of the ESD protection network are the *ESD clamps*. Under ESD clamp we will further understand a simple circuit that provides pulsed ESD current path under certain conditions. These conditions are generally defined as achieving the critical voltage level or a fast rise time. In most sophisticated cases, the clamp operation can be controlled or enabled by the additional control electrode. ESD clamps are discussed in Chapter 4.

The clamp can be designed using integrated components operating in normal operation mode of monopolar or bipolar current conduction. This principle is the basis of active clamps discussed in Chapter 4.

One of the most critical requirements of the ESD protection network toward competitive advantage of the product is to occupy the feasibly smallest space on the chip. Therefore, a proper way to achieve such capability is the implementation of small footprint device-level solutions, taking an advantage of several isothermal conductivity modulation mechanisms that can be realized in such devices. Thus, for analog design, the most useful clamps are the ones reversibly operating in high injection and breakdown modes.

Typical device-level ESD solutions are essentially pulsed power devices with some biasing components that are specifically designed to work in the high injection, breakdown, and conductivity modulation modes.

ESD clamp development involves a rather broad set of cross-disciplinary tasks in the fields of circuit design, physics of semiconductor devices, physical ESD clamp design with non-linear physics aspects of the operation, effects in interconnects, materials, and topological array problems to balance the current density distribution. Finally, the most important necessary expertise involves a deep understanding of process technology including the options and the limits.

Meantime, as has been shown in [9] and will be particularly illustrated in detail in Chapter 2, the physical phenomena responsible for conductivity modulation used in ESD devices are very limited to several physical mechanisms that can be analyzed using elementary diode, triode, and thyristor semiconductor structures. These practically useful mechanisms include avalanche breakdown, avalanche–injection, double-avalanche–injection, and double injection. At this point of ESD field evolution, there were no reports of using other conductivity modulation mechanisms for practical ESD design. Similarly, due to short ESD pulse time domain, the conductivity modulation mechanism based upon thermal carrier generation plays a secondary role, mainly limiting the high current capabilities of the ESD device itself [9]. This limitation is discussed in Chapter 3.

The operation in these breakdown conditions generates high current densities presented in Table 1.1. In case of avalanche breakdown, the carriers are generated in the region with a rather high electric field and are separated proving practically no mutual space charge neutralization. In this case, relatively low current density can be achieved. In case of avalanche–injection, the mutual space charge compensation of the carriers generated in the avalanche region and injected creates more favorable conditions for high current density. The highest current levels are provided in

Table 1.1 Conductivity modulation mechanisms realized in ESD devices for high current density

Conductivity modulation mechanism	Typical ESD devices	Typical lateral current density (mA/μm)
Avalanche breakdown	Avalanche diodes; blocking junctions, PMOS, PNP	0.01–0.1
Avalanche–injection	Snapback NMOS; NPN, field oxide devices	0.1–3
Double-avalanche–injection	P–i–n, M–i–n diodes	0.1
Double injection	LVTSCR, SCR, bipolar SCR, LDMOS-SCR	10–100

the case of double injection, when the avalanche multiplication is supressed in the structure (see Chapter 2).

One of the challenges in creating an appropriate ESD device is balancing the conductivity modulation current density inside the device to achieve an appropriate current level. In this case, a linear width scaling of the ESD current can be expected in the device. Since some of the mechanisms provide a positive feedback that in general can result in uncontrollable current density increase, a negative feedback loop should be implemented in the device to limit the current density below critical limits.

ESD devices are discussed in Chapter 3, while basic principles of the conductivity modulation in semiconductor structures are discussed in Chapter 2.

1.2.3 Absolute Maximum Limits and Pulsed SOA

As has been stated above, on a formal circuit design level upon given spec, the ESD functionality is achieved by implementation of a pulsed power circuit embedded into the normal circuit using shared and dedicated components. This partly virtual secondary pulsed power circuit should not only provide a pulsed power operation for the pin-to-pin current path scenario but also limit voltage below the damage level of the internal circuit blocks.

Thus, realization of the voltage waveform parameters in the ESD time domain is a major challenge, considering the absence of the limitations in normal circuit operation regime. Thus, the ESD protection network should provide voltage waveforms that will limit the voltage below the absolute maximum limits on the pin, but at the same time will not cause false turn-on during normal operation. Practically, this means that the turn-on voltage should be realized above absolute maximum limits specified for the circuit operation modes in all data sheet conditions including the temperature range.

These two limits define the so-called ESD protection window. While the lower limit of ESD protection window can be sourced from the circuit application spec, the upper limit is a more complex matter. In principle, a preliminary idea about

absolute maximum limits for the particular pin can be "extracted" from the pulsed SOA of the devices directly connected to the pin. However, the problem is that most of electrical design rules for process technology usually do not provide pulsed SOA in the ESD time domain.

Another major issue is unknown coupling effect of the control electrodes of the devices connected to the pin in the ESD test modes. In this case, the uncertainty is related to the selection of the SOA regime for identifying the ESD protection window.

There are no universal recipes for identifying the ESD protection window for analog circuit pins before the actual ESD tests. One of the most productive approaches is based upon transmission line measurements (TLP) for pulsed SOA. These SOA aspects are discussed in Chapter 3 for most typical devices realized in BCD (bipolar CMOS DMOS) process technology.

1.2.4 ESD Pulse Specification

During the era of integrated product development, various specifications for ESD pulse have been created and became industry or custom standards. The detailed description of the ESD pulse characteristics and the equivalent circuits can be found in the introductory chapters of numerous popular books in the field, for example [1–4], original publications [8], and standard documents, for example [10–13].

The standards for the human body model (HBM) pulse are as follows: ESDA (ANSI) STM5.1-2001; JEDEC JESD22-A114-E; IEC 613240-3-1; AEC Q100-002 REV-D; and EIAJ ED-4701/304. Similar standards can be found for the machine model (MM), the charged device model (CDM), and the ESD system level [13]. The consolidated summary of most commonly used ESD pulses is presented in Table 1.2. Standard non-system-level corporate requirements for the HBM, MM, and CDM ESD passing levels are 2 kV, 200 V, and 1 kV, respectively.

Table 1.2 The most common examples of non-system-level ESD pulse parameters

ESD pulse	Peak current to pulse voltage ratio (A/kV)	Rise time/pulse width (ns)
Human body model	0.67	2–10/150
Machine model	17.5	2–10/66–90
Charged device model	9	0.25/2
EN (IEC) 61000-4-2	3.75	0.2/50–150

From an ESD device design challenges perspective, there are two major spec types: the non-system level and the system level. The non-system-level spec usually targets some minimal requirements to protect the integrated circuit component while incorporating it into the system, packaging, handling, and electrical tests. For example, the HBM ESD pulse spec for the non-system level requires withstanding

some pulsed current level of ~1.33 A with the rise time of ~2–10 ns (Table 1.2). Respectively, the test is conducted in the conditions of the unpowered circuit.

In opposite to the non-system packaged specs, system-level specs are targeting protection of some circuit pins under normal operation conditions. In addition to this, usual system-level requirements target much higher current levels that can be practically realized in a non-ESD protected environment. The complexity of the system-level protection problem is related to a possibility of transient latch-up. Transient latch-up can be realized in case if ESD clamp provides a holding voltage lower than the power supply voltage under the minimum holding current below the current that can be provided by the power supply.

Due to fast rise time, in most cases ESD pulse automatically provides the conditions for pure electrical turn-on. Electrical current instability is initiated in quasi-isothermal conditions and provides further triggering of a high-current conductivity modulation state. In most practical cases, the lattice temperature change can be neglected before the triggering due to uniform current distribution and short time before the triggering.

After the switching, heat dissipation becomes significant. However, the heat dissipation scenario is significantly different from dc operation. Due to rather short pulse duration, the heat dissipation is realized in a rather small area of few microns in the vicinity of the device's active region. Thermal heat dissipation (as well as electro-mechanical stress and dielectric breakdown) and backend limits provide physical limitations for ESD device operation. These effects are illustrated in Chapter 3.

1.2.5 Breakdown and Instability

In the majority of cases, ESD events in semiconductor structure are close to adiabatic conditions. In spite of high current density, due to very fast switching time and fast ESD pulse (~100 ns), the heat generation is confined in rather local area (Fig. 1.1).

This phenomenon eliminates a significant amount of physical effects related to the carrier generation in the drift regions, epi-layers, substrate, and corresponding current instability phenomena.

The thermal effects further play an important role in the final irreversible catastrophic phenomena when ESD device fails.

The phenomena of irreversible breakdown, burnout, thermal and isothermal instability, and current filamentation are often mentioned in respect to semiconductor device failure in the case of both ESD and EOS events.

In this book, the notion "breakdown" preserves its elementary primary sense. The breakdown is treated similar to the effect in p–n semiconductor junctions as a process of sharp current increase that is caused by the carrier generation current.

Practically for the ESD field, the only important cases are isothermal avalanche and tunneling breakdown.

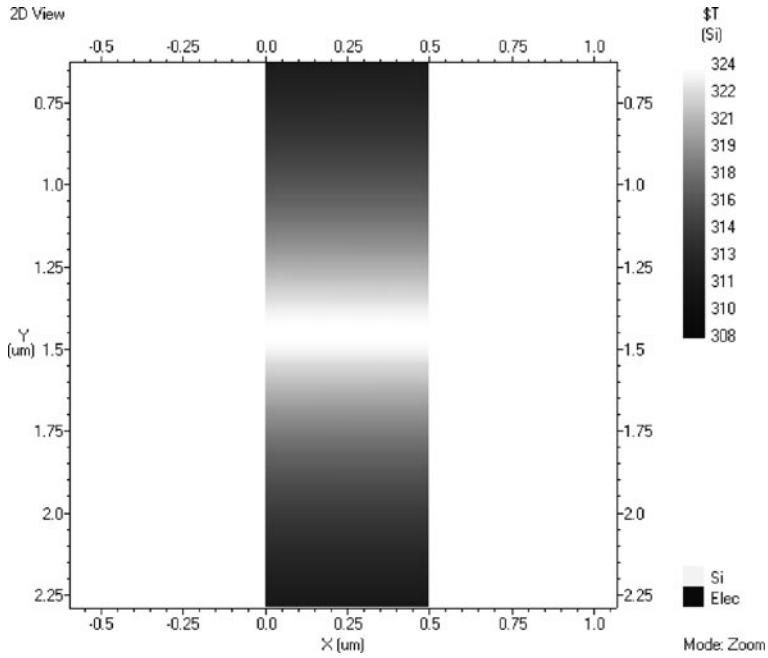

Fig. 1.1 Simulation example: local heating in collector region of NPN transistor caused by 100 ns stress pulse

In avalanche breakdown of the reverse-biased p–n junction, current I increases with voltage U increase according to the known empirical formula [14]:

$$I \sim \frac{1}{1 - \left(U/U_{\mathrm{BR}}\right)^{n}},$$

where $n = 4$–6 for Si material and U_{BR} is the avalanche breakdown voltage. The dependence $I(U)$ in this case of "classical" avalanche breakdown is strictly monotonic.

A different kind of breakdown could be observed in a case where injection and conductivity modulation are involved. In this case, current increase can create complex S-shaped I–V characteristics of the devices.

The current instability can be defined as a process of uncontrollable current increase due to voltage decrease.

This phenomenon in general may or may not result in irreversible device failure due to the appearance of some limiting factors. In the case of the ESD device, the current instability is used to create low dissipated power conditions in conductivity modulation mode. To avoid high-amplitude filaments, the local current density is limited internally on the device. Implementation of such limitation is an essential part of ESD device architectural design.

Thus, the physical definition of the breakdown is just a sharp current increase under positive differential conductivity. In other words, the breakdown itself does not include any positive feedback. The major breakdown mechanisms in semiconductors are the avalanche and the thermal, although several additional mechanisms can be found, for example, the breakdown related to the change in trap charge state or dielectric breakdown.

In opposite to the breakdown, different electrical and thermal instabilities [9] include a positive feedback. The thermoelectrical instability phenomena in semiconductor devices are rather complex. To provide a "quick start" in understanding the physical sense of these phenomena, we present below the example of thermal instability in semiconductor structure.

The best example is the avalanche–injection conductivity modulation in NPN structures discussed in Chapter 2. An accurate analytical description for conductivity modulation mechanisms is rather complex. An example of the analytical description for the case of thermal breakdown is used below to explain the current instability phenomenon itself. Often this thermal instability case can be responsible for the physical limitation of the current level provided by ESD device [9].

In the example of bulk semiconductor structure, if at a constant voltage $U << U_{BR}$ the devices are heated by some external current source, then from some temperature level the current through the sample will grow sharply according to an exponential dependence $I \sim \exp\left(-E_G/kT\right)$, where E_G, T, and k are the energy of band gap, lattice temperature of semiconductor material, and Boltzmann's constant, respectively. This thermogeneration process for carriers is considered as a thermal breakdown.

It is assumed that on a uniform sample of bulk semiconductor with length l and area S the voltage U is supplied. The current density j through the sample is equal to $j = \sigma E = \sigma U/l$, where E is the electric field in the sample and σ is the conductivity of semiconductor material. The conductivity of semiconductor material in this case can be expressed by $\sigma \sim \exp\left(-E_G/kT\right)$.

Then, the generated heat per volume unit is equal to σE^2. It is also further assumed that heat dissipation is provided by exchange with ambient space of fixed temperature T_S. Then, heat dissipation from the surface will be proportional to $(T - T_S)^\beta$, where T is the temperature of semiconductor region and $\beta = 1$–2. The heat balance equation is given by

$$\exp\left(-\frac{E_G}{kT}\right)\frac{U^2}{l^2} = K\,(T - T_S)^\beta\,, \tag{1.1}$$

where the proportionality factor K depends on physical and geometrical parameters of the device structure. In a certain range of values of U this equation can have two solutions: T_1 and T_2 (T_1, $T_2 > T_S$). The solutions correspond to two different current values I_1 and I_2.

The I–V characteristic of such a structure is no longer as simple as avalanche breakdown and has an S-shaped view (Fig. 1.2b).

The physical meaning of the I–V characteristic can be explained as follows. On the initial region "OC," the current increase obeys dependence close to Ohm's law.

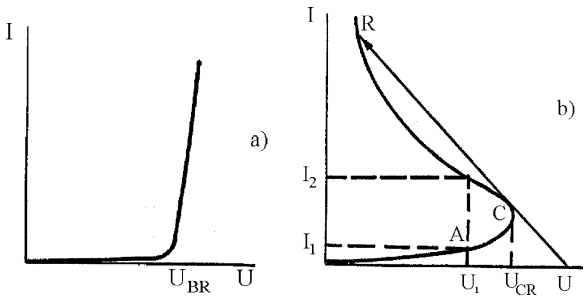

Fig. 1.2 *I–V* characteristic at avalanche breakdown of p–n junction (**a**) and at the thermal instabilities in semiconductor resistor (**b**)

An appreciable deviation from linear dependence begins when the heating reaches a higher level. The conductivity increase is connected with intensive thermogeneration of electrons and holes in the sample. Insignificant increase of the voltage on the thermal breakdown region "CA" results in a sharp increase of heat generation.

Up to a certain limit, the heat generation is balanced by an increase in temperature since the heat dissipation is proportional to $(T - T_S)^{\beta}$. However, at some $U > U_{CR}$, the exponential increase of the heat generation can no longer be compensated by heat dissipation. In this state, (1.1) has no solutions and the semiconductor sample has no stationary states, respectively. This means that in the voltage source regime at $U > U_{CR}$, a sample will be uncontrollably self-heated up to its destruction.

A similar loss of thermal stability or an uncontrollable process of transition into a new state usually means instability. In this case, the instability is of a thermal nature. From Fig. 1.2b, the stable states of a sample in the case of thermal instability can be achieved only at corresponding voltage decrease *U*. If the circuit provides a sufficient load resistance, then the thermal instability may finally evolve into a stable state that corresponds to an *I–V* characteristic with negative differential conductivity (NDC) (Fig. 1.2b, state R).

The load characteristic CR in the case of such a device in circuit operation could be called snapback.

Current instability in real device structures is not always easy to interpret due to an additional spatial current instability phenomenon.

Since in the case of current instability the local current density dependence upon voltage has negative differential resistance, a typical consequence is current stratification into filaments and hot spots.

These phenomena may or may not damage the device depending on the local damping implemented in the ESD device.

This damping can often act up to a certain electrical power limit followed by the hot spot formation in the silicon surface. Usually, the hot spot is a narrow region with a dimension of a few micrometers with concentrated current and elevated temperature. In bipolar transistors, similar current localization results in thermal breakdown. In this case, a sharp temperature increase may result in metallization melting.

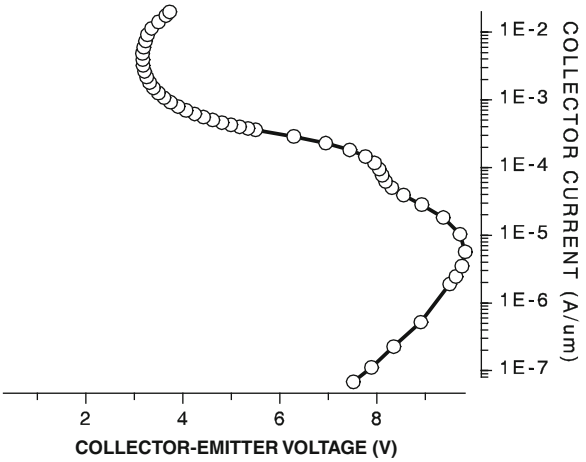

Fig. 1.3 Simulation example: snapback *I–V* in NPN

The example of thermal instability is provided above to deliver a primary understanding of processes that are extremely widespread in real device structures.

Alternatively to the analytical methods the thermal instability for given NPN structure can be obtained by numerical simulation results (Fig. 1.3) thus enabling additional way of learning.

A few summary points emphasized at the end of the introduction.

In opposite to digital, the analog circuits or analog domains in mixed-mode circuits are rather diverse in terms of the voltage tolerance and signal spec and often require small pin count. In this condition, practically every pad may require a separate ESD protection clamp limited by rather critical small footprint requirements.

This task could be solved in most cases only on the device level and thus requires understanding in three major key areas:

(i) The principles of operation of ESD devices operating in the breakdown and conductivity modulation conditions (secondary breakdown)
(ii) ESD clamp and ESD network design based upon these devices
(iii) Application of the ESD network to analog circuits and network–ESD circuit interaction

These key areas are addressed step by step in this book to enable a proficient, practical ESD design for those who are involved in the field.

Of course, once this understanding is established, a more detailed experience in the field is required based upon real product case studies. Nevertheless, we believe that in-depth knowledge about ESD components, networks, and practical examples for the analog circuit ESD protection (Chapters 6, 7, and 8) should bring ESD expertise to a new useful level and will be a relevant contribution to the field of ESD.