

## ESD MOSFET model calibration by differential evolutionary optimization algorithm

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### Anotace:

Článek prezentuje možnost využití difereciálního evolučního algoritmu ke kalibraci modelu ESD prvku na naměřená data bez nutnosti manuálního ladění parametrů tohoto modelu. Standardní přístup manuálního ladění modelu je ve srovnání s představenou metodou časově náročnější a vyžaduje dedikovaného specialistu. Zde představený přístup nebyl dle znalosti autorů dosud použit. Na úvod je vysvětlen princip funkce ESD NMOST ochrany a jejich vlastností, na což navazuje krátký popis diferenčního evolučního optimalizačního algoritmu. Na závěr jsou uvedeny výsledky kalibrace technologicky optimalizovaného makro-modelu NMOS tranzistoru na empirické, po částech lineární V-A charakteristiky

The aim of this paper is to present the utilization of modern optimization algorithm called Differential Evolution to automatically fit the measured data from test chip to the appropriate electrostatic discharge (ESD) model without the need of manual model-parameters tuning. In contrast with proposed method the traditional approach can be very time and resource consuming. To the best knowledge of the authors, this novel approach has never been previously used. Short introduction to ESD NMOST function and properties are presented along with basic overview of differential evolutionary optimization algorithm. Results of fitting the technology-optimized macro-model of NMOST to the simple piece-wise linear model of MOSFET snapback I-V characteristic will be presented.

### INTRODUCTION

The electrostatic charge has presented major danger for integrated circuits liability and lifetime since the beginning of history of a high integration. The rapid development of technologies pushes the dimensions of complementary metal-oxide-semiconductor (CMOS) devices into deep-submicron area, where especially gate oxides of input buffers are extremely prone to damage by resulted high electric field. The goal of ESD protection designers is to develop countermeasures, able to divert the charge away from the sensitive internal circuits and to clamp the resulting over-voltage below oxide-breakdown level [1]. Additionally, implemented protective measures shall not influence operational performance of protected device. Ideal protection device exhibits zero impedance in signal path and zero leakage to the ground or power supply line in off-state and zero impedance against the ground or power supply line during on-state.

This task can be very complicated because standard model libraries of metal-oxide-semiconductor transistors (MOSTs) based on Berkeley short-channel IGFET Model (BSIM) or EKV (initials of its developers C. C. Enz, F. Krummenacher, and E. A. Vittoz) models are unable to simulate appropriate behavior of ESD protection devices

during ESD event (so called snapback action), thus custom modifications of present process design kits (PDKs) – macro-models – or new compact models are being presented by researchers all over the world. The fitting process of ESD models can be very time- and resource-consuming [2]. Thus the automation of the fitting process can speed-up the integration of the ESD models into design library.

The very effective optimization method is called differential evolutionary optimization algorithm (DEOA) and was proven to be very efficient in solving many different optimization tasks (e.g., analog active filter design [3], antenna synthesis in electromagnetic field theory [4], etc.). This paper presents the novel method developed by the authors and results of implementation of the DEOA in ESD model fitting.

### SNAPBACK ACTION IN NMOST

The robust, fast, reliable yet relatively simple ESD protection device is NMOST. It can be used directly in pad or as a power clamp in pad-ring. After closer look on a structure of NMOST (Fig. 1), another structure than drain—gate—source in substrate bulk can be identified. There is also parasitic bipolar-junction NPN transistor (drain—substrate—source).

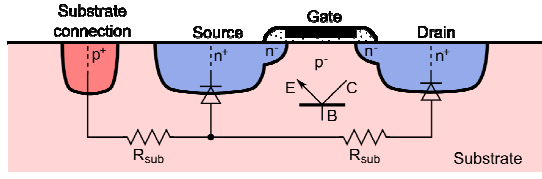


Fig. 1: Simplified structure of NMOST

This is an essential part of ESD NMOST in silicon substrate. It is responsible for a special kind of I-V characteristic that NMOST exhibits – after triggering, the protection device, it rapidly decreases voltage drop across itself, therefore decreasing power dissipation. This is called “snapback action” and it is very important property of NMOST protection. Simplified I-V characteristic of NMOST with grounded gate (i.e., GGNMOST – gate grounded NMOST) is shown in Fig. 2.

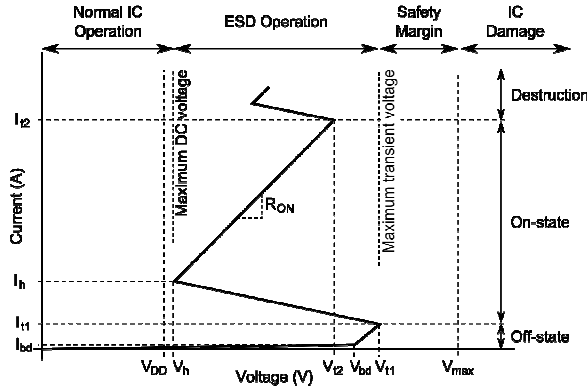


Fig. 2: Simplified snapback action I-V char. of GGNMOST

Several important regions and points can be identified on the characteristic: first region is *off-state* regime, where the device exhibits relatively low leakage (approx. tens to hundreds of nanoamperes). Increasing voltage on a drain of the NMOST results in increase of leakage because more minority holes can travel through reverse-polarized drain—substrate junction. This increase is rather low because the resistance is very high in this region of I-V characteristic. After reaching *breakdown point* ( $V_{bd}, I_{bd}$ ), there is enough energy that travelling holes or electrons can generate more free carriers after colliding with them. This phenomenon is called “impact ionization” and it rapidly increases so far low current leakage. This hole current flowing from drain side to the substrate region increases local potential under the gate. When the value of the potential reaches turn-on voltage of substrate—source junction (approximately 0.65 V), self-biasing parasitic NPN bipolar-junction structure is triggered. This corresponds to the *trigger point* on the I-V characteristic ( $V_{t1}, I_{t1}$ ). The NMOST device then decreases voltage drop between drain and source pins with increase of current flowing through drain, therefore exhibiting negative resistance. After

reaching  $V_{t1}$ , the NMOST is in *on-state* and majority of the ESD current is conducted through the parasitic BJT transistor. After the self-biasing of the BJT reaches equilibrium, another important point on I-V characteristic is reached: *holding point* ( $V_h, I_h$ ). Since then, the NMOST exhibits relatively low resistance. Last and also important point on the I-V characteristic regarding ESD design limits voltage and current the NMOST can experience before destructive second breakdown. These values are designated as  $V_{t2}, I_{t2}$ .

The shape of the I-V characteristic (i.e., off-state leakage, breakdown voltage  $V_{br}$ , trigger voltage  $V_{t1}$ , holding voltage  $V_h$ , on-state resistance  $R_{on}$  and second breakdown current  $I_{t2}$ ) can be influenced by layout style, technology properties or by circuit manners. More details about design and modeling of NMOST ESD protection device can be found in [5], [1], and [6].

## NMOST MODEL

Model of ESD NMOST device was presented in [7] and further improved in [8]. The schematic representation of the model is shown in Fig. 3.

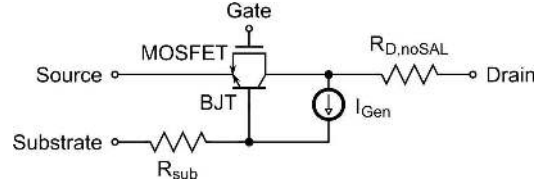


Fig. 3: Representation of NMOST model

The hole-current source  $I_{gen}$ , responsible for turning on the parasitic bipolar transistor, can be described as

$$I_{gen} = (M - 1) \cdot (I_{MD} - I_{BC}), \quad (1)$$

where the  $I_{MD}$  is a drain current of the internal NMOST model,  $I_{BC}$  is a collector current of the bipolar transistor model, and multiplication factor  $M$  can be defined as

$$M = \limexp[k_1 (V_{DS} - V_{dsat} - d_1)] + \limexp[k_2 (V_{DS} - V_{dsat} - d_2)], \quad (2)$$

where  $V_{dsat}$  is drain saturation voltage,  $\limexp(x)$  is a special type of exponential function used in Verilog-A hardware description language (HDL)

implementing internal limiting to aid better convergence, and  $k_1$ ,  $d_1$ ,  $k_2$ , and  $d_2$  are fitting parameters. The definition of multiplication factor in Eq. 2, presented in [8], has better convergence properties and was used instead of the original definition presented in [7]. The implementation in model is done via Verilog-A hardware description language (HDL).

The model part designated as ‘‘MOSFET’’ is standard EKV model implemented in the PDK and the ‘‘BJT’’ was described via VBIC model.

Model of the ESD NMOST substrate resistance described with the use of Verilog-A HDL was defined as

$$R_{\text{sub}} = R_0(V_{GS}) + R_1(V_{GS}) \cdot \text{limexp}(-V_{DS}) + R_2(V_{GS}) \cdot V_{GS} \cdot \text{limexp}(-V_{DS}), \quad (3)$$

where the  $R_0(V_{GS})$ ,  $R_1(V_{GS})$ , and  $R_2(V_{GS})$  are polynomial functions defined as

$$R_i(V_{GS}) = R_{ia} + R_{ib} \cdot V_{GS} + R_{ic} \cdot V_{GS}^3, \quad (4)$$

where  $R_{ia}$ ,  $R_{ib}$ , and  $R_{ic}$  are fitting parameters and  $i = 0, 1, 2$ .

In addition, authors enhanced the model by addition of a drain resistance to simulate a non-salication effect on the drain side of the NMOST. The resistor is technological, diffusion non-salicated  $n$ -type with dimensions corresponding to the width of the ESD NMOST and overlap of the non-salicated drain extension. This shall correctly model the additional drain resistance of the non-salicated region on the drain side of the ESD NMOST.

More information about various approaches in ESD protection device modeling can be found in [5].

## DIFFERENTIAL EVOLUTIONARY OPTIMIZATION ALGORITHM

Evolutionary optimization algorithms are in general very robust and fast-to-converge algorithms. The Evolutionary algorithms are less susceptible to misconvergence problem. Thanks to the natural selection of the most fitted member of the population of parameter vectors, the possibility of the premature convergence in a local minimum is minimized [9]. Moreover, the DEOA is in contrast with gradient-based optimization methods able to optimize in non-continuous fitting-function-space and enables the

designer to introduce for example penalty coefficients to detect optimization violations.

The functionality of DEOA algorithm can be described in the following way: let the vector of system parameters for specific member of the specific generation be designated as

$$\mathbf{x}_{i,G}, \quad i = 0, 1, 2, NP - 1, \quad (5)$$

where  $NP$  is the number of  $D$ -dimensional parameters in the *parameter vector* ( $D$  doesn't change during optimization process) and  $G$  determines the sequence of the generation. All the parameter vectors  $\mathbf{x}_{i,G}$  of the same generation are called *population*. If the initial values of parameters within the parameter vector are unknown, their values can be generated randomly by uniform probability distribution. After each generation, a new vector is generated and is used in next iterative step. The innovation of the differential evolution is the algorithm of generation of members of the new generation. The new member is derived as the sum of weighted difference of the first and the second member and of the third member. If the newly created parameter vector yields lower value of the *objective function*  $f_{\text{obj}}$  (qualitative evaluation of fitness of the specific member) than a predetermined one, the new member replaces the original one. In addition, the best fitted member of the population (i.e., the parameter vector with lowest objective function) is stored to keep track of the progress of the optimization process.

The detailed principle of generation and selection of the best fitted member of the population is as follows: for each parameter vector  $\mathbf{x}_{i,G}$ , a *trial vector*  $\mathbf{u}_i$  is calculated as

$$\mathbf{u}_i = \mathbf{x}_{r_1,G} + F \cdot (\mathbf{x}_{r_2,G} - \mathbf{x}_{r_3,G}), \quad (5)$$

where integers  $r_1 \neq r_2 \neq r_3 \neq i$  and  $r_1, r_2, r_3 \in \{0, 1, \dots, NP - 1\}$  are randomly chosen with uniform probability distribution,  $F$  is a real *weighting constant* determining the influence of the *differential variation vector*  $(\mathbf{x}_{r_2,G} - \mathbf{x}_{r_3,G})$ . The role of the trial vector can be seen in Fig. 4.

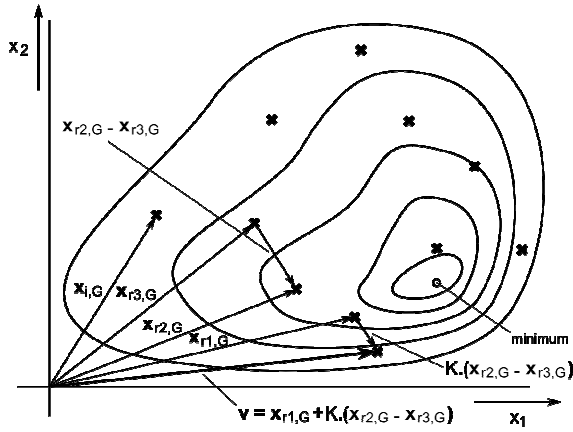


Fig. 4: Representation of the differential evolutionary algorithm in two-dimensional space [9]

To implement the principle of a mutation and crossover, the new  $D$ -dimensional vector  $\mathbf{t}_i$  needs to be created. The elements of the  $\mathbf{t}_i$  vector are random numbers with uniform probability distribution, where  $t_{i,j} \in \langle 0,1 \rangle$ ,  $j = 0,1,\dots,D-1$ . Now, each element  $t_{i,j}$  of the  $\mathbf{t}_i$  vector is compared against the value of  $CR$  crossover coefficient and in case the value of  $CR$  is higher than  $t_{i,j}$ , the  $u_{i,j}$  is placed in the crossover vector  $\mathbf{v}_i$  as  $j$ -th element, else the original value  $x_{i,j,G}$  is used. In addition, the dimension index  $j$  is compared against randomly generated integer  $R = 0,1,\dots,D-1$  with uniform probability distribution and in case of match, the  $v_{i,j} = u_{i,j}$ . This can be mathematically described as

$$v_{i,j} = \begin{cases} u_{i,j}, & t_{i,j} \geq CR \vee j = R \\ x_{i,j,G}, & \text{otherwise} \end{cases}, \quad (6)$$

where  $i = 0,1,\dots,D-1$ . The graphical representation of (6) is shown in Fig. 5.

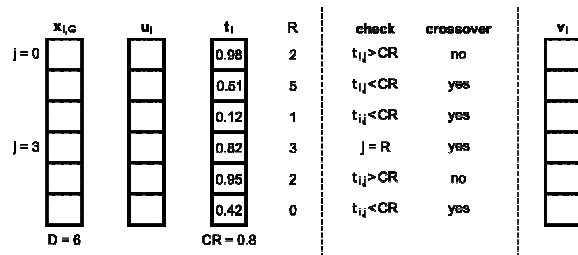


Fig. 5: Example of crossover process

The final step is to solve objective function for the crossover vector  $\mathbf{u}_i$  and compare its value against

the value of objective function of the original vector  $\mathbf{x}_{i,G}$ . The vector with lower objective function becomes the new member of  $(G+1)$ -th generation, mathematically written as

$$\mathbf{x}_{i,(G+1)} = \begin{cases} \mathbf{u}_i, & f_{\text{obj}}(\mathbf{u}_i) < f_{\text{obj}}(\mathbf{x}_{i,G}) \\ \mathbf{x}_{i,G}, & \text{otherwise} \end{cases}, \quad (7)$$

where  $f_{\text{obj}}(\mathbf{y})$  represents the value of the objective function for arbitrary  $\mathbf{y}$  vector in its argument and  $i = 0,1,\dots,NP-1$ . After each generation, the best member (the one with the lowest value of the objective function) is selected and stored for the next generation. This ensures the progress of determination of the best set of parameters. The algorithm can be repeated indefinitely, until the ideal solution is found, or the maximum number of generations can be specified to limit the number of iterations of the optimization.

More details about Evolutionary algorithm can be found in [9].

## FITTING PROCEDURE

Instead of set of different manual measurements for many different conditions that needs to be performed during standard model fitting method [2], proposed approach needs only the I-V characteristic of the “template” protection device (this can be obtained for example by TLP measurement). The main part of this method is the DEOA fitting algorithm developed for ESD model calibrations. It was completely written in Matlab-like programming language in Octave mathematical software (with all necessary interfaces to Cadence Spectre MDL batch extension). It uses DEOA core designated as “DE/rand/1/bin” [5]. This robust optimization algorithm minimizes possibility of missing the global minimum and can be used for optimizations in non-continuous space. To prevent algorithm to optimize model indefinitely, additional checks were implemented: user definable maximal acceptable value of the fitting function that whenever is reached, the optimization is ended, user can specify maximum total number of simulation runs, algorithm also checks for how long the algorithm didn’t find better parameter set (i.e., with lower value of the fitting function) and ends optimization if the specified number of runs has been reached to prevent further unnecessary optimization effort and limit total optimization time.

In principle the function of the proposed fitting method can be described in the following way: I-V characteristic constructed from for example TLP measurement is used as the template for the DEOA

algorithm which then tries to fit the model to this template. The calculations of the DEOA as well as control of the fitting procedure are conducted by an Octave script created especially for this purpose. The model to be fitted has to be instantiated in the simple testbench shown in Fig. 6 and netlisted to the Spectre-formatted netlist file. The netlist file includes the fixed parameters (constants) of the testbench (i.e., value of the initial current of the biasing DC current source, dimensions of the NMOST) and the variable parameters which need to be optimized to successfully fit the measured I-V characteristic of the NMOST to the developed model. The simulation defined in the netlist is then executed by MDL script and performed by Cadence Spectre. Each time before the Octave executes the script, the newly calculated set of parameters is written into the testbench netlist file by developed subroutines of the Octave script that create needed interface between optimization core in Octave and simulation core in Spectre. It would be even possible to very simply modify the interface scripts to cooperate with another type of simulator, therefore this property and the fact that the Octave is GNU licensed makes this tool very easily portable and suitable for industrial use. After the end of the simulation, the objective function is calculated and compared to the best achieved in earlier runs. This cycle continues until the objective function has better (lower) value than specified by its terminal-value or until the specific number of runs was performed (protection against the numerical errors while processing very small values of the objective function or against unrealistically low terminal-value of objective function). Schematic description of the fitting process is depicted on Fig. 7.

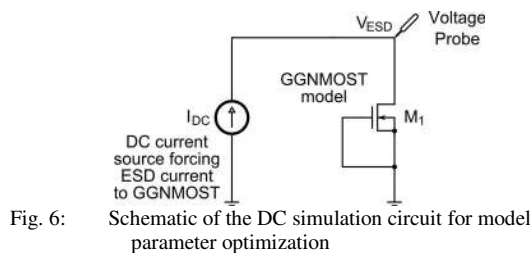


Fig. 6: Schematic of the DC simulation circuit for model parameter optimization

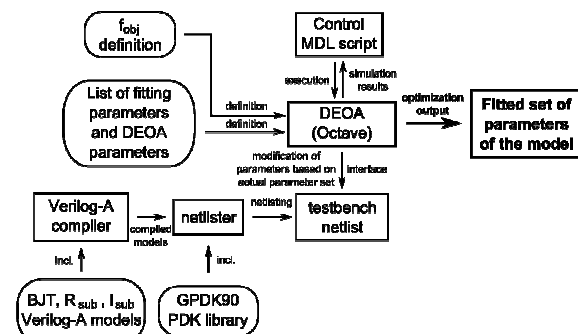


Fig. 7: Diagram of optimization process flow

The objective function  $f_{obj}$  is calculated as

$$f_{obj} = \sum_{i=1}^n \left( V_i^{[measured]} - V_i^{[simulated]} \right)^2, \quad (8)$$

where  $i$  couples specific voltages as measured/simulated by DC drain current sweep. The optimization method can be further improved by addition of other design variables (e.g., gate voltage  $V_{GS}$  of the NMOST) which can be automatically swept during one optimization step and thus can make the optimization task to take into account other dependencies (gate-voltage dependence of the I-V characteristic of the NMOST) and eventually ensure better fitting. Then the optimization task can be mathematically described as

$$f'_{obj} = \sum_{j=1}^m \sum_{i=1}^n \left( V_{j,i}^{[measured]} - V_{j,i}^{[simulated]} \right)^2, \quad (9)$$

where  $j = 0, 1, 2, \dots, (m-1)$  runs through all combinations of swept variables. This of course prolongs the total time and increase the amount of resources needed to successfully finish the optimization task.

## RESULTS

The automated optimization method presented in earlier section was tested by fitting standard GSPDK90 GGNMOST model to the empirical piece-wise linear I-V characteristic created by different type of model (piece-wise linear I-V characteristic simulation model for ESD) developed by authors and based on a measured data of 3.3 V transistors in 180 nm technology. Cadence Spectre 7.0 was used as technology simulator along with Octave 3.4.0 as DEOA core handler. The DEOA parameters were set as follows:  $NP = 60$ ,  $CR = 0.9$ ,  $F = 0.68$ . The optimization procedure ended after 4 626 iterations. The overall optimization time was less than 5 hours (2,3 GHz dual-core desktop computer with 6 GB RAM used). Even though neither the model nor the technology used for data extraction fits the PDK used for model implementation (only data for 180nm technology were available and only 90nm general purpose PDK was available at the time), the behavior of the fitted model closely resembles the one seen in the piece-wise-linear model – average difference between I-V characteristics of the template and fitted model is 0.2 V. Better fitting results shall be received in future, fitting the model to the corresponding TLP-measured data which are not available at the moment. The I-V characteristics of models are shown in Fig. 8

showing piece-wise-linear model I-V characteristic and fitted I-V characteristic of the earlier presented macromodel. The simulated response of the fitted model to the Human Body Model (HBM) testing pulse is shown in Fig. 9. It is apparent that behavior of the macromodel during high-speed high-current transient is very close to results presented in [2] after extensive fitting measurements (differs only in absolute values, curve shape is comparable and the snapback is modeled correctly). This proves that the balance between  $I_{gen}$  and BJT parameters which has to be achieved in the standard fitting procedure by many measurements of several device characteristics was achieved in less than 5 hours by fully automatic process.

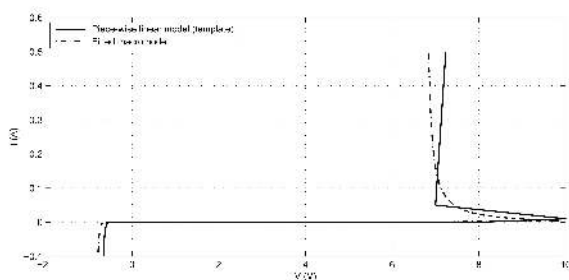


Fig. 8: Comparison of piece-wise linear (solid line) and fitted ESD GGNMOST model (dashed line) I-V characteristics

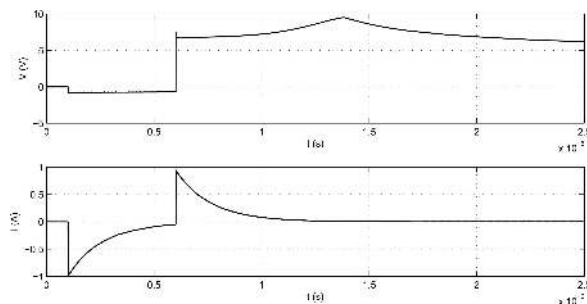


Fig. 9: Response of fitted ESD GGNMOST model to the HBM transient pulse

## CONCLUSIONS

The possibility of utilization of the DEOA for ESD model fitting was presented along with enhanced ESD-NMOST macro-model and developed portable simulator-independent Octave-Spectre interface. The usage of DEOA to fit ESD NMOST model to measured data were previously to the best knowledge of the authors never presented.

Proposed method was able to fit generic model to the piece-wise linear I-V characteristic to be able to simulate HBM pulse response and resulting snapback of the model connected as gate-grounded NMOST, all this in less than 5 hours lasting fully automatic optimization process. This shows that this approach is viable and can be used as alternative for time- and resource-consuming manual model calibration.

Future development will be focused on optimizing the DEOA parameters and using additional optimization methods along DEOA to increase optimization efficiency. NMOST model will be modified to comply with technology used for fitting and amended by additional effects that were omitted during optimization method development.

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## REFERENCES

- [1] S. G. Beebe, "Characterization, modeling, and design of ESD protection circuits". Advanced Micro Devices, Sunnyvale, California, Tech. Rep., March 1998.
- [2] J. J. Liou, "Electrostatic discharge (ESD) protection for RF applications". June 2007, presentation.
- [3] P. Ziska and P. Martinek, Algorithm of differential evolution and its use for zeros and poles identification of filter transfer function (in Czech). Czech Technical University in Prague, Faculty of Electrical Engineering, Department of Circuit Theory, Tech. Rep., 2004.
- [4] P. Rocca, G. Oliveri, and A. Massa, "Differential evolution as applied to electromagnetics". IEEE Antennas Propag. Mag., vol. 53, no. 1, pp. 38 – 49, February 2011.
- [5] T. Napravnik, ESD protection circuits. Master's thesis, Czech Technical University in Prague, Faculty of Electrical Engineering, Department of Microelectronics, June 2011.
- [6] T.-Y. Chen and M.-D. Ker, Analysis on the dependence of layout parameters on ESD robustness of CMOS devices for manufacturing in deep-submicron CMOS process, IEEE Transactions on Semiconductor Manufacturing, pp: 486 – 500, August 2003.
- [7] A. Amerasekera, M.-C. Chang, C. Duvvury, and S. Ramaswamy, "Modeling MOS snapback and parasitic bipolar action for circuit-level ESD and high-current simulations", IEEE Circuits

Devices Mag., vol. 13, no. 2, pp. 7 – 10, Mar 1997.

- [8] S. L. Lim, X. Y. Zhang, Z. Yu, S. Beebe, and R. Dutton, “A computationally stable quasi-empirical compact model for the simulation of MOS breakdown in ESD-protection circuit design. in Simulation of Semiconductor Processes and Devices”, 1997. SISPAD '97., 1997 International Conference on, September 1997, pp. 161 – 164.
- [9] R. Storn and K. Price, Differential evolution – a simple and efficient adaptive scheme for global optimization over continuous spaces, International Computer Science Institute, Berkeley, Tech. Rep., March 1995.