ESD Protection Design to Overcome Internal Damage on Interface Circuits of a CMOS IC With Multiple Separated Power Pins

Ming-Dou Ker, *Senior Member, IEEE*, Chyh-Yih Chang, *Member, IEEE*, and Yi-Shu Chang

***Abstract*—This paper reports a real case of electrostatic discharge (ESD) improvement on a complementary metal oxide semiconductor integrated circuit (IC) product with multiple separated power pins. After ESD stresses, the internal damage have been found to locate at the interface circuit connecting between different circuit blocks with different power supplies. Some ESD designs have been implemented to rescue this IC product to meet the required ESD specification. By adding only an extra ESD clamp N-channel metal oxide semiconductor with a channel width of 10 μm between the interface node and the ground line, the human-body-model (HBM) ESD level of this IC product can be improved from the original 0.5 to 3 kV. By connecting the separated vertical sync signal (VSS) power lines through the ESD conduction circuit to a common VSS ESD bus realized by the seal ring, the HBM ESD level of the enhanced version IC product with 12 separated power supplies pairs can be significantly improved from original 1 kV up to $>$ 5 kV, without noise coupling issue.**

***Index Terms*—Electrostatic discharge (ESD), ESD bus, ESD protection circuit, internal damage.**

I. Introduction

ELECTROSTATIC discharge (ESD) phenomenon continues to be a serious reliability issue in complementary metal oxide semiconductor (CMOS) integrated circuits (ICs) because of technology scaling and high integration of circuit blocks [1]. To improve electrostatic discharge (ESD) robustness, some advanced circuit techniques such as gate-coupled design [2], [3] or substrate-triggered design [4]–[6] had been used in the input/output ESD protection circuits of CMOS ICs. However, when performing the power pin to power pin ESD stress according to ESD standards [7], [8], even with the ESD protection circuits on the input/output pins and between VDD and vertical sync signal (VSS) power rails, some unexpected ESD damage may still happen across the internal circuits of CMOS ICs [9]–[15]. Such ESD stress induced internal damage is often difficult to be clearly inspected, even with a lot of failure analysis procedure and extra cost. As the CMOS process being continually scaled down, the internal circuits designed and drawn with minimum layout spacing in the design rules, smaller device dimension, and much thinner gate oxide are more susceptible to such ESD stress induced internal damage. Besides, more and more multiple separated power pins are used in the system-on-chip (SoC) IC for power management consideration. The IC products with more multiple separated power pins often have more broken paths for ESD current discharging, and easily cause internal damage beyond the ESD protection circuits on the input/output (I/O) pads. Therefore, how to design effective ESD protection solution to avoid ESD damage on the internal circuits has become a challenge to IC products in deep-submicron CMOS processes, especially to SoC products.

In this paper, a real case of internal ESD damage on interface circuits of a CMOS IC product with multiple separated power pins in a 0.35-μm CMOS process is reported [16]. This IC as a multiple clock generator has more than ten separated power supplies, which are fully isolated from each other because of noise coupling issue. The solutions used to improve its ESD level have been experimentally verified in this work.

II. ESD Failure in CMOS IC With Multiple Separated Power Pins

A clock generator IC had been fabricated in a 0.35-μm CMOS process and used to supply 11 clock signals to synchronize chip sets working in a computer system. To prevent the noise coupling issue, the power rails of circuit blocks in this IC are all isolated from each other, as shown in Fig. 1. To protect IC from ESD damage, the ESD protection circuits are traditionally placed between I/O pads and VDD lines, I/O pads and VSS lines, and VDD and VSS power rails. Referring to Fig. 2, the ESD protection devices Mn1, Mp1, Mn2, and Mp2 are placed on the I/O pads to their corresponding power rails. In general, digital I/O cell layout, the total channel widths of N-channel metal oxide semiconductor (NMOS) and P-channel metal-oxide semiconductor (PMOS) for output driver or ESD protection are often drawn with larger device dimensions.

When the I/O cell is used as an input pad, the NMOS (PMOS) devices are turned off by connecting all the poly-gate fingers to VSS (VDD) as ESD protection devices. When the I/O cell is used as an output pad, some poly-gate fingers of the MOS are connected to the prebuffer circuit as output driver. The number of poly-gate fingers connected to prebuffer circuit depends on the demand of output driving capability, and the other poly-gate fingers are turned off by tied to VSS or VDD as ESD

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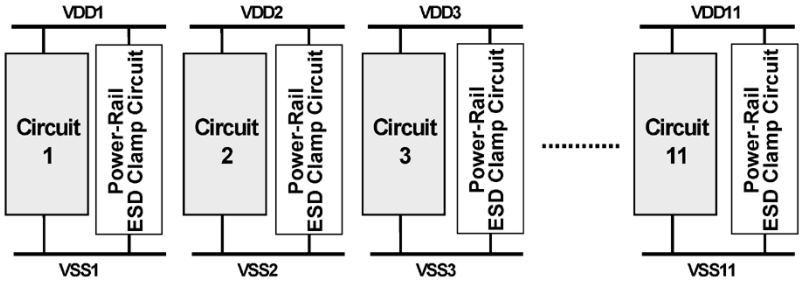


Fig. 1. Schematic diagram of the CMOS IC with multiple separated power pairs.

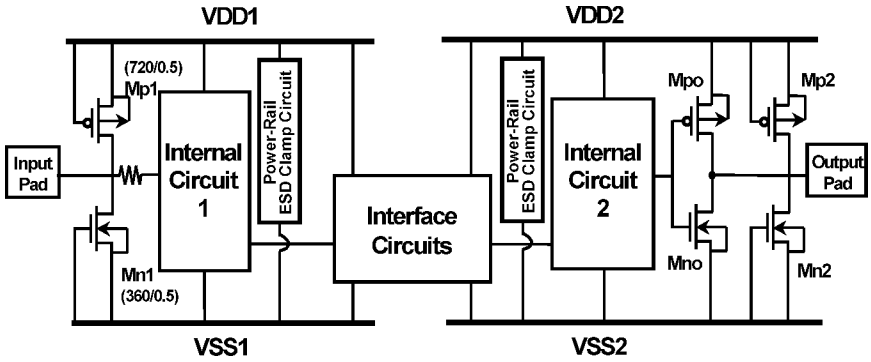


Fig. 2. ESD protection circuits for input and output pads of a CMOS IC with multiple separated power pins.

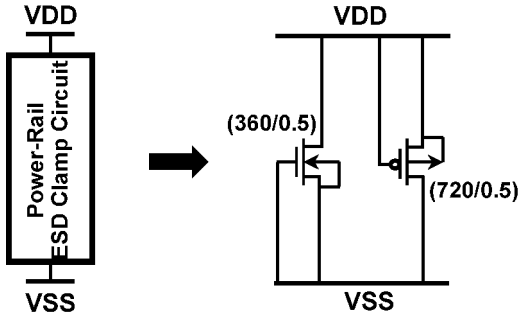


Fig. 3. Power rail ESD clamp circuit for all VDD and VSS pads of the CMOS IC with multiple separated power pins.

protection devices. In this IC product, the NMOS and PMOS in the I/O cell have the same channel length of 0.5 μm. The total channel width of NMOS is 360 μm, and that of PMOS is 720 μm. Therefore, the ESD protection devices used in the input pad of this IC product have NMOS of 360/0.5 and PMOS of 720/0.5 (μm/μm). On the other hand, the size of output ESD protection devices, Mn2 and Mp2, depends on the output driving capability demand.

The cell layouts of power pads (include VDD pad and VSS pad) are the same as the I/O cell. In the power cell layout, the gate of NMOS is tied to ground and the gate of PMOS is tied to VDD, thus the NMOS and PMOS are both used as the power-rail ESD clamp circuits, as those shown in Fig. 3.

With such large ESD protection devices in the I/O pads and power rails, the human-body-model (HBM) ESD level of I/O pins can pass 5 kV under the positive and negative ESD stresses between the I/O pin and the VSS (VDD) pin. However, when performing the ESD test between the separated power pins which have different voltage supply levels, this IC product can pass only 0.5-kV HBM ESD stress but fail at 1-kV HBM ESD stress. The test method of the ESD test is to zap ESD to one power pin with other power pins grounding and other I/O pins floating. Therefore, the pin combination includes first VDD pin to second VSS pin, first VDD to third VSS pins, and etc. After the ESD test, failure analyses are performed. The failure spots are found by photo-emission microscope (EMMI) and pictured in Fig. 4, which are located at the interface circuit between circuit blocks with separated power supplies, not on the zapped I/O pads.

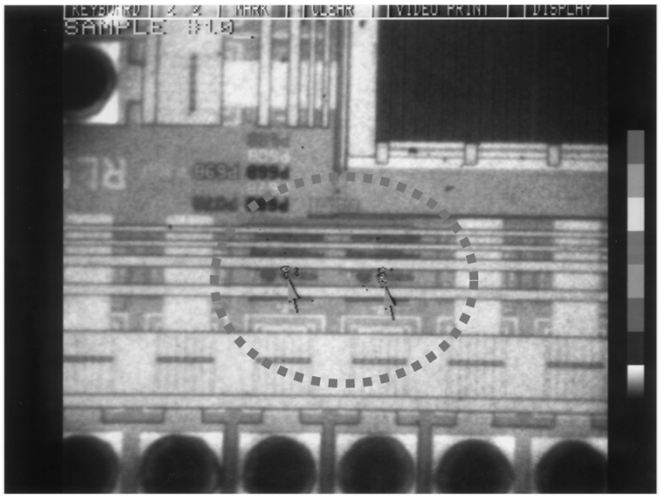
By tracing the original chip layout and comparing to the circuit schematic, the hot spots are found on the PMOS of the interface circuit between two circuit blocks with different VDD power supplies. Fig. 5 illustrates the equivalent circuit diagram across the interface circuit of the CMOS IC with separated power supplies, where the dashed lines with the arrows indicate the possible ESD current paths when an ESD stress is applied on VDD2 pin and the VSS1 pin relatively grounded. The ESD stress damage the gate oxide of PMOS Mp2 in Fig. 5, and induces a leakage current path between the power rails when all VDD and VSS power supplies are applied on the circuits.

III. Methods to Improve ESD Robustness

To solve the internal damage problems caused by ESD stresses across different power pins, there were four approaches used and verified in this work to enhance the ESD robustness of this IC product.

A. NMOS Clamps Between Interface and VSS Metal Line

For cost consideration, the usage of photo mask changing on only metal layers is the first choice for this IC product. In the original layout some dummy NMOS devices were placed



(a)

(b)

Fig. 4. (a) Internal damage caused by ESD stress across the separated power pins. (b) Zoomed-in picture on the left hot spot in (a).

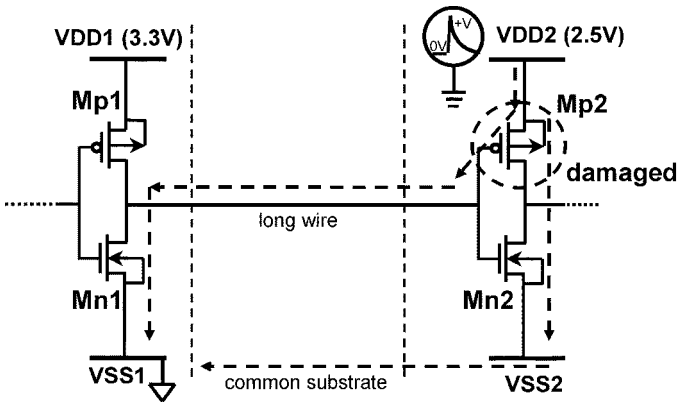


Fig. 5. Equivalent circuit diagram to show ESD current paths in the CMOS IC with separated power supplies, when ESD stress is applying on VDD2 with VSS1 relatively grounded. The dashed lines with the arrows indicate the possible ESD current paths.

in the chip which can be connected to the interface circuit by changing metal mask layout. Besides, a 1-μm wide metal line

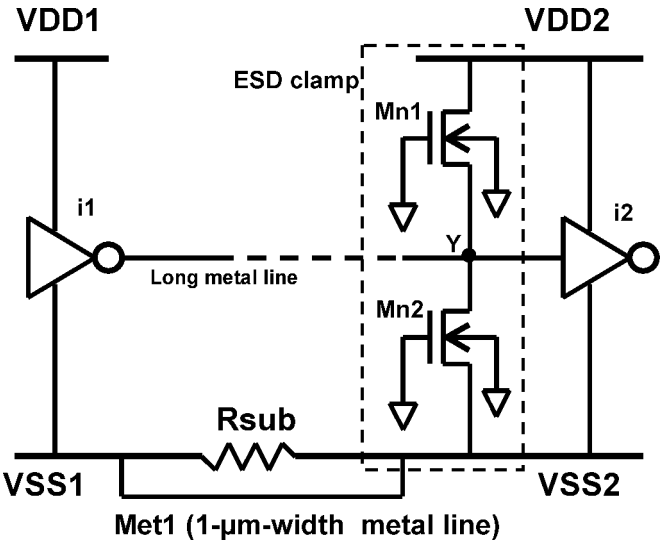


Fig. 6. ESD clamp devices directly added to the interface circuit to solve the internal damage by changing one metal mask in the IC layout.

(marked as "Met1" in this work) used to connect the VSS1 and VSS2 is also achieved by changing the same metal mask layout. Fig. 6 shows the schematic diagram of the equivalent circuit after changing one metal mask, where the Met1 is also illustrated to show the modification. In Fig. 6, the first gate-grounded NMOS Mn1 is connected between VDD2 (2.5 V) and the input node Y of inverter i2. The second gate-grounded NMOS Mn2 is connected between VSS2 (0 V) and the input node Y of inverter i2. Mn1 and Mn2 have the same channel width and channel length, which are 10 μm and 0.5 μm, respectively. The 1-μm wide metal line, Met1, is used to connect VSS2 (0 V) and VSS1 (0 V). Only one mask change is used to achieve the above layout modifications in this IC product for improving ESD robustness.

After the refabrication of this IC product, the ESD test is performed again, and the measurement results are listed in Table I. Focus ion beam (FIB) is also used to cut the metal connection to further investigate the performance of the extra ESD protection scheme shown in Fig. 6. After cutting the metal connection of Mn1 and Mn2 by FIB, the adding of only 1-μm wide metal line Met1 can improve the HBM ESD level to 2 kV. The most robust solution is combining Mn2 and Met1 that can improve the sustained HBM ESD level to 5.5 kV. However, the noise coupling issue between the VSS1 and VSS2 power rails makes this solution unacceptable for this IC application. Referring to Table I, one interesting result is found. By only adding the Mn2, the HBM ESD level of this IC product can be improved to 3 kV. However, with adding both Mn2 and Mn1 (Mn1 + Mn2), the sustained ESD level degrades to 1 kV. Originally, the Mn1 and Mn2 in this chip are not designed and drawn for ESD protection purposes. Only a few contacts are used to contact the drain/source diffusion and have the minimum layout spacing between the drain/source contacts and the poly gate. Because the Mn1 used in Fig. 6 is originally not drawn for bypassing ESD current, Mn1 could be damaged by ESD stress when the ESD stress was zapping on the VDD2 pin and the VSS1 pin relatively grounded. In the case of adding Mn2 only, the Mn2 properly suppress the over-stress voltage on the node Y and does not sink the ESD current. The modification design with

TABLE I
ESD TEST RESULTS OF THE IC PRODUCT WITH MULTIPLE SEPARATED POWER PINS BY USING DIFFERENT SOLUTIONS TO IMPROVE ESD LEVEL

Before Modification	Only Mn2	Only Met1	Mn1+Mn2	Mn2+Met1	Mn1+Mn2+Met1
0.5 kV	3 kV	2 kV	1 kV	5.5 kV	3.5 kV

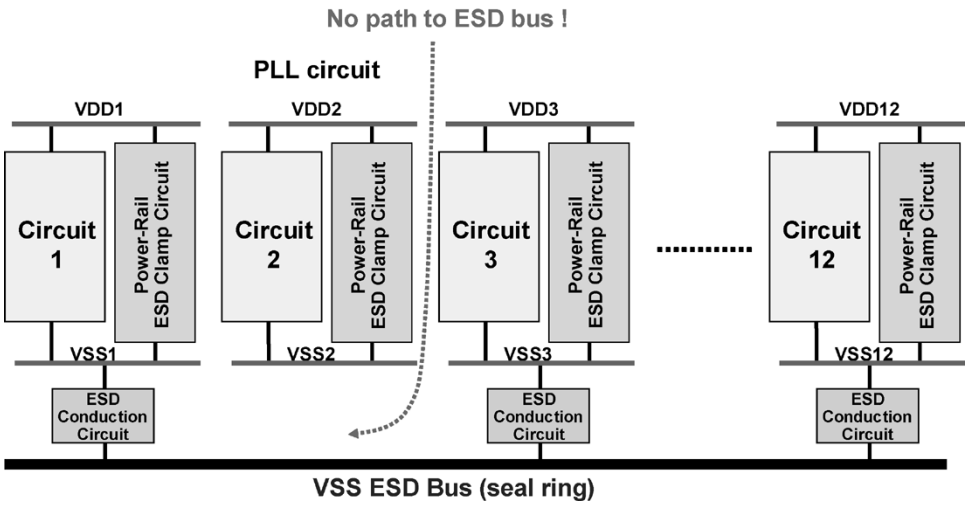


Fig. 7. Enhanced IC product includes 12 separated power pairs to supply 12 internal circuit blocks. The common VSS ESD bus is used to connect VSS power line of each circuit block through ESD conduction circuit except the PLL circuit block.

Mn1 + Mn2 + Met1 has an ESD level of only 3.5 kV, because the Mn1 degrades the ESD robustness. Comparing the measurement results and considering the practical application and noise issue, the advisable solution is only adding NMOS device Mn2 on the interface circuits between the input node Y and VSS2. Finally, the HBM ESD level of this IC product with multiple separated power supplies can be rescued to 3 kV successfully.

B. VSS ESD Bus

The ESD bus can provide the common ESD current discharging path along the whole chip of a CMOS IC with separated power lines [17], [18]. The ESD bus design was therefore incorporated in the enhanced version of this IC product with multiple separated power pins to improve the ESD level. This enhanced IC product includes 12 separated power pairs to supply 12 internal circuit blocks connected by individual interface circuits, as those shown in Fig. 7. Each circuit block comprises the ESD protection schemes as those shown in Figs. 2 and 3. In this enhanced IC product, the VSS2 power line of a phase-locked loops (PLL) circuit does not connect to the common VSS ESD bus through the ESD conduction circuit because of the limited layout area and the noise coupling issue. The ESD conduction circuit comprises of two series diodes in a bidirectional connection [19], as shown in Fig. 8. These two series diodes can provide isolation of about 1-V noise between the VSS power lines and the common VSS ESD bus.

Between each two VSS power lines, there are equivalent four series diodes to provide a noise margin of approximately 2 V which is the summation of the cut-in voltages of four diodes. Fig. 9 illustrates the schematic layout of the diode used in the ESD conduction circuit which is realized by the P+ diffusion

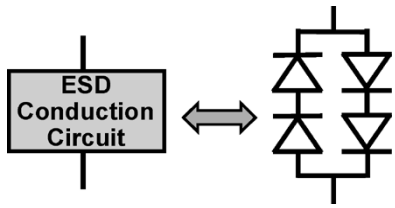


Fig. 8. ESD conduction circuit comprises two series diodes with bidirectional connection [16].

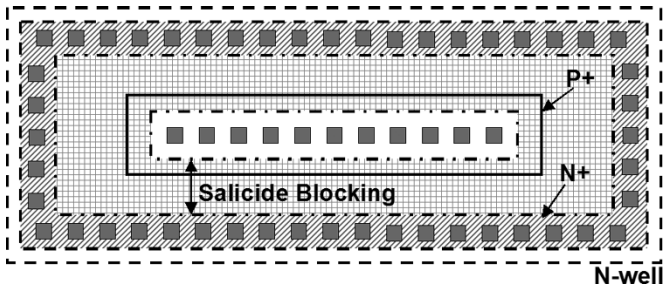


Fig. 9. Layout schematic of the diode used in ESD conduction circuit.

in an N-well. The salicide-blocking mask is used to block the silicide on the diode diffusion across the junction region.

The common VSS ESD bus, shown in Fig. 7, is constructed by the seal ring structure. The abbreviation "FOX" denotes the field-oxide isolation structure in CMOS technology. Originally, the seal ring is used to prevent the mechanical stress on the die when wafer being sawed. Fig. 10(a) and (b) show the cross-sectional views of the design rule suggested seal ring and the modified seal ring used as the common VSS ESD bus in this enhanced IC product, respectively. In Fig. 10(b), the metal contacts of the seal ring directly connect to the polysilicon layer instead of to

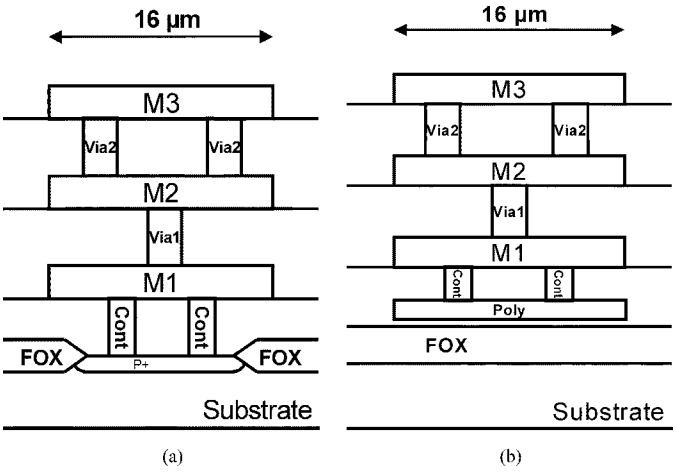


Fig. 10. Cross-sectional views of (a) the seal ring suggested in the design rule and (b) the modified seal ring used as the common VSS ESD bus in this new design. The FOX layer is the field-oxide isolation layer in CMOS technology.

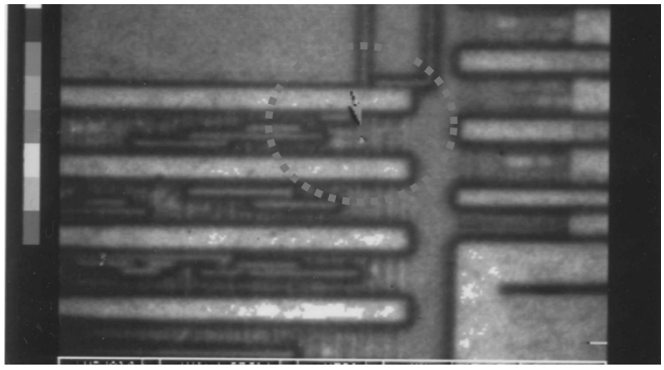


Fig. 11. Internal damage caused by ESD stress on the enhanced IC product, which is still located at the interface circuit between the PLL circuit block and the other circuit blocks with separated power supplies.

the P+ diffusion in the substrate. Therefore, the noise in the substrate does not couple into the common VSS ESD bus and does not couple into the VSS power lines of the circuit blocks.

Accordingly, each pin of this enhanced IC product can sustain the HBM ESD level of greater than 5 kV, except the pins for the PLL circuit block which can sustain the HBM ESD level of only 1 kV. Because the VSS2 of the PLL circuit block is not connected to the common VSS ESD bus through the ESD conduction circuit, the ESD stress across the different power pins easily causes the stress on the interface circuit between the PLL circuit block and the other circuit blocks. Again, ESD damage is still found on the interface circuit between the PLL circuit block and the other circuit blocks with separated power supplies; the EMMI failure picture is shown in Fig. 11.

C. Modified High-Impendence Interface Circuit

Fig. 12 shows the equivalent circuit of the interface circuit between the PLL circuit (with VDD2/VSS2 power supplies) and the other circuit block (with VDD1/VSS1 power supplies) in the enhanced IC product. The PLL circuit receives the output signal from an internal buffer through a long metal wire, longer than 25 μm. The input circuit of the PLL circuit has an inverter inv1 and a transmission gate TG1. From the failure spot shown in

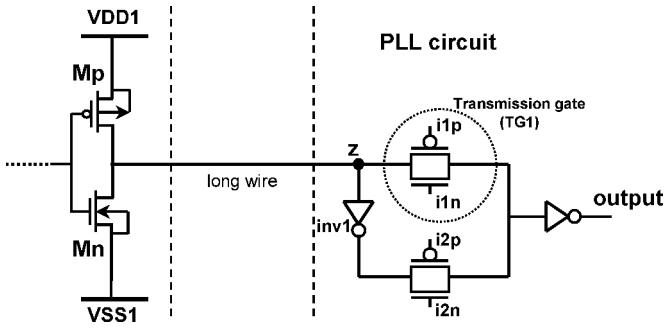


Fig. 12. Interface circuit between the PLL circuit block and another circuit block of the enhanced IC product.

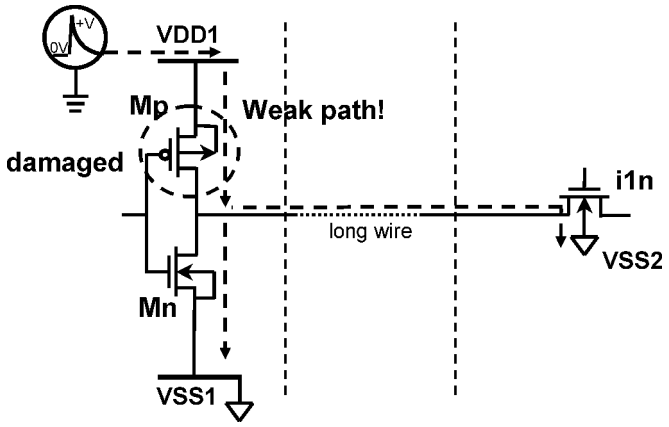


Fig. 13. Equivalent circuit diagram to show the ESD current path flowing through the interface circuit when an ESD event occurs on VDD1 with VSS1 and VSS2 relatively grounded.

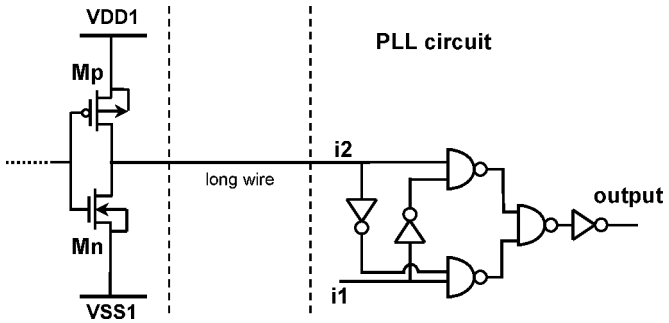


Fig. 14. Modified input circuit of the PLL circuit block without using the transmission gate TG1 of Fig. 12.

Fig. 11, the damage location is found at the output PMOS (Mp) of the internal buffer with VDD1/VSS1 power supplies. The equivalent circuit shows the ESD current path as illustrated in Fig. 13. When the PLL circuit input circuit is modified without the transmission gate, as shown in Fig. 14, the ESD level of this IC product can be increased from 1 to 2 kV. From the experimental data, the interface circuit with the transmission gate is sensitive to ESD events.

D. Final Solution

The final version of whole-chip ESD protection design for this enhanced IC product with 12 separated power pairs is shown in Fig. 15. The ESD conduction circuit is added to connect the

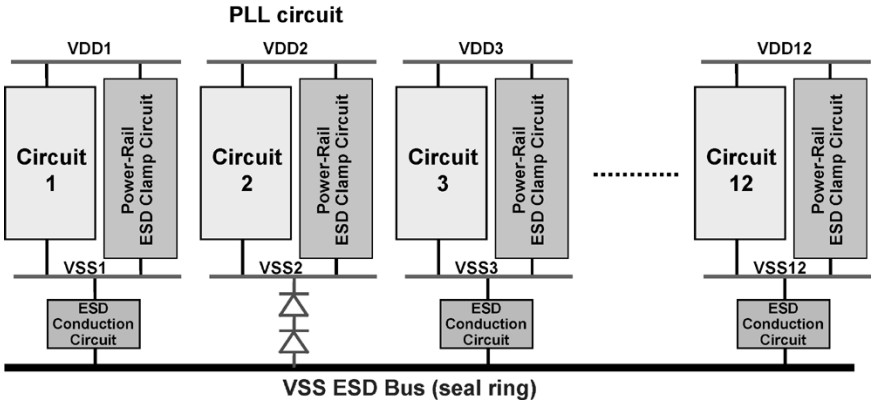


Fig. 15. Final version of ESD protection scheme of the enhanced IC product with 12 separated power pairs.

VSS2 of the PLL circuit block to the common VSS ESD bus line. For consideration of noise coupling issue, only two series diodes in one direction are added in the ESD conduction circuit, where the anode of the series diodes is connected to the common VSS ESD bus line and the cathode of the series diodes is coupled to VSS2 of PLL circuit block. Thus, the noise generated by PLL circuit block would not couple to other circuits through the common VSS ESD bus line. Besides, the input buffer of PLL circuit block in the interface circuit is realized by the modified circuit, as that shown in Fig. 14 without using the transmission gate TG1. The HBM ESD level of the final version of this enhanced IC product with 12 separated power pairs and the whole-chip ESD protection design shown in Fig. 15 is improved from the original 1 kV to become $>$ 5 kV, including the ESD stresses across the different power pins. With the successful improvement on ESD robustness, this final version of the IC has been in mass production.

To further provide an effective ESD discharging path from VSS2 to the common VSS ESD bus with high enough isolation for noise coupling, the bidirectional silicon-controlled rectifier (SCR) devices with suitable ESD-detection circuits can be used to replace the series diodes in the ESD conduction circuits [20]. The SCR device in the off state has a high voltage blocking effect between its anode and cathode to overcome the noise coupling issue or leakage current issue [21]. The SCR device in the on state can sustain much higher ESD level in a small layout area. The ESD conduction circuit, realized with the bidirectional SCR devices, is suggested to this IC product for future product version in a 0.18-μm CMOS process.

IV. Conclusion

A real case of ESD improvement on an IC product with a lot of multiple separated power pairs has been studied in detail. The I/O pins can pass the 5-kV HBM ESD stress, but some internal damage has been found located at the interface circuit between the circuit blocks with different power supplies. A final solution with the common ESD bus line, realized by the modified seal ring, is added to surround the whole chip with ESD conduction circuit connecting to every separated VSS power line. The two series diodes in bidirection connection are used in the ESD conduction circuit to provide the ESD current discharging path between the separated VSS power lines, and also to provide high enough noise margin between the separated VSS power lines. The overall HBM ESD level of this IC product with 12 separated power pairs has been successfully improved from the original l kV to greater than 5 kV. This study provides an important example of the effectiveness of an ESD bus for effective whole-chip ESD protection design which will become more useful in the sub-quarter-micron CMOS technologies with the much thinner gate oxide and the system-on-a-chip (SoC) products with more separated mixed-voltage power supplies.

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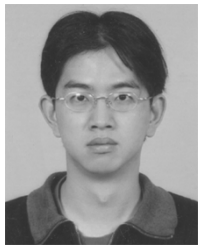

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