ESD Protection Design With Lateral DMOS Transistor in 40-V BCD Technology

Chang-Tzu Wang, *Student Member, IEEE*, and Ming-Dou Ker, *Fellow, IEEE*

***Abstract*—An electrostatic discharge (ESD) protection design for smart power applications with lateral double-diffused MOS (LDMOS) transistors is investigated. With the gate-driven and substrate-triggered circuit techniques, the n-channel LDMOS can be quickly turned on to protect the output drivers during an ESD stress event. The proposed gate-driven and substrate-triggered ESD protection circuits have been successfully verified in a 0.35-μm 5 V/40 V bipolar CMOS DMOS (BCD) process, which can sustain ESD voltages of 4 kV in human-body-model (HBM) and 275 V in machine-model (MM) ESD tests. In addition, the power-rail ESD protection design can also be achieved with a stacked structure to protect 40-V power pins without a latchup issue in the smart power integrated circuits.**

***Index Terms*—Bipolar CMOS DMOS (BCD) process, electrostatic discharge (ESD), ESD protection, latchup.**

I. Introduction

DMOS power transistors have been commonly used as output drivers in smart power technologies [1], [2], including the automotive integrated circuits (ICs). Such high-voltage transistors are often self-protecting against an electrostatic discharge (ESD) stress. The DMOS devices were employed for the ESD protection of high-voltage pins by channel current under a gate biasing condition [3]. However, the high-voltage device with a large amount of finger numbers did not have a high ESD robustness after entering the snapback breakdown region. Such a device exhibits random and unconstrained failures during the snapback breakdown before reaching its intrinsic limitation [4]. The medium-sized drivers are usually not robust enough to pass the typical industrial ESD specifications of 2 kV for the human body model (HBM) [5] and 200 V for the machine model (MM) [6]. This is attributed to the current crowding effect among the multiple fingers and then inducing inhomogeneous triggering of the parasitic BJT to cause the nonuniform turn-on issue [7], [8]. Therefore, an additional ESD protection design is needed to protect such output drivers in the high-voltage technologies [9].

To improve the turn-on speed of MOS transistors for the ESD protection, a resistance_capacitance-based ESD protection design (with a MOS capacitor) has been widely used in advanced CMOS processes [10]. However, no MOS capacitor is available to sustain the high-voltage operation due to the thin gate oxide structure of the lateral DMOS transistor (e.g., Vd = 40 V and Vg = 5 V) in such a high-voltage technology studied in this work. If the MOS capacitor is implemented by such thin gate oxide and biased at a high voltage level, the overstress voltage will damage the thin gate oxide. Furthermore, the ESD ballast resistor of several hundred ohms is forbidden to be placed between the output pad (O/P) and the output driver, which was often designed with a specification of small turn-on resistance in applications. In such a case, the additional ESD protection circuit is placed in parallel with the output driver from the pad to the ground. If the additional ESD protection circuit was not turned on quickly enough, the output driver would be damaged during an ESD stress event. Therefore, it is important to develop an efficient ESD protection circuit that can effectively protect the high-voltage output drivers for various applications.

In this paper, two efficient ESD protection designs with n-channel lateral DMOS (LDNMOS) transistors are proposed without suffering the gate oxide reliability under the normal circuit operation. With the gate-driven and the substrate-triggered circuit techniques, the turn-on speed of the LDNMOS device can be improved during an ESD stress event. Such an ESD protection design with the gate-driven ESD detection circuit can be further modified to achieve a latchup-free power-rail ESD protection circuit for the high-voltage power pins. The proposed ESD protection circuits have been successfully verified in a 0.35-μm 5 V/40 V bipolar CMOS DMOS (BCD) process.

II. Characteristics of LDNMOS With Gate-Biased and Substrate-Triggered Effects

The device cross-sectional view and the layout top view of the LDNMOS with a field oxide (FOX) located at the drain region in a 0.35-μm 5 V/40 V BCD process are shown in Fig. 1(a) and (b), respectively. The gate oxide thickness of such a device is only 14 nm, limiting the maximum applicable gate voltage to 5 V. The N-drift and the P-body layers in Fig. 1(a) are lightly doped regions. The device is completely surrounded by the deep n-well (DNW) structure. The LDNMOS used as the ESD clamp device in the ESD protection circuit is drawn in multiple octagonal cells, as shown in Fig. 1(b). The side length of the octagon is 10 μm (the channel length of each

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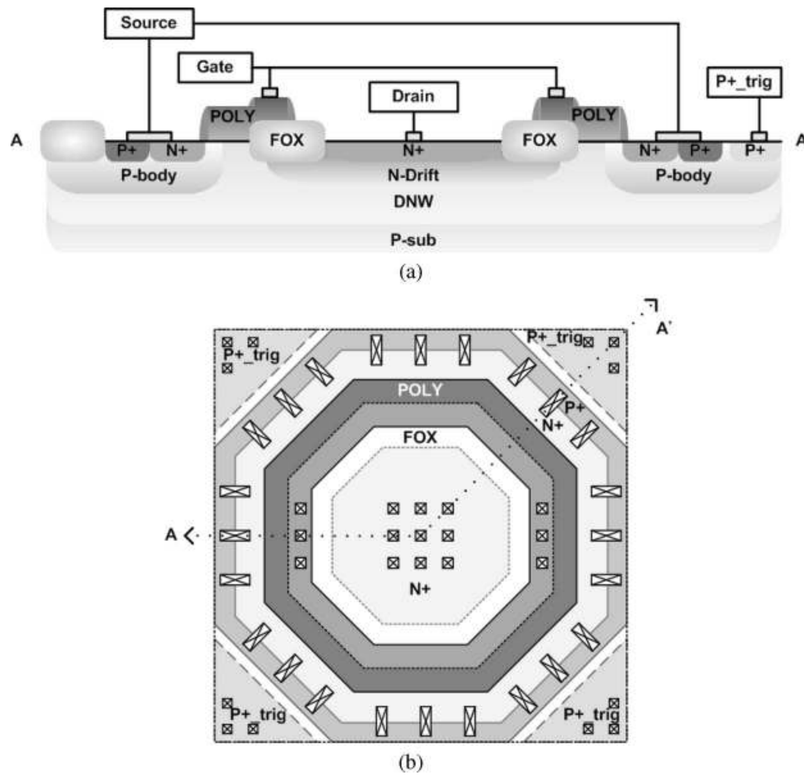


Fig. 1. (a) Device cross-sectional view and (b) layout top view of the octagonal unit cell of the LDNMOS with 5-V gate oxide and 40-V drain-to-source operating voltage in a 0.35-μm 5 V/40 V BCD process.

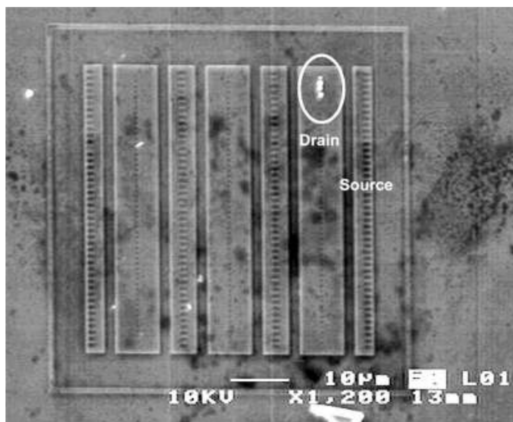


Fig. 2. After a 3-kV HBM ESD stress, the failure spots were found only at a few contacts at the drain side of the LDNMOS drawn with the multiple-finger structure.

side), and therefore, the perimeter of each cell is 80 μm. The P+_trig regions at the four corners are drawn as the trigger nodes for implementation of the substrate-triggered technique. In the traditional multiple-finger structure, the P-body regions of all fingers are fully separated by the FOX, and the individual P-body regions could worsen the nonuniform turn-on behavior of the LDNMOS device. Fig. 2 shows the ESD failure location of the gate-grounded LDNMOS device drawn by a traditional multiple-finger structure after a 3-kV HBM ESD stress. Only a few contacts were damaged at the drain diffusion during an ESD stress event. Therefore, the nonuniform turn-on phenomenon among the multiple fingers of the LDNMOS device is easily observed, and the ESD robustness is hard to be improved by only increasing the device dimension. On the other hand, the P-body regions at the source side are connected to each other if the LDNMOS is constructed by multiple octagonal cells with the P+_trig regions located around the LDNMOS. The LDNMOS can be assembled by multiple cells of row number and column number to reach a larger total device width for higher current conducting capability. In this paper, the LDNMOS is built up by 2×2 octagonal cells, and the equivalent total device width is 320 μm, as shown in Fig. 3. Moreover, such an octagonal structure can be applied for the gate-biased technique or the substrate-triggered technique (which is widely used in CMOS process [11]) by connecting the gate node or the P+_trig node to the bias/trigger circuits. To clarify the effectiveness of the gate-biased and substrate-triggered techniques on a high-voltage (HV) LDNMOS device, the technology computer-aided design (TCAD) simulation study is performed in the following. The device structure of the LDNMOS for TCAD simulation for this work is shown in Fig. 4.

A. LDNMOS With the Gate-Biased Technique

The TCAD-simulated I–V curves of the LDNMOS with different gate-biased conditions are shown in Fig. 5. Without the bias voltage on the gate terminal ($\mathrm{Vg} = 0$ V), the trigger voltage of the LDNMOS is around 58 V. When the bias voltage is increased, the channel current is generated to improve the turn-on speed of the parasitic n-p-n bipolar junction transistor (NPN BJT) (DNW/P_Body/N+), and then, the trigger voltage of the LDNMOS can be reduced. The trigger voltage can be reduced to 47 V when a 5-V bias is applied at the gate of the

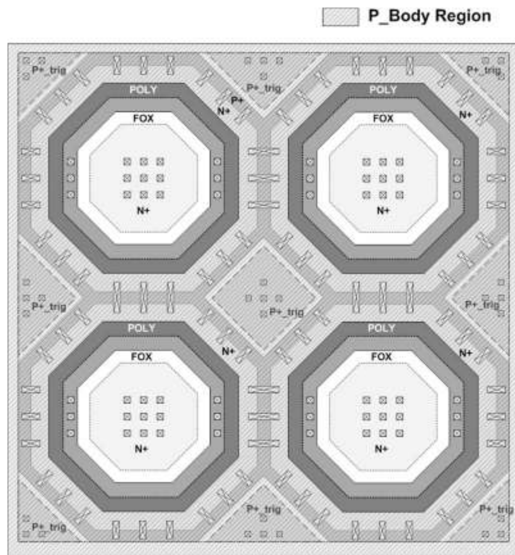


Fig. 3. Layout top view of an LDNMOS, which is constructed by 2 × 2 octagonal cells. In this structure, the P_Body regions of all the cells are connected to each other.

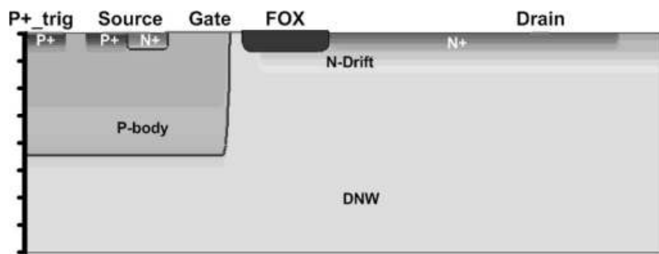


Fig. 4. Device structure of the LDNMOS for TCAD simulation.

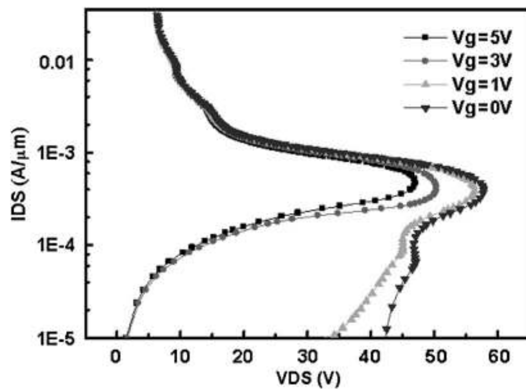
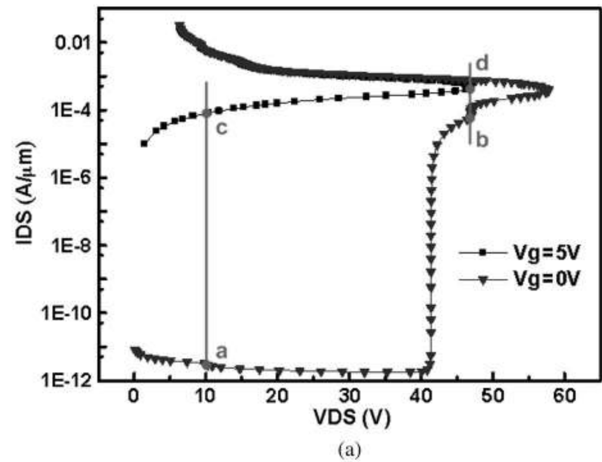


Fig. 5. TCAD-simulated I–V curves (IDS_VDS) of the LDNMOS device with different gate biases.



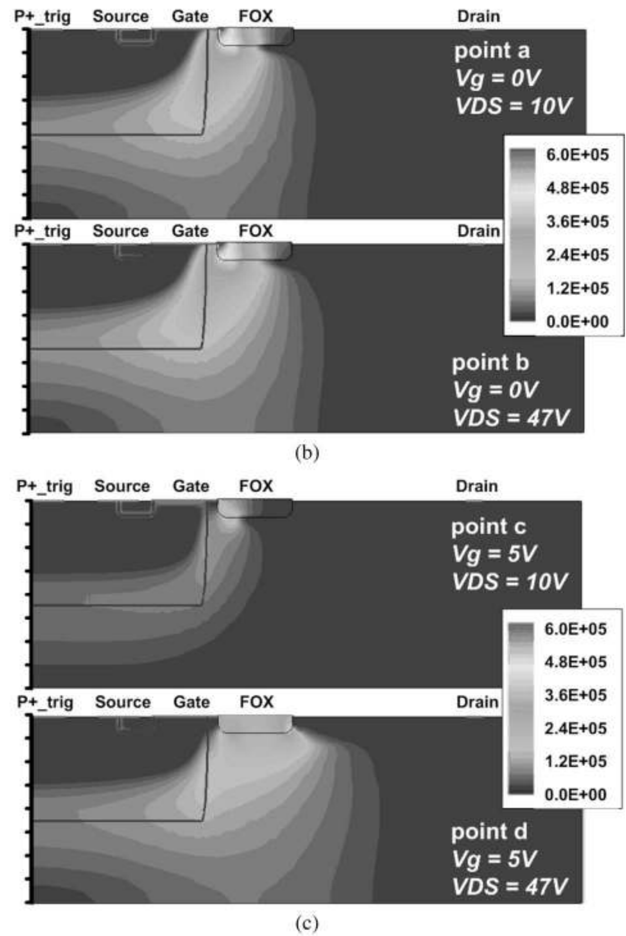


Fig. 6. (a) TCAD-simulated I–V curves of the LDNMOS device and the corresponding electric field distribution of the LDNMOS device with Vg of (b) 0 V and (c) V under VDS of 10 V and VDS of 47 V.

LDNMOS. To compare the difference between the LDNMOS device with and without gate bias, the I–V curves of the LDNMOS with Vgs of 0 and 5 V are replotted in full scale and shown in Fig. 6(a). Points a, b, c, and d are marked on the curves to compare the corresponding electric field distribution under VDSs of 10 and 47 V (the trigger voltage of LDNMOS with Vg of 5 V). The electric field distribution of the LDNMOS with Vg of 0 V at points a and b of the I–V curve are shown in Fig. 6(b). Without gate bias voltage, the electric field distribution localizes at the FOX edge, and no turn-on phenomenon appears even if the VDS is increased to 47 V. On the other hand, the electric field distribution of the LDNMOS with Vg of 5 V at the points c and d of the I–V curve are shown in Fig. 6(c). With a gate bias of 5 V, the channel current along the surface can release the amplitude of the electric field and accelerate the turned-on speed of the parasitic NPN BJT in LDNMOS. When the VDS is increased to 47 V, the LDNMOS is going to enter the snapback region, and the localization of electric field

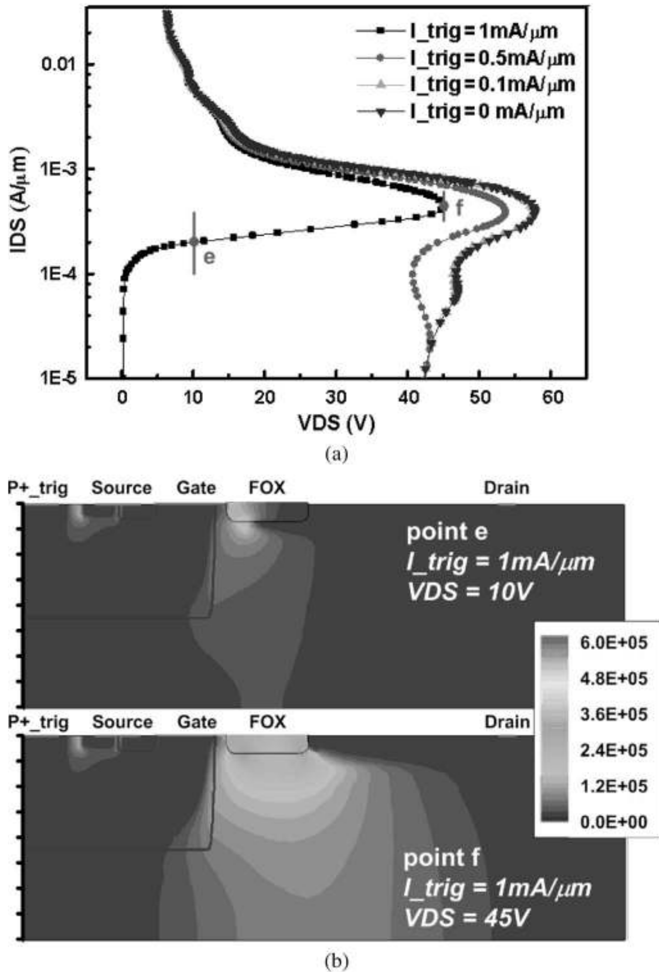


Fig. 7. (a) TCAD-simulated I–V curves of the LDNMOS device with different substrate-triggered currents (I_trig) and (b) the electric field distribution at VDS of 10 V and VDS of 45 V under I_trig of 1 mA/μm.

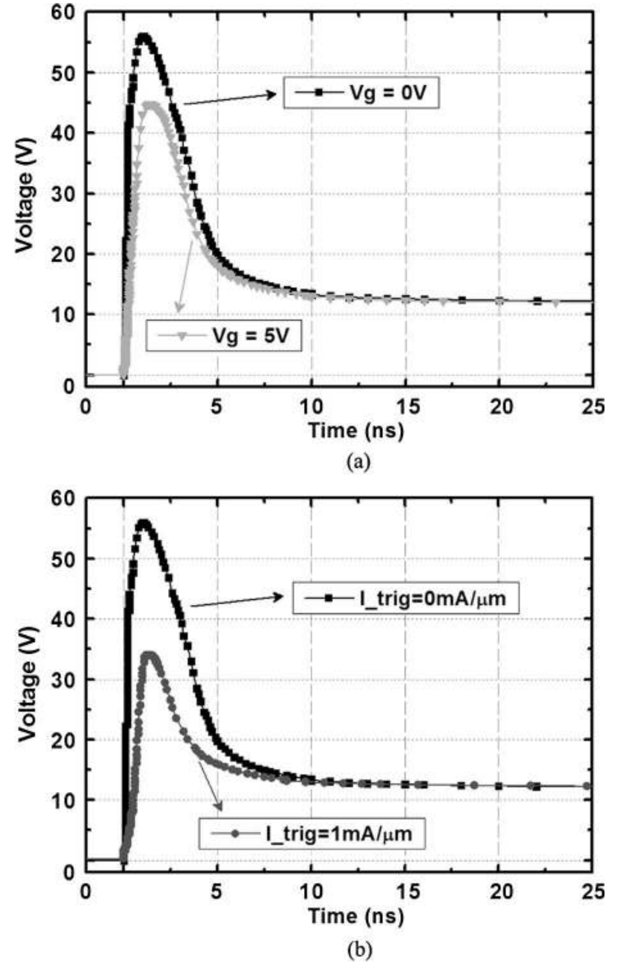


Fig. 8. TCAD-simulated transient behaviors of the LDNMOS with and without (a) gate-biased voltage or (b) substrate-triggered current, where a 5-mA/μm current pulse with a rise time of 10 ns is applied to the drain side of the LDNMOS.

distribution is shifting from the FOX edge to the N_Drift region at the drain side. From the simulation, the gate-biased technique can improve the turn-on behavior of the LDNMOS device.

B. LDNMOS With the Substrate-Triggered Technique

The TCAD-simulated I–V curves of the LDNMOS with different substrate-triggered currents (I_trig) are shown in Fig. 7(a). The substrate-triggered current flowing from P_trig to N+ region at the source side will provide the base current of the parasitic NPN BJT to trigger it on. When the substrate-triggered current is higher than 0.5 mA/μm, the trigger voltage of the LDNMOS will be reduced. With I_trig of 1 mA/μm, the trigger voltage is reduced to 45 V. The electric field distributions of the LDNMOS with I_trig of 1 mA/μm at point e (under VDS of 10 V) and point f (under VDS of 45 V) of the I–V curve are shown in Fig. 7(b). In the simulation, the substrate-triggered current flowing from the P_trig to N+ region is obvious, and it generates a voltage difference between the base and the emitter of the parasitic NPN BJT to trigger on the LDNMOS. Therefore, the substrate-triggered technique is also a useful method for accelerating the turn-on speed of the LDNMOS device for ESD protection.

C. Transient Behavior of LDNMOS With Gate-Biased and Substrate-Triggered Techniques

The transient behaviors of the LDNMOS and the LDNMOS with the gate-biased and the substrate-triggered techniques under fast-transient ESD-like event are shown in Fig. 8(a) and (b), where a 5-mA/μm current pulse with a rise time of 10 ns is applied to the drain side of the LDNMOS in this simulation. In Fig. 8(a), the LDNMOS with Vg of 0 V is turned on when the drain voltage is higher than 57 V. However, the LDNMOS with Vg of 5 V can be accelerated to be turned on when the drain voltage is higher than 45 V. On the other hand, the LDNMOS with I_trig of 1 mA/μm can be turned on when the drain voltage is higher than 35 V, as shown in Fig. 8(b). From the TCAD simulation, the turn-on period of LDNMOS can be shortened by applying the gate-biased or the substrate-triggered effects.

III. Implementation of ESD Protection Circuit With LDNMOS

The proposed ESD protection designs with the gate-driven ESD detection circuit (gate-biased technique) and the substrate-triggered ESD detection circuit are shown in Fig. 9(a) and (b),

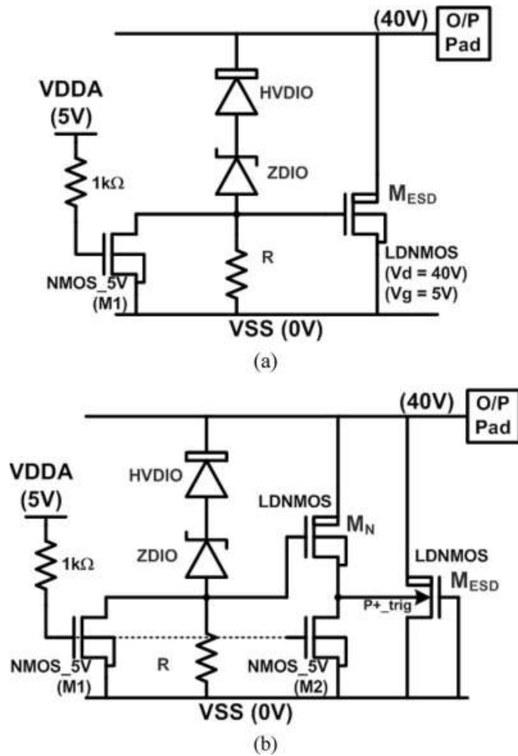


Fig. 9. Proposed ESD protection circuits with (a) gate-driven and (b) substrate-triggered ESD detection circuits.

respectively, which are named as the gate-driven ESD protection circuit and the substrate-triggered ESD protection circuit in this paper. The ESD clamp device (M_{ESD}) is implemented by the LDNMOS with 2 × 2 octagonal cells, as discussed in Section II. In Fig. 9(a), the gate-driven ESD detection circuit is composed of a 40-V HV diode (HVDIO), a 7-V Zener diode (ZDIO), a 10-kΩ resistor (R), and a 5-V NMOS device (M1). The reverse-biased HVDIO and the ZDIO are connected in series to sustain the high-voltage (40 V) applications on the O/P during the normal circuit operating condition. A margin of 7 V from the total breakdown voltage of the diodes to the operating voltage is used to avoid mistriggering on the LDNMOS, even if a 10% overshooting voltage happens to the pad. Therefore, the gate-driven ESD protection circuit can be ensured against the gate oxide overstress issue under the normal circuit operating condition. The gate of M1 is connected to the low-voltage power supply (VDDA). The turned-on NMOS (M1) keeps the gate of the LDNMOS at VSS, so the ESD clamp device (M_{ESD}) is guaranteed to be kept off during the normal operating condition. When a positive fast-transient ESD voltage is applied to the O/P with VSS grounded and VDDA floating, the HVDIO and the ZDIO will enter the breakdown mode to conduct some of ESD current across the resistor R to generate a bias voltage to the gate of M_{ESD}. Therefore, the gate voltage of M_{ESD} can be quickly pulled up to turn itself on by the gate-biased technique during ESD stress. After that, the ESD clamp device enters the snapback region to discharge the ESD current from the O/P to VSS. The VDDA is initially floating with an initial voltage level of ∼0 V during an ESD stress event, so M1 is kept in the OFF-state without an influence on the operation of the ESD clamp device.

In Fig. 9(b), the substrate-triggered ESD protection circuit includes not only the HVDIO, ZDIO, R, and M1 (which are used in gate-driven ESD detection circuit), but also an additional LDNMOS (M_N) as driving element and a 5-V NMOS device (M2). The gates of M1 and M2 are connected to VDDA to keep the voltage levels at the gate of M_N and the P+_trig node of the ESD clamp device (M_{ESD}) at VSS. During the ESD transient event, the driving element M_N is turned on by the gate-biased effect from the diodes in breakdown mode and then generates some channel current through M_N into the P+_trig node of the ESD clamp device (M_{ESD}). The substrate-triggered effect can be accomplished to accelerate the turn-on speed of the ESD clamp device.

IV. Experimental Results

The proposed ESD protection circuits have been fabricated in a 0.35-μm 5 V/40 V BCD process. No any additional mask layer is needed to fabricate the proposed ESD protection circuits. The typical gate-coupled LDNMOS, by connecting a resistor from its gate to VSS, has been also fabricated in the same wafer for comparison with the proposed gate-driven and the substrate-triggered ESD protection circuits. The gate-coupled LDNMOS is drawn by a multiple-finger structure with each finger width of 75 μm, and the total device width is 300 μm. On the other hand, the ESD clamp device in the proposed ESD protection circuits are drawn by 2 × 2 octagonal cells with an equivalent total device width of 320 μm. To investigate the device behavior during ESD stress, the transmission line pulsing (TLP) technique [12] has been widely used to measure the trigger voltage (Vt1) and the secondary breakdown current (It2) of the ESD devices. The TLP generator with a pulsewidth of 100 ns and a rise time of 10 ns is used in this work to find the Vt1 and It2 of the LDNMOS with the gate-biased or substrate-triggered technique. The HBM ESD levels and the MM ESD levels of the ESD protection circuits are measured by the KeyTek ZapMaster, and the failure criterion is defined as the I–V characteristic curve shifting over 20% from its original curve after three continuous ESD zaps at every ESD test level.

A. *TLP Characteristics of Stand-Alone LDNMOS With Gate-Biased or Substrate-Triggered Effects*

The TLP-measured I–V characteristics of the LDNMOS device drawn by 2 × 2 octagonal cells with an equivalent total device width of 320 μm under different gate-biased voltages (Vg) are shown in Fig. 10. Without any gate-biased voltage, the Vt1 of the LDNMOS device is ∼60 V. When the gate-biased voltage is increased to 1, 3, and 5 V, the Vt1 of the LDNMOS device is reduced to around 57, 50.5, and 48 V, respectively. With gate-biased voltages of 8 and 10 V, the Vt1 of the LDNMOS device can be reduced to ∼40 V. The TLP-measured I–V characteristics of the LDNMOS device drawn by 2 × 2 octagonal cells with an equivalent total device width of 320 μm under different substrate-triggered currents (I_trig) are shown in Fig. 11. When the applied substrate-triggered current is higher than 130 mA (equivalent to 0.4 mA/μm), the parasitic

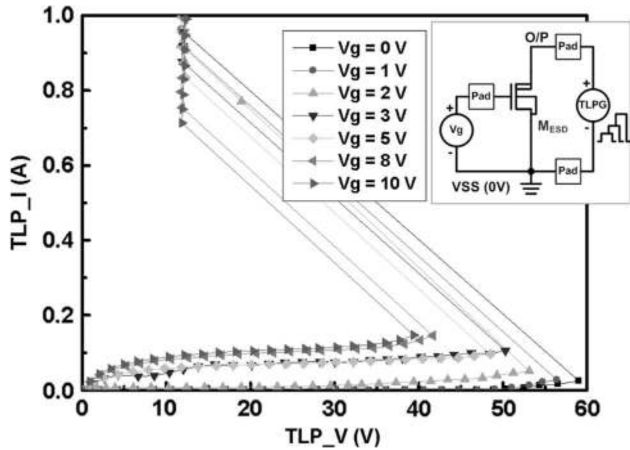


Fig. 10. TLP-measured I–V curves of the LDNMOS device drawn by 2 × 2 octagonal cells with a device width of 320 μm under different gate-biased voltages (Vg).

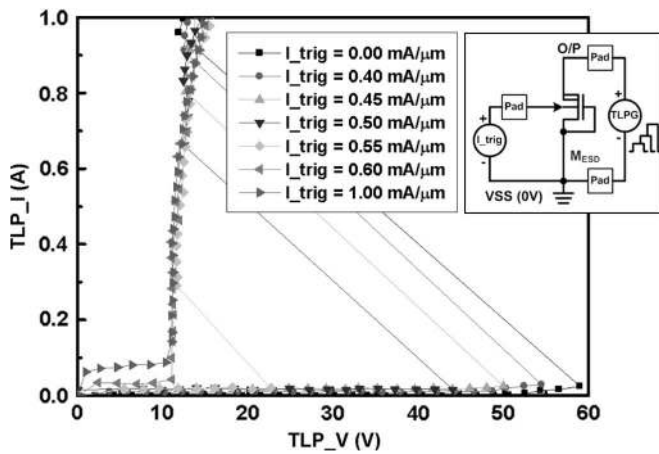


Fig. 11. TLP-measured I–V curves of the LDNMOS device by with 2 × 2 octagonal cells with a device width of 320 μm under different substrate-triggered currents (I_trig).

NPN BJT in the LDNMOS device starts to be turned on, and the Vt1 of the LDNMOS device is reduced. When the I_trig is increased to 0.5 and 0.55 mA/μm, the Vt1 can be reduced to 45 and 23 V, respectively. When the I_trig is higher than 0.6 mA/μm, the LDNMOS can be turned on rapidly to enter the snapback region without the breakdown mechanism, so the Vt1 is observed as ∼11 V. From the experimental results of the TLP characteristics of the LDNMOS device with a gate-biased voltage and a substrate-triggered current, the acceleration to the turn-on speed of LDNMOS device can be achieved by the gate-biased or the substrate-triggered techniques.

To further evaluate the turn-on behaviors of the LDNMOS with gate-biased effects, the measured voltage waveforms clamped by the LDNMOS under different TLP voltage levels are shown in Fig. 12(a)–(f), where the rise time and the width of the applied pulse is 10 and 100 ns, respectively. In Fig. 12, with a higher gate-biased voltage, the LDNMOS can be turned on under a smaller applied TLP voltage. The applied 54-V TLP voltage can be clamped by the LDNMOS with Vg of 5 V. However, at that time, the LDNMOS without any gate-biased voltage is still inactive. When the applied TLP voltage is as high as 60 V, the LDNMOS with all the gate-biased conditions can be turned on, but the turn-on time to clamp the applied voltage is different for each condition. The turn-on time to clamp the applied voltage can be shortened when the gate-biased voltage is increased. On the other hand, the measured voltage waveforms clamped by the LDNMOS with different substrate-triggered currents under different TLP voltage levels are shown in Fig. 13(a)–(d). Under a TLP applied voltage of 50 V, the LDNMOS with I_trig higher than 0.5 mA/μm can be turned on when the voltage is higher than 30 V. From these results, the acceleration of the turn-on speed by the gate-biased or the substrate-triggered effects can be verified.

B. ESD Performance of LDNMOS With Gate-Coupled Design

The TLP-measured I–V characteristics of the gate-coupled LDNMOS with resistances of 10 and 50 kΩ are shown in Fig. 14. The trigger voltage of the gate-coupled LDNMOS with device width of 300 μm is still ∼60 V, which is the same as the Vt1 of the standalone gate-grounded LDNMOS with the same device width. Moreover, there is no obvious difference between these two conditions with resistances of 10 and 50 kΩ because the parasitic capacitance from gate to drain of the LDNMOS device is too small to couple sufficient transient voltage to the gate for triggering on the LDNMOS device.

C. ESD Performance of LDNMOS With Gate-Driven and Substrate-Triggered ESD Detection Circuits

The TLP-measured I–V characteristics of the gate-driven ESD protection circuit and the substrate-triggered ESD protection circuit are shown in Fig. 15, where the I–V characteristic of the gate-coupled LDNMOS with a resistance of 10 kΩ is also plotted into the figure for comparison. As seen in Fig. 15, the LDNMOS starts to be turned on by the gate-driven or the substrate-triggered ESD detection circuit when the applied voltage is higher than 47 V. The Vt1 of the LDNMOS with the gate-driven ESD detection circuit and the substrate-triggered ESD detection circuit can be reduced to ∼55 and ∼51 V, respectively. From the TLP-measured I–V curves, both the gate-driven and the substrate-triggered ESD detection circuits are effective in triggering the LDNMOS device, where the substrate-triggered ESD detection circuit gains more benefits to reduce the Vt1. However, it needs an additional device M_N as the driving element, which will occupy some layout area. The leakage current of the gate-coupled LDNMOS was obviously increased when the TLP current is higher than 2.1 A. The failure criterion for the It2 measurement is determined by leakage current increasing by 30% compared to that of fresh samples in this work. Therefore, the It2 level of the gate-coupled LDNMOS is determined as 2.1 A. However, the It2 of the LDNMOS drawn by 2 × 2 octagonal cells with the gate-driven and the substrate-triggered ESD detection circuits can be improved up to 2.6 and 2.7 A, respectively.

The HBM and MM ESD levels of the gate-coupled LDNMOS, the gate-driven ESD protection circuit, and the substrate-triggered ESD protection circuit are listed in Table I. The gate-coupled LDNMOS has ESD levels of 3 kV in HBM and 200 V in MM ESD tests. With the gate-driven ESD

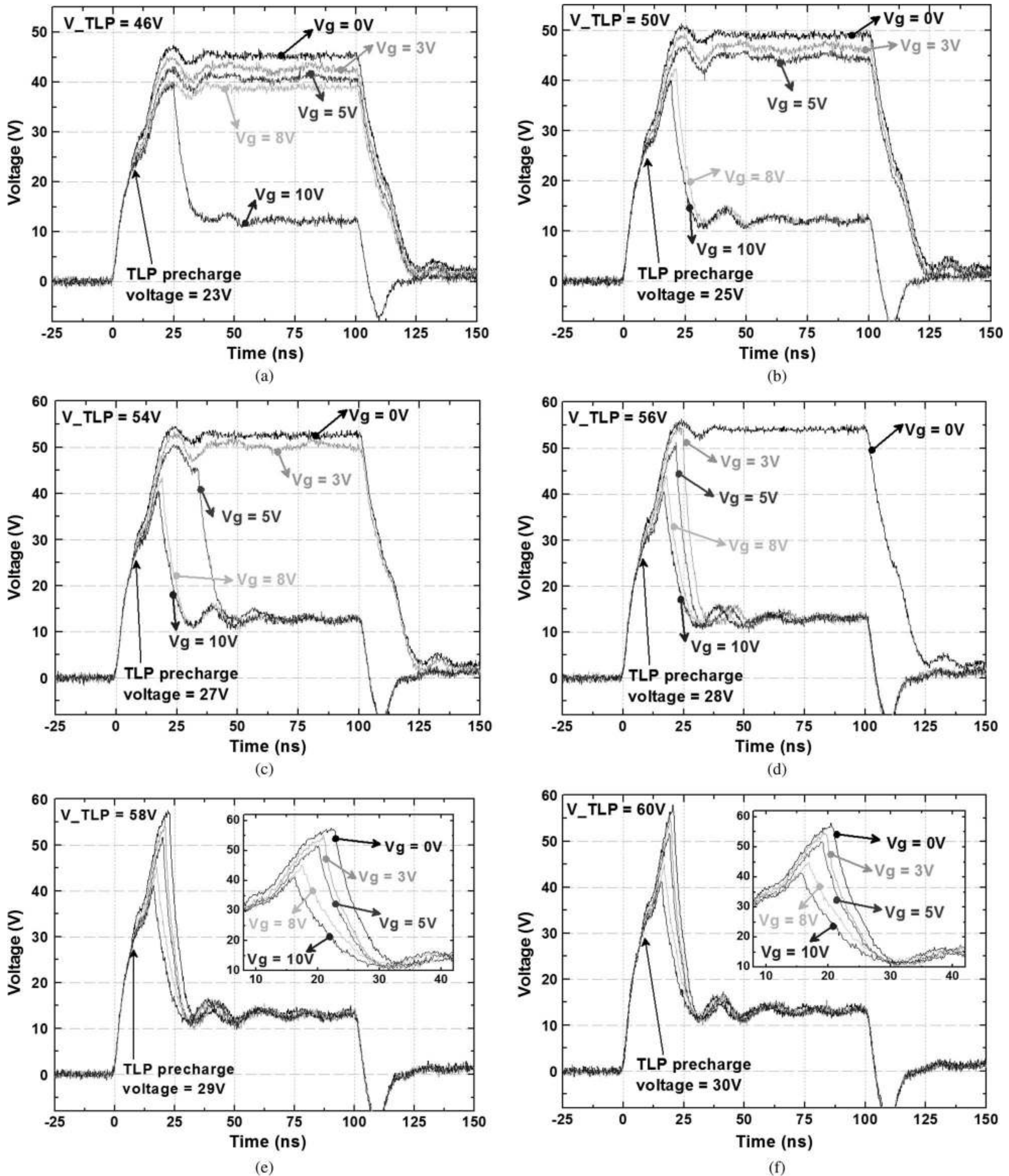


Fig. 12. Measured voltage waveforms clamped to verify the turn-on efficiency of the LDNMOS with different gate-biased voltage by applying a TLP voltage pulse with the voltage level of (a) 46 V, (b) 50 V, (c) 54 V, (d) 56 V, (e) 58 V, and (f) 60 V.

detection circuit, the HBM and the MM ESD levels of the LDNMOS can be improved to 4.4 kV and 275 V, respectively. With the substrate-triggered ESD protection circuit, the HBM and the MM ESD levels of the LDNMOS are 4.2 kV and 275 V, respectively. No obvious difference in the ESD robustness of the LDNMOS device with these two ESD detection circuits because each octagonal cell of the LDNMOS device can be turned on uniformly. If a higher ESD level is desired, the number of the octagonal cells in the LDNMOS should be increased to sustain the ESD stress.

D. Failure Analysis

The experimental results have shown that the trigger voltage of the LDNMOS device can be substantially reduced by the gate-driven and the substrate-triggered ESD detection circuits.

Fig. 13. Measured voltage waveforms clamped to verify the turn-on efficiency of the LDNMOS with different substrate-triggered current by applying a TLP voltage pulse with the voltage level of (a) 50 V, (b) 52 V, (c) 56 V, and (d) 60 V.

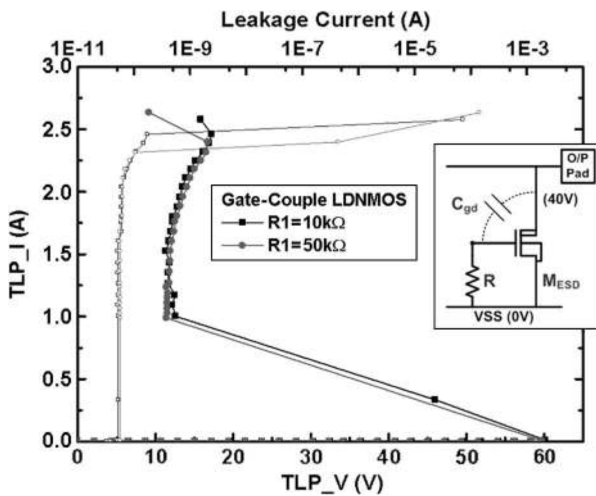


Fig. 14. TLP-measured I–V characteristics of the gate-coupled LDNMOS (drawn by multiple-finger structure with a width of 300 μm) with resistances of 10 and 50 kΩ connected from gate to source.

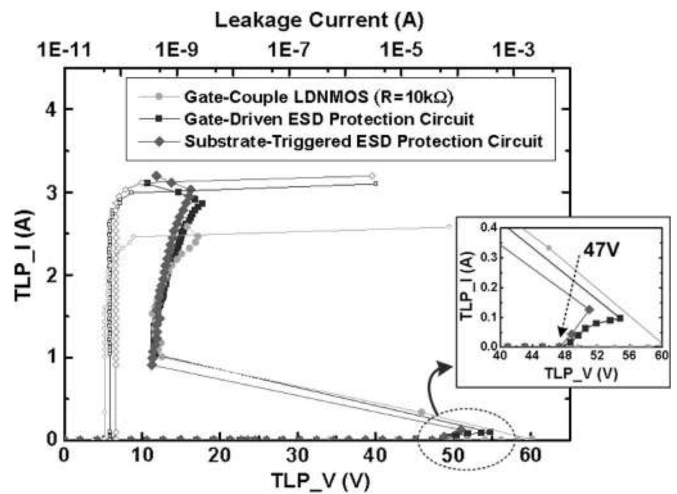


Fig. 15. TLP-measured I–V characteristics of the LDNMOS with the proposed ESD detection circuits and the gate-coupled LDNMOS.

Failure analyses carried by the scanning electron microscope [13] images provide the visual evidence to the LDNMOS device drawn in multiple octagonal cells, which can be triggered on uniformly by the ESD detection circuit. Fig. 16 shows the ESD failure locations on the proposed gate-driven ESD protection circuit after a 4.6-kV positive-to-VSS HBM ESD stress. The failure spots were found at the drain contacts in each cell of

TABLE I
COMPARISON OF ESD ROBUSTNESS AMONG THE GATE-COUPLED LDNMOS, GATE-DRIVEN ESD PROTECTION CIRCUIT, AND SUBSTRATE-TRIGGERED ESD PROTECTION CIRCUIT

	Layout Type of M_{ESD}	Width of M_{ESD}	HBM ESD Level	MM ESD Level	It2 (TLP)
Gate-Coupled LDNMOS	Multiple-Finger	300μm	3kV	200V	2.1A
Gate-Driven ESD Protection Circuit	Octagonal Cells	320μm	4.4kV	275V	2.6A
Substrate-Triggered ESD Protection Circuit	Octagonal Cells	320μm	4.2kV	275V	2.7A

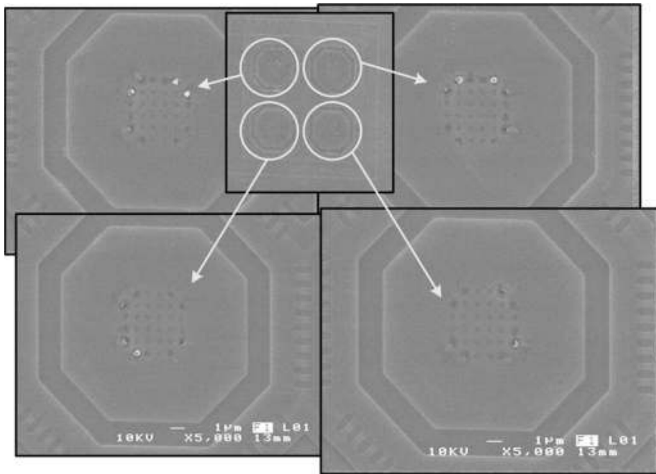
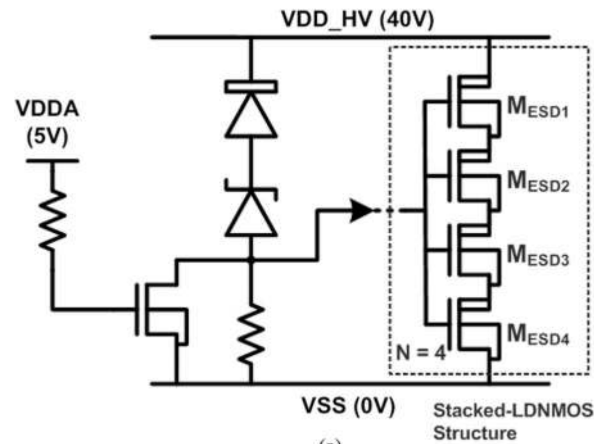


Fig. 16. After a 4.6-kV HBM ESD stress, the failure spots were found at the drain contacts of each unit cell of the LDNMOS device with the gate-driven ESD protection circuit.



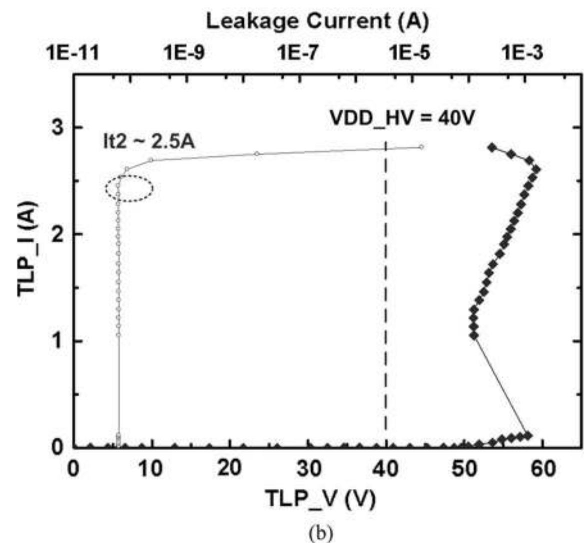


Fig. 17. (a) Latchup-free ESD protection circuit realized with four stacked-LDNMOS devices and the gate-driven ESD detection circuit for 40-V power pins and (b) the corresponding TLP-measured I–V characteristics.

the LDNMOS device, indicating that the LDNMOS device has been uniformly turned on by the proposed gate-driven ESD detection circuit.

V. Power-Rail ESD Protection Design

From the TLP-measured I–V characteristic in Fig. 15, the snapback holding voltage of LDNMOS with the gate-driven or substrate-triggered ESD detection circuit is ~12 V, which is smaller than the HV power supply voltage (VDD_HV) of 40 V. Such an ESD element used in the power-rail ESD protection circuit may be mistriggered on by the system-level ESD transient pulse to cause a latchup failure [14], [15]. To overcome the latchup issue between the power rails, the stacked-LDNMOS structure is used to increase the total holding voltage. With the gate-driven ESD detection circuit, the trigger voltage of the stacked-LDNMOS structure can still be kept the same as that of the design in Fig. 9(a). The circuit diagram of the stacked-LDNMOS structure (four LDNMOS devices in series, where each LDNMOS is drawn by multiple-finger structure with a width of 300 μm) with the gate-driven ESD detection circuit is shown in Fig. 17(a). The corresponding TLP-measured I–V characteristic is shown in Fig. 17(b). During an ESD stress, the stacked-LDNMOS can be triggered into the snapback region to discharge the ESD current. With a total holding voltage of ~50 V, the latchup issue can be successfully overcome for 40-V applications [16]. Therefore, the latchup-free power-rail ESD protection circuit can be safely applied in IC products with a high-voltage power supply voltage of 40 V. The It2 level is still kept at ~2.5 A, so the ESD performance of the stacked-LDNMOS structure with the gate-driven ESD detection circuit can be kept as good as that of a single LDNMOS device. Of course, the stacked-LDNMOS can also be implemented with the layout of octagonal cells in the power-rail ESD protection circuit.

VI. Conclusion

The device characteristics of the LDNMOS with the gate-biased and the substrate-triggered effects have been investigated in details by the TCAD simulation and the TLP measurement. Based on such device behaviors, two ESD protection circuits cooperated with LDNMOS transistors for 40-V O/P have been successfully verified in a 0.35-μm 5 V/ 40 V BCD process. The proposed ESD protection circuits with the gate-driven and the substrate-triggered techniques have performed the efficient turn-on uniformity with robust

ESD levels, which are excellent design solutions to protect the high-voltage output drivers for smart power applications. By using the stacked-LDNMOS structure with the gate-driven ESD detection circuit, the latchup-free ESD protection circuit can be achieved for protecting the high-voltage power pins.

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