ESD Protection Device and Circuit Design for Advanced CMOS Technologies

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Dedication

"To my wife, Eva Guerassimova,
for her patience, understanding,
support and encouragement"

Oleg Semenov

"To my parents, Ashraf Moghimi
and Mohsen Sarbisaei"

Hossein Sarbishaei

"To my graduate students"

Manoj Sachdev

Contents

Preface

The challenges associated with the design and implementation of Electrostatic Discharge (ESD) protection circuits become increasingly complex as technology is scaled well into nano-metric regime. One must understand the behavior of semiconductor devices under very high current densities, high temperature transients in order to surmount the nano-meter ESD challenge. As a consequence, the quest for suitable ESD solution in a given technology must start from the device level. Traditional approaches of ESD design may not be adequate as the ESD damages occur at successively lower voltages in nano-metric dimensions.

This book makes an attempt to address ESD circuit design issues in a systematic manner. As ESD event is a high current/voltage phenomenon, predicting device behavior in this regime is only possible with device-level simulators. Yet, in a modern CMOS technology most of the process parameters are not available to majority of designers, especially in fabless companies. Therefore, the device parameters should be first calibrated with the given process technology at normal operating conditions. In the next step these process parameters are used to create and simulate the individual ESD protection devices in the device simulation environment. After successful design of an ESD protection element, mixed-mode, circuit-device level simulations are carried out to ensure proper ESD circuit design for a given purpose, say I/O or a clamp. Finally, a test chip is fabricated to evaluate performance of the ESD protection circuit with standard ESD measurement equipments, i.e. HBM/MM/CDM testers and TLP tester.

We started to investigate the ESD circuit design issues at University of Waterloo in 2001 for high speed I/Os. Very soon it became apparent that

ESD circuit design and layout is an art rather than a science. Our objective was to establish a design flow so that interested ESD designers could use it for robust ESD protection circuit design. Furthermore, we were also interested in establishing a cause and effect relationship between design parameters and achieved ESD protection early in the design phase in order to reduce the design time. Over the last several years, we designed a variety of ESD protection circuits in different technologies following the above mentioned design flow. They are described in various chapters of the book.

This book is intended for engineers working in the areas of device and I/O circuit design. In addition, as the problems associated with ESD failures and yield losses become significant in the modern semiconductor industry, the demand for graduates with a basic knowledge of ESD is also increasing. Today, there is a significant demand to educate the circuits design and reliability teams in ESD, since nuisance value of inadequate ESD protection is very high. It should be noted that a large volume of work has done on various aspects of ESD and is scattered in publications. Authors acknowledge that there are few very good quality books on the subject. We have made an effort to optimize ESD as well as circuit design objectives. In addition, we have tried to cover some of the recent topics. Some of the highlights of the book are listed below:

(i) The charge board ESD (CBM) testing that is becoming popular in robust PCB designs used in wireless products such as cell phones and PDAs.

(ii) The impact of burn-in testing (accelerated test methods) on the ESD robustness of deep sub-micron ICs.

(iii) Distributed ESD protection networks optimized for sub-90 nm CMOS ICs.

(iv) ESD protection strategies for smart power ICs that are widely used in automotive industry.

ESD professionals have a several challenges to face as we further scale into nano-metric regime. Due to technology scaling and expansion of automated handling, failures in ICs caused by Charged Device Model (CDM) ESD are an increasingly important reliability issue. Even today, a significant portion of ESD field returns is due to damages originating from CDM stress. Moreover, CDM discharges can cause latent damages which could degrade and eventually lead to definite failures in the ICs. The ESD protection design for current and future sub-65 nm CMOS circuits is a challenge for high I/O count, multiple power domains and flip-chip products. For example, 90 nm

CMOS ASIC design systems offer over 1,500 I/Os and more than 200 analog and high speed serial I/Os. As a consequence, the development and testing of a new sub-65 nm CMOS ESD protection circuits will become a crucial task for academia and semiconductor industry.

Acknowledgments

Several individuals, and organizations have contributed in one way or the other to further the objectives of our ESD research presented in this book. Authors would like to acknowledge several discussions with Vasilis Papanikolaou, Efim Roubakha, Manuel Palacios and Andrew Neely from Gennum Corporation on analog circuits design, ESD protection concepts and ESD measurements.

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Chapter 1

INTRODUCTION

1. NATURE OF ESD PHENOMENA

One of the most observed sources of electrostatic charge is the shock caused by touching a doorknob after walking in a carpeted room. This shock is a result of discharging the body's accumulated charge through a conductive object. Normally, this electrostatic discharge can be a few kilo-volts. In semiconductor industry the discharge path can be through semiconductor devices. Before going through the details of this phenomenon in semiconductor devices, a brief review of static electricity is necessary.

Static electricity is the creation of electrical charge by an imbalance of electrons on the surface of a material which produces an electrical field. When two objects with different electrical potentials are brought in contact, a charge transfer occurs between these two objects. This phenomenon is called electrostatic discharge. There are different ways to create a charge on a material: triboelectric charging, induction, ion bombardment and contact with another charged object. The most common mechanism is triboelectric charging. Triboelectric charging is the creation of charge by the contact and separation of two materials. Consider contact and separation of two uncharged materials. As a result, based on the nature of materials, electrons transfer from one material to the other. Therefore, material that looses electrons becomes positively charged while the other material becomes negatively charged. The amount of this triboelectric charge depends on many factors such as area of contact, speed of separation and relative humidity. Table 1-1 shows some examples of the amount of generated electrostatic charge under different conditions and for two different relative humidity

O. Semenov et al. (eds.), ESD Protection Device and Circuit Design for Advanced CMOS Technologies, 1–19.

situations. It can be seen that higher humidity reduces the generated charge significantly. Electrostatic discharge occurs when this charge is transferred to another material. The resistance of the actual discharge circuit and the contact resistance at the interface between contacting surfaces determines the charge that can cause damage.

As mentioned earlier, the polarity and magnitude of the electrostatic charge depends on the material's characteristic. A table called triboelectric

Table 1-1. Examples of generated electrostatic charge.

Means of generation	10–25% Relative humidity (kV)	65–90% Relative humidity (kV)
Walking across carpet	35	1.5
Walking across vinyl tile	12	0.25
Worker at bench	6	0.1
Poly bag picked up from bench	20	1.2
Chair with urethane foam	18	1.5

Table 1-2. A typical triboelectric series.

Material	Electrostatic polarity
Air	
Human skin	Most positive (+)
Glass	
Human hair	
Nylon	
Wool	
Silk	
Aluminum	
Paper	
Cotton	
Steel	
Wool	
Hard rubber	
Nickel, copper	
Brass, silver	
Gold, platinum	
Acetate fiber (rayon)	
Polyester (mylar)	
Celluloid	
Orlon	
Polystyrene (styrofoam)	
Polyurethane	
Saran	
Polyvinyl chloride	
Silicon	
Teflon	Most negative (–)
Silicon rubber	

series classifies different materials based on their electrostatic property. Table 1-2 shows the triboelectric series table for different materials. It can be seen that air and human skin are capable of carrying the most positive charge, while silicon rubber, teflon and silicon are capable of carrying the most negative charge.

In a triboelectric charging event, the object that is closer to the top of the table takes a positive charge and the other one takes a negative charge. In addition, materials that are further apart on the table generate higher charge than those that are closer. Based on the triboelectric series table, all materials can be electrically charged. However, the amount of generated charge and where and how fast the charge goes depend on the material's electrical characteristics. Insulators, due to their very high resistance, are capable of storing a huge amount of electrostatic charge. As this charge cannot move, it remains on the surface of the material. On the other hand, when an inductor is charged, due to its very low resistance, the generated charge uniformly distributes across the surface of the material.

2. ESD FAILURES IN NANOMETRIC TECHNOLOGIES

Electrostatic Discharge (ESD) is a common phenomenon in the nature. As mentioned in the previous section, the amount of electrostatic charge can be a few kilovolts, which is being discharged extremely fast (in the order of tens of nanoseconds). ESD is a subset of a class of failures known as electrical overstress (EOS). The EOS class is composed of events that apply conditions outside the designed operating environment of the part. These conditions include voltage, current, and temperature.

ESD events occur throughout a product's life. ESD first affects the integrated circuit (IC) early in the wafer-fabrication process. Clean-rooms are good sources for charge-generating materials due to the extensive use of synthetic materials in containers and tools [1]. The electrostatic discharge may reduce the product yield in two ways. A photolithography operation transfers the mask image to the silicon wafers. The ESD event distorts the fine pattern defined on the mask. If the mask is damaged by ESD, then each circuit is printed with this damage [2]. The second mode of ESD damage is a direct discharge to the wafer. This event results in a gate oxide and junction damages [3].

The next stage in a product's life is the assembly operation, where additional ESD hazards are present. In the assembly operation, the wafers must be cut to yield individual dies. These dies are then inspected and placed

in packages. Wires are attached to allow signals to travel from the outside pins to the die. Finally, the package is formed around the die. All of these operations are capable of producing ESD events [4].

As microelectronics technology continues shrink to nano-metric dimensions, ESD damage in integrated circuits has become one of the major reliability issues. Several studies carried out over the past two decades ranked ESD and EOS (electrical overstress) as the major cause for field returned ICs, as it shown in Table 1-3. It was found that ESD related failures can reach up to about 70% failure modes, depending on the product type [5].

Table 1-3. The EOS/ESD failure percentage as total failure modes studied by different author over the years. (Adapted from [6].)

Percentage	51%	72%	23%	38%	45%	43%	39%
Author (year)	Green (88)	McAteer (88)	Euzent (91)	Merill (93)	Wagner (93)	Shumway (95)	Brodbeck (97)

The thinner gate oxide and shallower junction depth used in the advanced technologies make them very vulnerable to ESD damages. The silicidation reduces the ballast resistance provided by drain contact to gate edge spacing (DCGS) with at least a factor of 10. As a result, scaling of the ESD performance with device width is lost and even zero ESD performance is reported for standard silicided devices [6].

ESD failures are caused by at least one of three sources: localized heat generation, high current densities, and high electric field intensities. The current densities associated with an ESD stress unavoidably imply high power dissipations, with consequent rise in the lattice temperature that often results in thermal damages. Silicon has a negative resistance relationship with temperature coefficient, so very high power dissipation in a small volume will result in higher temperatures and thermal runaway. As long as the rate of heat removal is greater or equal to the rate of heat generation, the junction temperature does not increase. When the rate of heat generation becomes greater than the rate of heat removal, the junction temperature in hot spot region starts to increase and thermal runaway occurs.

For CMOS circuits, the electric field intensity refers to the voltage developed across the dielectric and junctions in the circuit. The gate oxide is the most vulnerable dielectric owing to its thinness. Structural defects and sharp corners in layouts result in higher electric field and current crowding making failure more likely at these points.

ESD induced failures can be grouped in two categories: soft and hard failures. In case of soft failure, the device has a partial damage typically resulting in an increased leakage current that might not meet the requirements for a given circuit. Still, the basic functionalities of the device are operative but without any guarantee about potential latency effects. In case of hard failures, the basic functionalities of the device are completely destroyed during the ESD event. Each ESD failure mode is traced to one or more of four fundamental damage mechanisms [7].

2.1 Oxide Rupture (Breakdown)

Typically, gate oxides can withstand an electric field of 6–10 MV/cm before it breaks down. In CMOS technology input/output buffers require an ESD protection circuit that limits the peak voltage during an ESD event that could cause irreversible failure (rupture) of the gate oxide. Being the peak voltage (V_{peak}) the maximum voltage across the protected device, it is necessary to maintain a margin between this voltage and the gate oxide breakdown (V_{BD}) to avoid oxide failures. The gate oxide breakdown (V_{BD}) is a critical function of its thickness. But with the scaling down of the device sizes, the gate oxide thickness is also reduced resulting in a decrease of the V_{BD}. Figure 1-1 shows the gate oxide damage in a MOS transistor after the CDM stress.

This defect results in a low-ohmic short of gate and drain terminals in damaged transistor [8]. The gate oxide is not the only concern in integrated circuits. Both bipolar and MOSFET processes can have dielectric ruptures in oxides over active circuitry. This may be the oxide grown over a diffused resistor or an isolation region. If a conductor passes on top of this oxide, a rupture can occur.

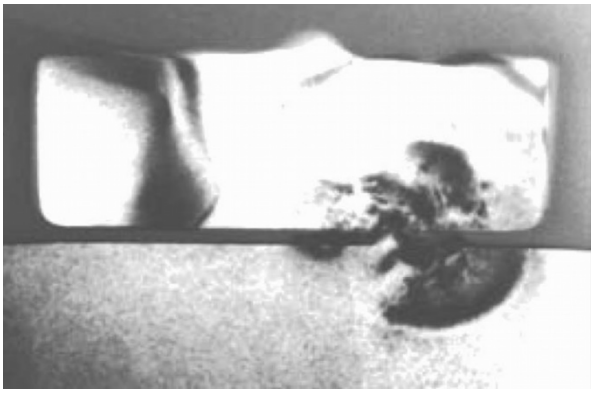

Figure 1-1. Gate oxide damage in MOS transistor after the CDM stress.

2.2 Junction Filamentation and Spiking

Junction filamentation causes an increase in the reverse bias leakage of a *p-n* junction. In the worst case, the junction is shorted. The ESD event causes current to flow through the junction. The high power dissipated in the junction cause the temperature to rise until a region of silicon melts. When silicon melts, its resistance drops by a factor of 30 or more [9]. This causes more of the current to flow in the narrow, melted region which further heats the melted region, leading to thermal runaway. This phenomenon is often referred to as the second or thermal breakdown [10]. In MOSFET devices the drain junction filamentation is typically located close to the surface in the gate to drain overlap region, where the dielectric acts a thermal insulator, as it shown in Figure 1-2.

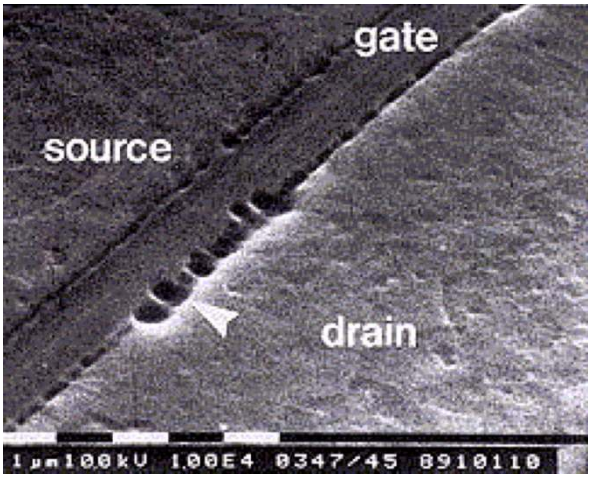

Figure 1-2. Drain junction filamentation in MOS transistor due to the ESD stress [11].

Therefore, devices, in which hot spot regions are located deeper in the silicon (like BJT, SCR and Thick Field Oxide Device), are used as a high reliable ESD protection devices. In bipolar junction transistors (BJTs) the base-emitter junction is the most susceptible to the filamentation damage. Junction spiking is a similar mechanism, except the melted region grows until it intercepted by a metal contact, causing the degradation of aluminum and silicon. The damage thresholds are lower for aluminum contacts because the aluminum-silicon eutectic forms at 577°C rather than at the melting point of silicon (1,415°C) [12].

2.3 Metallization and Polysilicon Burn-out

Thin-film fusing affects each conducting film in a circuit. These include the metal interconnects, polysilicon interconnect, and thin-film and diffused resistors. The most susceptible to damage are circuits with thin-film resistors. It is important during the chip design that the resistor be made wide enough to handle an ESD current pulse for the desired level of protection. Because of the high temperatures induced by the ESD pulse, a metal or polysilicon line, located close to the hot spot region in *p-n* junction, can be melted resulting in a metal opens, as it shown in Figure 1-3.

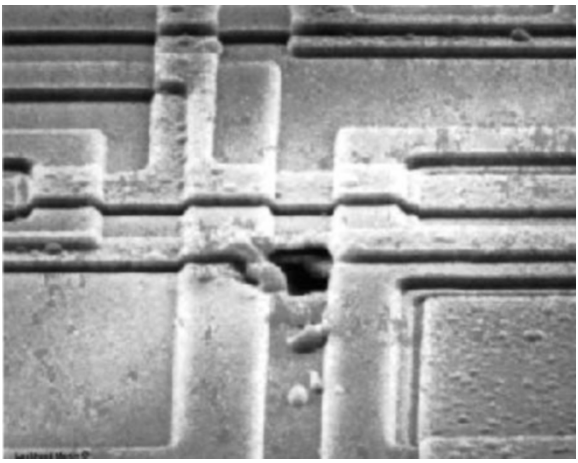

Figure 1-3. Interconnects damage due to the ESD stress [13].

2.4 Charge Injection

The last degradation mechanism is the charge injection into the gate oxide by avalanche breakdown of *p-n* junction. This occurs when an ESD event causes a reverse-biased junction to conduct by avalanche multiplication. Some of the carriers have enough energy to surmount the oxide-silicon energy barrier, as it is illustrated in Figure 1-4. If the junction is the drain of a MOSFET, it results a shift in the threshold voltage of transistor [14]. The degree of degradation in oxide reliability is also related to the current density of the injected charge as well as the total charge injected [15]. A localized charge injection during the drain junction avalanche breakdown at the ESD event causes more damage than the uniform charge injection from the gate to the body of a transistor at normal operating conditions. The charge injection induces the increasing of leakage current in the damaged devices.

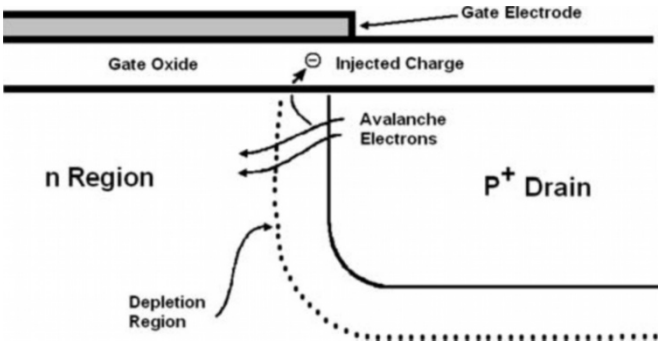

Figure 1-4. Mechanism of charge injection in gate oxide region under ESD stress [7].

3. CIRCUIT RELIABILITY: ESD MODELS

The most challenging aspect for ESD reliability is the protection circuit effectiveness or ESD protection level, especially in highly susceptible advanced CMOS technologies. Higher current densities and reduced ballasting resistances favor localization of stress currents and degrade the ESD performance of I/O protection devices in advanced CMOS processes with shallow Source/Drain junctions and silicided diffusions. Currently, the most commonly used ESD models for the reliability estimation of VLSI ICs are: Human Body Model (HBM), Machine Model (MM) and Charge Device Model (CDM). The basic model for ESD protection is the HBM intended to represent the ESD caused by human handling of ICs. Typically, HBM events occur at 2–4 kV in the field, hence, protection levels of this range are necessary. Besides human handling, contact with machines is also an ESD-type stress event. Since the body resistance is not involved here, the stress is severe with relatively higher current levels, thus, protection levels of 200 V for this model usually ensure adequate device reliability. The CDM ESD is intended to model the discharge of a packaged IC. Charges can be placed on an IC either during the assembly process or on the shipping tubes [16]. The protection level of 500 V for CDM ESD stress is typically used to ensure the chip reliability. The details of reliability ESD models are discussed in Chapter 2.

4. ESD CHALLENGES FOR ADVANCED CMOS TECHNOLOGIES

Semiconductor technology evolution results in technology scaling of geometric dimensions and lower power supplies. It introduces a new materials, features, devices and integration. Evolutionary changes in CMOS technology included the moving from local oxidation (LOCOS) based isolation to shallow trench isolation (STI), from diffused n-well to retrograde implanted wells, from non-salicide to salicide junctions, etc. In addition, the recent technology scaling from 180 nm CMOS to 65 nm CMOS resulted in moving from aluminum (Al) to copper (Cu) metallization and from silicon dioxide to low-k materials for inter-level dielectrics (ILD). All of these changing impact the ESD robustness of semiconductor products with both positive and negative ramifications.

4.1 Scaling of Metal Interconnects: Aluminum to Copper

The trend in advanced CMOS technology generations is a migration to interconnect systems using the dual damascene Cu-based metallization, exhibiting an improvement in the electrical conductivity compared to Al based interconnects with the same effective line thicknesses. The need for reduced resistance and capacitance interconnects has led to an evolution from Ti/Al/Ti based technology to Cu-based interconnect processes, since the Cu wiring has 35% lower resistance, higher allowed current density and 20% lower cost compared to Al-based interconnects [17].

As metal lines decrease in thickness with each technology generation they are becoming “fuses” in the Electrostatic Discharge (ESD) protection path if not sized correctly. The continuous scaling down of ICs for faster switching speed has decreased the size of both the devices and the metal lines that form interconnects between the devices and power rails in a chip. This reduction in the dimensions of interconnects affects their ESD robustness. It is therefore important to characterize the heating effects of copper lines under ESD conditions and set guidelines consistent with the wire current carrying capability to handle an ESD event. During an ESD stress, metal lines fail if Joule heating results in raising the conductor temperature beyond its critical temperature (T_{crit}). In addition, an ESD induced electromigration may also cause the conductor failure [17, 18]. Figure 1-5 shows a cross section of a Ti-clad aluminum and cladded dual-damascene Cu-based interconnects placed in a polymeric dielectric insulator [19].

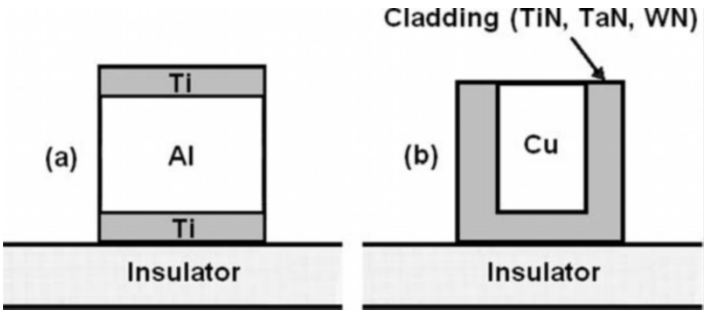

Figure 1-5. Cross section of Al (a) and Cu (b) interconnect with cladding material. (Adapted from [17].)

In the damascene process, the polyimide film is etched, followed by cladding material and Cu film deposition. The liner cladding material can be TiN, WN, Ta, TaN, or TaSiN to form good adhesion and act as a copper diffusion barrier. Copper interconnects are geometrically different from the Ti/Al/Ti interconnects in that the cladding is on the bottom and the two sides. In a dual-damascene Cu-based fabrication process, Cu-vias are filled concurrently with the Cu-interconnects by creating a trough in the polyimide with two different depths.

The ESD robustness of Cu-based interconnects has been shown to be two or three times superior to Al-based interconnects (for wires and vias, respectively) based on transmission-line-pulse (TLP), HBM, and MM testing

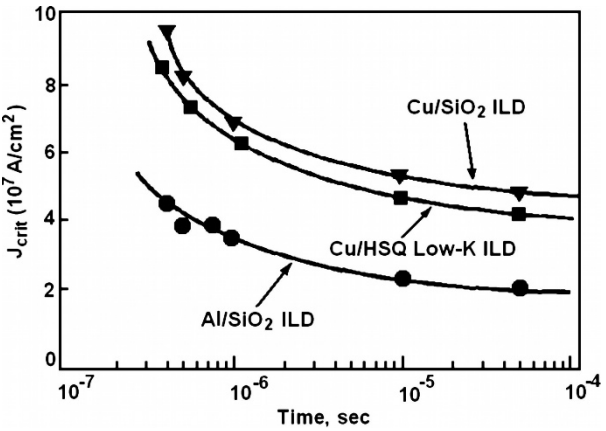

Figure 1-6. Jcrit as a function of ESD pulse width for copper and aluminum interconnects with different ILD materials: SiO_2 and low-k hydrogen silsesquioxane (HSQ) [20].

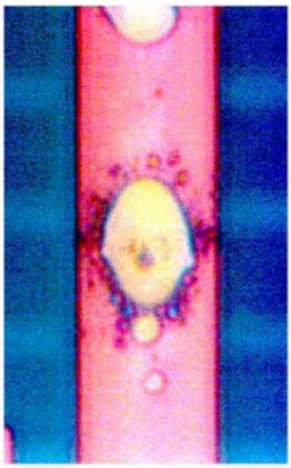

Figure 1-7. ESD induced failure of a copper interconnect [21].

(Figure 1-6) [20]. By migrating to Cu-based interconnects, the critical-current-density to failure (J_{crit}) and ESD HBM and MM improvements allow to continue scaling of metal film thickness and line width, which improves *rc* delay and ESD reliability. The low resistivity, high melting point and good mechanical strength explain the better ESD performance of Cu interconnects than interconnects implemented from conventional materials such as Al or AlCu alloy. Note, that Cu melting temperature is 1,034°C in comparison to an Al melting temperature of 660°C [17]. Al-clad and Cu-clad interconnect failures are different because of the geometry and materials in the interconnect structure. In Al-based interconnects, the cladding is on top and bottom. In this case, the dielectric cracking and extrusion occurs laterally. In Cu-based interconnect systems, cladding is on the two sides and bottom; dielectric cracking occurs vertically and weak extrusion occurs laterally. Figure 1-7 shows an example of the onset of ESD-induced failure of a Cu interconnect film. The peak temperature occurs in the center of the wire leading to the onset of failure in the center region [21].

4.2 Scaling of Inter-Level Dielectrics: SiO_2 to Low-k Materials

Low-k inter-level dielectric (ILD) materials further reduce interconnect capacitance. The International Technology Roadmap for Semiconductors (ITRS) states that ILD electrical permittivity must be scaled from k = 4.0 to k = 1.5 to meet signal delay requirements for sub-0.18 μm CMOS technologies [22]. From an ESD perspective, the thermal properties of low-k ILD