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There is a trend to revive mature technologies while including high voltage options. ESD protection in those technologies is challenging due to narrow ESD design windows, NMOS degradation issues and the creation of unexpectedly weak parasitic devices. Different case studies are presented for ESD protection based on latch-up immune SCR devices.

ESD Protection Solutions for High Voltage Technologies

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Abstract - There is a trend to revive mature technologies while including high voltage options. ESD protection in those technologies is challenging due to narrow ESD design windows, NMOS degradation issues and the creation of unexpectedly weak parasitic devices. Different case studies are presented for ESD protection based on latch-up immune SCR devices.

I. Introduction

Many companies extend mature, less expensive CMOS technologies (0.35um and above) with new options and features such as high voltage (HV) or bipolar modules for instance for specific automotive or consumer electronics products. The strategy of technology upgrading offers significant economical advantages in this competitive market segment. For HV technology upgrades, HV MOS transistors are equipped with thick gate oxides and lowly doped drain/source implants to increase the voltage tolerance of the devices. This allows driving the maximum operating voltages to the limits of the process technology. ESD protection elements used in the HV domains need to be able to withstand these high voltages. However, the implant envelopes applied for HV compatibility dramatically degrade the high current behavior of conventional protection elements, such as ggNMOS transistors. In addition, other issues as for example weak parasitic current paths and high latch-up susceptibility are commonly observed.

First, the paper reviews serious key issues commonly encountered for standard HV ESD transistors. The focus of the paper is on alternative solutions based on latch-up immune Silicon Controlled Rectifiers (SCR). HV-compatible SCR power protection devices were already described in [1] and will therefore be briefly reviewed only. The ESD-on-SCR represents an efficient high-voltage IO protection device for highly sensitive output drivers. A novel trigger concept preconditions the SCR for turn-on during ESD but avoids unintended triggering during normal circuit operation conditions.

II. ESD related issues in HV technologies

In mature low voltage technologies of 0.35um and earlier, the ggNMOS is still widely applied as the 'workhorse' for ESD protection design due to straightforward implementation and sufficient high current capabilities in the parasitic NPN snapback mode with a normalized ESD performance per gate width of typically 10-15mA/um. Moreover, the clamping behavior indicated by the trigger and holding voltages as well as the dynamic on-resistance is sufficient to protect the relatively thick gate oxides (~15nm) exposed to ESD stress in mature LV technologies. The snapback holding voltage typically needs to exceed the maximum supply voltage specification not imposing any potential latch-up risk for power protection application. However, the above described NMOS qualities are eliminated by introducing the upgrades required for MOS HV compatibility. The following sub-sections summarize the related issues commonly observed in high-voltage technologies, e.g. in HV-CMOS.

A. Strong snapback

In high voltage technologies additional low doping implants are typically used as an envelope around the MOS drain and source diffusions, cf. Figure 1, of the low-voltage MOS transistors to obtain the high junction breakdown voltages. These low doping concentrations strongly impact the snapback behavior.

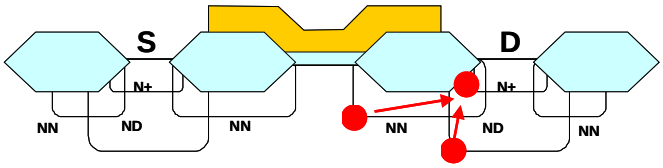

Figure 1: Schematic cross-section of a typical high-voltage NMOS transistor equipped with lowly doped diffusions (NN, ND) enveloping N+ source and drain for high voltage compatibility. Hot spot migration towards the FOX bird's beak caused by the Kirk effect in high current bipolar operation is indicated.

As shown in Figure 2, the snapback trigger voltage Vt1 of a ggNMOS (43V 0.5um CMOS technology) is increased to the expected high value of Vt1~73V due to the high avalanche breakdown voltage of the drain-bulk junction. On the other hand, the snapback holding voltage Vhold still occurs at relatively low values Vhold~10V and can be related to the corresponding low-voltage NMOS elements.

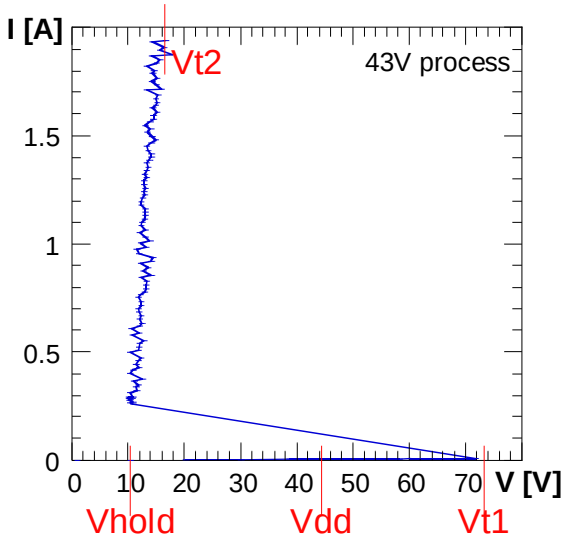

Figure 2: Typical snapback TLP-IV curve of a HV-ggNMOS in a 43V, 0.5um-CMOS technology. Characteristic is the strong snapback due to high triggering voltage and relatively low holding voltage.

Responsible for this behavior is the so-called Kirk or base-push-out effect appearing in the high-current bipolar mode [2-3]. This mechanism pushes the avalanching region from an initial location at the lowly doped drain curvature at breakdown (see spots at NN, ND on Figure 1) to the highly doped N+ diffusion in a fully conducting bipolar mode. Hence, this shift to a high doping results eventually in a large intrinsic avalanche field that sustains parasitic NPN operation at a relatively low external (holding) voltage. If the gradual hot-spot migration to the N+ region occurs at elevated bipolar currents the hot-spot transition is sometimes accompanied by a double-snapback effect, i.e. an initial higher holding voltage with a subsequent second snapback can be distinguished [4]. The low holding voltage results in serious issues when applying the NMOS for ESD protection design or protecting an NMOS output driver.

B. Multi-finger non-uniformity issue

HV NMOS multi-finger triggering is extremely difficult to accomplish due to the fact that the uniformity condition Vt1<Vt2 (trigger voltage smaller than failure voltage) is largely violated [5]. Simple ballast resistance integration into each finger does not solve the problem because of the huge voltage gap to be bridged. The ESD performance data of various HV-ggNMOS single- and multi-fingers in Figure 3 clearly demonstrates a poor scaling behavior. The performance scaling issue within a single finger is also caused by the strong snapback behavior in conjunction with a reliability issue discussed below.

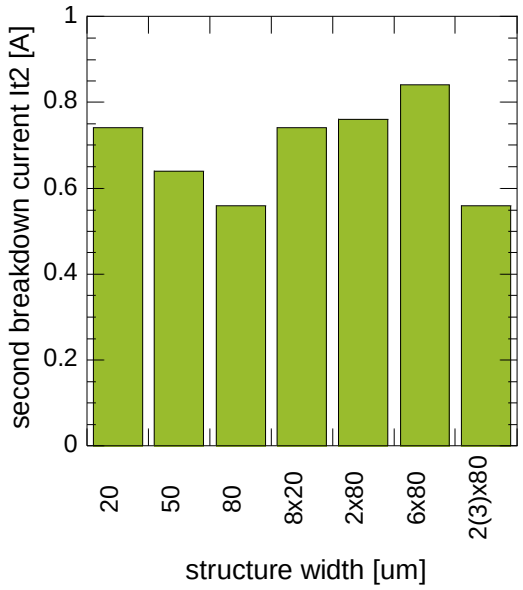

Figure 3: TLP It2 data for various HV ggNMOS single- and multi-finger structures indicating poor performance width scaling.

In general, static gate/bulk biasing schemes for Vt1 reduction cannot be successfully applied either since the maximum supply voltage is too high as compared to the holding voltage. A Vt1 reduction to the minimum allowed operating voltage plus some safety margin would not significantly improve the multi-finger trigger behavior. Transient biasing schemes added at the HV NMOS output drivers to improve the ESD robustness level (for example capacitive gate-coupling circuits) would interfere with normal circuit operation performance.

C. Intrinsic HV NMOS reliability issue

In particular for mature technologies with FOX-bound active areas, a serious intrinsic device reliability weakness occurs. During high-current bipolar operation, the impact ionization hot-spot is located at the N+ diffusion (high injection mode) closely to the FOX bird's beak as explained above, cf. Figure 1. As a result, hot carriers can be injected into the SiO_2 material and can be trapped there easily ('charge trapping'), because the bird's beak is a region with a high defect density. This leads to a local reduction of the breakdown voltage and in turn results in a current focusing mechanism. Even single-fingers are prone to non-uniform ESD performance scaling as demonstrated above in Figure 3 and by the TLP data in Figure 4.

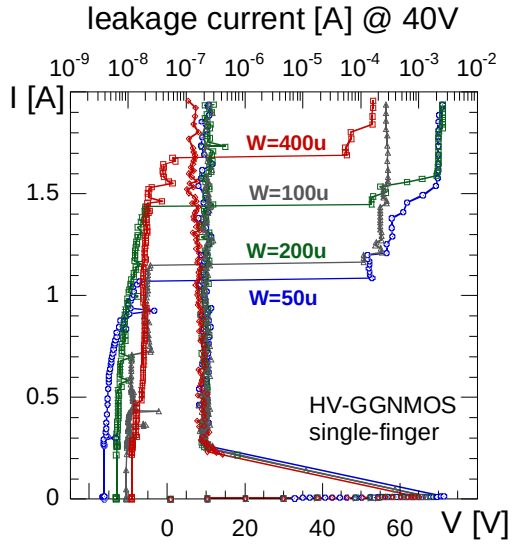

Figure 4: Non-uniform conduction of ESD current demonstrated for different HV-ggNMOS transistors.

Moreover, due to the charge trapping mechanism in the FOX at the bird's beak, the HV NMOS shows critical endurance test problems, if stressed with multiple ESD pulses. A gradual increase of leakage current occurs for multiple TLP zaps at roughly the same amplitude (Figure 4 and Figure 5). This leakage increase reflects gradual device degradation if the parasitic NPN operates under high current conditions and is caused by a locally reduced junction breakdown voltage due to charge trapping in the FOX.

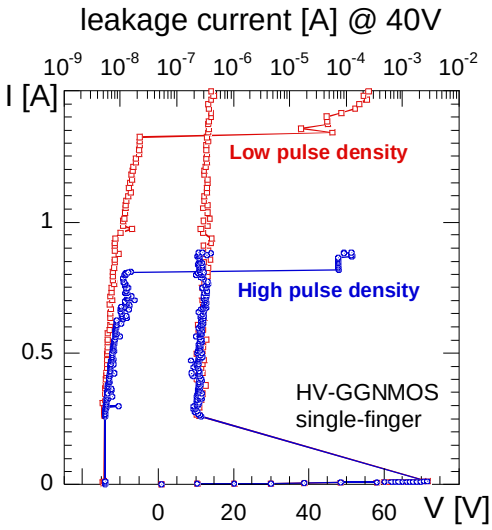

Figure 5: TLP measurements of a grounded gate HV NMOS snapback clamp in a 0.5um (43V) technology. After snapback, at roughly 73V, a clear and steady degradation is visible in the leakage current. The final failure current is dependent on the pulse density. When a small stress step is applied, the It2 failure current is much lower.

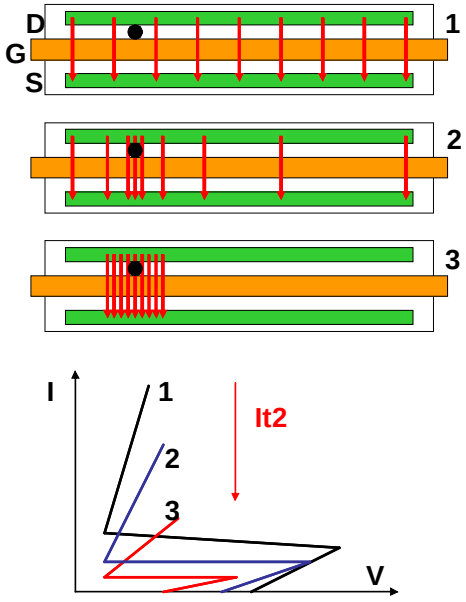

Figure 6: Charge trapping in the Field Oxide at the bird's beak reduces the breakdown voltage locally, represented by the black spot at the drain. Due to the reduced breakdown voltage the following ESD stress current (2,3) will be localized at the black spot, preventing uniform conduction through the whole finger.

Figure 5 shows TLP measurement results on two identical HV ggNMOS devices using different TLP stress step levels. This technique is used before to define the real failure current level [6]. The final degradation point (to uA leakage) occurs earlier when the stress steps are closer together (high pulse density on the figure). The effect is explained in Figure 6, showing the current localization and increased degradation during each stress pulse.

D. High Latch-Up risk

The ggNMOS holding voltage is much smaller than the maximum supply voltage specification in many HV technologies. If the device is applied as a power clamp between VDD and VSS, unintended triggering by static or transient latch-up stimuli may occur due to the relatively low holding current of the NMOS multi-finger device. Triggering would be very critical since the supply voltage can not recover without going thru a renewed power-up cycle. In the worst case the high DC supply current (from e.g. a car battery) could damage the power clamp. This latch-up issue prevents the application of HV-ggNMOS devices as a power clamp.

E. Parallel NMOS output driver protection challenge

A major challenge is the design of ESD-robust HV NMOS output drivers due to the multi-finger triggering challenge but also due to an intrinsic device reliability weakness described above. Therefore, often the introduction of an additional protection appears to be the only feasible solution. However, trigger competition between the weak driver and the parallel ESD clamp must be prevented. This objective is difficult to accomplish due to the fact that the trigger voltage of the ESD device must satisfy the high-voltage conditions (i.e. trigger above VDD with Vt1>43V). On the other hand, the protection must turn on below the ESD trigger voltage of the parasitic NPN inherent to the NMOS driver. This sensitive parasitic in the driver can reveal relatively low triggering voltages because transient gate-biasing during ESD stress strongly reduces Vt1. Thus, to fulfill normal operation requirements (high Vt1>VDD) as well as ESD conditions (low Vt1(protection)<Vt1(driver)) it is often impossible to apply static trigger schemes for parallel NMOS driver protection. In this paper another solution is presented where the trigger condition of the local clamp is based on the Vdd potential.

F. High resistive ESD elements

In HV technologies, the depletion regions reach much larger distances due to the lowly doped diffusions introduced for all HV compatible elements. In order to prevent punch- or reach-through problems leading to high IC leakage for instance, critical distances must be increased to relatively large dimensions. This has a negative impact for example on the dynamic series resistance of crucial ESD diodes where the anode-cathode spacing becomes relatively large. The TLP-IV characteristic of a typical HV N/Pwell diode in Figure 7 reveals a resistance of almost 5 Ohms (W=50um). This is almost one order of magnitude larger than the diode series resistance obtained in standard CMOS technologies for corresponding widths.

The high voltage drop across ESD diodes combined with the relatively high bus resistance due to the limited number of available metal layers (typically less than 4) leaves only little ESD design margin for critical stress cases.

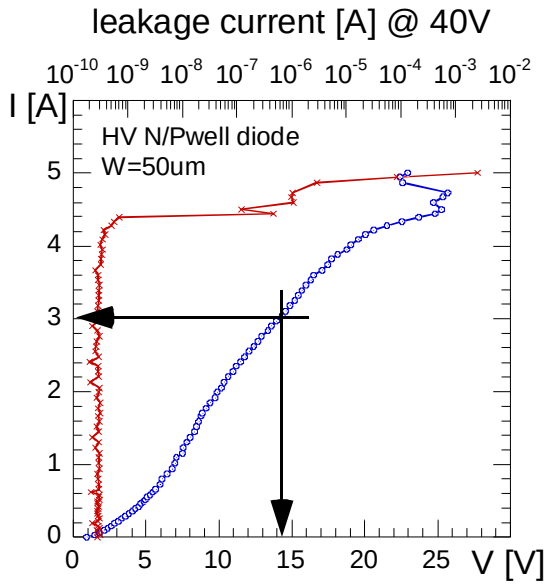

Figure 7: TLP data of HV-N/Pwell diode (W=50um) revealing a large dynamic series resistance.

In conclusion, in many high-voltage technologies standard snapback based NMOS protection is not feasible due to intrinsic device weakness and serious ESD design issues. Alternative solutions including parallel driver protection applying appropriate triggering schemes must be incorporated. This paper will describe an efficient SCR based alternative.

III. SCR-based, Latch-Up-immune power protection

Because the HV ggNMOS device has a very low holding voltage and non-uniform conduction in the parasitic NPN mode, it can not be used as a power protection clamp. One could use a RC triggered bigFET or Active MOSFET power protection in conjunction with dual diode protection for the IO circuits ('rail based protection scheme' as in [7-9]) where the destructive snapback mode is not used. However, due to the large voltage drops across the diode and bus resistance in typical HV applications, the voltage margin in the ESD design window is reduced drastically in those solutions.

SCR based power protection can enable the ESD protection between Vdd and Vss thanks to an excellent clamping behavior at high currents. Its low holding voltage opens the ESD design window and creates margin for the bus resistance and diode voltage drops.

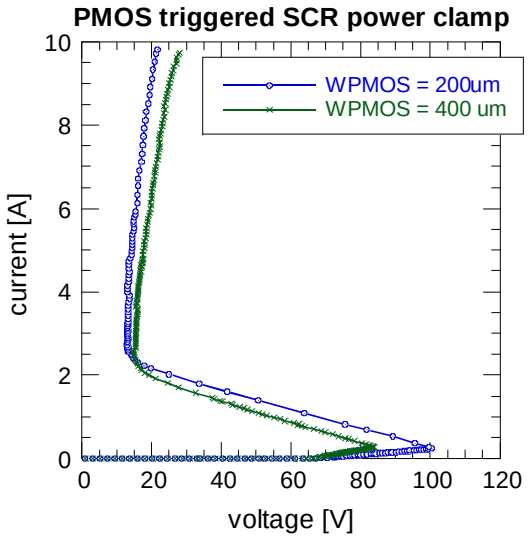

Figure 8: TLP measurement data on PMOS triggered SCR for power protection. The Vt1 trigger voltage and It1 trigger current are determined by the external trigger circuit (PMOS and external resistances as in Figure 9). The SCR-based protection shows a perfect low holding voltage clamping behavior and a very high ESD performance of more than 10A for a 56um wide SCR.

To enable SCR based power protection a number of issues have been solved.

(1) First, the SCR needs to be triggered into the low resistive mode. Typical for the HV technologies is the very high well-to-well breakdown voltage (~150V) that is too high for a Vt1 trigger voltage because the core breakdown voltage is typically lower. An external, optimized trigger element needs to be added to lower the Vt1 trigger voltage. To prevent NMOS degradation and non-uniformity issues, the optimal trigger element for HV SCR based protection is a PMOS device. Figure 8 and Figure 9 show a 43V application where a HV PMOS transistor handles the low ESD stress currents. When the ESD stress current reaches 300mA, defined by the external resistors at G2, the SCR is triggered into a low ohmic conduction.

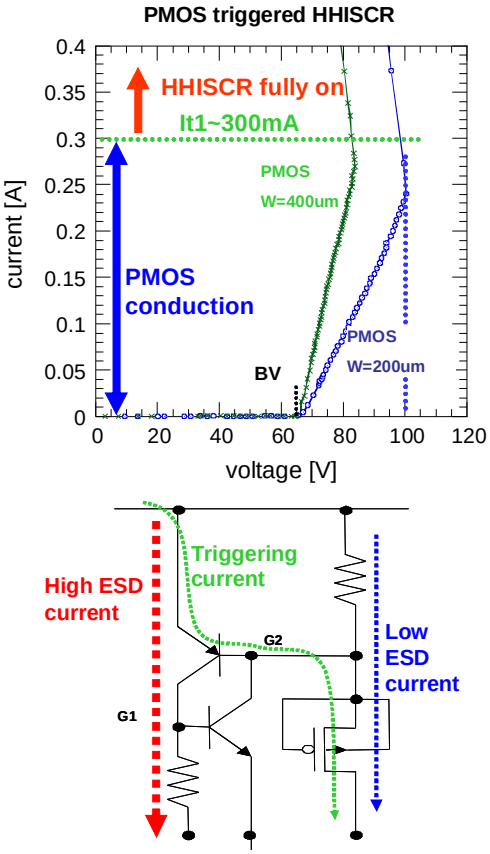

Figure 9: PMOS triggered SCR in a 0.5um, 43V CMOS technology, showing a high trigger current of about 300mA due to low external resistances between G2 and Anode. The low resistance values prevent unwanted triggering of the SCR during normal operation. The trigger current is determined mostly by the external resistance values while the trigger voltage can be tuned to the desired voltage by selecting an appropriate size for the PMOS trigger element.

(2) Secondly, the static trigger current and voltage for the SCR needs to be engineered to a high value to prevent unwanted triggering during normal operation. In one case of latch-up tests (Figure 11, left side) one adds a fast, positive pulse to the power supply and checks for an increase in the steady-state operation leakage (Iddq). By designing the trigger element and shunt resistance correctly (small value of ~5Ohm) a high trigger current can be achieved easily. The trigger

element needs to deliver the trigger current at a voltage higher than the Vdd potential to ensure latch-up immune triggering. The PMOS trigger element shows an advantage over NMOS based triggering because the NMOS would create a latch-up issue due to the low holding voltage in the parasitic bipolar conduction mode. Both on Figure 9 and on Figure 10 large trigger currents are demonstrated by the TLP measurements.

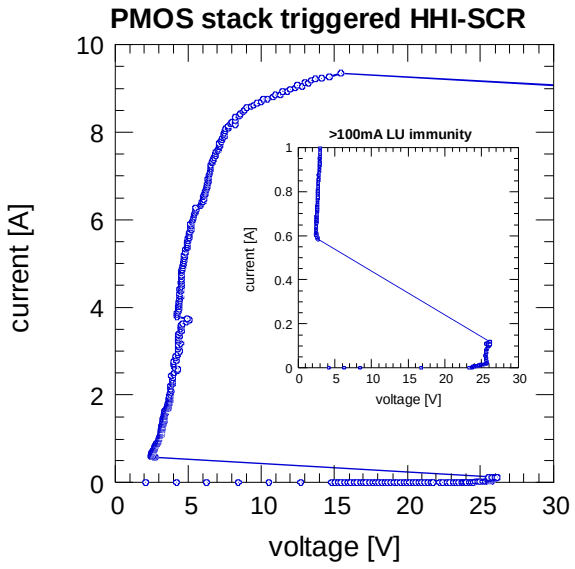

Figure 10: TLP measurement data on an SCR-based power protection for a 22V/0.5um BiCMOS technology. The SCR is triggered by a stack of two PMOS devices. On the inset of the figure a high trigger current of almost 200mA can be seen. The high trigger current improves latch-up immunity by preventing unwanted triggering during normal operation. Thanks to the excellent clamping behavior of the SCR device, a very low holding voltage can be obtained which leaves a large voltage margin for other voltage drops in the ESD current path.

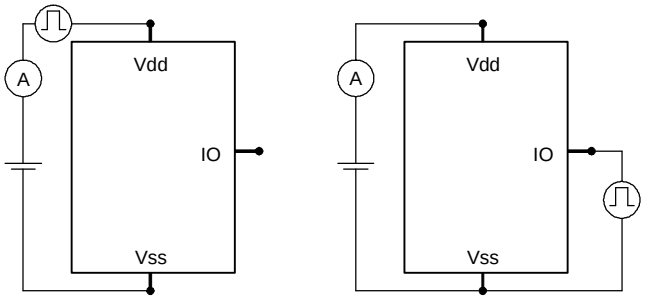

Figure 11: Two main types of latch-up tests. On the left figure the chip is powered up and an additional short voltage pulse is applied on the Vdd line. On the right figure, the chip is powered up and a current pulse (~100-200mA) is injected into the different IO's. Steady-state core leakage is compared before and after the pulse. In the case of a latched powerclamp the leakage measurement will show an increased value.

(3) Finally the SCR clamp needs to be designed with a sufficiently high holding current to prevent triggering by substrate current that is injected into a nearby IO-pad. This current injection is typically performed in a second type of latch-up test (Figure 11, right side) where the device is powered up and current pulses are injected at the different IO's. Good guard band protection around the IO's and power protection elements, sufficient spacings and a segmented layout of the SCR [1] can increase the latch-up immunity levels for this kind of requirement. Also small values for the external resistances at G1 and G2 can improve the latch-up immunity level because they provide a safe shunt path for nearby injected Latch-up carriers.

IV. Local protection using ESD-on-SCR

The previous section described the different options for power protection in high voltage technologies. This section first discusses the issues with output driver protection. For input-only pads there is no danger because the transient gate oxide breakdown is very high due to the thick gate oxide used in these high voltage applications. For input-only pads a dual diode ESD protection is sufficient and preferable. However due to the intrinsic weakness of the HV NMOS output driver a local protection needs to be added for IO or output-only pads. This is required because the high bus resistance, large voltage drops over basic diodes and the low Vt1 triggering voltage of 'floating gate' NMOS output drivers.

First, the design window for output pads is determined for both the 0.5um HV CMOS and the 0.5um BiCMOS examples. Secondly, the operation principle of the ESD-on-SCR clamp is described. Finally, the influence of the circuit elements is discussed.

A. Design windows in the 43V/0.5um CMOS application example

The 43V technology is used for the automotive and display driver market. The application example is a 128x output OEL (Organic Electroluminescent) display driver chip. Although the maximum supply voltage is defined as 43V, the power clamp leakage needs to be limited below 1nA for voltages up to 54V. Latch-up immunity (at room temperature) up to 300mA is specified, by extrapolation from the LU specification of 100mA at 125C. The 200V MM (approx. 3A peak current) specification further defines the ESD design window for the power clamp and demands a device with a rather low-ohmic clamping

characteristic. The power clamp has been created using a PMOS triggered SCR as described above (Figure 9) and showed latch-up immunity levels up to 300mA and ESD MM levels above 250V in a real product application.

The maximum output voltage during normal operation is defined as 43V. For the local protection of the output driver, the minimum trigger voltage is defined by this maximum signal voltage plus 10% safety margin (47V). The maximum trigger voltage is defined by the lowest Vt1 trigger voltage of the NMOS and is limited to merely 54V to avoid trigger competition between the protection clamp and the output driver NMOS device with floating gate (undefined potential at the gate during ESD). The local protection needs to prevent a snapback event in the output driver device because such snapback will cause degradation in the HV NMOS (See Figure 4). A summary of the narrow design window is depicted on Figure 12: The Vt1 trigger voltage needs to be between 47V and 54V. Because it is challenging to tune a junction breakdown (as a trigger condition) to such a narrow window, another approach has been selected as will be discussed below.

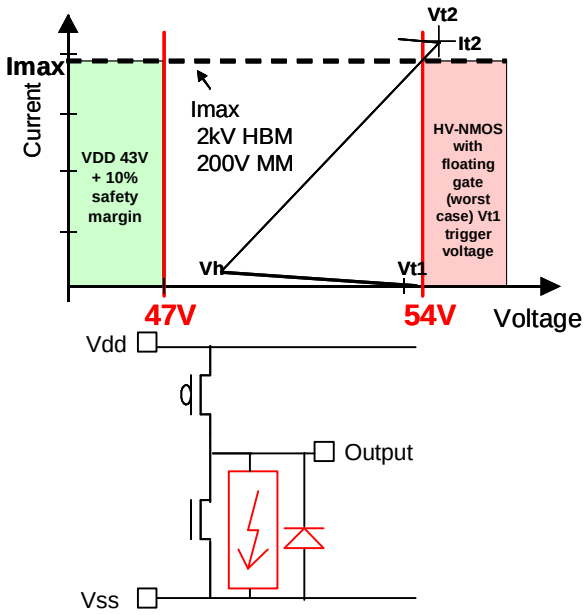

Figure 12: Summary of the design window for the output driver in a 43V/0.5um CMOS technology. The required robustness level (Imax=3A) of the local protection is defined by the HBM (2kV) and MM (200V) specifications and is based on correlation measurements in the process under study. The minimum static trigger voltage is 47V as defined by the Vdd+10% normal operation region. The maximum trigger voltage is defined to prevent triggering of the HV NMOS output driver (54V)

B. Design windows in the 22V/0.5um BiCMOS application example

The second example shows data in a 22V technology. The minimum power clamp triggering voltage is 24V. Because the NMOS holding voltage is below Vdd=22V, it cannot be used to trigger the SCR clamp due to latch-up considerations. The PMOS breakdown is at 11V and that a stack of two PMOS devices is used as a back-up path for the first 200mA. A TLP measurement (and zoom-in) that fits inside the design window is depicted in Figure 10.

C. Principle of ESD-on-SCR

In both examples the design window for the local protection of the NMOS output driver is narrow and a static voltage triggered protection is not feasible. A novel approach has been used in stead.

By connecting the G2 (Nwell) of an SCR to the Vdd line a ‘self-controlled’ or ‘self-aligned’ protection element is created [similar approach as in 10]. The schematic and cross section are shown on Figure 13.

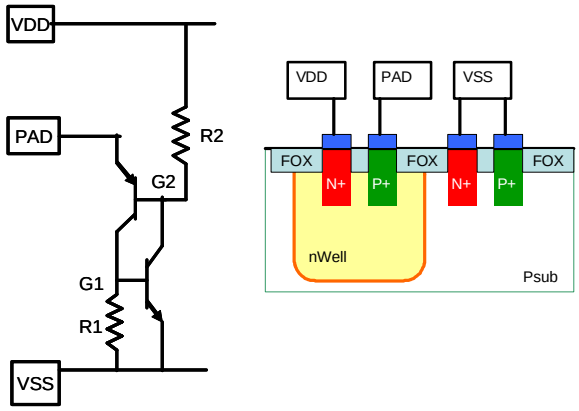

Figure 13: Schematic and cross-section of the ESD-on-SCR. The G2 node (Nwell connection) is connected to Vdd to minimize leakage by keeping the SCR off during normal operation and to maintain a low capacitive input protection. During ESD stress between Pad and Vss, the Vdd is floating which enables very low voltage triggering. When the Nwell is floating, the SCR will turn on ‘instantly’.

1. Low leakage

A DC measurement with a Vdd bias of 50V (Figure 14) shows that the leakage specification can be met because the anode-G2 diode will be reverse-biased for voltages up to (Vdd + ~0.6V). Whenever there is a diode ‘up’ between the pad and the Vdd line - as in a dual diode protection approach or the intrinsic parasitic P+/Nwell diode in PMOS output drivers - a similar DC IV-curve would be measured because the

diode ‘up’ between Pad and Vdd would start to conduct once the pad voltage is above the applied Vdd potential.

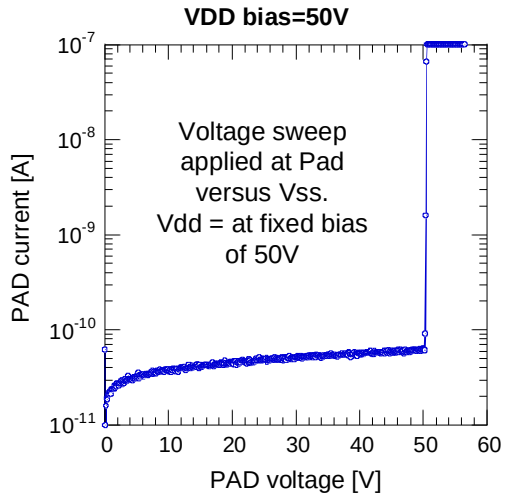

Figure 14: DC measurement (on 0.5um 43V technology) to detect the leakage level at the maximum operating voltage of the process (Vdd bias is at 50V). The SCR only conducts current after the pad-Vss voltage exceeds the Vdd, which was set at 50V. The Nwell connection (G2) of the SCR is connected to the Vdd supply line to prevent SCR triggering during normal operation.

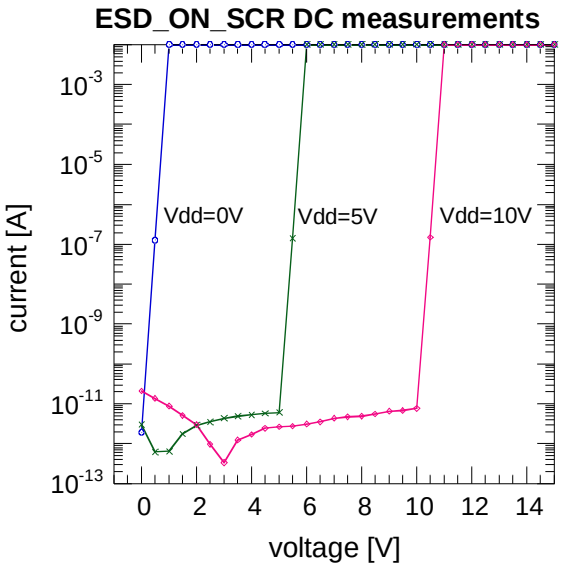

Figure 15: DC measurements (on 0.5um 22V technology) with different Vdd bias at G2 of an ESD-on-SCR device. The SCR is completely off for pad voltages below the applied Vdd voltage.

2. Vdd voltage dependence

In HV technologies it is typical to change the operating voltage depending on the specific display application and customer, which means that the minimum trigger voltage for the local protection is not fixed. Figure 15 shows measurement results for different Vdd supply voltages. The SCR has a low leakage value up to the applied Vdd voltage. The SCR triggers only when the voltage at the IO-pad rises above the Vdd potential. The trigger condition for ESD stress between IO-pad and Vss is explained in the next part.

3. Triggering

In the case of an ESD stress between the Pad and the Vss line, the SCR triggers almost immediately at a low voltage because the Vdd line (and thus G2) is floating which makes it easy to forward bias the Anode-G2 (emitter-base junction) of the PNP. Because the SCR is instantly on during ESD, the device is called an ‘ESD-on-SCR’.

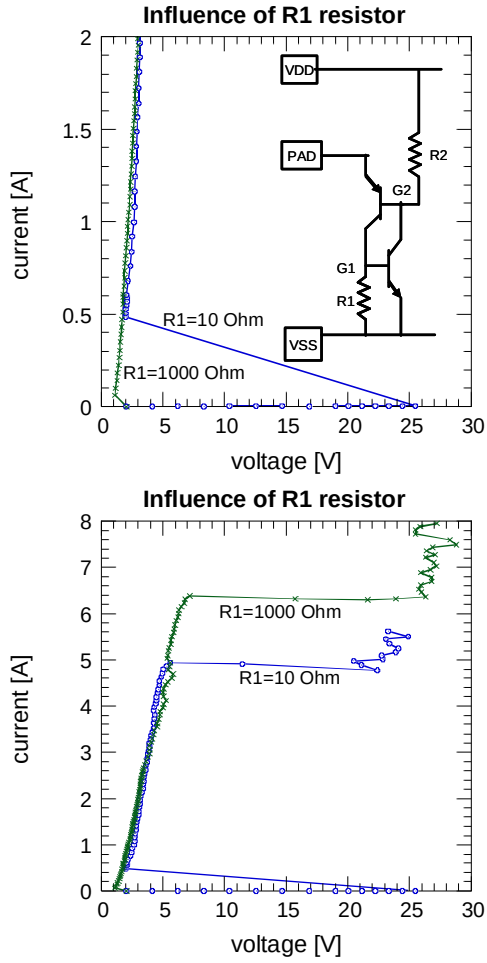

Figure 16: TLP measurements on 2 ESD-on-SCR devices (22V BiCMOS technology with isolated Pwell) with different G1 to substrate resistances. In the case of a small R1 value more current is needed through the PNP to forward bias the base emitter junction of the NPN device which shows up as a much higher SCR trigger voltage Vt1. The ESD-on-SCR devices show a current capability of more than 5A for 100um total Anode/Cathode width.

In case of an ESD stress (as in the TLP measurements shown in Figure 16) between IO-pad and Vss, the Vdd line is capacitively coupled to the Vss potential by the chip capacitance (Figure 17). The diode from anode to G2 can easily be forward biased, charging up the Vdd to Vss capacitance through the G2-Vdd connection.

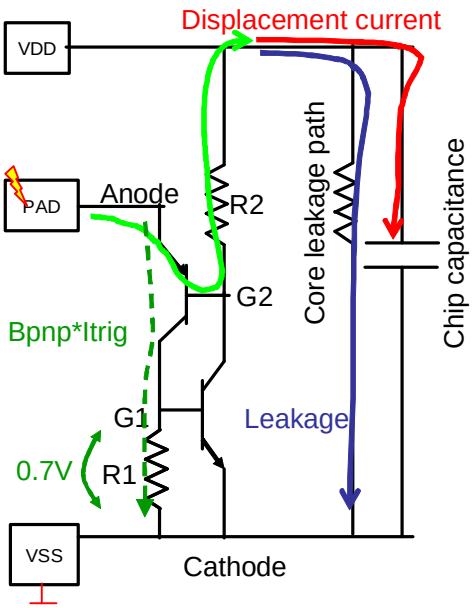

Figure 17: Trigger concept of the ESD-on-SCR: (A) The anode-G2 junction is easily forward biased during an ESD event between pad and Vss due to a floating G2 node. (B) The base current in the PNP will be amplified and flows to Vss through the R1 resistor. The NPN and thus the SCR will be turned on when 0.7V is created across resistor R1.

Additionally, during this ESD stress case, the core between Vdd and Vss is in an undefined state, which can typically be represented by a leakage path of a few kilo ohms. The current that flows from G2 to Vdd is the base current for the parasitic PNP device within the SCR. The current $Ibase_{PNP}$ in the base gets amplified between the collector and the emitter with a factor of $Beta_{PNP}$ (Figure 17). When that amplified current creates a voltage drop of 0.7V over the resistor R1 between G1 and the cathode, the SCR will latch into a low holding state, clamping the anode (IO-Pad) and the cathode (Vss) together thereby protecting the IO circuit. The trigger condition for the SCR can be written as:

$$Ibase_{PNP} \times R1 \times Beta_{PNP} = 0.7V.$$

The Vt1 trigger voltage of the protection device is a function of the base current in the PNP that is needed to fulfill the above relation. The influence of the R1 resistor on the Vt1 trigger point can be clearly seen on Figure 16, where TLP measurements with two values of R1 are compared. For a small R1, a large current is needed through the PNP, which means that more base current is needed. The higher base current will flow from Vdd to Vss through the leakage path and increase the Vdd to Vss potential. A higher voltage at the pad is needed to sustain a forward biased anode-G2 diode, resulting in a larger Vt1.

As a conclusion, the ESD-on-SCR can trigger at very low Vt1 voltages and can remain in a low leakage state during normal operation.

D. Influence of circuit elements

There are some issues that need to be considered when implementing this type of local protection clamp. It is required that there is sufficient base current in the PNP device. Suppose a diode-'up' is added between the IO-pad and the Vdd line. The ESD current injected at the IO pad has two parallel paths to flow to Vdd: through the emitter-base of the PNP and a second competing path through the diode-'up'. In most cases the diode-'up' is less resistive than the anode-G2 diode, which means that less current will flow through the PNP base. This has a negative impact on the Vt1 trigger voltage however measurements have shown only a limited effect on the Vt1 trigger voltage.

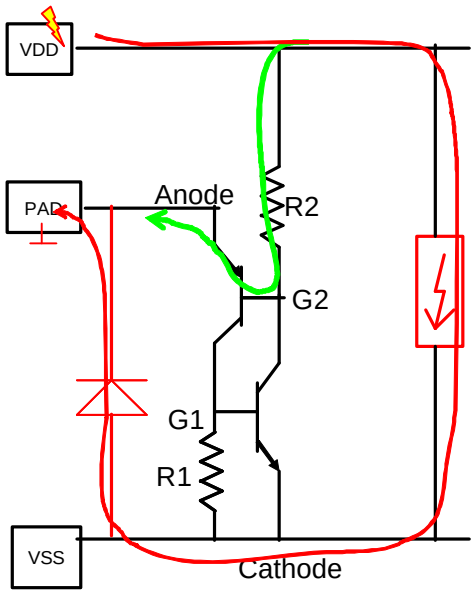

Figure 18: ESD stress from Vdd to Pad can damage the Anode-G2 junction from the ESD-on-SCR when the trigger voltage Vt1 of the power clamp is much higher than the failure voltage Vt2 of this junction. This can be prevented by inserting a resistance R2 which then protects the Anode-G2 junction.

In the ESD-on-SCR approach, the anode and the G2 node are not connected together. This can introduce additional leakage between Vdd and IO-pad when the reverse breakdown voltage of the P+/Nwell diode is

lower than the supply voltage. For positive ESD stress applied at the Vdd versus the IO pad (Figure 18), a part of the ESD current can flow through the Anode-G2 junction of the ESD-on-SCR when the Vt1 trigger voltage of the power clamp is higher than the P+/Nwell breakdown. The critical condition is determined by the Vt2 failure voltage of the Anode-G2 junction, the Vt1 trigger voltage of the power clamp and the voltage drop over the diode down:

Vt2_diode > Vt1_Powerclamp + Vdiode_down

The Anode-G2 junction can be protected by adding another diode or a resistance R2. In both cases the Vt2 failure voltage of this current path will increase. However, these additional elements have a negative effect on the Vt1 trigger voltage of the ESD-on-SCR because more trigger current is needed to turn on the SCR which results in a slightly higher Vt1 trigger voltage as can be seen on Figure 19.

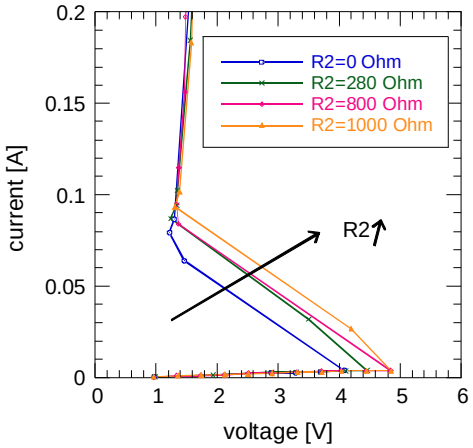

Figure 19: Influence of the R2 resistance between G2 and Vdd on the trigger behavior of the ESD-on-SCR.

Conclusions

This paper reviewed different issues that are typically encountered in high voltage technologies. Measurement data from different medium and high voltage technologies showed the NMOS degradation issue disabling the parasitic NPN current conduction for use in ESD solutions due to current non-uniformity. Further, the low holding voltage at high injection (Kirk-effect) prevents the use of ggNMOS power protection clamps based on latch-up constraints.

Because of the high resistive voltage drops in basic ESD protection elements and power bus sections, the power clamps in HV applications need an extremely low holding voltage. This paper focused on SCR based power protection triggered by PMOS elements and this technique is successfully applied in two different technologies showing very high ESD performance and high latch-up immune product applications.

The HV NMOS output driver has been successfully protected using an SCR-based local clamp in different technologies. Due to the extremely narrow design window, static triggering is typically not an option. In this paper a novel triggering scheme for SCR protection, based on Vdd-potential detection, has been shown and discussed in detail. The ESD-on-SCR allows protection of critical nodes at low Vt1 trigger voltages during ESD while ensuring low leakage operation during normal operation. Although this clamp was discussed for HV applications it can also be applied with the same ease to protect thin gate oxides in advanced CMOS technologies maintaining a low leakage and a low capacity at the input node.

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About Sofics

Sofics (www.sofics.com) is the world leader in on-chip ESD protection. Its patented technology is proven in more than a thousand IC designs across all major foundries and process nodes. IC companies of all sizes rely on Sofics for off-the-shelf or custom-crafted solutions to protect overvoltage I/Os, other non-standard I/Os, and high-voltage ICs, including those that require system-level protection on the chip. Sofics technology produces smaller I/Os than any generic ESD configuration. It also permits twice the IC performance in high-frequency and high-speed applications. Sofics ESD solutions and service begin where the foundry design manual ends.

Our service and support

Our business models include

- Single-use, multi-use or royalty bearing license for ESD clamps
- Services to customize ESD protection
  - Enable unique requirements for Latch-up, ESD, EOS
  - Layout, metallization and aspect ratio customization
  - Area, capacitance, leakage optimization
- Transfer of individual clamps to another target technology
- Develop custom ESD clamps for foundry or proprietary process
- Debugging and correcting an existing IC or IO
- ESD testing and analysis

Notes

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