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Abstract

Simultaneous switching noise (SSN) resulting from IC devices can result in significant power bus noise, as well as radiation problems. An approach for estimating the power bus noise spectrum is presented in this paper. The power bus noise caused by digital circuits injecting high-frequency noise onto the DC buses feeding digital devices is calculated. The transient current drawn by an IC device is modeled using the load current and the shoot-through current through the power dissipation capacitance. Modeling and experimental results for several digital chips are shown. The modeling agrees well with the experimental results.

Keywords

Power-bus noise; EMI.

INTRODUCTION

The high-frequency noise on the DC power bus in multi-layer printed circuit design is a primary concern in meeting EMI requirements. For most PCBs, power bus noise is attributed to the switching noise of IC devices, including CPUs, and ASICs [1], [2]. The simultaneous switching noise (SSN) propagates throughout the entire power planes, and results in significant noise problems [3], [4]. The propagating power bus noise can lead not only to improper circuit functions, but can also be coupled to I/O circuits. In addition, the noise at the board edge can be coupled to metal enclosures and apertures in proximity, and as a result, EMI problems occur. The switching noise, commonly known as delta-I noise, results from pulses of current that flow between the planes during the high-to-low or low-to-high transitions of logic gates in digital integrated circuits [5], [6]. The high-frequency current that is injected from the power/ground terminal of an IC to the DC power bus is considered as a noise source, i.e. an exciter of the power bus [7]. For analysis, a current source is needed as an exciter of the power bus. But there are no device models that are widely available to represent the actual transient power current, IC impedance, or power bus impedance [8], [9]. Suitable transient current modeling is beneficial for evaluating the power bus design and developing design guidelines.

In this paper, an algorithm for transient current estimation modeling the shoot-through current with the power dissipation capacitance C_{PD} and the load current is described. Once the IC current is known, the noise voltage can be found if the impedance of the DC power bus is known for the frequency range of interest. The network analyzer was applied herein, and used to evaluate the validity of the transient current modeling. The agreement between the modeled and the measured results demonstrates that the proposed estimation can be used for engineering design.

ESTIMATING THE POWER BUS NOISE SPECTRUM

The procedure of estimating the power bus noise spectrum is outlined in this Section. Presently only IC clock buffers have been considered. First, the transient current drawn from the power bus is approximated by a triangular waveform, as shown in Figure 1. The current peak I_{P2} is the portion due to the shoot-through current, which can be estimated using the power dissipation capacitance C_{PD}, and it occurs on both the rising and falling edges of the clock cycle. The current peak I_{P1} is then the sum of I_{P2} and the load current sum for all I/O drivers, and it occurs at the leading edge of the clock cycle. Charging time of the load IC device is t_1, and it is equal to the rise time. Discharging time equal to the fall time is t_2. In general, they are different, but they are assumed to be equal in the calculations.

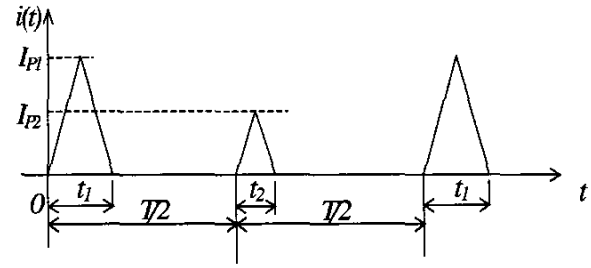

Figure 1. A triangular approximation for the transient current.

Next, the current spectrum I_{CC} is calculated using this time-domain information. An example of a modeled current spectrum is shown in Figure 2.

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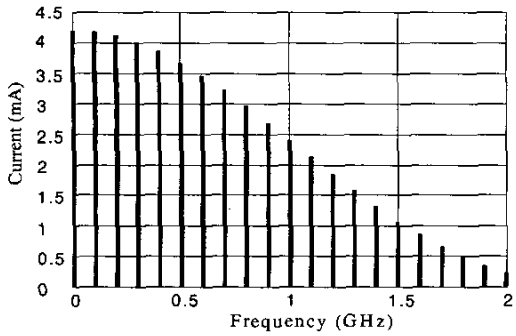

Figure 2. The modeled current spectrum.

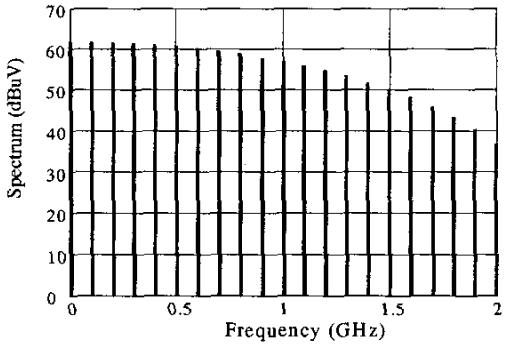

Figure 3. The modeled voltage spectrum.

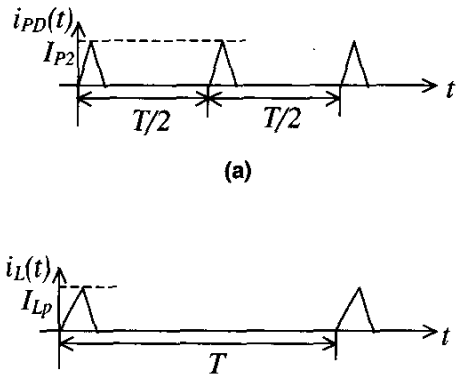

Figure 4. The relationship between the load and power dissipation current. (a) The portion of the current due to C_{PD}, and (b) The portion of the current due to C_L.

Finally, the spectrum of the noise voltage in the power bus structure is calculated using

$$V(n) = 20 \times \log\left[(I_{CC}(n) \times |Z(n)|)/10^{-6}\right], \quad (1)$$

where $V(n)$ is the voltage amplitude of the n^{th} harmonic, $I_{CC}(n)$ is the current amplitude of the n^{th} harmonic, $|Z(n)|$ is the impedance seen at the power pins of the device when looking into the power bus at the n^{th} harmonic, and 10^{-6} is the factor to convert dBV to $dB\mu V$. An example of the modeled noise voltage spectrum is shown in Figure 3.

The transient current $i(t)$ can be divided into two parts. One part, shoot-through current $i_{PD}(t)$, is due to the power dissipation capacitance C_{PD}. The other part, load current $i_L(t)$, is due to the capacitive loads C_L. The relationship between two current parts and the clock cycle are shown in Figure 4.

Since the shoot-through current appears on the switching time interval, the period of the peak current I_{P2} should be half of the operating period of the device. It can be estimated from the power dissipation capacitance C_{PD}. The total value of I_{P2} depends on the number of outputs that effectively switch simultaneously every clock cycle. The peak shoot-through current can be calculated as

$$I_{P2} = C_{PD} \times m \times V_{CC} / \Delta t_2, \quad (2)$$

where V_{CC} is the DC power bus voltage, Δt_2 is the switching time of the IC device equal to the rise time, m is the number of outputs. For most CMOS devices, the switching time interval Δt_2 and C_{PD} are available in the datasheet. But compared with the load current, the magnitude of the shoot-through current is relatively small and sometimes can be neglected.

Since the load charging current occurs only at the leading edge of the clock cycle, the period of the peak current I_{LP} is the same as the operating period of the device. The total value of I_{LP} depends on the number of outputs that are loaded. It can be calculated from a simple approximation as

$$I_{LP} = C_L \times n \times V_{CC} / (\Delta t_1 / 2), \quad (3)$$

where C_L is the load capacitance, V_{CC} is the DC power bus voltage, and Δt_1 is the charging time of the load IC device, and is equal to the rise time, and n is the number of the loaded outputs.

Alternatively, the load current can be calculated with an SI-tool and IBIS model, e.g., HyperLynx. For one output, the load current can be estimated using HyperLynx, as shown in Figure 5. Since 10 Ω is a typical series source termination and a 10-pF capacitor is a typical CMOS load, so for estimation, the loads of the output pins are taken as a 10-Ω resistor and 10-pF capacitor, and the IC chip is MPC946. Multiplied by the number of the loaded outputs, the total peak current I_{LP} is obtained. From Figure 5, the charging time t can be determined as well.

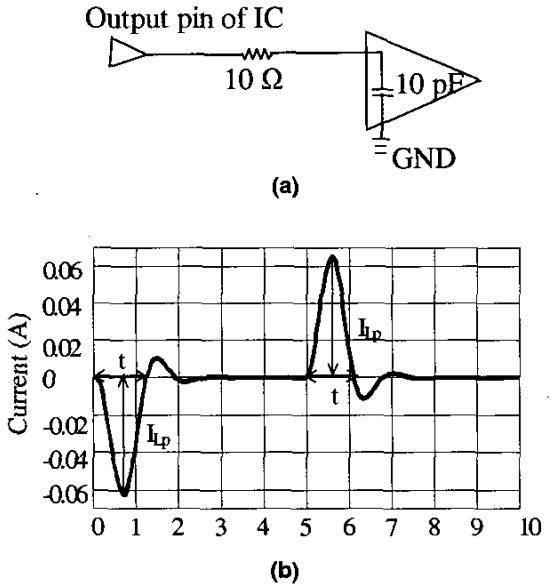

Figure 5. Estimating the load current. (a) the HyperLynx device model, and (b) the modeling result.

COMPARISON OF POWER BUS NOISE ESTIMATION WITH MEASUREMENTS

Power bus noise current models for three commercial devices, specifically, MPC946, MPC905, and CDC208, were developed. Vendor data sheet parameters are shown in Table 1.

Table 1. The modeling values for three ICs

	MPC905	MPC946	CDC208
C_{PD}	19.5 pF per output	25 pF per output	96 pF per bank (enable) or 12 pF per bank (disable)
V_{CC}	3.3 V	3.3 V	5 V
m (number of outputs)	6	10	8 or 4
n (number of loads)	6	8	8 or 4
f (operating frequency)	100 MHz	100 MHz	60 MHz
t_r(MAX)	4 V/nS	1.0 nS	10 nS/V

The experimental PCB with the device is shown in Figure 6. The PCB under test was a two-sided board. The size of boards was 10 cm × 6 cm (3.94 inches × 2.4 inches), and 0.1 cm (0.045 inches) thick. The bottom side of the PCB was a copper power plane and the topside of the PCB was a copper ground plane, excluding the signal traces. The sample IC chip is an MPC905. All the power/ground pins were connected to the power/ground plane. The output pins were loaded with a series 10-Ω resistor and 10-pF capacitor. For the MPC946, 8 of 10 output pins were loaded. For the MPC905, all 6 output pins were loaded. For the CDC208, 4 or 8 output pins were loaded. The unused pins were left floating. The IC was soldered on the upper side of the PCB and 5 SMT capacitors, each with a value of 10 μF, were soldered between the planes as the decoupling capacitors. In addition, 3 SMA coaxial test probes were located on the upper side of the boards. The probes are numbered from left to right, clockwise. The power bus spectrum was measured with a Rohde/Schwarz FSEB30 spectrum analyzer.

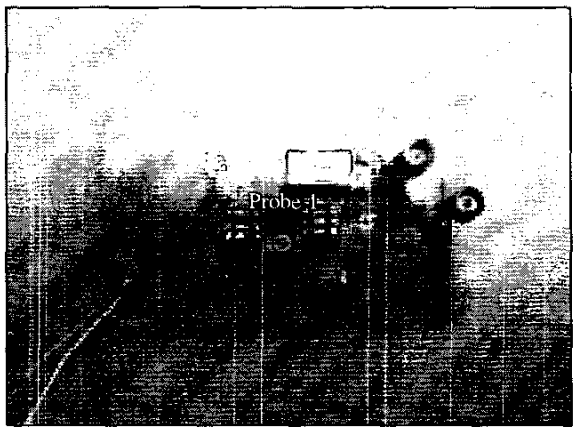

Figure 6. The test board considered in the experimental studies. The sample IC chip is MPC905.

According to (1), knowledge of the power bus impedance over the frequency range is necessary when estimating the power bus noise. This impedance can be measured using an HP8753D network analyzer. After calibration and port extension had been performed, the scattering matrix parameter S_{11} was measured using the network analyzer. The power bus impedance was then calculated as

$$Z = Z_0 \times (1 + S_{11})/(1 - S_{11}) \quad (4)$$

where Z_0 is 50 Ω.

All the measured and simulated results for voltage at the probe1 are shown in Figure 7. To make comparison easier, the measured spectra are plotted using a line, and for the simulated spectra, only the peak points at each harmonic are plotted with symbols.

The load current was estimated using the formula (3) and the HyperLynx model, and they differ slightly, as seen in Figure 7, and the difference is within ±10 dB. Although the power bus noise spectrum for the MPC946 and MPC905 is different, the algorithm makes a good prediction, and modeling and the measured results agree well. The modeling and the measured results are close for the

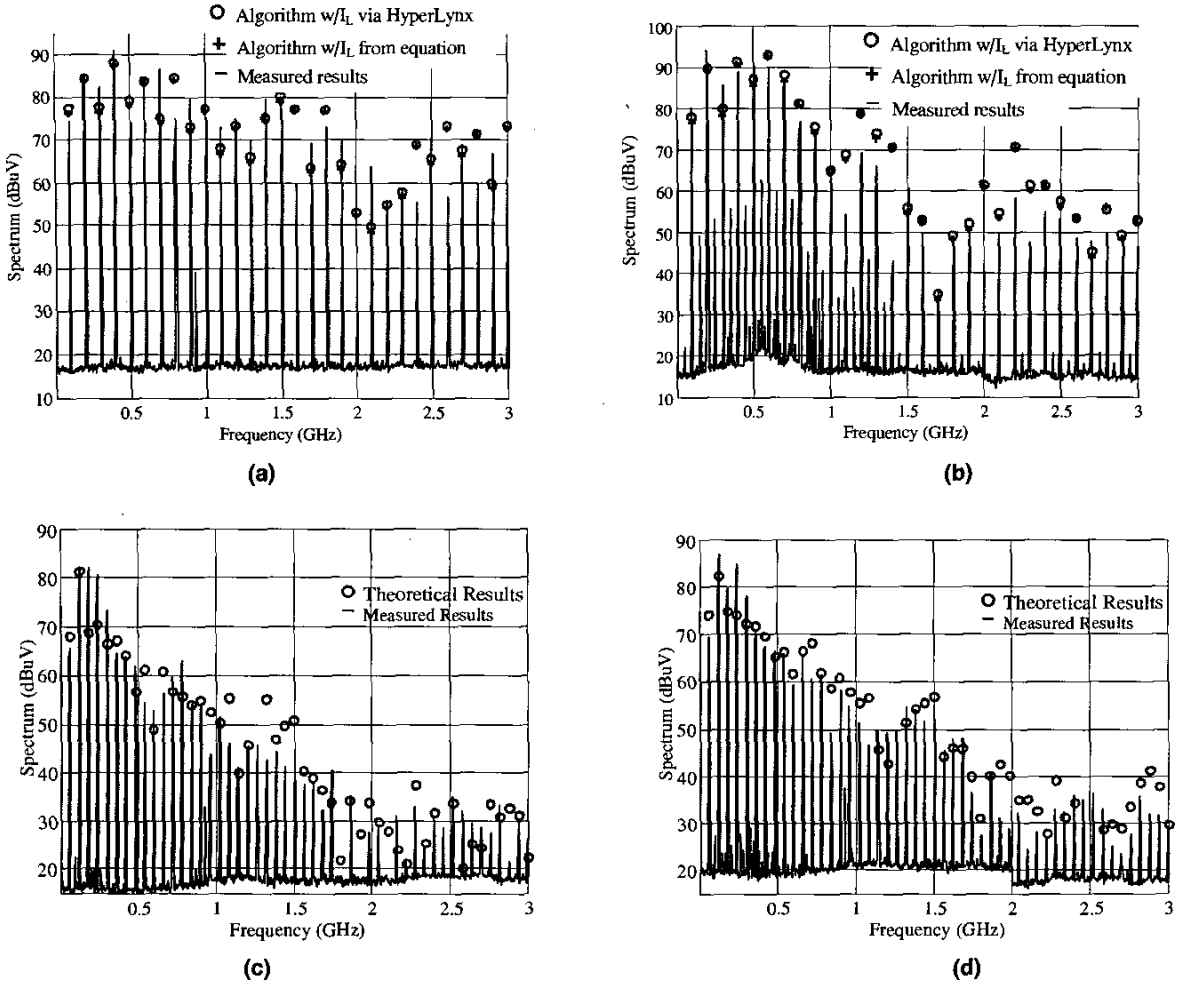

Figure 7. Comparison of the measured and simulated power bus spectra. Results for the (a) MPC905, (b) MPC946, (c) CDC208 (4 outputs loaded), and (d) CDC208 (8 outputs loaded).

CDC208 too, although the number of loaded outputs is different. It is found that the simulated spectra are a little higher than the measured spectra at higher frequencies. This might be due to the triangular approximation of the transient current waveform. The Fourier series representation of the triangular waveforms produces significantly larger amplitudes at the higher harmonic frequencies than those in the actual smoother waveform. In general, the agreement between the measurements and the proposed algorithm are within engineering accuracy, so that this algorithm can be useful in EMC design.

CONCLUSIONS

A power bus noise estimation algorithm is proposed in this paper. The transient current drawn by an IC device is modeled with the load current and the shoot-through current with the power dissipation capacitance C_{PD}. The power bus noise spectrum caused by the transient current is modeled with the transient current and the impedance of the board. In this paper, an agreement within engineering accuracy between the modeling and the measurement was achieved for three IC chips, MPC946, MPC905, and CDC208, with known values of power dissipation capacitance C_{PD}. The agreement indicates that the proposed algorithm can be a useful modeling approach in EMC design.

REFERENCES

[1] R. Senthinathan and J. L. Prince, *Simultaneous Switching Noise of CMOS Devices and Systems.* Boston, MA: Kluwer, 1994.

[2] H. W. Johnson and M. Graham, *High-Speed Digital Design, a Handbook of Black Magic.* Englewood Cliffs, NJ: Prentice Hall, 1993.

[3] S. Radu, and D. M. Hockanson, "An investigation of PCB radiated emissions from simultaneous switching noise," in *Proc. IEEE Int. Symp. Electromagn. Compat.*, Seattle, WA, Aug. 1999, pp. 893-898.

[4] W. Cui, "Modeling and design of DC power bus interconnects, segmentation, and signal via transitions in multi-layer printed circuit boards using FDTD and a mixed-potential integral equation approach with circuit extraction," Ph.D. Thesis, Univ. Missouri-Rolla, Rolla, MO, 2000.

[5] G. T. Lei, R. W. Techentin, B. K. Gilbert, "High-Frequency Characterization of Power/Ground-plane structures," *IEEE Trans. Microwave Theory Tech.*, vol. 47, pp. 562-569, May 1999.

[6] H. Hu, T. H. Hubing, and T. P. Van Doren, "Estimation of Printed Circuit Board Power Bus Noise at Resonance Using a Simple Transmission Line Model," in *Proc. IEEE Int. Symp. Electromagn. Compat.*, Montreal, Canada, Aug. 2001, pp. 896-898.

[7] Y. Fukumoto, T. Matsuishi, T. Kinoshita, O. Wada, Y. Toyota, and R. Koga, "Power current model of LSI and parameter identification for EMI simulation of digital PCBs," in *Proc. IEEE Int. Symp. Electromagn. Compat.*, Montreal, Canada, Aug. 2001, pp. 1185-1190.

[8] J. Chen, "Power bus radiation measurements and modeling," UMR Technical Brief, University of Missouri-Rolla EMC Laboratory, Sept. 1999.

[9] O. Wada, Y. Takahata, Y. Toyota, R. Koga, T. Miyashita, and Y. Fukumoto, "Power current model of digital IC with internal impedance for power decoupling simulation," in *Proc. 4th European EMC Symp.*, Bruges, Belgium, Sept. 2000, pp. 315-320.