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FINAL REPORT

EVALUATION OF ADVANCED MICROELECTRONIC FLUXLESS SOLDER-BUMP CONTACTS FOR HYBRID MICROCIRCUITS

Prepared For

GEORGE C. MARSHALL SPACE FLIGHT CENTER
MARSHALL SPACE FLIGHT CENTER
ALABAMA 95812

In Response To

CONTRACT NAS 8-31496

June 1976

Applied Technology
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NASA CONTRACTOR
REPORT

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NASA Technical Manager: S. V. Caruso, Electronics and Control Laboratory

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ABSTRACT

The trend in advanced electronic systems packaging is toward LSI hybrid microcircuitry in which a large number of monolithic integrated circuit chips of various types are incorporated with other active and passive components in a dense, multilevel, large-area module. However, such a circuit implementation requires a very large number of fine wire interconnections - 500 to 1,000 or more. The substantial cost associated with such a large number of independent, sequential operations, including the cost of required quality assurance procedures, is well known.

Alternative interconnection technologies have found application during the past few years, but various shortcomings have prevented them from becoming widely employed for most hybrid microcircuit requirements.

An in-depth study on the current use of flip-chip technology by the microelectronics industry was performed as part of this work and is presented herein. The advantages and disadvantages of this approach as compared to other methods are outlined, and the limitations of flip-chip techniques currently in use are discussed.

In the work described herein, a fluxless solder-bump contact technology was evaluated. Multiple solder-bump contacts were formed on silicon integrated circuit chips, which were then bonded directly to thick-film gold pads and to thin-film gold pads. No flux whatsoever was used in any part of the attachment process, thus precluding device degradation and failure due to flux residues.

These solder-bumps were electroformed onto device pads with the aid of thick dry film photomasks. Bump dimension was approximately 3 mils high and 4 mils by 4 mils in cross-sectional area (0.075mm x 0.1mm x 0.1mm).

Each bump was comprised of a rigid nickel underlayer and a compliant solder overlayer. The nickel underlayer served as a pedestal for collapse control during chip attachment. Two different solder alloys were evaluated; a gold-coated gold/lead/silver alloy, and a silver-coated indium/lead alloy.

Bump processing details are given herein.

The devices were interconnected to gold bonding pads by means of ultrasonic die attachment/solder reflow processes.

Fluxless solder-bump bond quality and reliability were evaluated by observing and measuring the effects of centrifuge, thermal cycling, and high temperature storage on bond visual characteristics, bond electrical continuity, and bond shear tests. The results of this evaluation are presented herein.

The feasibility of joining fluxless solder-bump contacts to thick-film pads by means of conductive epoxy was explored.

Applicability to CMOS device processing was investigated.

The applicability and suitability of this interconnection technology for hybrid microelectronic packaging, with special attention given to joining reliability, low-cost, economical processing, adaptability to currently available devices, adaptability to automated processing, and implementability by both manufacturers of semiconductor devices and hybrid users is discussed.

1. INTRODUCTION

The electrical and mechanical interconnection of microcircuit chip devices to form integrated electronics currently presents a reliability and economic problem in the microelectronic packaging industry. The traditional and most commonly used method for single device and multichip (hybrid) packaging is achieved by first mechanically attaching the back side of the chip to a substrate. Then, small diameter wires are used to provide interconnections between the device and substrate metallizations.

This approach results in versatile interconnection with respect to routing flexibility, but it also produces fundamental reliability and cost difficulties. For each wire interconnection, two bonds must be made. For a multiplicity of interconnections, all performed one at a time by a human operator, each bond becomes somewhat unique, and, even with a high level of quality control, the probability that a complex microcircuit will contain at least one unacceptable bond becomes appreciable.

To improve circuit reliability, a series of complex screening procedures have been developed, including thermal cycling, centrifuging, high-temperature burn-in, etc. In addition, a technique has been developed for non-destructive pull-testing of each individual wire after it has been bonded to test for bond integrity, but this procedure nearly doubles the cost of the wire-bonding operation, which is very high already, and the test is a very delicate one, requiring a very careful operator in order to improve bond quality assurance rather than reduce bond quality. As a result, the cost of reliable wire-bonded interconnections constitutes a major part of the cost of fabricating reliable microcircuits.

Further, it has been shown by both NASA and DOD that interconnections produce the greatest single failure rate in high reliability electronic systems. It is perhaps somewhat ironic that although the development of microelectronic technology has resulted in reducing the relative number of discrete interconnections significantly, interconnections remain a major reliability problem for microelectronics.

The trend in advanced electronic systems packaging will continue toward larger-scale integration and increased component density. This trend will be sustained by a combination of larger-scale integrated monolithic devices incorporated into increasingly complex hybrids.

Ultra-large-scale integrated monolithic devices will not provide the total answer to advanced packaging requirements because of:

- o Cost

  Greater complexity requires more area for both the increased number of devices and for the associated interconnect routing. Very large monolithic chip size results in lower yield, which in turn results in higher cost. Eventually, a point of rapidly diminishing returns is reached as complexity is increased on a single chip, with respect to yield and therefore of cost.

- o Design Flexibility and Lead Time

  Very large-scale monolithic devices do not provide design flexibility, and require very long lead times. For relatively small quantities, unit cost is very high.

- o Integration of Different Types of Devices

  Hybrid integration is usually the best way to combine various types of technologies for required and/or optimum performance, such as bipolar and MOS, low power and high voltage, specialized photo-detection properties, integrated surface acoustic wave processing, etc.

- o Final Utilization

  The more complex monolithic chips would be incorporated into advanced hybrid microcircuits.

High density LSI hybrid microcircuits, employing substrates with multilevel interconnections, are being designed and fabricated now with more than 400 interconnection wires, or over 800 wire bonds per microcircuit. In addition, LSI hybrids are being designed with as many as 1500 wires, or 3000 wirebonds per microcircuit. For these microcircuits, none of the required wirebonds can be missing, and each one must be of satisfactory quality. Thus, the demands on the wirebonding operators and on the quality assurance methods and implementation procedures are becoming critical.

Progress has been made toward automating or semi-automating the wire bonding process, but the problems (and costs) of required quality assurance procedures remain. The current absence of a practical, readily implementable alternative to wire-bonded interconnections is adversely affecting the microelectronics industry, and is overdue.

Three alternatives to wirebonding have been developed and include: (1) beam lead technology; (2) plastic film carrier technology and (3) flip chip technology. Each of these are viable methods and have been used with varying amounts of success. There are major objections to each of these approaches and therefore none have been developed to a degree that any has seriously competed with or replaced the wire-bonding technology.

However, the flip-chip technique appears to be a very promising general method for advanced development as an alternate to wire bonding for interconnection technology. The study reported herein concerns an investigation and evaluation of an advanced flip-chip interconnection method for application to high reliability low cost hybrid microcircuitry.

II. PROGRAM OBJECTIVE AND GENERAL APPROACH

A. Program Objective

The objective of this study is to evaluate an improved method for forming contacts on semiconductor devices, permitting all required mechanical and electrical interconnections to the device to be performed in a single, convenient, economical and reliable bonding operation, compatible with automated processing.

B. General Approach

This program was conducted in two phases, as follows:

1. Phase I

An in-depth study was performed on the current use of flip-chip technology by the microelectronics industry. The advantages and disadvantages of this approach as compared to other methods was determined. A list of the various flip-chip techniques currently used was compiled, and the limitations of each was outlined.

2. Phase II

A test program to evaluate microelectronic fluxless solder-bump interconnect technology was conducted, as follows:

a. The evaluation was comprised of the following tasks:

(1) Collect/measure appropriate solder metallurgical data

(2) Fabricate arrays of simulated integrated circuit chips on silicon wafer blanks; fabricate solder bumps on the simulated IC contact pads, with minimum of sixteen contacts per chip, and separate the chips

(3) Fabricate thick-film and thin-film flip-chip bonding pads

(4) Demonstrate fluxless assembly compatibility to thick-film gold pads and thin-film gold pads

(5) Demonstrate that this technology can be applied to several types of devices (PNP, NPN, CMOS, SOS, etc.)

(6) Test bond quality and reliability by means of visual examination and characterization, electrical continuity, and bond shear strength of bonded chips, for the following environmental test conditions:

(a) 10 temperature cycles from -65°C to +150°C

(b) 10,000 G and 15,000 G centrifuge

(c) High temperature storage at +150°C up to 1000 hours.

b. The microelectronic fluxless solder-bump interconnect technology was evaluated on the basis of the following criteria:

(1) Reliability of electromechanical interconnection of semiconductor chips

(2) Low cost processing

(3) Implementability by both manufacturers of semiconductor products and purchasers of these products

(4) Compatibility with available bonding equipment and materials

(5) Economy for both large and small volume production

(6) Adaptability to automatic procedures

(7) Compatibility with a large number of bump contacts per chip.

III. CURRENT USE OF FLIP-CHIP TECHNOLOGY BY THE MICROELECTRONICS INDUSTRY

A. Current Use of Flip-Chip Technology

Data gathered in a technology and utilization survey as part of this study shows that there are primarily five organizations currently employing flip-chip technology to a significant extent; namely IBM, Delco Electronics, General Electric, Motorola, and Micro Components Corporation.

Two of these organizations - IBM and Delco - are strictly internal manufacturer/consumers of flip-chipped devices; that is, they consume all of their own internal production of flip-chip devices, neither procuring nor selling such parts external to the organization itself.

A brief description and discussion of the technology employed by each of these five organizations follows.

1. IBM

IBM has been the most prominent and most consistent promoter of flip-chip technology to date. However, because of the relative isolation of IBM in the hybrid microelectronics world (due to the special business circumstances peculiar to IBM), IBM has had only a second-order influence on flip-chip technology external to IBM until comparatively recently (i.e., until the 1970's). However, IBM's internal usage of this technology is and has been enormous, relatively speaking.

Current IBM chip joining technology employs solder reflow processes, and is termed "Controlled Collapse" by IBM.

Bump metallization is basically done as follows. A thin molybdenum metal mask, with through-holes etched through the mask to coincide with device interconnection pads on the silicon wafer, is aligned and clamped to the wafer. Within a vacuum chamber, glow discharge bombardment is used to clean the contact surface areas. Then metallization layers are deposited through the metal mask onto the contact pad areas, comprised of approximately 1000 Å chromium, 500 Å chromium/copper alloy, 5000 Å - 10,000 Å, copper, and finally 1000 Å gold. At this point, the mask is changed; another molybdenum mask, with an identical through-hole pattern, but with larger diameter holes, is aligned and clamped to the wafer. Within a vacuum chamber, lead-tin alloy is deposited over the gold dot pattern, to a thickness of approximately 0.05mm. Considerable fractionation of the lead/tin alloy source material takes place, resulting in a bump which is tin-rich at it's surface, but the equivalent composition of the bump alloy is 95 wt.% lead, 5 wt.% tin. The bumps are subsequently melted by heating the wafers in a reducing atmosphere, forming hemispheres of a relatively uniform solder alloy composition.

The oversize solder deposit, achieved by means of larger through-holes in the solder deposition mask, achieves a useful purpose in that, when the bumps are melted to form hemispheres, the diameter of the solder constricts to the diameter of the underlying metallization layers; thus, the final height of the solder bump increases to more than 0.075mm from the original thickness of 0.05mm, without requiring additional deposition time and while minimizing problems with the mask. The diameter of completed bumps is approximately 0.1 to 0.125mm (4 to 5 mils).

Finally, the wafer is sawed into individual devices.

In this process, it is reported that 40 to 50 wafers are processed at a time, and that 30 minutes of labor is required for each batch in order to build up the required thicknesses of metallization.

The counter-substrates employed are comprised of alumina, with palladium/silver thick-film conductors, coated with 90 lead/ 10 tin solder. Glass dams

over selected portions of the conductor surfaces are used to restrict solder flow. The total volume of solder on the semiconductor devices and on the substrate bonding pads is controlled in order to achieve reliable joints. A white rosin flux is applied over the substrate bonding pad surface before chip placement, to act as a temporary adhesive and to promote wetting during solder reflow. Joining is performed in reflow furnaces in a nitrogen atmosphere.

The flip-chip bumped devices are manipulated and bonded automatically at high handling rates.

A major reason for employing 90 lead: 10 tin on the substrate pads is to maintain the melting point of this joint above that of the lead/tin eutectic, which is used in subsequent module processing steps, and to achieve proper joining at the flip-chip bump.

2. Delco Electronics

At Delco, flip-chip devices are processed as follows. Thin chromium and gold layers are vacuum-deposited over the aluminum contact pads which constitute the silicon wafer metallization, to serve as the bump underlayer. An electroforming process, using a photoresist mask, is used to form the pure silver bumps. Final bump dimensions are approximately 5 mils diameter and 3 mils high (0.125mm diameter by 0.075mm high).

The counter-substrates employed are alumina with thick-film conductors. The bonding areas are coated with lead/tin eutectic, applied primarily by means of solder screening, or alternatively by means of solder dipping. Chip joining is done by means of solder reflow, with the aid of a fluxing agent.

Delco uses a single 6-bump chip on each voltage regulator microcircuit produced by Delco, and a single 9-bump chip on each electronic ignition module. Total flip-chip device usage rate is approximately 60,000-80,000 flip-chip devices per day.

These same two device types have been produced and used by Delco for the past several years, at approximately the same rate, with little or no change in the technology or the numbers and types of flip-chip devices used.

3. General Electric

Flip-chip devices are manufactured at GE's Integrated Circuits Center at Syracuse, NY. Little data can be gathered regarding the particular processes and construction employed in these devices because GE considers their process to be proprietary. However, the flip-chip solder metallization is 95 lead: 5 tin, and bump geometry is very similar to that of the corresponding IBM parts. GE claims that all of their flip-chip parts are passivated with silicon nitride.

Devices currently being supplied are bipolar, although it is claimed that MOS devices have been processed on an experimental basis with good results.

GE's Mobile Radio Products Division at Lynchburg, VA is a volume user of flip-chip parts from GE's Integrated Circuits Center, from Motorola Semiconductor Products Division, and from Micro-Components Corporation. The flip-chip parts are joined to eutectic tin-lead solder-coated thick-film conductors on alumina substrates. Solder reflow with the aid of flux is employed. GE claims that bonding yields approach 100%.

GE's Heavy Military Electronic Systems Division at Syracuse, NY has reportedly started using flip-chip technology in very moderate volume on a highly classified project within the last year.

4. Motorola

Motorola has made flip-chipped devices available on a commercial basis during the last 2 or 3 years. The flip-chip metallization process and bump structure appears to be similar or identical to that of IBM.

Motorola is primarily a manufacturer of flip-chip devices rather than a user, although it is rumored that the Ft. Lauderdale Communications Division of Motorola will begin employing flip-chip technology in 1976.

At the present time, Motorola offers only bipolar integrated circuits in flip-chip form, although the feasibility of supplying MOS and CMOS devices in flip-chip form is being investigated. The recent move of much of Motorola's MOS and CMOS operations to a facility in Austin, Texas seems to be affecting this feasibility verification work. A major process problem affecting the successful processing of MOS and CMOS parts at Motorola will probably involve a step in which Motorola cleans the base aluminum contact pads with a glow discharge prior to depositing additional metallization layers, in order to achieve a reliable low-resistance electrical contact. An alternative method for assuring a reliable low-resistance contact will have to be employed.

5. Micro Components Corporation

At Micro Components, flip-chip devices are processed as follows, starting with oxide-passivated wafers, with windows opened at the contact pads.

A clean aluminum metallization pad surface is assured by means of careful processing at the time that windows are opened in the surface oxide passivation layer. Then a series of metal layers is deposited over the entire wafer; first aluminum (approximately 2500 Å); then aluminum/nickel alloy (approximately 5000 Å); and finally nickel (approximately 3000 Å). A photomask is applied, and nickel is etched away everywhere except at the contact pad areas, leaving the continuous aluminum layer in place over the entire wafer. The photomask is then removed and a second "reverse" photomask is applied, such that only the contact pad areas remain exposed. Then electrolytic copper (approximately 15 μm thick) and finally a 95 lead / 5 tin solder alloy (approximately 0.075mm thick) is electroformed onto the contact pad areas. The photomask is then removed, the exposed aluminum film is etched away, and the solder terminals are formed into hemispheres by melting in an inert atmosphere.

The purpose of the copper layer is to form a surface readily wetted by solder. The purpose of the nickel and nickel/aluminum layers is to provide a surface which would remain intact in the event that the entire copper layer were entirely converted to copper/tin intermetallic, thus providing some final measure of adhesion to the solder during repeated solder reflow cycles. The aluminum layer provides adhesion to the wafer surface.

Micro Components presently has available 8 families of devices in flip-chip form, and is reportedly producing hundreds of thousands of such devices per month.

In addition to the five organizations employing flip-chip technology to a significant extent as outlined above, others might be mentioned that have pursued the technology in the past, and more that some indications suggest may be joining what appears to be a rapidly growing reviving interest in this technology. However, available data regarding current important users of flip-chip technology indicate that the list shown in Figure 1 is essentially complete.

When reviewing Figure 1 it becomes evident that the IBM technology has now achieved a marked impact on current flip-chip technology. Delco's technology, which is the major exception, has apparently been applied to only two devices of note, both of which were first developed several years ago; accordingly, even though volume usage continues to be impressive, and reliability is excellent under the extremely difficult operational environment associated with proximity to automible engines, Delco appears to have stagnated somewhat in this technology.

During the 1960's, IBM employed what they referred to as the "SLT" technology which was applied to their System/360 computer. This technology was notable in that copper spheres were incorporated into the solder bump structure to provide chip stand-offs. During the beginning of the 1970's the SLT technology evolved into the so-called

ORGANIZATION/LOCATION	VOLUME MFG	VOLUME USER	GENERAL FLIP-CHIP BUMP TECHNOLOGY DESCRIPTION	COMMENTS
IBM, INCLUDING IBM COMPONENTS DIVISION EAST FISHKILL FACILITY HOPEWELL JUNCTION, NY	X	X	CHROMIUM, CHROMIUM/COPPER ALLOY, COPPER, AND GOLD LAYERS ARE VACUUM-DEPOSITED OVER THE ALUMINUM DEVICE METALLIZATION THROUGH METAL MASKS. 96 LEAD: 5 TIN BUMPS, APPROXIMATELY 0.05 MM HIGH, ARE THEN VACUUM-DEPOSITED ONTO THE GOLD LAYER THROUGH METAL MASKS, AND SUBSEQUENTLY REFLOWED TO FORM HEMISPHERES APPROXIMATELY 0.075 MM HIGH. CHIP ATTACHMENT BY REFLOWING 90:10 LEAD/TIN SOLDER IN NITROGEN, USING FLUX.	TOTALLY IN-HOUSE MANUFACTURER/USER. IBM HAS BEEN THE MOST PROMINENT PROMOTER OF FLIP-CHIP TECHNOLOGY OVER THE PAST 10 TO 12 YEARS
DELCO ELECTRONICS KOKOMO, IN	X	X	CHROMIUM AND GOLD LAYERS ARE VACUUM-DEPOSITED OVER THE ALUMINUM DEVICE METALLIZATION. PURE SILVER BUMPS, 0.125 MM IN DIAMETER AND 0.075 MM HIGH, ARE ELCTROFORMED OVER THE GOLD LAYERS. CHIP ATTACHMENT BY REFLOWING TIN/LEAD EUTECTIC SOLDER, USING FLUX.	TOTALLY IN-HOUSE MANUFACTURER/USER. DELCO USES A 6-BUMP FLIP-CHIP ON THEIR VOLTAGE REGULATOR MICROCIRCUIT AND A 9-BUMP FLIP-CHIP ON THEIR ELECTRONIC IGNITION MODULE. TOTAL USAGE IS ABOUT 60,000 TO 80,000 FLIP-CHIP DEVICES PER DAY.
GENERAL ELECTRIC: A. MOBILE RADIO PRODUCTS DIVISION, LYNCHBURG, VA B. INTEGRATED CIRCUITS CENTER, SYRACUSE, NY C. MILITARY ELECTRONIC SYSTEMS DIVISION SYRACUSE, NY	X	X	THE GE FLIP-CHIP BUMPING PROCESS IS CONSIDERED TO BE PROPRIETARY BY GE, AND LITTLE TECHNOLOGY DATA IS AVAILABLE. GE'S DEVICES ARE PASSIVATED WITH SILICON NITRIDE, AND THE BUMPS ARE PRIMARILY COMPRISED OF LEAD/TIN SOLDER WITH HIGH LEAD CONTENT.	GE PURCHASES FLIP-CHIP DEVICES FROM MOTOROLA AND MICRO-COMPONENTS CORPORATION, IN ADDITION TO SUPPLYING SOME OF THEIR OWN IN-HOUSE DEVICE REQUIREMENTS. GE IS A VOLUME USER OF FLIP-CHIPS.
MOTOROLA SEMICONDUCTOR PRODUCTS DIV. PHOENIX, AZ & MESA, AZ	X		FLIP-CHIP METALLIZATION TECHNOLOGY IS ESSENTIALLY IDENTICAL TO THAT OF IBM, DESCRIBED ABOVE.	
MICRO COMPONENTS CORPORATION CRANSTON, RI	X		ALUMINUM, ALUMINUM/NICKEL ALLOY, AND NICKEL LAYERS ARE VACUUM-DEPOSITED OVER THE WAFERS, AND THE NICKEL IS PATTERN-ETCHED. ELECTROFORMED BUMPS OF COPPER AND 95:5 LEAD/TIN ALLOY ARE THEN PLATED OVER THE NICKEL. EXPOSED ALUMINUM IS THEN ETCHED AWAY, AND THE SOLDER IS MELTED, FORMING BUMPS APPROXIMATELY 0.1 MM HIGH.	

Figure 1. Current Use of Flip-Chip Technology by the Microelectronic Industry

"controlled collapse" technology described above, with the chief advantage that the joints which resulted were much more ductile and therefore more reliable.

The Motorola technology appears to be essentially identical to that of IBM for all practical purposes. The Micro Components technology is substantially different from that of IBM in many details, but the general characteristics of the final product is essentially identical to that of IBM. General Electric's technology, no doubt, falls within this same classification range also. Thus, in summary, the current leading flip-chip technologies employ lead/tin solder bumps, lead/tin bonding pads, and solder reflow joining with the aid of a fluxing agent, as first pioneered by IBM.

B. Limitations of Flip-Chip Techniques Currently in Use

The flip-chip bumping technology employed by IBM, Motorola, and (probably) General Electric are essentially identical. This technology basically consists of vacuum-depositing thin metal bump base layers onto wafer contact pad areas through a special metal shadow-mask, followed by vacuum-deposition of thick lead-tin solder bumps onto the base layers using a second special metal shadow-mask.

The flip-chip bumping technology at Micro Components is somewhat different in that the thin metal base layers are applied by means of vacuum deposition followed by subtractive etching. Thick lead-tin solder bumps are then applied onto the metal base layers by means of an electroforming process. However, the final bump structure is very similar to that of IBM/Motorola/GE.

The flip-chip bumping technology at Delco is rather unique among these five. The thin metal base layers for the bumps are applied by means of vacuum deposition followed by subtractive etching. Thick bumps of pure silver are then formed over the metal base layers by means of electroforming process. The Delco technology can also be classified as a solder bump technology because, in common with IBM/Motorola/GE/Micro Components, solder present on the counter-substrate is used for chip joining by means of solder reflow.

Thus, all currently prevalent flip-chip joining techniques employ solder chip joining, as opposed to ultrasonic or thermocompression chip joining.

All of the flip-chip bumping and joining technologies currently employed, as outlined above, require complex processing, both for the bumping processes and the chip joining processes. Complex processes are objectionable from both reliability and yield/cost viewpoints.

For these bumping processes, either two sequential metal-shadow masking steps are required, or two sequential photoresist masking steps.

The IBM process requires two special metal shadow-masks for each wafer type. Metal shadow-mask making involves relatively expensive, complex processes. Mask handling and alignment is critical, and the metal masks used during solder deposition require cleaning after each deposition. In general, vacuum deposition processes are relatively complex and time-consuming, requiring relatively expensive equipment. However, it should be noted that vacuum deposition processes employing metal shadow-masking is relatively very clean, provided that intimate mask contact is assured during the deposition process in order to prevent metal from reflecting between the mask and the wafer, which could otherwise result in metal "halos" and consequent device shorting or other problems.

Chip joining associated with these flip-chips is also complex, in that substrate bonding pads must first be pre-coated with solder, and then coated with solder flux.

Solder flux is especially objectionable in that, following solder reflow chip joining, a second process step is required in order to remove the flux residue. However, it is difficult to reliably remove flux residues after they have been heated to soldering temperatures (for flux materials which are sufficiently active to permit reliable joining), especially in the close spacings between bonded devices and substrate. It is well known that flux residues can lead to subsequent device degradation and failure.

Circuit rework requires a second application of flux, solder reflow, and a second cleaning step to remove flux residue.

In addition, the IBM "Controlled Collapse" chip joining technology requires the use of both solder dams and closely-controlled volumes of solder on the substrate bonding pads, which is an additional complication factor.

A further disadvantage of these technologies is that, to minimize leaching by the solder, thick-film materials containing either palladium or platinum are employed, in conjunction with high-lead solders. Thick-film inks containing palladium or platinum are expensive because of the high cost of these precious metals. The use of high-lead solders requires relatively high-temperature processing.

IBM's selection of lead/tin for their thermally deposited solder bump alloy rather than lead/indium is puzzling. As shown in Figure 2, the extent of lead/tin alloy fractionation during evaporation is 500 times greater than that for lead/indium. Thus, process control for lead/indium alloy deposition would be much simpler than that for lead/tin, resulting in improved, more reliable composition control for lead/indium. Indium depresses the melting point of lead in a manner very similar to tin; e.g., the liquidus of both 90 wt.% lead/10 wt.% tin and 90 wt.% lead/10 wt.% indium is 300°C. Lead/indium alloys are much less likely to attack solderable bump base metallization layers than lead/tin. The mechanical properties of lead/tin and lead/indium are nearly identical and they form compatible solder joints when joined to each other.

Finally, it might be mentioned that glow discharge cleaning of wafer device pads prior to deposition of the initial bump base metallization layer may not be compatible with MOS device process requirements.

FIGURE 2

VAPOR PRESSURES OF SELECTED METALS AT 1105°K.

Element	Approximate Vapor Pressure at 1105°K.	Fractionation Ratio at 1105°K for Lead Alloys $\left(\frac{p^o}{p^o_{Pb}}\sqrt{\frac{M_{Pb}}{M}}\right)$	Component Preferentially Evaporated
Lead	1×10^{-1} torr	1	-
Tin	2×10^{-6} torr	2.6×10^{-5}	Pb
Indium	1×10^{-3} torr	1.3×10^{-2}	Pb
Silver	1×10^{-4} torr	1.4×10^{-3}	Pb
Gold	2×10^{-8} torr	2×10^{-7}	Pb

In summary, flip-chip techniques currently in use feature the traditional advantages of solder-bump flip-chip joining, including the following features:

- o High speed gang-bonding
- o Rugged terminals
- o No special tooling required in order to handle each device size
- o Automatic chip alignment and leveling during solder reflow
- o Ductile, annealed chip joints

The major limitations and disadvantages of prevalent flip-chip techniques are outlined below:

1. Complex solder bump processing
   - o Two masking steps are required, with critical alignment.
2. Complex chip joining processing
   - o Substrate bonding pads must be pre-coated with solder, which must in turn be pre-coated with flux.
   - o The amount of solder at the bonding pad area must be closely controlled, by using solder dams and closely-controlled solder thickness.
   - o To minimize leaching, thick-film conductors containing either platinum or palladium must be used, which are expensive, in combination with high-lead solders.

- o The use of high lead solders requires relatively high temperature processing.
- o Flux residues must be removed.

3. Flux residues

- o It is difficult to reliably remove flux residues after they have been heated to soldering temperatures, especially in the close spacings between bonded devices and substrates. Flux residues can lead to subsequent device degradation and failure.

C. Advantages and Disadvantages of Flip-Chip Technology Compared to Other Methods

The three major alternatives ro gang-bonded interconnections are the flip-chip, beam-lead, and beam-tape technologies.

In flip-chip technology, metal bumps integrated with the chip and extending well above the chip surface are used to interconnect the chip in a face-down position to substrate circuit pads, as illustrated in Figure 3.

Flip-chip technology can be divided into two major categories, distinguished by the method of attachment; namely, ultrasonic-bump and solder-bump. Ultrasonic-bump flip-chips may employ aluminum as the chief bump metallization, formed by means of vacuum deposition through a metal mask or by means of photolithography. Solder-bump flip-chips typically employ 95% lead/5% tin as the solder metallization. Solder-bump flip-chip attachment is depicted in Figure 4.

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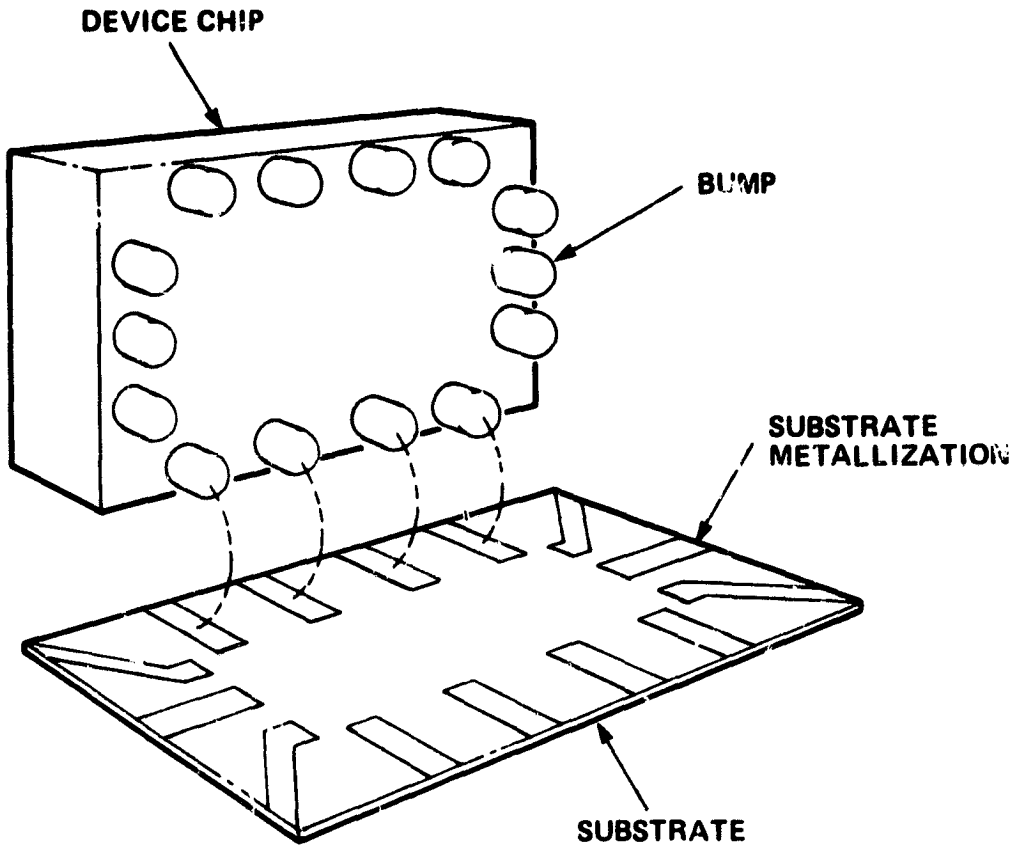

Figure 3. Flip Chip Attachment

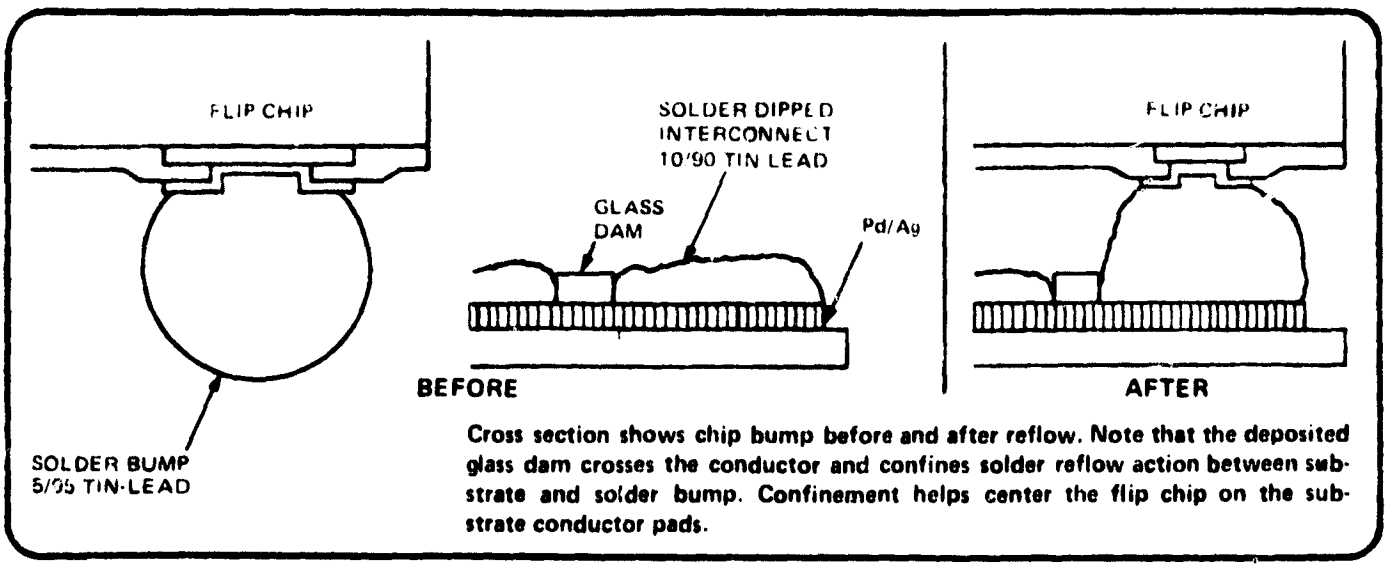

Figure 4. Solder Bump Attachment

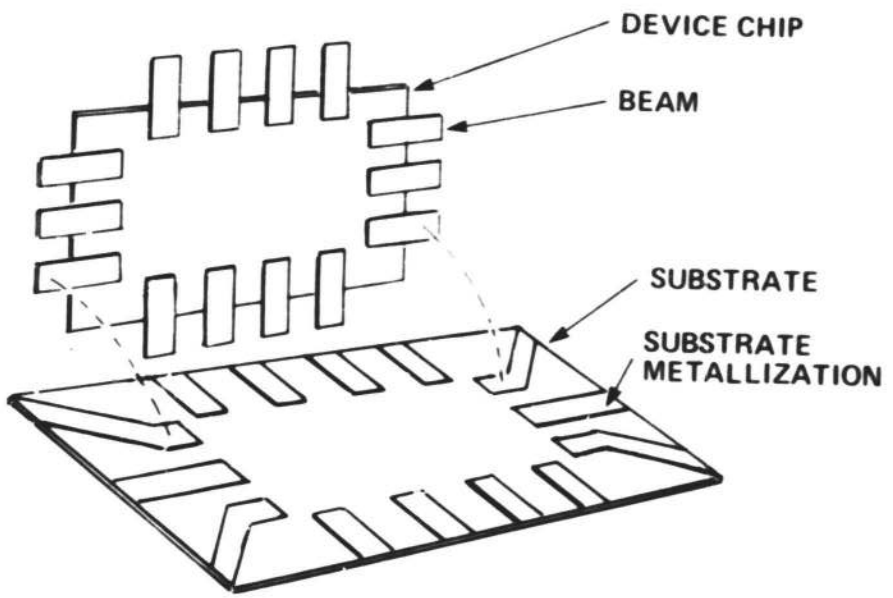

Figure 5. Beam Lead

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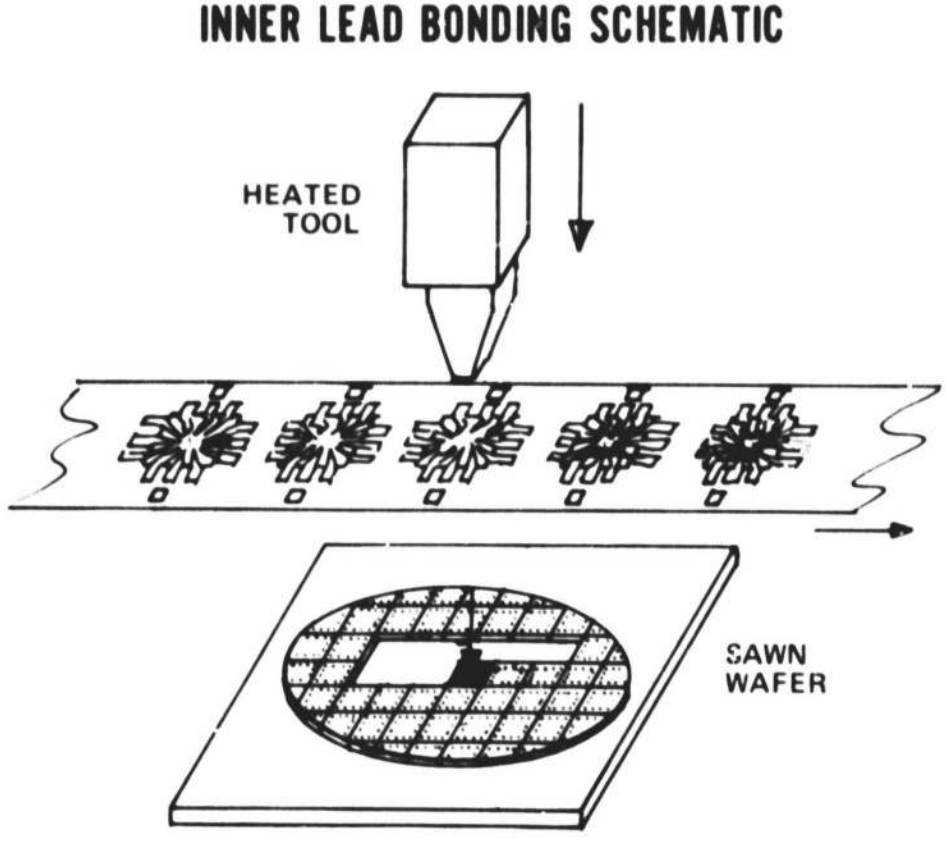

Figure 6. Beam Tape

7605-4550-11

Figure 7. Beam Tape Bonding Machine

7605-4550-10

INTERCONNECTION PROCESS SEQUENCE

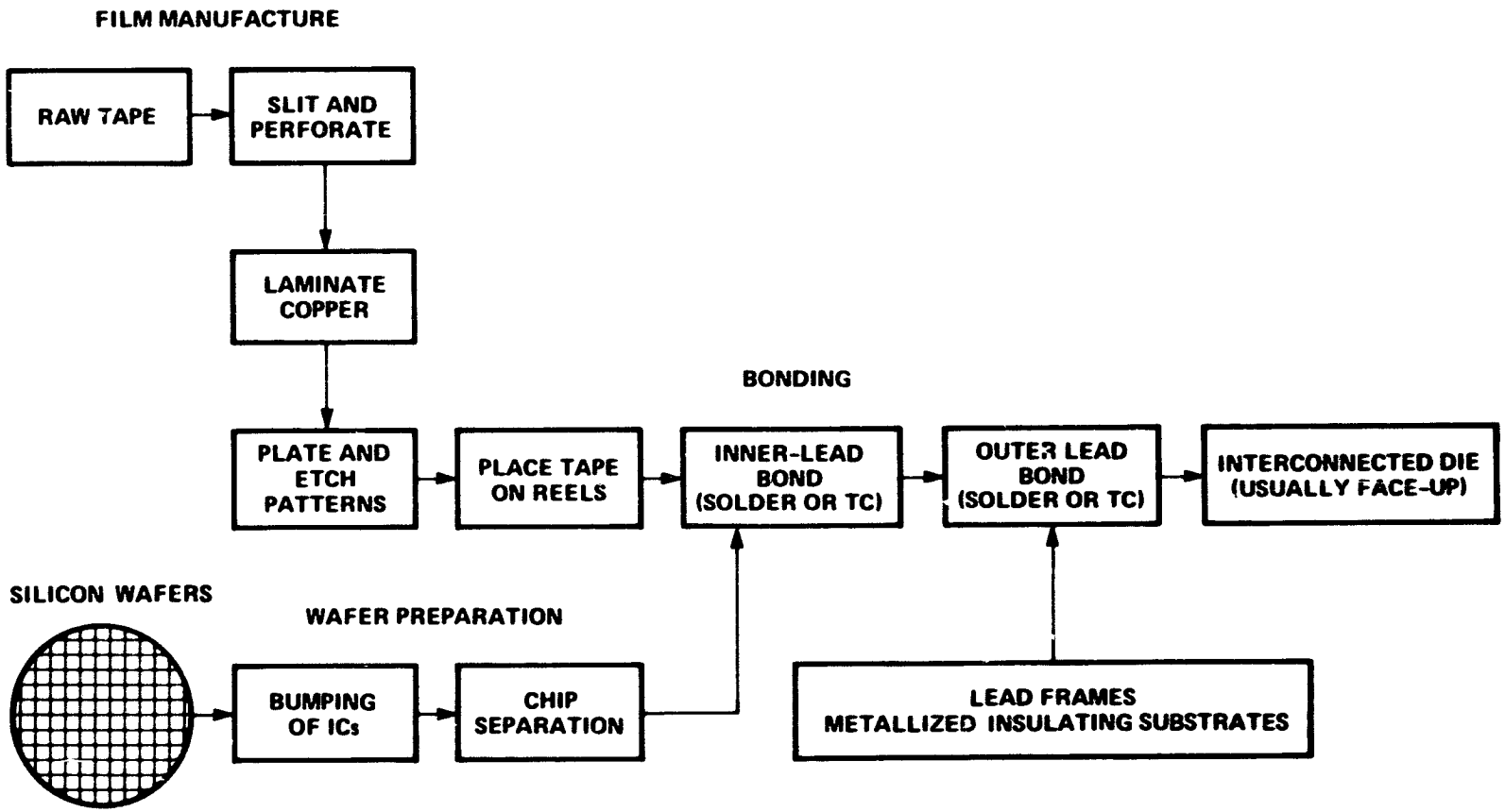

Figure 8. Beam Tape

2. Disadvantages of beam-lead technology compared to flip-chip technology.

- o Special circuit layouts must be used on the silicon wafer, in order to provide room for beam formation; and, if chips are separated by means of anisotropic etching, specific silicon crystallographic orientation is required. Thus, the technology cannot employ the great majority of circuit layouts currently available, and the semiconductor manufacturer's basic process might need to be modified. Also, most of the latest high-performance devices cannot be obtained in beam-lead form.

- o Fewer circuit chips can be formed on a silicon wafer of a given size, because of the need to allow room for the beams, resulting in fewer devices per wafer and increased device cost.

- o Beam-lead processing is complicated, involving two or three additional photomasking steps, resulting in increased device cost and reliability impact in small volume production.

- o Beam-leads are fragile (susceptable to bending), creating handling and shipping problems.

- o Beam-lead device attachment is difficult to reliably automate. Automatic handling and bonding is difficult, and alignment to bonding pads is critical.

- o For gang-bonding processes, a special-size bonding tool is required for each die size.

3. Advantages of beam-tape technology compared to flip-chip technology.

- o Convenient bond inspection.
- o Long lead-lengths are readily provided (well suited for packaging single devices in plastic-encapsulated DIP's).

4. Disadvantages of beam-tape technology compared to flip-chip technology.

- o Electrical and mechanical interconnections are made in two separate mechanical steps, rather than the single step of flip-chip (or beam-lead) interconnection. Twice as many discrete joints are required.
- o For reliable joining, it is desirable to form raised bumps on the chip pads, somewhat similar to that employed in flip-chip interconnections, to which the beam-tape is bonded. Thus, processing and attachment is more complex than for flip-chip technology.
- o The process is difficult and expensive to automate. The critical alignment requirements of both the etched film over the chip devices and the beam-tape assembly to external circuit pads dictates that specialized, elaborate equipment must be used.
- o The extensive tooling requirements, comprising both mechanical equipment and custom etched beam-tape patterns, necessitates very high unit production in order to be cost effective.

- o Special bonding tools are required for each die size.

- o Packaging is not as dense as for flip-chip.

5. Disadvantages of flip-chip technology.

a. Ultrasonic-bump

- o Considerable pressure must be applied to multiple-bumped chips during bonding, in order to achieve high bond strength, which can cause chip breakage or crack propagation. Also, bumps can be scrubbed right through thin-film metallization, resulting in poor interconnection reliability, unless care is exercised.

- o Ultrasonic waves can propagate through the substrate material during device attachment, which can affect bond strengths of previously-bonded chips.

- o Alignment to bonding pads is critical.

- o The integrity of the multiplicity of bonds cannot be verified by optical inspection alone.

b. Solder-bump

- o Substrate bonding pad construction is complex, requiring pre-coating with solder and flux and requiring solder dams to restrict solder flow and closely controlled volumes of solder on the solder pads.

- o Flux residues must be removed from the close spacing between chip and substrate. Flux residue contamination is a reliability risk.

- o Lead-tin solder is not metallurgically compatible with the formation of joints with films containing gold.

- o Relatively high temperature processing is required.

- o Bump processing can be complex, comprising multiple photolithographic operations.

6. Advantages of flip-chip technology compared to beam-lead technology.

   - o Special wafer layouts are not required in order to provide space for beam-lead formation.

   - o Wafer chip density is not reduced, which would otherwise result in fewer devices per wafer and increased device cost.

   - o Chip separation by means of anistropic etching is not required, so that wafer crystallographic orientation constraints are relaxed.

   - o Flip-chip processing is simpler and less expensive than beam-lead processing.

   - o Flip-chip bumps are more rugged than beam-leads, thus facilitating handling and shipping.

   - o A special tool is not required for each flip-chip die size, as is the case for beam-lead gang-bonding.

- o Flip-chip devices cost less to process than beam-lead devices.

7. Advantages of flip-chip technology compared to beam-tape technology.

   - o Half as many discrete joints are required for flip-chip interconnections, as compared to beam-tape interconnections. For beam-tape, two discrete joining operations are required for each device.
   - o Silicon wafer processing is nearly as complex for beam-tape as for flip-chips, because raised bumps should be provided on device pads for reliable beam-tape joining. Overall, chip joining is more complex for beam-tape.
   - o Beam-tape is both difficult and very expensive to automate, as compared to flip-chip.
   - o Special tooling is not required for each flip-chip die size.
   - o Flip-chips can be packaged more densely than beam-tape interconnected devices.

8. Disadvantages of solder-bump technology compared to beam-lead and beam-tape technology.

   - o Flip-chip bond joints are not as easy to inspect as beam-lead or beam-tape bond joints.
   - o Solder-bump flip-chip joining may require the use of solder flux.
   - o Flip-chip substrate bonding pads may have to be fabricated from expensive materials containing palladium or platinum in order to minimize solder leaching.

o. Further discussion.

With reference to ease of bond joint inspection, as mentioned above, it should be pointed out that there is a great deal of similarity between beam-lead and beam-tape bond joints and wire bond joints, as far as the basic mechanism of joint formation and the subsequent optical inspection procedure are concerned. It should be noted that it may be so difficult to assure the bond integrity of wire bond joints by means of certified bonding equipment, processes, and operators in conjunction with optical inspection, in addition to other reliability assurance procedures such as thermal cycling, high temperature burn-in, and centrifuge, that some organizations have resorted to 100% non-destruct wire bond pull testing for additional quality assurance. Thus, the intrinsic value of optical inspection of beam-lead or beam-tape joints in itself is of limited quality assurance significance.

Unless special provisions are made to extend flip-chip bumps to the edge of the chip, the joint is much more difficult to inspect than beam-lead joints, but the visual appearance of the solder meniscus, and the assurance of an annealed joint may be more meaningful than the information conveyed by the deformation pattern on the surface of a beam-lead or beam-tape joint.

An intriguing future potential exists for chip devices supplied pre-bonded to beam-tapes in a standard fan-out pattern; however, (1) a substantial device handling problem would still be present, similar to the situation for beam-leaded devices; and (2) it is not clear that it would be faster to interconnect such beam-tape devices than wire-bonded devices, unless a special gang-bonding tool is used for each beam-tape size.

A great deal has been said of the advantages of the so-called sealed junction properties of the beam-leaded devices. The sealed junction devices employ a platinum silicide ohmic contact, a silicon nitride surface passivation, and a titanium/platinum/gold-layered metallization overlapping the edges of the silicon nitride windows. This construction has proved to be effective in resisting contamination in humid environments. However, it should be recognized that an analogous device construction applied to another type of interconnection technology would be equally effective in resisting contamination in humid environments. This desirable characteristic need not necessarily be associated only with beam-leads.

IV. FLUXLESS SOLDER-BUMP TECHNOLOGY

In fluxless solder-bump technology, flip-chip solder-bumped devices are bonded to gold circuit pads without the use of any flux whatsoever.

A schematic of fluxless solder-bump construction is shown in Figure 9.

The bump structure consists of two chief metallization layers. First, a relatively hard metal or alloy layer of relatively high melting point is applied adjacent to the base semiconductor device metallization. Then a relatively soft solder alloy layer of relatively low melting point is applied as the bump extremity.

The solder layer has the function of forming a solder bond to gold circuit bonding pads for device mechanical and electrical interconnection. The compliant properties of the solder layer permits multiple-bumped devices to be reliably interconnected despite some degree of non-planarity of the joining surfaces. It also accommodates disparate thermal expansion between bonded chip and substrate. A thin precious metal coating over the solder layer prevents or minimizes environmental effects on the bonding surface, to permit reliable fluxless solder attachment.

The chief function of the hard underlying metal layer is to serve as a rigid pedestal to control bump distortion characteristics during bonding. Without this pedestal layer, much of the solder distortion during bonding might take place at the semiconductor device surface. This pedestal layer assures that bump dimensions at the device surface remains constant, and that any solder bump collapse which occurs during bonding, prior to solder reflow, takes place at the bonding surface. The pedestal layer also serves as a metallurgical transition layer between the semiconductor device metallization and the solder layer.

The pedestal comprises approximately 1/3 of the bump height, and the solder layer the remaining 2/3. Total bump height is approximately 3 mils (0.075mm).

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1. FLUXLESS SOLDER-BUMP FLIP-CHIP TECHNOLOGY (BOND DIRECTLY TO GOLD CIRCUIT PADS WITHOUT THE USE OF FLUX)

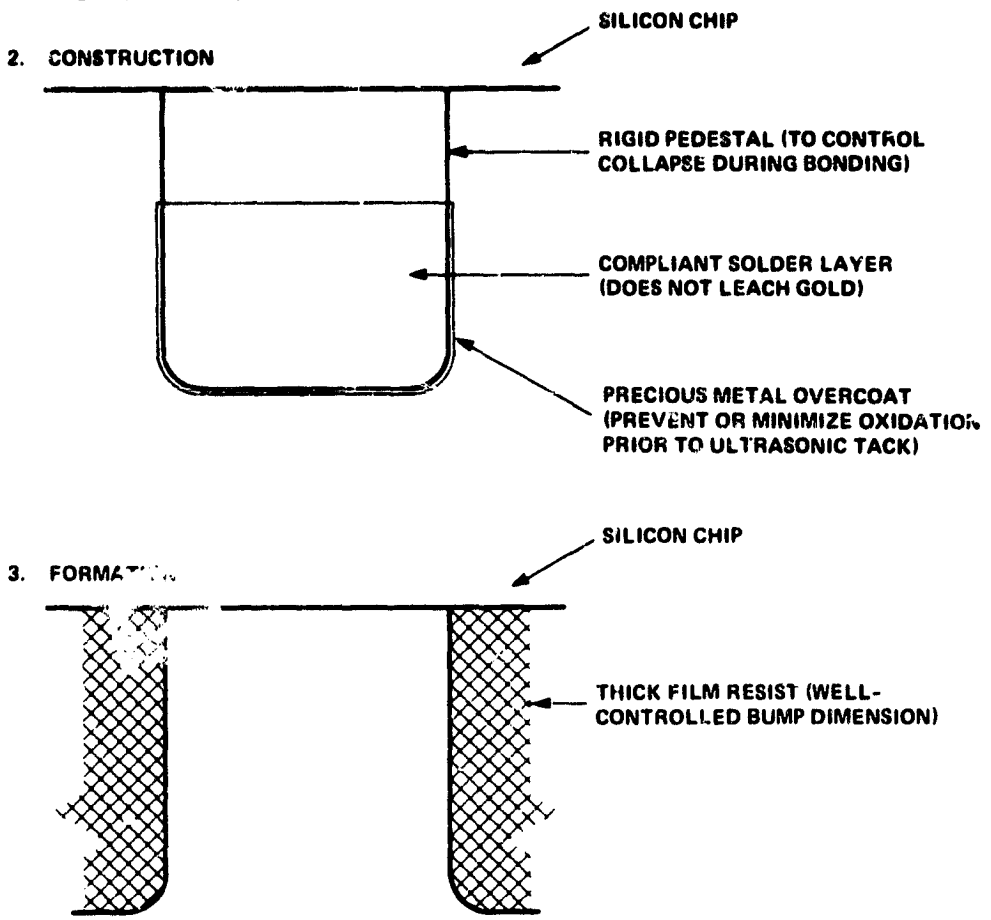

Figure 9. Fluxless Solder-Bump Technology

For low-cost processing, electroforming techniques are used to form the solder bumps. Since electroforming processes require electrical contact to every bump position, a continuous metal film is first coated over the entire wafer, over the device base metallization and surface passivation layer. Then a thick-film photomask is applied over the metal surface film, and windows are opened in the photomask at the future bump sites. The thick-film photomask helps to assure very well-controlled bump diameters.

For the solder layer material, lead alloys were selected, primarily because lead forms compliant, corrosion-resistant, low temperature solders. In addition, some lead alloys are compatible with the formation of reliable, metallurgically-compotible joints to precious metal bonding pads such as gold.

In general, two types of alloy mechanisms can minimize gold leaching from bonding pads. In each case, the solidus temperature of the solder must exceed the bonding temperature at the bonding interface when some small incremental quantity of gold is absorbed into the solder at the bonding interface, or when some small incremental quantity of solder diffuses into the gold bonding pad, or both.

In this regard, two different solder alloys are especially notable for application to fluxless solder-bumps. For solder alloys containing both lead and gold, the solidus temperature for certain compositions increases dramatically as the gold content is increased. The same is true for solder alloys containing both lead and indium.

As part of this program, chips metallized with both gold/lead/silver and indium/lead/silver solder-bumps were evaluated. It is believed that these two solder compositions, of all possible solder compositions, are best suited for fluxless solder-bump materials, on the basis of their particular combination of desirable material properties, including softness, ductility, convenient melting point, good corrosion resistance, low vapor pressure, and minimization of gold leaching effects.

During assembly, the chips are tacked down to bonding pads by means of an ultrasonic die bonder equipped with a combination ultrasonic/vacuum pick-up tool. This bonding operation deforms the soft-solder portion of the bumps, giving reliable contact to multiple-bumped devices. A heating operation then reflows the solder, forming annealed, alloyed bonds to the interconnection pads. Solder wetting is localized at the ultrasonically-scrubbed regions of the bonding pads.

This fluxless solder-bump method is not penalized by any of the objections outlined in Section III C for beam-lead or beam-tape technologies. In addition, most of the disadvantages of flip-chip technology are also eliminated.

Advantages of fluxless solder-bump technology include:

- Simplified solder-bump processing

  Maximum of one masking step (might be combined with window etch mask step).

- Simplified chip joining.

  Uncoated gold bonding pads are used (no solder pre-coat, no flux pre-coat, no solder dams, lower temperature processing, no flux residue removal).

- No flux residues

  Simplifies contamination control.

- Metallurgically-compatible interfaces with gold films.

- Well-controlled bump dimensions.

  Well-controlled bump dimensions are provided, with the potential for bump extension to the edge of the chip for easier chip alignment and bond inspection.

- Bumps with magnetic properties can be provided to facilitate chip handling and storage.

  It is convenient to employ either nickel or nickel/cobalt alloy as the pedestal material, thus imparting magnetic properties to the bumps. These metals are easy to plate, in addition to being rigid and corrosion-resistant. Magnetic properties are useful for convenience of chip handling and storage.

The general fluxless solder-bump metallization process itself is conceptually quite flexible, and can be modified to suit particular process preferences.

V. METALLURGICAL INVESTIGATION

Data has been gathered on metallurgical properties of five selected solder alloys containing gold/lead and indium/lead, in addition to 90 lead/10 tin for the purpose of comparison, as shown in Figure 10. These measurements were necessary because of a paucity of pertinent available published data. For most trinary alloys especially, such data is not available.

The first three columns give alloy composition, liquidus/solidus temperatures, and tensile strength. The fourth column shows Young's Modulus, which is the stress required to produce unit strain (or unit change-of-length). The fifth column gives hardness (Rockwell W). Since the equipment available could not reliably measure hardnesses greater than 100 Rockwell W, quantitative measurements are shown for only three alloys, and relative order of hardness for all six. The last column shows percent elongation at the break point.

The measured liquidus/solidus temperatures of the binary lead/indium alloy are lower than expected, and are at variance somewhat with published data.

A. Test Sample Preparation Method

The starting materials used are detailed below.

Starting Materials

Metal	Purity	Supplier	Comments
Lead	M5N5	Alfa Products	Remelted to further eliminate oxide formation.
Indium	M5N	Apache Chemical	
Tin	M5N	Apache Chemical	
Gold	M5N	Apache Chemical	
Silver	M6N	Apache Chemical	

ALLOY (COMPOSITION IN WEIGHT %)	MELTING POINT OR LIQUIDUS/SOLIDUS TEMPERATURE	TENSILE STRENGTH @ 25°C	YOUNG'S MODULUS @ 25°C	HARDNESS @ 25°C (3.18 MM DIAMETER TOOL)	% TOTAL ELONGATION AT BREAK POINT @ 25°C
15.0 GOLD, 82.9 LEAD, 2.1 SILVER	213°C	5,450 PSI 383 KG/CM^2	2.9 × 10^6 PSI 200,000 KG/CM^2	(5)	
15.3 GOLD, 84.7 LEAD	215°C	9,180 PSI 645 KG/CM^2	3.0 × 10^6 PSI 210,000 KG/CM^2	(6)	0.9%
12.5 GOLD, 85.0 LEAD, 2.5 SILVER	214°C	4,830 PSI 340 KG/CM^2	(2.7 × 10^6 PSI) (190,000 KG/CM^2)	(4)	1.5%
32.9 INDIUM, 64.4 LEAD, 2.7 SILVER	199–247°C	4,126 PSI 290 KG/CM^2	1.3 × 10^6 PSI 91,000 KG/CM^2	(3) 110 ROCKWELL W @ 15 KG LOAD	4%
33.8 INDIUM, 66.2 LEAD	202–241°C	3,283 PSI 231 KG/CM^2	1.3 × 10^6 PSI 91,000 KG/CM^2	(2) 85 ROCKWELL W @ 15 KG LOAD	2.5%
90.0 LEAD, 10.0 TIN	277–303°C	3,190 PSI 224 KG/CM^2	2.3 × 10^6 PSI 160,000 KG/CM^2	(1) (SOFTEST) 60 ROCKWELL W @ 15 KG LOAD	10%

Figure 10. Some Metallurgical Properties of Selected Solder Alloys

The appropriate amount of each metal was weighed on a Mettler Balance and transferred to a 15 x 20 mm quartz vacuum tube having a 12 mm O.D. restricted neck. The tubes were then evacuated to a pressure no greater than 5 microns and then sealed while under vacuum. The sealed ampules were then continuously coated in a small oven for one (1) hour at 500° - 550°C. After this fire period, the tubes were removed from the oven and allowed to reach room temperature.

The alloys were cast into the dumbbell-shaped samples required for Instron stress-straining analysis using a graphite mold.

To cast the sample, the evacuated tubes were cracked at the top, and quickly reheated to 400°C. along with the graphite mold. The mold was removed from the oven, and the liquid alloy poured into the mold and allowed to cool to room temperature. The cast sample was then removed from the mold, sanded to remove flashing, and drilled to accept the pins on the Instron machine. All samples were then annealed at 185°C. for 2 hours in a vacuum oven followed by overnight cooling in the turned-off oven. A time-temperature schedule of the annealing process is shown in Appendix I, Graph A.

The samples were then submitted for stress/strain analysis in the Instron machine. Following these tests, the samples were cut apart and subjected to hardness and melting temperature determinations.

B. Liquidus/Solidus Temperatures

Liquidus/solidus temperatures were determined by using a differential scanning calorimeter (DSC). These results are listed below.

Liquidus/Solidus Determination (DSC)

Alloy #	Composition - Wt. %	Liquidus/Solidus Temp. °C.	Type of Melting Point
1	15.0 Au - 82.9 Pb - 2.1 Ag	213	Sharp with tail
2	15.3 Au - 84.7 Pb	215	Sharp
3	12.5 Au - 85.0 Pb - 2.5 Ag	214	Sharp with tail
4	32.9 In - 64.4 Pb - 2.7 Ag	199 - 247	Broad
5	33.8 In - 66.2 Pb	202 - 241	Broad
6	90.0 Pb - 10.0 Sn	277 - 303	Medium wide

Alloy #2 is a gold-lead eutectic and thus has a very sharp melting point. Adding silver to the eutectic mixture (alloys #1 and #3) reduced the melting temperature only slightly and produced a small broadening of the melting range. The lead-indium alloy #5 exhibited a rather broad melting range (202 - 241°C) and adding a small amount of silver (alloy #4) expanded this range slightly at both ends (199 - 247°C). The lead-tin (alloy #6) had a medium wide melting range (277 - 303°C) as expected.

C. Stress/Strain Analysis

All stress/strain analysis work was performed using dumbbell-shaped samples in conjunction with an Instron machine. To supplement the numerical data, a representative graph is shown in Appendix I for stress/strain measurements on each alloy. Since three samples of each alloy were prepared, individual numbers on the graphs may not agree with the value in the data chart, which represents the average value of all readings taken. The numerical data is summarized below.

Stress/Strain Analysis

Alloy #	Composition (wt.%)	Young's Modulus X 10^3 kg/cm^2	Ultimate Tensile Strength (kg/cm^2)
1	15.0 Au - 82.9 Pb - 2.1 Ag	200	383
2	15.3 Au - 84.7 Pb	210	645
3	12.5 Au - 85.0 Pb - 2.5 Ag	190 (est)*	340
4	32.9 In - 64.4 Pb - 2.7 Ag	91	290
5	33.8 In - 66.2 Pb	91	231
6	90 0 Pb - 10.0 Sn	160	224

*No real proportional limit from which to calculate Young's Modulus.

In discussing this data in more detail, refer to Appendix I. Graph #4 shows the stress/strain curve for the lead-indium alloy #5. By examining the stress/strain curve in Graph #4, it can be seen that the first point reached is the proportional limit, in this case 60 kg/cm^2. In this region, strain is proportional to stress up to the proportional limit. The slope of the stress/strain curve is, by definition, the Young's Modulus of the material - in this example 91,000 kg/cm^2. The next point on the graph is the yield point (200 kg/cm^2). The region between the proportional limit and the yield point is referred to as the elastic region. In other words, if the stress is removed at any point up to the yield point, the material should return to its original length. Beyond the yield point, should the stress be removed, the material will exhibit a "permanent set". The yield point is arbitrarily defined to occur at 0.2% elongation for the purpose of this work. A line drawn parallel to the proportional region of the curve and intersecting the percent elongation axis at 0.2% then defines the yield point of the alloy. However, the arbitrary nature of the 0.2% criterion, especially as applied to soft alloys, must be emphasized. The final point on the graph is the ultimate te. sile strength or breaking point of the sample and indicates the stress required to break the dumpbell-shaped sample into two halves (239 kg/cm^2 in Graph #4).

By comparing each of the six graphs, some insight can be gained into the nature of each of the materials. In general, the greater the modulus of the alloy, the more brittle is the sample. For example, all alloys containing gold tended to be substantially more brittle than those without gold; thus Graphs #1, #2, and #5 indicate higher modulus readings. It may be noted on Graph #5 that no clearly defined proportional region occurred, thus preventing computation of a modulus for this alloy. This lead-gold-silver alloy is very "rubbery" in nature and thus has no proportional region. Note also that the two lead-gold-silver alloys (Graphs #1 and #5) tend to be more elastic than the lead-gold alloy (Graph #2) as is evidenced by a greater tangential slope in the elastic region of the lead-gold alloy (Graph #2) as opposed to the lead-gold-silver alloys (Graphs #1 and #5).

Comparing ultimate tensile strengths, it can be seen that addition of gold to the lead alloys substantially increases tensile strength. The lead-gold alloy #2 has the highest strength reading (645 kg/cm^2). Addition of silver (alloys #1 and #3) reduced the tensile strength to approximately 340 kg/cm^2. The lead-indium alloy #5 had a tensile strength of 231 kg/cm^2 and addition of silver to this alloy increased the reading to 290 kg/cm^2. The lead-tin alloy #6 has a tensile strength of 224 kg/cm^2, similar to that of the lead-indium alloy.

Some insight can also be gained into the brittleness of the alloys by comparing the total percent elongation of the material at the breaking point. These values are given in order of decreasing stretch before break in the table below.

Percent Total Elongation at Breaking Point

Alloy #	Composition - wt. %	% Total Elongation at Break Point
6	90.0 Pb - 10.0 Sn	10.0
4	32.9 In - 64.4 Pb - 2.7 Ag	4.0
5	33.8 In - 66.2 Pb	2.5
3	85.0 Pb - 12.5 Au - 2.5 Ag	1.5
1	82.9 Pb - 15.0 Au - 2.1 Ag	
2	84.7 Pb - 15.3 Au	0.9

The lead-tin alloy exhibits the greatest strain before breaking. Note that adding silver to the lead-indium alloy increased the total percent elongation compared to the lead-indium alloy alone. Again, the alloys containing gold have the least percent elongation at break. The silver-lead-gold alloys clearly show more elastic behavior as compared to the lead-gold alloy alone.

D. Hardness Measurements

All hardness tests are Rockwell Superficial Hardness measurements. The Rockwell Superficial hardness test involves applying first a minor load to a hard steel ball, of known diameter, into the surface of the metal being tested. Next a major load of 15, 30, or 45 kg is applied and then released. After a specific time period has elapsed, a reading is taken with the major load released, but the minor load still applied. This reading represents the difference in penetration between the minor load alone and the minor load after the major load has been applied and released. The larger the number, the harder the material. Due to the fact that the largest diameter ball available was 3.18mm, the six alloy samples had to be run using 3 different major load scales. This makes the data more difficult to compare. The alloys have been listed below in order of increasing hardness based on the data taken.

Superficial Rockwell Hardness Values
(3.18 mm Diameter Ball - W Scale)

Alloy #	Composition - wt.%	Major Load	Reading	
6	90.0 Pb - 10.0 Sn	15 Kg.	50	Softest
5	66.2 Pb - 33.8 In	15 Kg.	85	
4	64.4 Pb - 32.9 In - 2.7 Ag	15 Kg.	110	
3	85.0 Pb - 12.5 Au - 2.5 Ag	30 Kg.	80	
1	82.9 Pb - 15.0 Au - 2.1 Ag	45 Kg.	55	
2	84.7 Pb - 15.3 Au	45 Kg.	109	Hardest

This table gives the relative hardness of the six alloys. Alloy #6, the lead-tin combination is the softest alloy. Alloy #5, lead-indium is next hardest. Addition of silver increases the hardness further (Alloy #4). The lead-gold-silver alloys are next in line, with alloy #1 being harder than alloy #3. Finally, the lead-gold binary alloy is the hardest material tested.

E. Conclusions

The above measurements show the lead-gold binary alloy to be the strongest, hardest and possibly the most brittle alloy tested. Addition of silver to this combination resulted in a loss of tensile strength, and a gain in softness and elasticity. Addition of silver to the lead-indium alloy resulted in an increase in hardness and tensile strength. The lead-tin alloy had the lowest tensile strength, was the softest alloy tested and had the highest elastic behavior in terms of percent elongation before break.

Thus, the addition of silver to gold/lead alloys makes the alloys significantly softer and more elastic, with only minor changes in the melting points of these alloys. It is also expected that, on joining to gold-metallized substrates, the mechanical characteristics of the solder bump/gold bonding pad interface will also be similarly modified in a desirable manner.

The addition of silver to indium/lead solder bumps is also desirable. As an overplate, silver will both help prevent bump surface oxidation and, when alloyed, should improve elongation properties without affecting melting point significantly. In addition, in an analogous fashion to the gold/lead solder alloy, it might be expected that, on joining to gold-metallized substrates, the mechanical characteristics of the solder-bump/gold bonding pad interface would also be similarly modified in a desirable manner.

Thus, it can be concluded that silver is a highly desirable constituent for both gold/lead and indium/lead fluxless solder-bumps.

Although enough data was not taken to permit optimization of the silver content of either alloy, the data does permit solder-bumps with acceptable and desirable properties to be defined.

The data taken was extrapolated and interpolated somewhat, using engineering judgement, to yield the following desired solder compositions for fluxless solder-bump metallization (i.e., stated for solder-bumps melted in the absence of a bonding pad, such that the precious metal bump coating is homogeneously alloyed into the solder bump).

Gold/Lead/Silver Solder-Bumps		Indium/Lead/Silver Solder-Bumps	
gold	10-12 wt.%	indium	approximately 24.5 wt.%
lead	84-87 wt.%	lead	approximately 74 wt.%
silver	3-4 wt.%	silver	approximately 1.5 wt.%

VI. FABRICATION OF BUMP CONTACTS ON INTEGRATED CIRCUIT CHIPS

A. Simulated Integrated Circuit Chips

1. Base Metallization and Photomask

a. Fabrication of Simulated Integrated Circuit Wafers

In order to facilitate bonding and electrical continuity testing, simulated integrated circuit chips were fabricated, to be used for preliminary tests in place of electrically-complex integrated circuits. The simulated semiconductor chip metallization pattern (i.e., one unit of the wafer array) is shown in Figure 11.

In this very simple circuit, sixteen evenly-spaced bonding pads, each 0.1mm x 0.1mm in area, are electrically interconnected into pairs. The bonding pads are each spaced 0.25mm apart (0.35mm center-to-center). The simulated integrated circuits are repeated on 1.75mm centers.

Two masks were used in fabricating this circuit. One mask was used for metallization pattern definition, and the other to open 0.1mm x 0.1mm windows through the surface dielectric passivation film, to expose the bonding pads.

These simulated integrated circuit arrays were formed on 3.8 and 5 cm diameter polished single-crystal silicon wafer blanks.

The general process sequence for the simulated IC wafer fabrication was as follows:

(1) Thoroughly clean the silicon wafer.

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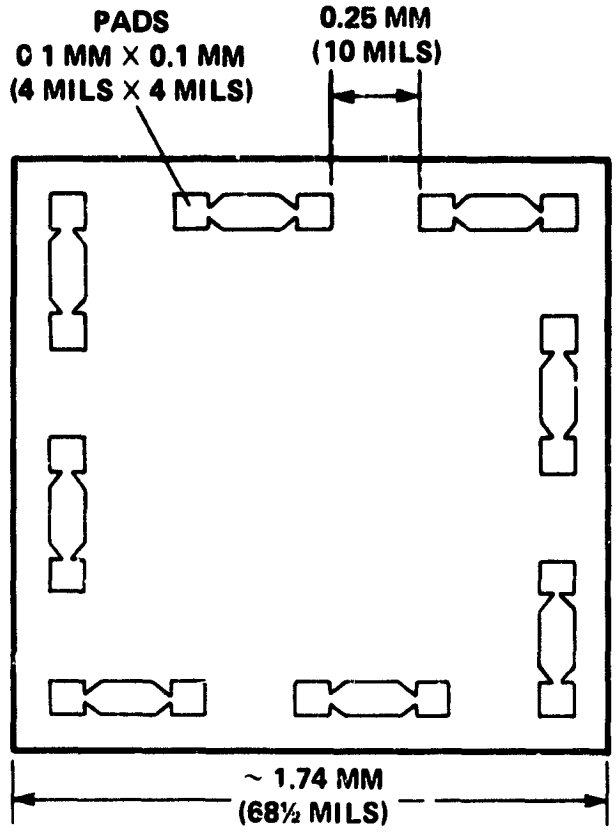

PATTERN STEPPED AND REPEATED
1.75 MM CENTER-TO-CENTER
ACROSS A 5 CM DIAMETER

Figure 11. Simulated Semiconductor Chip Metallization Geometry

(2) Deposit 2000 Å of molybdenum by means of RF sputter deposition.

(3) Apply a negative photoresist circuit mask (747 resist).

(4) Etch the molybdenum circuit with Mo etchant (alkalai ferricyanide).

(5) Strip the resist and clean the wafer.

(6) Deposit 5000 Å of silicon nitride by means of reactive RF sputter deposition.

(7) Deposit 300 Å of molybdenum over the silicon nitride by means of RF sputter deposition (to act as a silicon nitride etch mask).

(8) Apply a negative photoresist window mask (747 resist).

(9) Etch a molybdenum window pattern with Mo etchant (aikalai ferricyanide). Strip the photoresist.

(10) Etch the window pattern through the silicon nitride film using 85% phosphoric acid at approximately 168°C. for approximately 10 minutes, thus exposing the molybdenum pad areas.

(11) Thoroughly clean the wafer.

b. Application of the Base Metallization

An electrical contact to each bump location is required in order to build up bump metallization by means of electroforming. This electrical contact is achieved by means of a continuous thin metal film deposited over the entire wafer, applied as follows:

(1) Thoroughly clean the wafer.

(2) Deposit 300 Å of molybdenum by means of RF sputter deposition.

(3) Deposit 12,000 Å of copper by means of RF sputter deposition.

The copper film serves as both an electrical conductor for bump electroforming, and as a desirable base metallization for electroforming. Copper is the most convenient plating base, from the standpoint of ease of surface preparation (i.e., cleaning or "activation") prior to plating.

A cross-section of the base metallization (not to scale) is shown in Figure 12.

c. Application of the Photomask

The wafers are then laminated with Riston 30S dry film resist and windows are opened through the resist at the contact pad areas. This dry film photomask, which is approximately 0.074mm thick, restricts subsequent bump metallization build-up to the contact pad areas.

The dry film photomask application process is outlined in detail in Appendix II.

The most critical part of the dry film photomask application process, by far, is the opening of clean window areas. The most critical stages in the opening of clean window areas are steps 7 and 9 of Appendix II - namely, pattern printing and pattern development.

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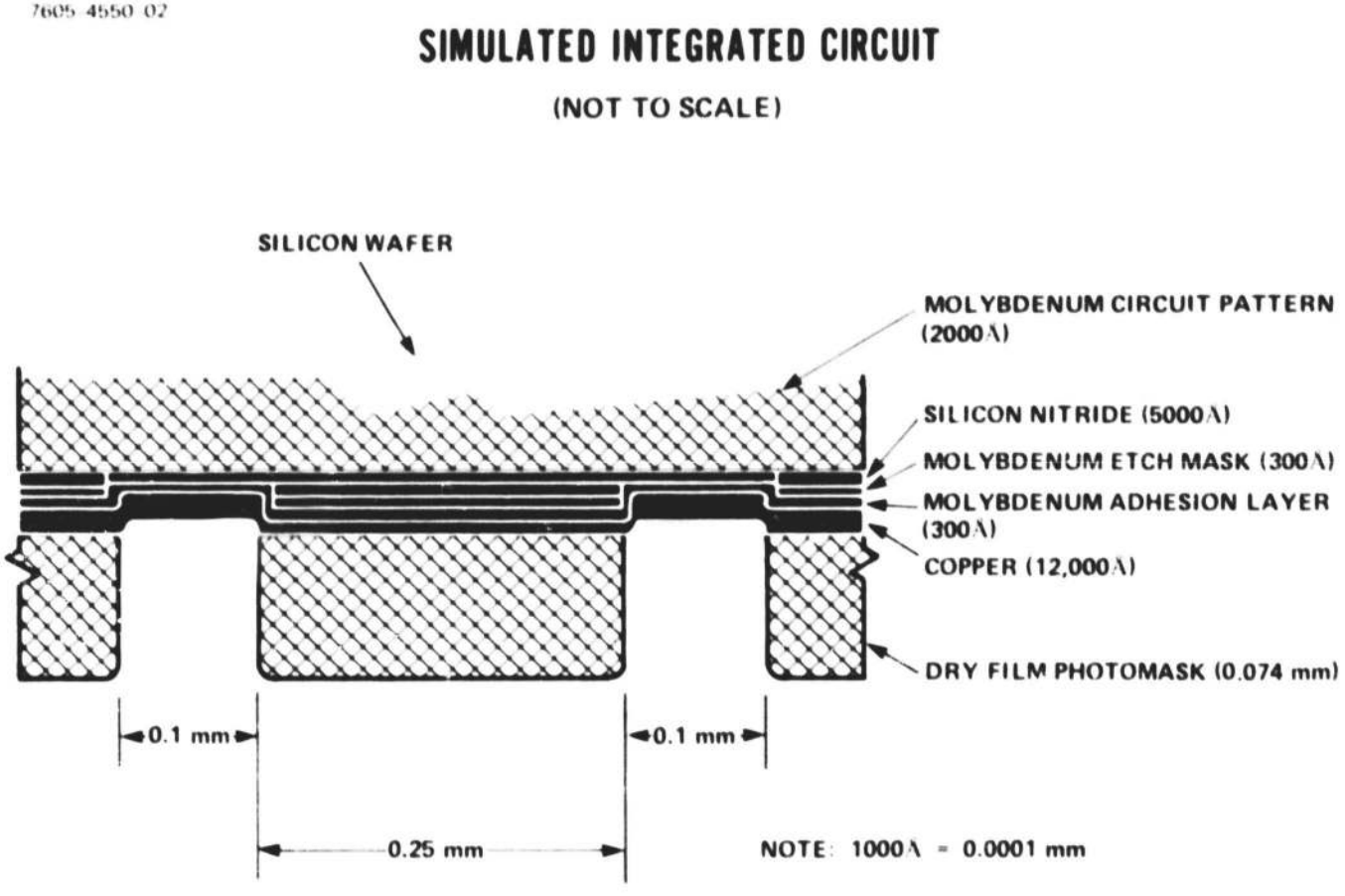


Figure 12. Base Metallization and Photomask Cross-Section

For proper printing, two parameters are important:

- o A well-collimated light source, and proper mask contact.
- o A correct exposure time-intensity product.

A standard Kasper mask aligner/printer will provide satisfactory light collimation and mask contact. Correct exposure time-intensity must be determined empirically, for proper exposure.

Proper development is critical in opening satisfactory windows. It is absolutely necessary that spray development be used, such that a fine, high velocity spray of developer is directed perpendicular to the surface of the photomask. It has been suggested that air injected into the spray system might atomize the spray to improve fine line definition further.

A photograph of the base metallization with the laminated dry film photomask is shown in Figure 13.

2. Bump Formation Process

a. Preplate Process Procedure

The preplate process procedure is given in Appendix III.

Rigorously clean window areas are required for good bump adhesion. Even though high resolution optical microscopy and electron microscopy did not show organic contamination on the floor of the dry film photomasked surface, it was found that further cleaning was required in order to achieve satisfactory bump adhesion. This cleaning was done by immersing the wafers in a glow discharge within a vacuum

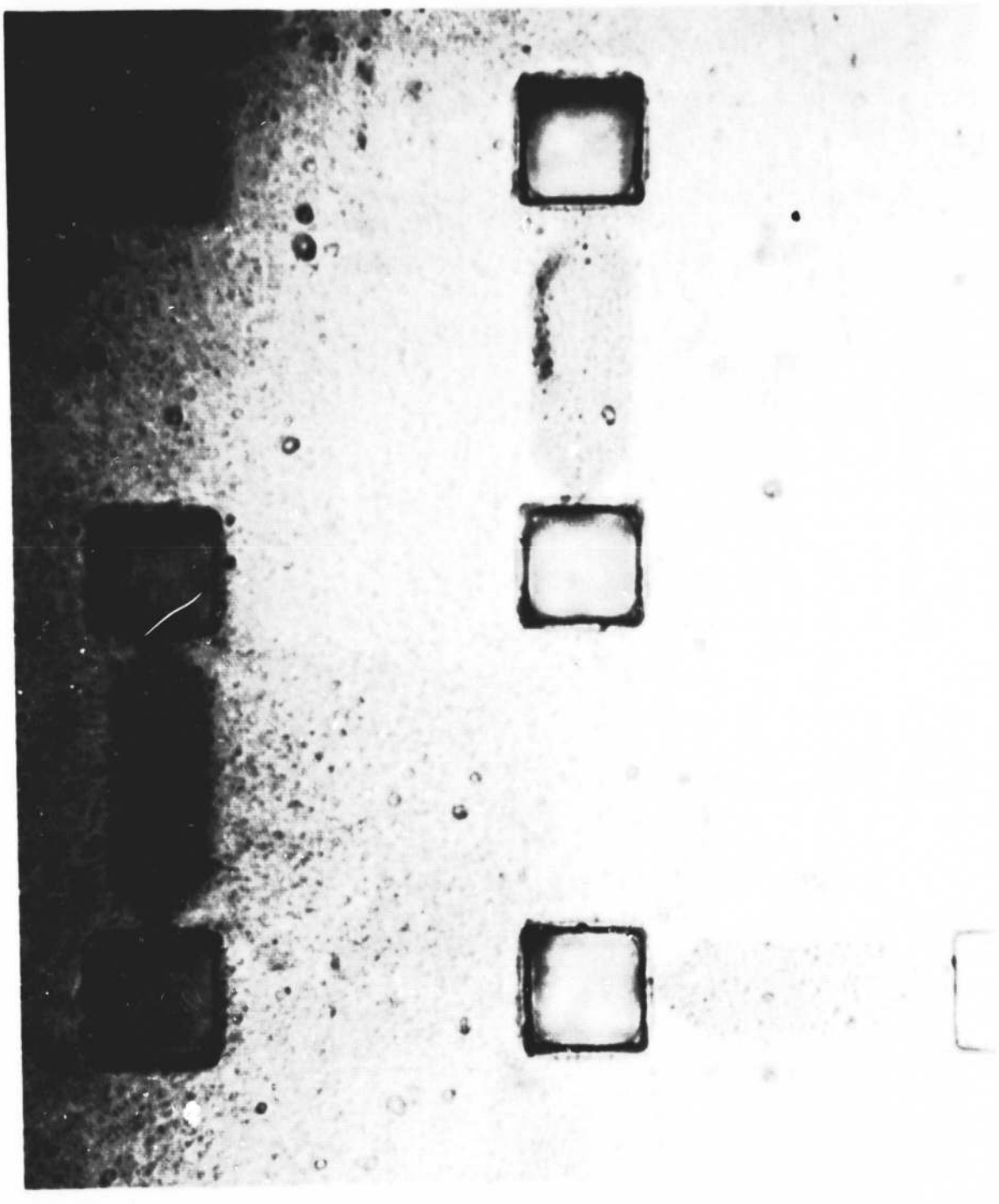


Figure 13. Base Metallization and Photomask Photograph Simulated Integrated Circuit Chips

chamber for about 15 minutes. A single spring-loaded edge clamp to each wafer suspended the wafers vertically within the vacuum system, with the photomasked surface directed toward the glow discharge source, and provided the electrical connection to maintain the wafers at ground potential.

A great deal of attention was paid to plating thickness uniformity across the surface of the wafers, as determined by measurements obtained by cross-sectioning bumps located at different points on the wafers.

At first, satisfactory uniformity was not obtained. Special techniques such as the addition of a concentric plating ring mounted around the periphery of the wafers only served to amplify plating thickness nonuniformity.

Finally, it was found that satisfactory uniformity was best obtained with no special fixturing at all, but by masking off the edges of the wafers.

Apparently, since 95% of the surface area of the wafer is masked off by photoresist, and since the approximately 10,000 windows measuring 0.1mm x 0.1mm are well distributed, on the average, across the surface of the wafer, the electric field within the plating bath is very uniform across the surface of the wafer when only the window areas are exposed.

In spite of the small surface area presented by the edge of the wafer, it seems to be quite important to mask off these edges, as provided in Appendix III, Step A-2. This masking off of the wafer edges results in excellent bump uniformity.

Application of tape to the back surface of the wafer prevents any plating on that surface.

The final steps outlined in the Preplate Procedure activates or prepares that surface for plating.

b. Gold/Lead/Silver Solder-Bump Procedure

(1) General process sequence

The general process sequence for applying gold/lead/silver solder-bumps to wafers is as follows:

(a) Clean the window areas for good bump adhesion.

(b) Electroplate nickel (0.025mm thick).

(c) Electroplate copper (approximately 1 micrometer thick).

(d) Electroplate silver (1.7 to 2.25 micrometers thick).

(e) Electroplate gold (2.3 to 2.95 micrometers thick).

(f) Electroplate lead (0.045 to 0.046mm thick).

(g) Strip away the plastic resist film.

(h) Etch away the interconnecting copper film.

(i) Alloy the gold/lead/silver solder (60 seconds at 350°C in a forming gas or nitrogen atmosphere).

(j) Etch away the interconnecting molybdenum film.

(k) Plate conversion gold (2500 angstroms thick).

(l) Clean the wafer.

The overall solder composition corresponding to the thicknesses and tolerances given in steps (d) through (k) above translates to 10-12% gold: 84-87% lead: 3-4% silver by weight. Each bump, when completed, measures approximately 4 mils x 4 mils x 3 mils high (0.1 mm x 0.1 mm x 0.075 mm high).

(2) Electroform Procedure

The electroform procedure for gold/lead/silver solder-bumps is given in Appendix IV, Section A.

In this procedure, it is important that the steps shown be performed in succession in a single working day, from the chemical activation of the plating surface as described in the final steps of Appendix III to the completion of the electroforming procedure, keeping the surfaces to be plated continuously wet with the appropriate chemical solution during the process.

The total plating surface area for the bump windows is quite small. For the 5 cm diameter wafers, with approximately 10,000 bump windows, the total plating area corresponds to only about 1 cm^2 per wafer, which is equivalent to a single opening 1 cm x 1 cm in area. In this work, total effective plating area was maintained at about 6.4 cm^2 per wafer, taking into account all plating surfaces, including the clip used to make electrical connection to the wafer.

Because of the small total surface area of the contact pads, plating current control, and therefore plating rate and thickness control, is conveniently obtained by using a low current regulated power supply.

It was difficult to reproducibly maintain the 10-12 gold: 84-87 lead: 3-4 silver relative composition. The target tolerance windows are as follows:

Metal	Total Thickness Tolerance	Relative Thickness Tolerance
Gold	0.625 micrometers	23.7% (or ± 11.8%)
Silver	0.55 micrometers	27.8% (or ± 13.9%)
Lead	1.25 micrometers	2.8% (or ± 1.4%)

It was easy to maintain the required thickness tolerances of the gold and silver layers, but the lead thickness tolerance was very difficult. In some cases, prior to stripping the photoresist, the exposed lead was back-etched in a solution of 2 parts glacial acetic acid + 1 part hydrogen peroxide (30%) at room temperature for thickness adjustment.

(3) Postplate Procedure

The postplate procedure for gold/lead/silver solder-bumped wafers is given in Appendix V, Section A.

Some comment might be made regarding the alloying of the gold, lead, and silver layers to form gold/lead/silver solder (step V-A-3). Although the rate of dissolution and diffusion of gold and silver into molten lead at 350°C was not investigated, optical observation of bump cross sections clearly showed that the alloying was complete. Cross sections of unalloyed bumps clearly showed the gold, silver, and copper layers, while cross sections of alloyed bumps showed that the copper layer remained intact, but with no evidence of the gold and silver layers. However, although these observations showed that all of the gold and silver had alloyed, it was not proven that the final bump was completely homogeneous in composition.

The copper layer, whose function is to assure adhesion of the solder to the nickel pedestal, measured approximately 1 micrometer thick both before and after the alloying at 350°C for 60 seconds.

The plating time for step V-A-5, the plating of conversion gold over the alloyed bumps, is shown as 5 minutes rather than the 20 minute plating time actually used in processing these wafers.

Using the manufacturer's data, a 20-minute plating period was used in processing these wafers. However, subsequent cross-section measurements showed the gold thickness to be approximate / 7500 angstroms rather than the intended 2500 angstroms. Accordingly, this plating time has been corrected in Appendix V, to give a plating thickness of approximately 2500 angstroms.

c. Indium/Lead/Silver Solder-Bump Procedure

(1) General Process Sequence

The general process sequence for applying indium/lead/silver solder-bumps to wafers is as follows:

(a) Clean the window areas for good bump adhesion.

(b) Electroplate nickel (0.025mm thick).

(c) Electroplate copper (approximately 1 micrometer thick).

(d) Electroplate lead (0.0336mm thick).

(e) Electroplate indium (0.0173mm thick).

(f) Electroplate silver (6900 angstroms thick).

(g) Plate conversion gold (500 angstroms thick).

(h) Strip away the plastic resist film.

(i) Etch away the interconnecting copper film.

(j) Etch away the interconnecting molybdenum film.

(k) Clean the wafer.

The overall solder composition corresponding to steps (d) through (f) above translates to 24.6 indium: 73.9 lead: 1.5 silver by weight. Each bump, when completed, measures approximately 4 mils x 4 mils x 3 mils high (0.1 mm x 0.1 mm x 0.075 mm high).

(2) Electroform Procedure

The electroform procedure for indium/lead/silver solder-bumps is given in Appendix V, Section B.

Comments made in the discussion of the electroform procedure for gold/lead/silver solder-bumps applies here also, with the exception of those made regarding composition control.

The ± 10% tolerances of the lead, indium, and silver layer thicknesses were convenient to maintain.

The very thin gold layer, applied to inhibit silver surface tarnishing, is applied using a conversion plating solution. This plating takes place by means of a replacement reaction, and so is self-limiting in thickness buildup.

(3) Postplate Procedure

The postplate procedure for indium/lead/silver solder-bumped wafers is given in Appendix V, Section B.

d. Fluxless Solder-Bump Cross-Section Schematics

Fluxless solder-bump cross-sections are depicted in Figure 14, for both gold/lead/silver and indium/lead/silver solder-bumps. The upper two figures correspond to the bumps at the completion of the electroform procedures. The lower two figures corresponds to the bumps at the completion of the postplate procedures.

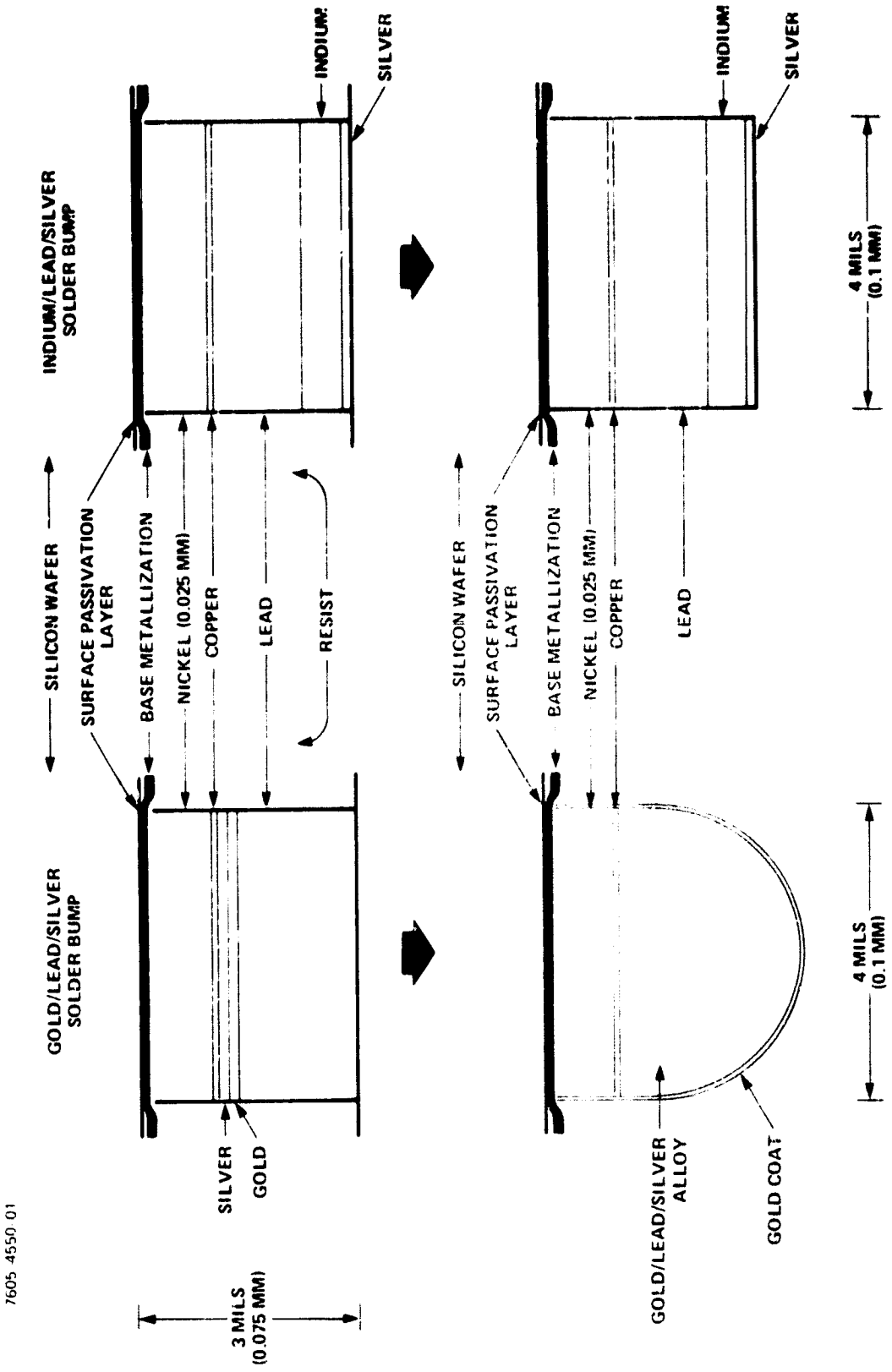


Figure 14. Fluxless Solder-Bump Cross Sections

3. Device Separation

The bumped wafers were separated into individual chips by means of wafer sawing.

The wafer sawing procedure used is described in Appendix VI.

A photograph of a sawed simulated IC chip is shown in Figure 15.

B. Complementary MOS Integrated Circuit Chips

1. Base Metallization and Photomask

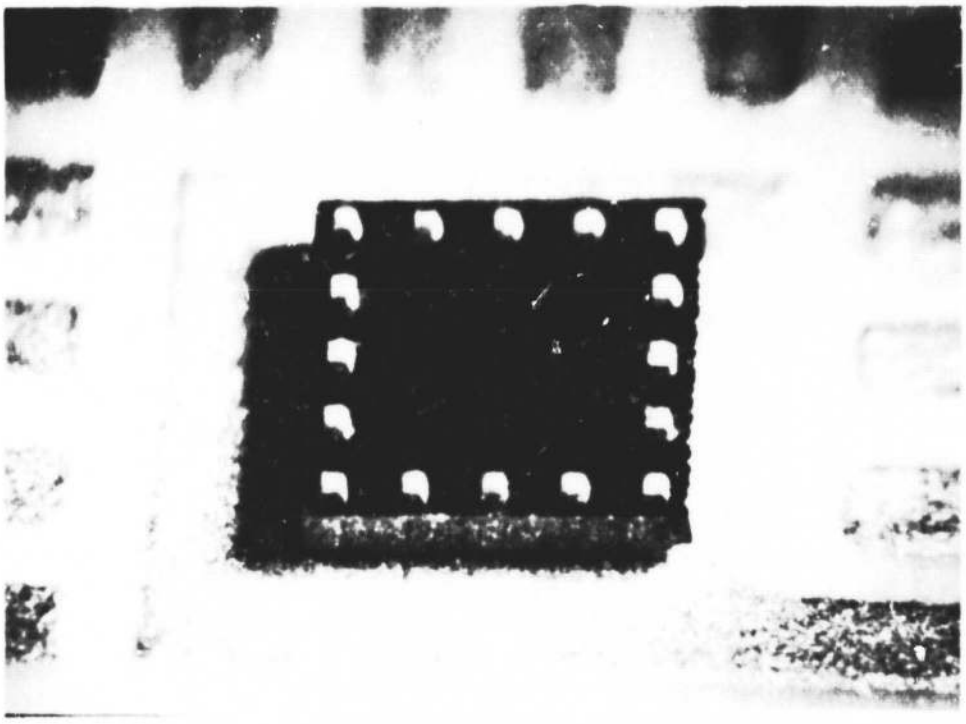
a. Application of the Base Metallization

Prior to the deposition of the base metallization, the wafers were cleaned according to the following sequence:

- Methanol rinse (nanograde)
- TCE liquid rinse (nanograde)
- TMC vapor immersion
- Methanol rinse (nanograde)
- D.I. water rinse
- Methanol rinse (nanograde)
- TMC vapor immersion

The base thin-film metallization applied was as follows:

(1)	Chromium	250 Å
(2)	99% Aluminum: 1% Copper	5000 Å



**SOLDER BUMPS ON
SIMULATED IC CHIP**

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Figure 15. Solder Bumps on Simulated IC Chip

(3)	95% Nickel : 25% Cobalt Alloy	2500 Å
(4)	Copper	2500 Å
(5)	75% Nickel : 25% Cobalt Alloy	1000 Å
(6)	Copper	2500 Å

These metals were vacuum-evaporated from hot filament sources in order to minimize static charge effects. The nickel/cobalt alloy was evaporated from an alumina-coated filament, the chromium and copper from tungsten filaments, and the aluminum from a tantalum filament.

A quartz crystal microbalance was employed for film thickness monitoring. Wafer temperature at the initiation of film deposition was approximately 150°C.

In this base metallization proceaure, the purpose of applying a thin base layer of chromium is to help assure good adhesion. The function of the aluminum layer is to serve as a metal diffusion buffer between the base aluminum device metallization and the nickel pedestal. This layer also prevents the chromium from becoming oxidized, which would make the chromium difficult to etch. The addition of copper impurity to the aluminum serves to strengthen the aluminum.

Nickel/cobalt alloy deposits with very little film stress, in contrast with the behavior of pure nickel or pure cobalt. High deposited film stress would distort or fracture the wafer.

The intermediate copper film serves as a plating base. Copper is a good plating base because it is easy to clean.

The top two layers permit the base of the photomask windows to be cleaned by means of selective etching, prior to electroforming bumps, for good bump adhesion. These top two layers do not become a part of the final bump structure. Aluminum could have been used as the uppermost layer in place of copper.

Of course, these metal layers also provide the electrical contact required for the electroforming of bumps.

Thus, four source materials are required to deposit the base metallization. Four sources are easily accommodated in most vacuum systems.

A cross-section of the base metallization (not to scale) is shown in Figure 16.

b. Application of the Photomask

The CMOS wafers were then laminated with Riston 30S dry film resist (approximately 0.074mm thick), and windows were opened through the resist at the contact pad areas.

The dry film photomask application process is given in Appendix II. This is the same process used for the simulated integrated circuit wafers. Special precautions were not taken to protect the wafers from static charge effects when applying this photomask, because at this point all sources, drains, and gates are shorted together by the base metallization layer applied prior to this step. However, it is known that during ordinary dry film processing, considerable static charge is generated when the polyethylene film is removed from the resist just prior to lamination, and again when the mylar film is removed just prior to pattern development.

The critical parts of the dry film application process were mentioned in Section VI-A-1-c above, and need not be repeated here.

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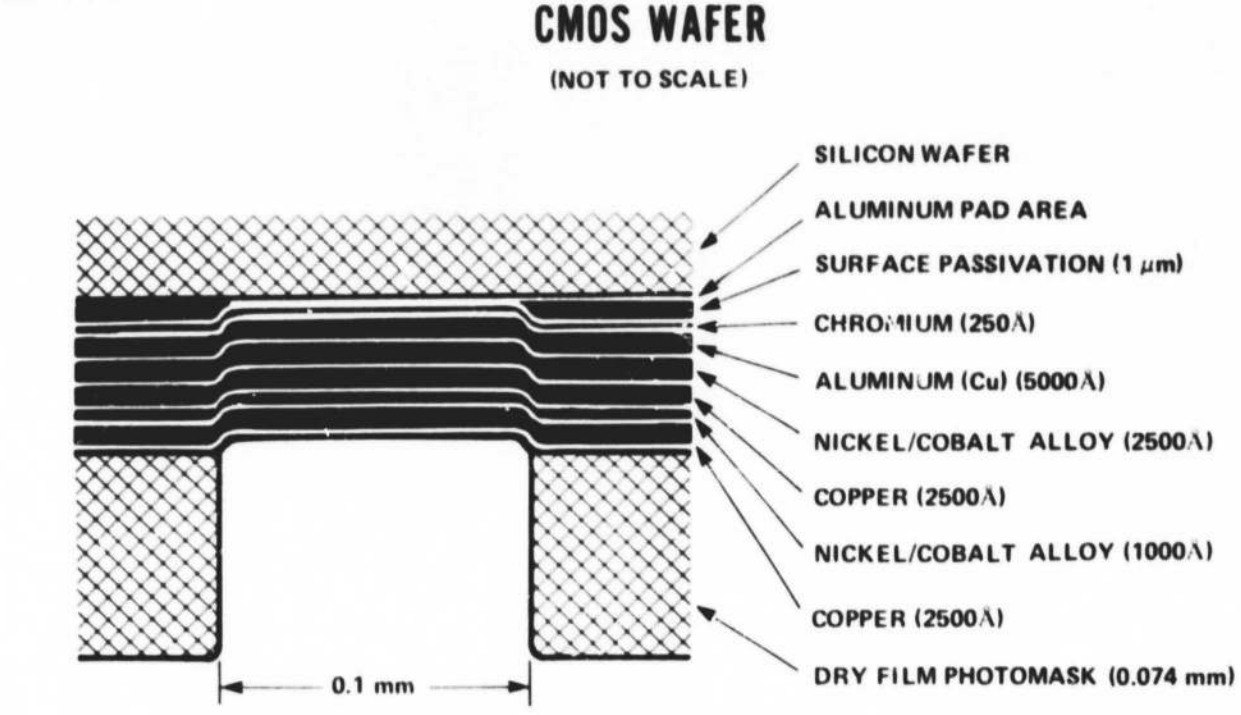

NOTE: 1000Å = 0.0001 mm

Figure 16. Base Metallization and Photomask Cross Section

2. Bump Formation Process

a. Preplate Process Procedure

The preplate process procedure is given in Appendix VII.

In Appendix VII-A, Step 2 permits good plating uniformity to be achieved. Steps 3 and 4 provide clean window areas. Steps 5 and 7 prepare the copper surface for plating.

b. Electroform Procedure

The electroform procedure is given in Appendix IV.

It is identical to that employed for simulated integrated circuit wafers. The comments made in Sections VI-A-2-b-(1) and (2) and VI-A-2-c-(1) and (2) above apply here as well.

c. Postplate Procedure

The postplate procedure for CMOS wafers is given in Appendix VIII.

d. Flux less Solder-Bump Cross-Section Schematic

The fluxless solder-bump cross-sections are depicted in Figure 14.

3. Device Separation

The bumped wafers were separated into individual chips by means of wafer sawing.

The wafer sawing procedure is described in Appendix VI.

VII. ASSEMBLY TO THICK- AND THIN-FILM SUBSTRATES

A. Substrate Materials and Interconnect Patterns

1. Interconnect Patterns

Two basic circuit patterns were generated, and are shown in Figure 17. In each case, actual substrate size is 2.54cm x 1.27cm.

In the first circuit, two flip-chip die are mounted on each substrate. A "finger" pattern consisting of 32 individual traces extends inward from the edge of the substrate to each bonded flip-chip bump, thus allowing easy probing for continuity checking after flip-chip bonding and environmental testing.

In the second circuit, eight flip-chip die are mounted on each substrate. The interconnection pattern is such that the series continuity of each bonded flip-chip device can be examined, as well as the continuity of all eight bonded flip-chip die in series (128 bonded interconnections). This pattern also provides for probing for continuity checking after bonding and after environmental testing.

2. Substrate Materials

Both of the above interconnect patterns were fabricated from both thick-film and thin-film conductive materials, as follows:

a. Thick-film

(1) Metallization Material - ESL 8835-1B low frit gold, approximately 15 micrometers thick.

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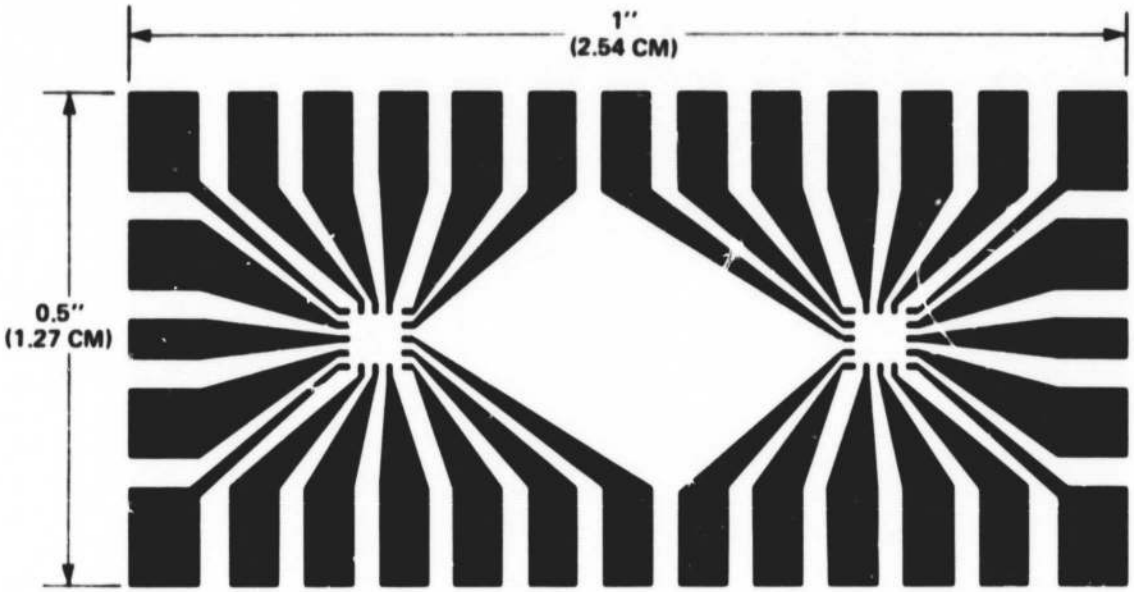
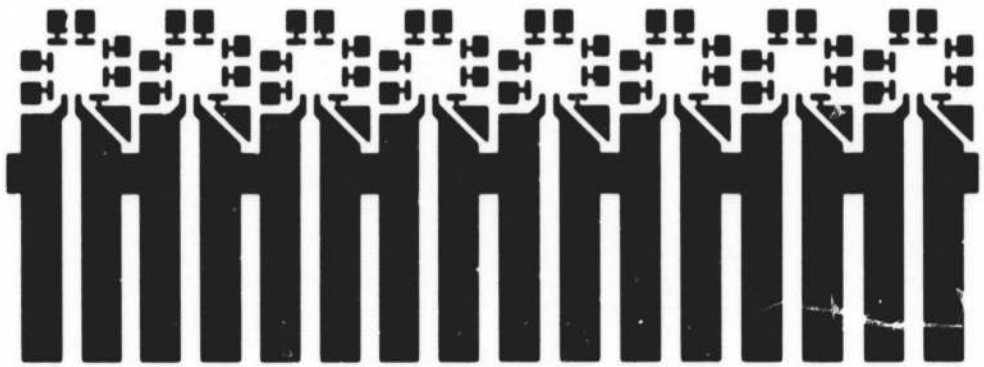


TWO-CHIP
SUBSTRATE METALLIZATION PATTERN



EIGHT-CHIP
SUBSTRATE METALLIZATION PATTERN

Figure 17. Thick and Thin Film Interconnect Patterns

(2) Substrates - 96% alumina with a 1.25 micrometer surface finish. 99.5% alumina with a 0.1 micrometer surface finish (as-fired).

(3) Processing - Standard thick-film print and fire.

b. Thin-film

(1) Metallization Material - 6 micrometers sputtered gold over 750 Å of sputtered molybdenum.

(2) Substrates - 99.5% alumina with a 0.1 micrometer surface finish (as-fired).

(3) Processing - Standard thin-film photolithography.

B. Attachment Processes

Basically, fluxless solder-bump bonding takes place first by means of an ultrasonic tack, using the simultaneous application of ultrasonic energy and pressure at the bonding interface for primary attachment, followed by solder reflow of the solder-bumps to form the final bond.

As part of this evaluation program, many possible bonding schedules were investigated. Many different bonding schedules work satisfactorily.

However, two particular bonding schedules were identified which seem to work well for both solder-bump materials:

- gold/lead/silver solder-bumps
- indium/lead/silver solder-bumps

as well as for both types of bonding pads:

- o thick-film gold bonding pads
- o thin-film gold bonding pads.

Further bonding optimization probably could have been achieved by development of four or eight custom bond schedules, but it was believed that more consistent comparative data might be obtained with as few schedules as possible.

These fluxless solder-bump attach methods were as follows:

1. Equipment

   Hughes Model 2906 Ultrasonic Bonder equipped with hot stage and nitrogen blanket.

2. Method I

Ultrasonic Energy	High Power Setting (1)
Scrub Time	260 ms
Clamping Force	150 gm
Hot Stage Temperature	250°C

3. Method II

Ultrasonic Energy	High Power Setting (1.0)
Scrub Time	380 ms
Clamping Force	120 gm
Hot Stage Temperature	183°C
Subseqeunt Bump Reflow in Nitrogen or 90% N_2/10% H_2	
Reflow Furnace Temp.	300°C

Using Method I, both gold/lead/silver and indium/lead/silver solder-bumped chips were attached to thick-film gold pads and thin-film gold pads.

The same was also done using Method II. It is believed that a 300°C. reflow temperature was needed for Method II because the gold bump overcoat on the gold/lead/silver bumps was applied to a thickness of approximately 7500 angstroms rather than the desired 2500 angstroms. The higher temperature was then required to alloy the higher concentration of gold into the gold/lead/silver bumps. If the gold overcoat thickness had been 2500 angstroms, a 250°C. reflow furnace temperature should have been adequate.

As it turned out, more chips were attached using Method I than for Method II.

In this program, a Hughes Model 2906 ultrasonic bonder was used, although this machine is no longer in production. However, the Unitek Corporation (Monrovia, CA) does offer a current production machine, Model #8-149-01-02 Flip-Chip Bonder, suitable for either ultrasonic or thermocompression bonding. Both the Hughes and the Unitek machines feature a dual-view mirror system, which permits the operator to orient the chips face-down on the mirror, and yet view the face of the chip for proper orientation for manual bonding. The chips are manipulated from their back side by means of a vacuum chuck.

The ultrasonic attachment process is simultaneously dependent upon the following parameters: hardness of the solder, clamping force (pressure), ultrasonic vibration frequency and amplitude, dimensions of the bumps, number of bumps, hardness of the bonding pad, the metallurgical nature of the bonding interface, the surface characteristics of the bonding interface, and the temperature of the bonding interface.

Subsequent solder reflow, when employed, was done in a tube furnace in a nitrogen or forming gas atmosphere.

No flux whatsoever was used in any part of these bonding processes.

To demonstrate solder reflow temperature latitude, both gold/lead/silver-bumped devices and indium/lead/silver-bumped devices, bonded to gold pads, were stored in a furnace at 350°C for one hour. No evidence of gold bond pad leaching was observed on the basis of bond shear tests and visual observation of the sheared bond area.

VIII. BOND QUALITY AND RELIABILITY

A. Introductory Discussion

The bond quality and reliability of fluxless solder-bumped simulated integrated circuit chips, bonded to thick- and thin-film gold pads, were tested. The environmental test conditions were:

- o 10,000 G and 15,000 G centrifuge.
- o 10 temperature cycles from -65°C to +150°C .
- o High temperature storage at +150°C up to 800 hours.

Testing consisted of:

- o visual examination and characterization
- o electrical continuity measurements
- o bond shear strength measurements (destructive).

Both gold/lead/silver and indium/lead/silver solder-bumped devices were tested. An advantage of evaluating bumps of two different solder compositions is that a comparison between two different sets of data might be made, which could help clarify the meaning and the implications associated with that data.

All of the simulated IC solder-bumped chips tested were taken from a single gold/lead/silver-bumped wafer and a single indium/lead/silver-bumped wafer.

Over 1000 solder-bumped chips were tested.

The bond interface visual characteristics are best examined by viewing the edge of the chip through a microscope (i.e., with the substrate turned on it's side, such that one can look at or through the space between the bonded chip and the substrate). Viewed in this manner, the bond itself can readily be seen. The bonded bump looks like an unbonded bump with the exception of a slight widening at the substrate interface which looks much like a liquid meniscus. The appearance of this meniscus is a good indication of proper wetting, and thus of good bonding.

Electrical continuity was measured by means of a two-point probe and a digital ohmmeter.

Bond shear strengths were measured with a calibrated hand-held shear tester.

B. Centrifuge

All of the bonded devices which were environmentally tested were first subjected to 10,000 and 15,000 G tensile centrifuge in a Centrisafe centrifuge machine. The results were as follows:

- o No chip debonded.
- o No change in
  - Visual appearance.
  - Electrical continuity.
  - Bond shear strengths.

This result is perhaps not surprising. The bumped chip weighs only about 0.15 milligrams. Thus, 10,000 G's would exert only about 15 grams of tensile force on the chip, or less than one gram per bump. 15,000 G's would exert about 1.5 grams per bump. However, typical bond shear strengths (which roughly approximate tensile strengths) average in the neighborhood of 10 grams per bump. Thus, 10,000 to 15,000 G's is not sufficient to affect the bond.

C. Thermal Cycle

Thermal cycle conditions were 10 cycles, from -65°C to +150°C, with a 15 minute dwell. An automatic Blue M thermal cycling oven was used.

The results were as follows:

Bump Material	Attach Method	Average Shear After Bond	Average Shear After Temperature Cycle
Indium/lead/silver	1	240 grams	200 grams
Indium/lead/silver	2	180 grams	170 grams
Gold/lead/silver	1	160 grams	145 grams
Gold/lead/silver	2	145 grams	135 grams

Both immediately after bonding and after thermal cycle, the bonds were examined visually and electrical continuity was tested.

After thermal cycling, there was no change in visual appearance or in electrical continuity for any of the bonded devices.

Thermal cycling tests the ability of the solder to accommodate any difference in thermal coefficient of expansion between the flip-chip part and the substrate.

The thermal coefficient of expansion of 99.5% alumina is 6.6×10^{-6} per C°. ; that of silicon is 2.6×10^{-6} per C.° Thus, the magnitude of the disparity is 4.0×10^{-6} per C.° Thus, for a silicon chip measuring 5mm on a side (7.07mm diagonally), and for a total temperature excursion of 315°C.(i.e., +250°C. bonding temperature, low temperature swing of -65°C.), the total worst case displacement would be about 0.0089mm diagonally, which corresponds to a relative displacement of approximately 0.0044mm for each diagonal bump. This is to be compared to a typical bump width of approximately 0.1mm. However, soft bumps relax after cooling to room temperature following bonding. As a result, when

temperature cycling from -65°C. to +150°C., the effective relative displacement would correspond to only about 0.003mm for each diagonal bump (which is worst-case), for the example discussed above, which amounts to about 1.5% of the bump width. Soft solders can readily accommodate displacements of this small magnitude.

Flip-chip bumps are, of course, increasingly compliant as bump height is increased.

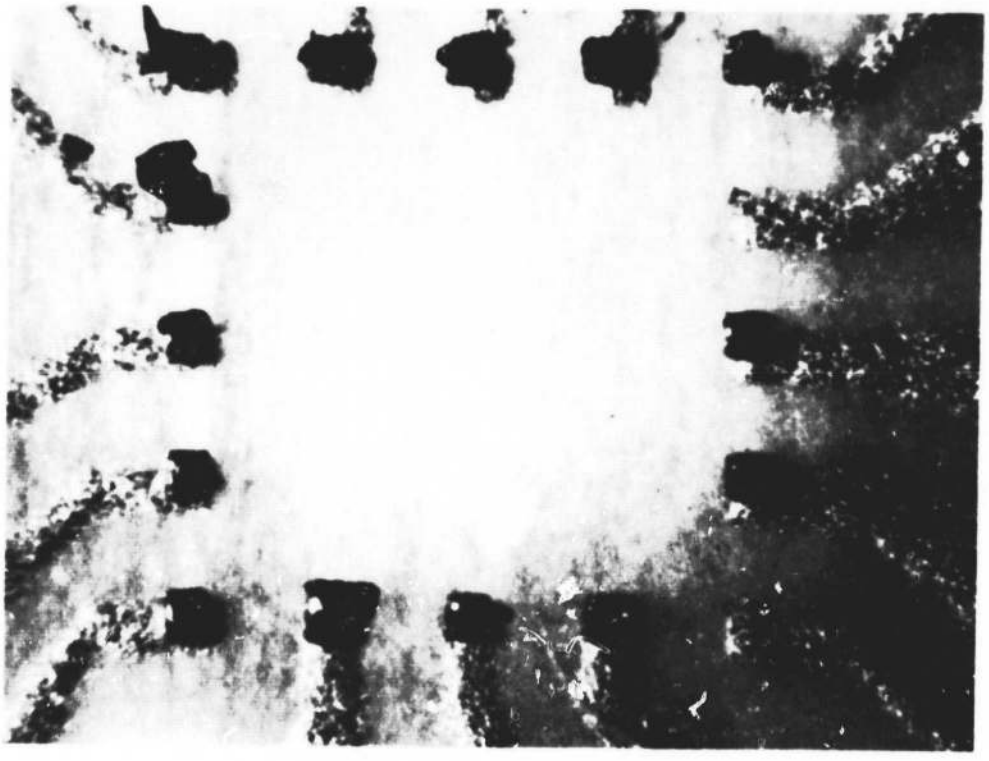
The more ductile solders are well able to withstand temperature cycling without damaging either the solder joint or the semiconductor chip, for the bump dimensions and solder-bump materials used here.

Thick- and thin-film substrate bonding pads after device shear tests are shown in Figures 18 and 19. The bonds shear either at the silicon surface, at the solder/pedestal interface, or at the bonding pad. The first two shear modes show up well on the photographs, but the separation at the bonding pad does not. Under proper illumination, the footprint at the bonding pad shows up very well as an alloyed area.

D. High Temperature Storage

Bonded devices were stored at +150°C. in a circulating hot air oven. Periodically, the bonded devices were removed from the oven, visually inspected, electrically tested, and a number of the bonded devices were destructively shear-tested. The remaining devices were then returned to the oven.

These bonded devices were destructively shear-tested at 0 hours, 48 hours, 194 hours, 500 hours, and 800 hours. The results are shown in Figure 20.



THICK FILM Au SUBSTRATE METALLIZATION AFTER DEVICE SHEAR TESTS

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Figure 18. Thick Film Au Substrate Metallization After Device Shear Tests

THIN FILM Mo/Au SUBSTRATE METALLIZATION AFTER DEVICE SHEAR TESTS

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Figure 19. Thin Film Mo/Au Substrate Metallization After Device Shear Tests

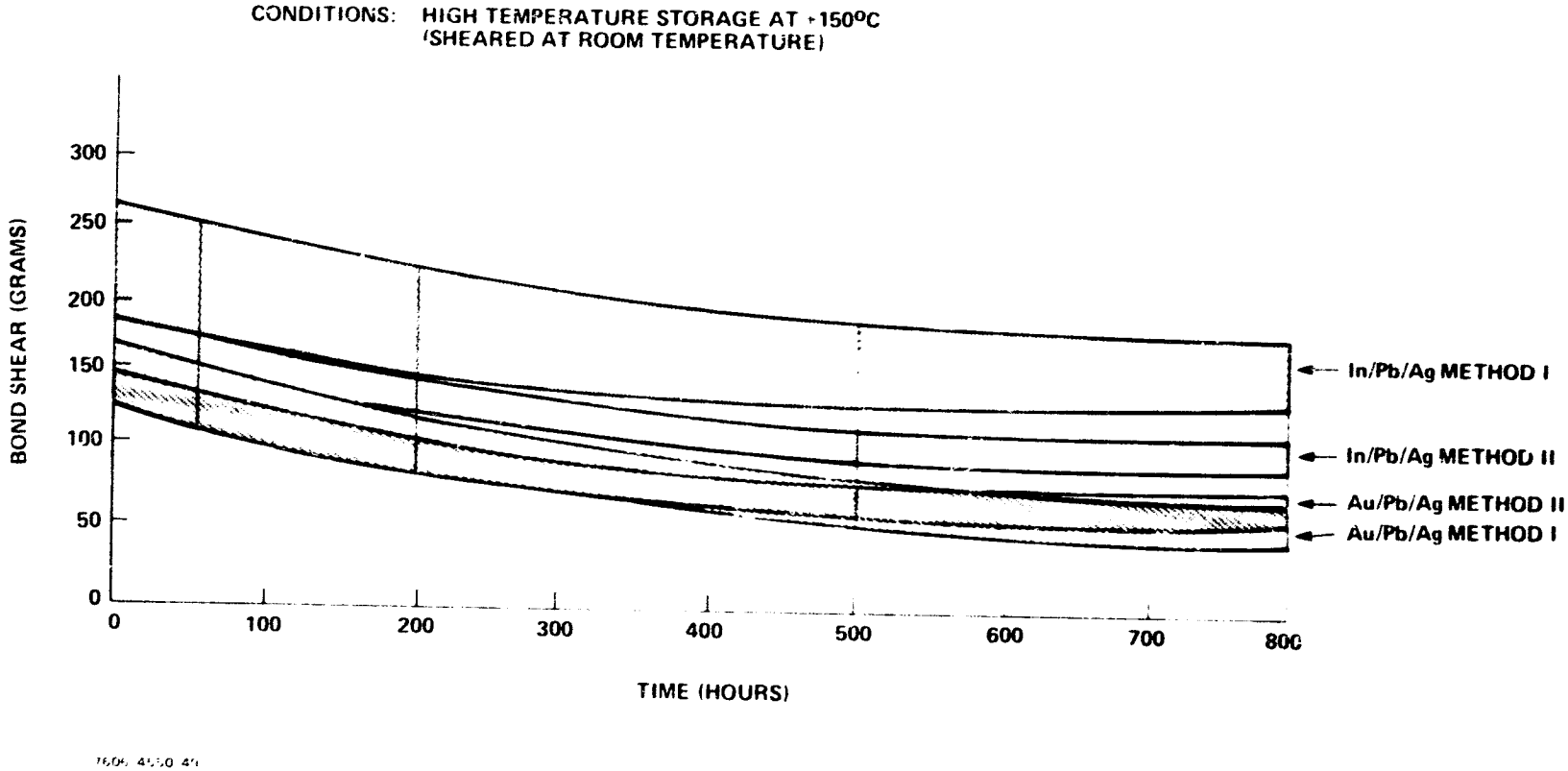


Figure 20. High Temperature Storage (Thick- and Thin-Film Gold)

This graph combines the data for both thick-film gold substrates and thin-film gold substrates, because no appreciable difference in bond shear strengths could be seen for thick- and thin-film gold bonding pads.

However, there is a difference for the two solder alloys and for the two bonding methods.

It is believed that the poorer result shown for the gold/lead/silver solder alloy is due to the overly thick gold overcoat which was applied over the bump - 7500 angstroms rather than the intended 2500 angstroms. This overly thick overcoat probably inhibited proper solder bump alloying to the bonding pads. It was observed that, during shear testing, most of the gold/lead/silver solder-bumps separated at the gold bonding pads, rather than shearing silicon.

After 800 hours at +150°C., the indium/lead/silver solder-bumped chips sheared at an average of about 160 grams and 100 grams, depending on method of attachment, while the gold/lead/silver solder-bumped chips sheared at an average of about 60 grams.

For the indium/lead/silver solder-bumps, after 800 hours there appeared to be some visual changes at the solder/pedestal interface, possibly associated with the intermediate copper layer.

In addition, the solder/bonding pad interface appeared to be somewhat more grainy for the aged indium/lead/silver solder joints. The visual appearance of these joints was somewhat similar to that found in the Indalloy #7 joining work reported in NASA TM X-64937 (Caruso & Honeycutt, "Investigation of Discrete Component Chip Mounting Technology for Hybrid Microelectronic Circuits").

There was little change in the visual appearance of the gold/lead/silver solder joints.

During the 800 hours of high temperature storage, electrical continuity test results were as follows (loss of a single electrical contact in a device was considered to be a failure):

Indium/lead/silver:	Method I -	0/160
	Method II -	1/128
Gold/lead/silver	Method I -	4/128
	Method II -	2/122

E. Concluding Discussion

These tests have shown that the bonded devices withstand centrifuge and thermal cycle very well.

The electrical continuity test data correlates with the bond shear strength trend in high temperature storage.

The gold/lead/silver-bumped chips showed a relatively high failure rate for electrical continuity. However, as discussed earlier, this result can probably be explained by the overly thick gold overcoat on these bumps, which probably inhibited proper solder alloying to the bonding pads.

IX. CONDUCTIVE EPOXY ASSEMBLY

A. Conductive Epoxy Attachment

Fluxless solder-bump flip-chips from the same lots being tested for ultrasonic attachment/solder reflow assembly as described above, were attached to thick-film gold pads by means of conductive epoxy in order to assess the feasibility of this type of interconnection. Attachment to thin-film gold pads by means of this technique would be considered a simpler, more straightforward assembly then for attachment to thick-film.

ESL 8835-1B low frit thick-film gold pads were used. The epoxy material was EpoTek H44 gold epoxy and H31D silver epoxy, applied by means of screening through a 200 mesh screen. The thickness of the screened epoxy was just under 25 micrometers.

The precious metal coating on the solder-bumps was expected to allow a good electrical contact to be made to the epoxy interface.

The chief problem experienced was associated with screening 0.1 or 0.125mm epoxy lines on 0.25mm centers using the EpoTek H44 gold epoxy material. Accordingly, the H31D silver epoxy was screened onto the bonding pads for this investigation.

For device manipulation, a K & S model 576 beam-lead bonder was used, but only for device placement using the vacuum pick-up feature for this bonder; no mechanical scrub was used. Following device placement, the epoxy was cured at 150°C for 45 minutes. Chips with both gold-coated gold/lead/silver solder-bumps and silver-coated indium/lead solder-bumps were bonded.

The contact resistance of an epoxy-bonded bump, measured with a 2-point probe, indicated a resistance of about 50 milliohm (uncorrected). However, since the probe contacts themselves would be expected to contribute about 50 milliohms of resistance,

it can be concluded that the contact resistance of the epoxy-bonded bump is negligible for microelectronic applications.

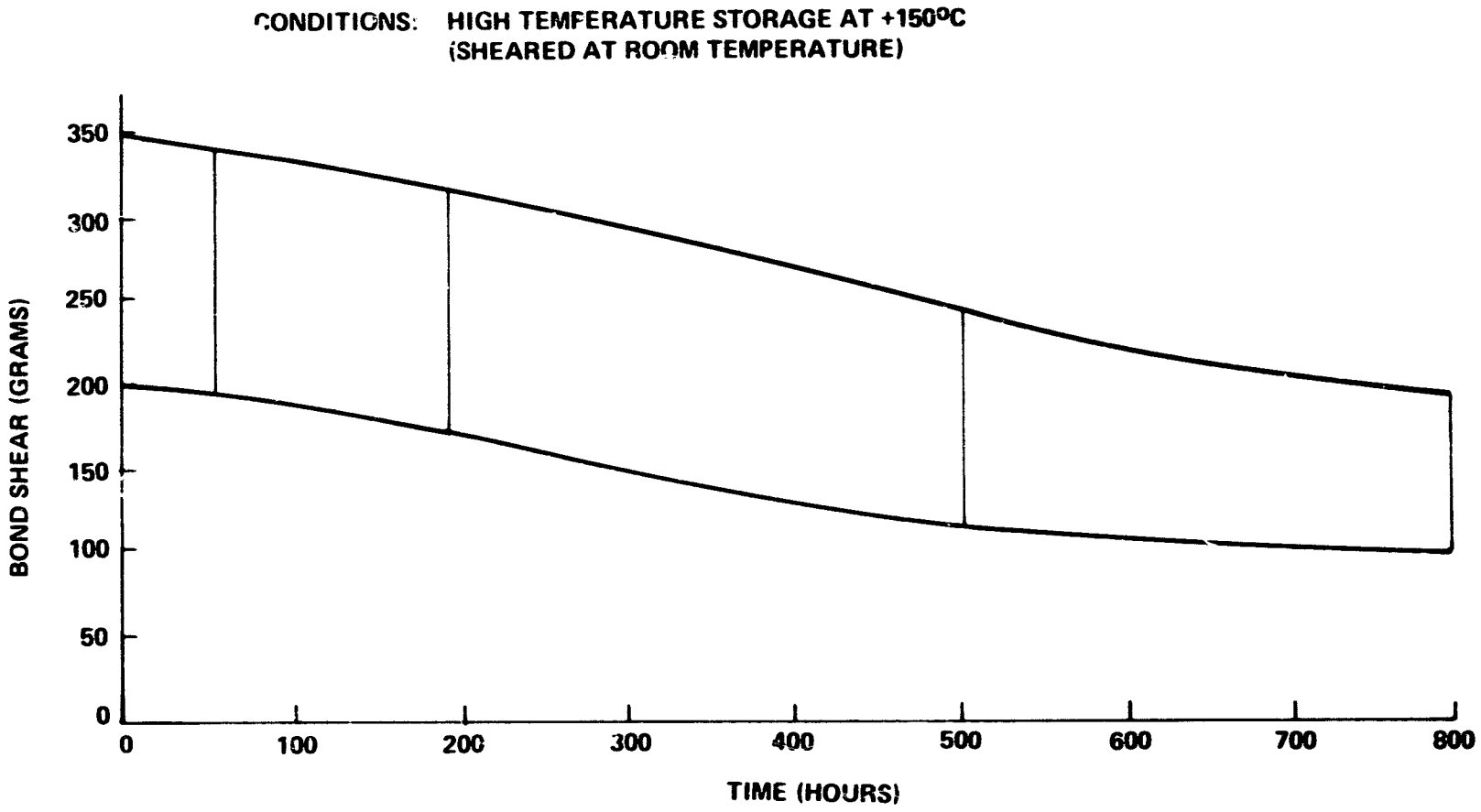
The epoxy-bonded chips were not affected by 10,000 G or 15,000 G centrifuge, and were negligibly affected by temperature cycling.

A limited number of chips were subjected to storage at +150°C., and samples were sheared at 0 hours, 48 hours, 194 hours, 500 hours, and 800 hours. The results are shown in Figure 21. Bond shear strengths are quite high, averaging more than 160 grams after 800 hours.

No electrical contact was lost to any of the chips tested up to 800 hours.

Thus, conductive epoxy attachment can be used as an alternative to ultrasonic/solder reflow attachment for these bumped devices.

To optimize the bumps for conductive epoxy attachment, it might be recommended that the bumps be designed to extend to the edge of the chip, or somewhat beyond the edge of the chip, to allow for easier, more accurate alignment during chip placement and improved visual inspectability after bonding. In addition, bumps 0.125 or 0.15 mm high would probably also be advantageous (formed with the aid of a double thickness of dry film resist), in combination with the bump extension to somewhat beyond the edge of the chip. Finally, the metallurgy of the bump could be modified somewhat. Although the fluxless solder-bump compositions work well, the bump metallurgy could be simplified if it is limited to conductive epoxy attachment. Such a simplified bump might consist of a nickel pedestal layer comprising the lower half of the bump, and a soft gold layer comprising the upper half of the bump.



/606-4550-80

Figure 21. Conductive Epoxy Attachment

B. Conductive Epoxy Bumps

A brief exploratory investigation was conducted to determine whether it might be possible to form conductive epoxy flip-chip bumps by means of squeegee application of the conductive epoxy into windows in thick dry film resist.

Riston 30S dry film resist was applied to a silicon wafer and a flip-chip bump photomask pattern was developed, consisting of an array of windows in the resist measuring 0.1mm x 0.1mm in area and approximately 0.074mm deep. H44 conductive gold epoxy was then applied to the photomask by means of a Presco thick-film printer. It was observed that the windows filled very nicely, but after about an hour some settling had occurred, such that the photomask cavities were not quite full. After the one hour settling period, H44 conductive gold epoxy was again applied by means of the squeegee, thus re-filling the openings, and the epoxy was cured at 125°C for 1.5 hours. When the photomask was stripped, it was observed that well-formed epoxy bumps, about 0.1mm x 0.1mm in cross-section and approximately 0.074mm high had been formed. Bump adhesion was poor in this experiment because no attempt had been made to clean out the windows before application of the epoxy material.

This technique was most impressive with respect to the speed and ease with which the bumps were formed.

Regarding the electrical resistance of epoxy bumps, a calculation shows that an epoxy bump, comprised of H44 gold epoxy and measuring 0.1mm x 0.1mm in cross-section and 0.15mm high, would have a resistance of 0.12 ohms. This is the same resistance as a 25.4m-diameter aluminum wire about 2.2mm long. This resistance is quite tolerable for almost all microelectronic applications. The electrical resistance of silver epoxy is, in general, less than that of gold epoxy. The electrical and thermal conductivities of the more highly conductive silver epoxies approximate those of the metal bismuth.

A candidate epoxy bump process sequence might be as follows:

1. Apply a thick-film photomask (0.1 to 0.15mm thick) to the wafer.

2. Clean the window areas.

3. Apply a vacuum-deposited thin-film coating over the wafer, coating the aluminum pad areas (e.g., chromium, aluminum, nickel/cobalt alloy, very thin gold).

4. Fill the window cavities with conductive gold or silver epoxy, using conventional thick-film printing equipment.

5. Cure the epoxy.

6. Strip the photoresist, and clean the wafer.

7. Saw the wafer into chips. Clean the chips.

8. Die attach using conductive epoxy.

The bumping procedure is shown in a cross-sectional schematic in Figure 22.

The purpose of the vacuum-deposited thin-film is to serve as a buffer between the aluminum device metallization and the conductive epoxy material.

Epoxy attach would be done by either screening conductive epoxy onto the bonding pads, or by means of an epoxy transfer technique, carried on the epoxy bumps.

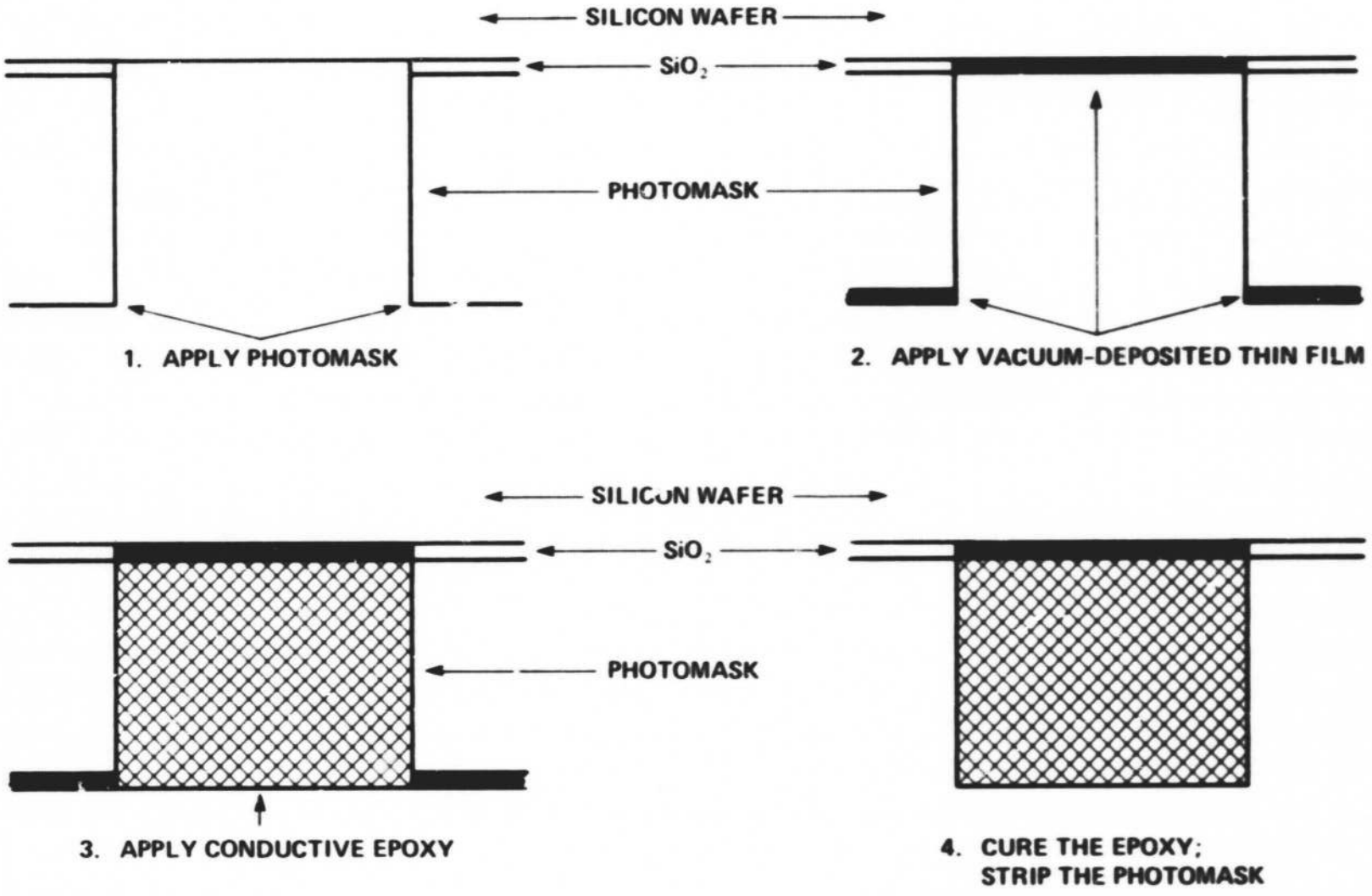


Figure 22. Conductive Epoxy Bumping Process

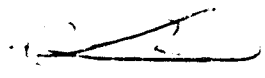
It is anticipated that the two chief problems to be resolved during such a process development program would be:

- o Cleaning of the window areas for good adhesion.
- o Protection from static charges during processing.

If the surface passivation oxide layer is not etched prior to resist application, both of the above might be solved in one step. The intact surface passivation layer would help protect the devices from any static charge, and clean window areas could be achieved by etching the windows in the surface passivation layer following development of the photomask (in Figure 22, after Step 1 and before Step 2). This procedure has the advantage that a photomasking step is eliminated; the passivation layer window etch mask is combined with the flip-chip bump mask.

If windows are already present in the oxide passivation layer, a duplex photomask might be employed to help with window cleaning and static protection; first, a thin-film of negative resist such as 747 or 752 applied by means of spinning, and then a thick dry film resist layer applied over the thin-film resist. A single printing and development would be done for both resist layers.

Since the dry film resist does not need to withstand alkaline plating solutions for epoxy bump processing, a semi-aqueous-soluble thick dry film resist might be employed, such as duPont M818, which develops more cleanly and easily. M818 is only 0.05mm thick, but a double or triple thickness could be used.



X. APPLICABILITY TO VARIOUS DEVICE TYPES

It was desired to demonstrate that fluxless solder-bump technology can be applied to several types of devices, including PNP, NPN, CMOS, SOS, etc.

Of these device types, MOS devices are by far the most sensitive to such processing because of their sensitivity to static electricity. Accordingly, CMOS wafers were chosen for processing as part of this program, to demonstrate applicability to the most demanding integrated circuits.

Three electrically-tested CMOS integrated circuit wafers were purchased from National Semiconductor, of the type shown in Figure 23.

The IC's are National Semiconductor MM4601 quadruple two-input NOR gates, as described in National's specification shown in Figure 24.

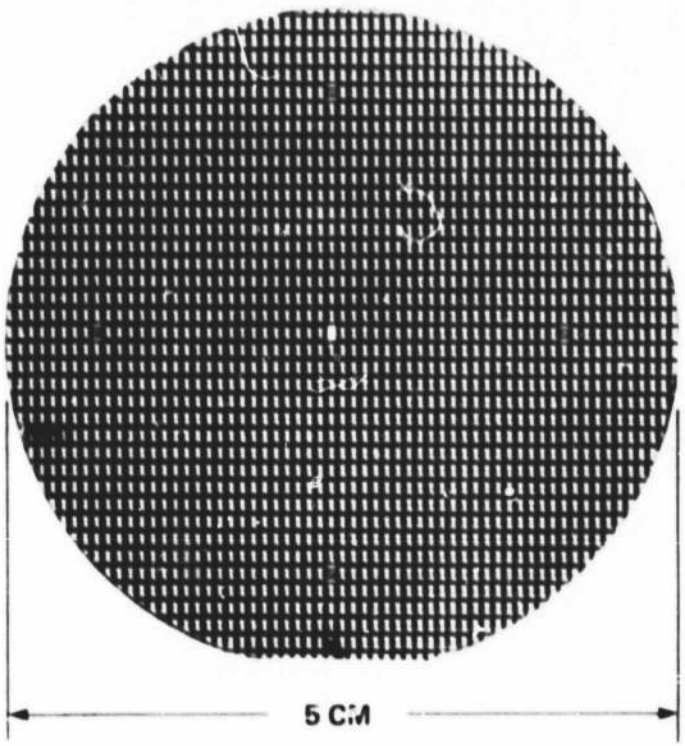
These CMOS IC devices each have 14 bonding pads, which are approximately 0.088 x 0.088mm in area. Device center-to-center spacing on each wafer is approximately 0.84mm x 1.32mm.

Before the CMOS wafers were cleaned they were photographed, because the cleaning process removes the ink present on the wafers which identifies those devices which are not electrically acceptable. This ink is readily soluble in methyl alcohol. After processing, the photographs were used to help identify electrically-good devices on the wafers.

Photographs of the wafers processed are shown in Figures 25, 26 and 27.

C-2

MM4601 QUADRUPLE TWO-INPUT NOR GATES



N AND P CHANNEL ENHANCEMENT MODE DEVICE (16 PER IC)
DEVICE CENTER-TO-CENTER SPACING:
0.84 MM × 1.32 MM (33 MILS × 52 MILS)
14 BONDING PADS PER IC

7605-4550-05

7520-242

Figure 23. CMOS Wafer

MM4601A/MM5601A quadruple two-input NOR gate

general description

The MM4601A/MM5601A is a monolithic complementary MOS (CMOS) quadruple two-input NOR gate integrated circuit. N and P channel enhancement mode transistors provide a symmetrical circuit with output swings essentially equal to the supply voltage. This results in high noise immunity over a wide supply voltage range. No DC power other than that caused by leakage current is consumed during static conditions. All inputs are protected against static discharge and latching conditions.

features

- Wide supply voltage range — 3V to 15V
- Low power — 10 nW (typical)
- High noise immunity — 0.45 V_{DD} (typical)

absolute maximum ratings

Voltage at Any Pin (Note 2)	V_{SS} − 0.3V to V_{SS} + 15.5V	Storage Temperature Range	−65°C to +150°C
Operating Temperature Range		Package Dissipation	500 mW
MM4601A	−55°C to +125°C	Lead Temperature (Soldering, 10 sec)	300°C
MM5601A	−40°C to +85°C	Operating V_{DD} Range	V_{SS} + 3V to V_{SS} + 15V

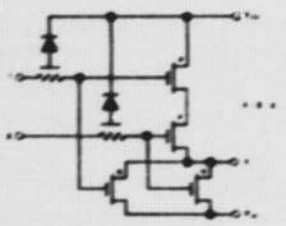
electrical characteristics

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Data Input Levels					
Logical "1" Input Voltage	V_{OUT} = 0.3 V_{DD} I_{OUT} = 0	0.7 V_{DD}		V_{DD} + 0.3	V
Logical "0" Input Voltage	V_{OUT} = 0.7 V_{DD} I_{OUT} = 0	−0.3		0.7 V_{DD}	V
Data Input Leakage	V_{IN} = 15V All Other Pins GND		0.005	0.5	μA
Data Input Capacitance	V_{IN} = 0.0V, f = 1.0MHz All Other Pins GND (Note 1)		2.5	7.5	pF
Data Output Levels					
Logical "1" Output Voltage	V_{IN} = GND I_{OUT} = 0			V_{DD} − 0.05	V
	I_{OUT} = −1.0 mA, V_{DD} = 5V			V_{DD} − 0.1	V
Logical "0" Output Voltage	V_{IN} = V_{DD} I_{OUT} = 0			0.05	V
	I_{OUT} = 0.5 mA, V_{DD} = 5V			0.10	V
Propagation Delay to a Logical "1" (t_{PD1})	C_L = 15 pF, T_A = 25°C				
MM4601A	V_{DD} = 5V			65	ns
	V_{DD} = 10V			40	ns
MM5601A	V_{DD} = 5V			90	ns
	V_{DD} = 10V			55	ns
Propagation Delay to a Logical "0" (t_{PD0})					
MM4601A	V_{DD} = 5V			65	ns
	V_{DD} = 10V			40	ns
MM5601A	V_{DD} = 5V			75	ns
	V_{DD} = 10V			45	ns

Note 1: Capacitance is guaranteed by periodic testing.

Note 2: This device should not be connected to circuits with the power on if the quadruple high voltage may be high while logic permanent voltage

schematic and connection diagrams



Dual-In-Line Package

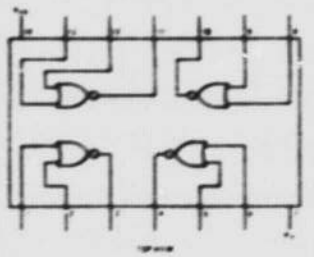
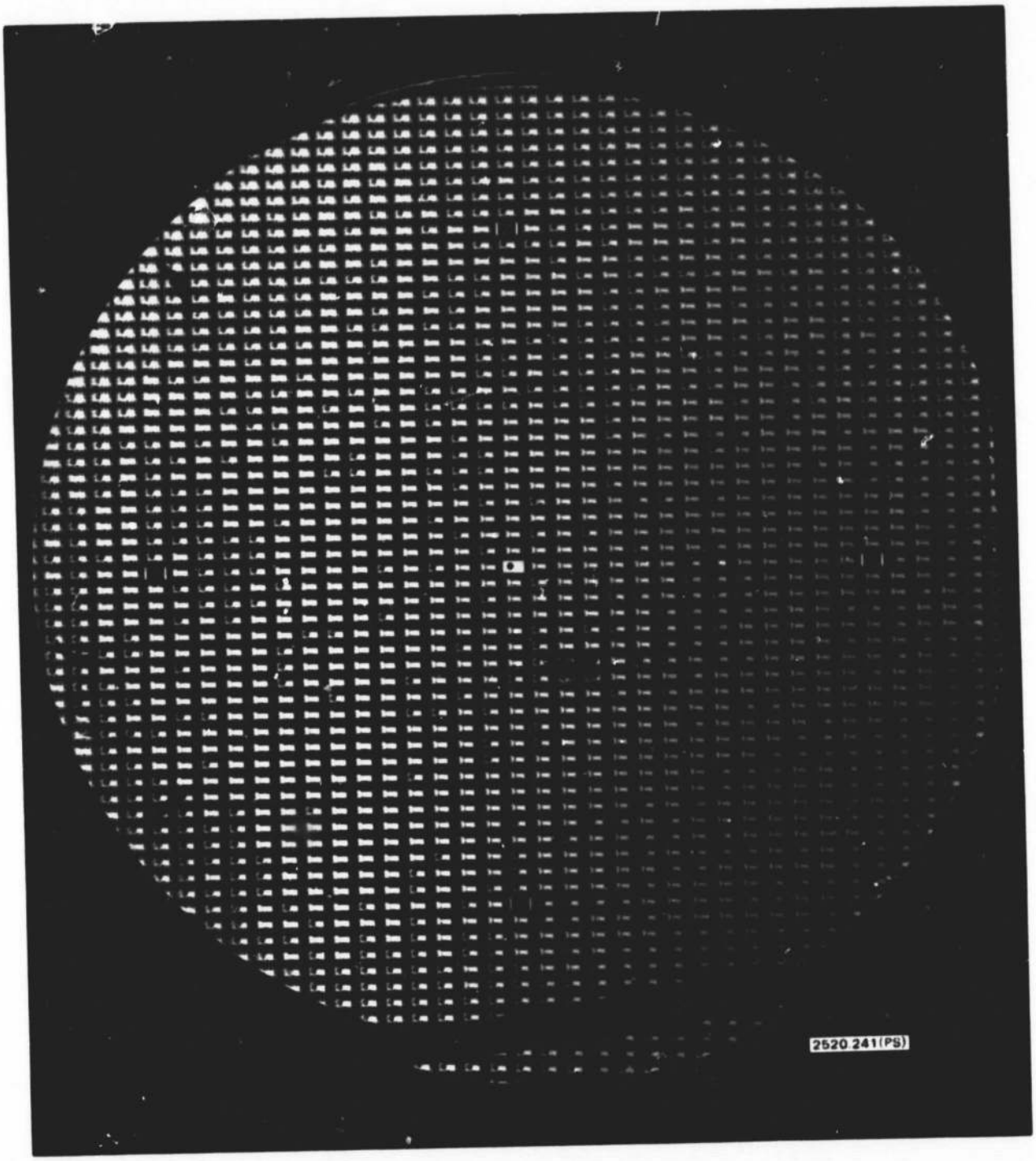
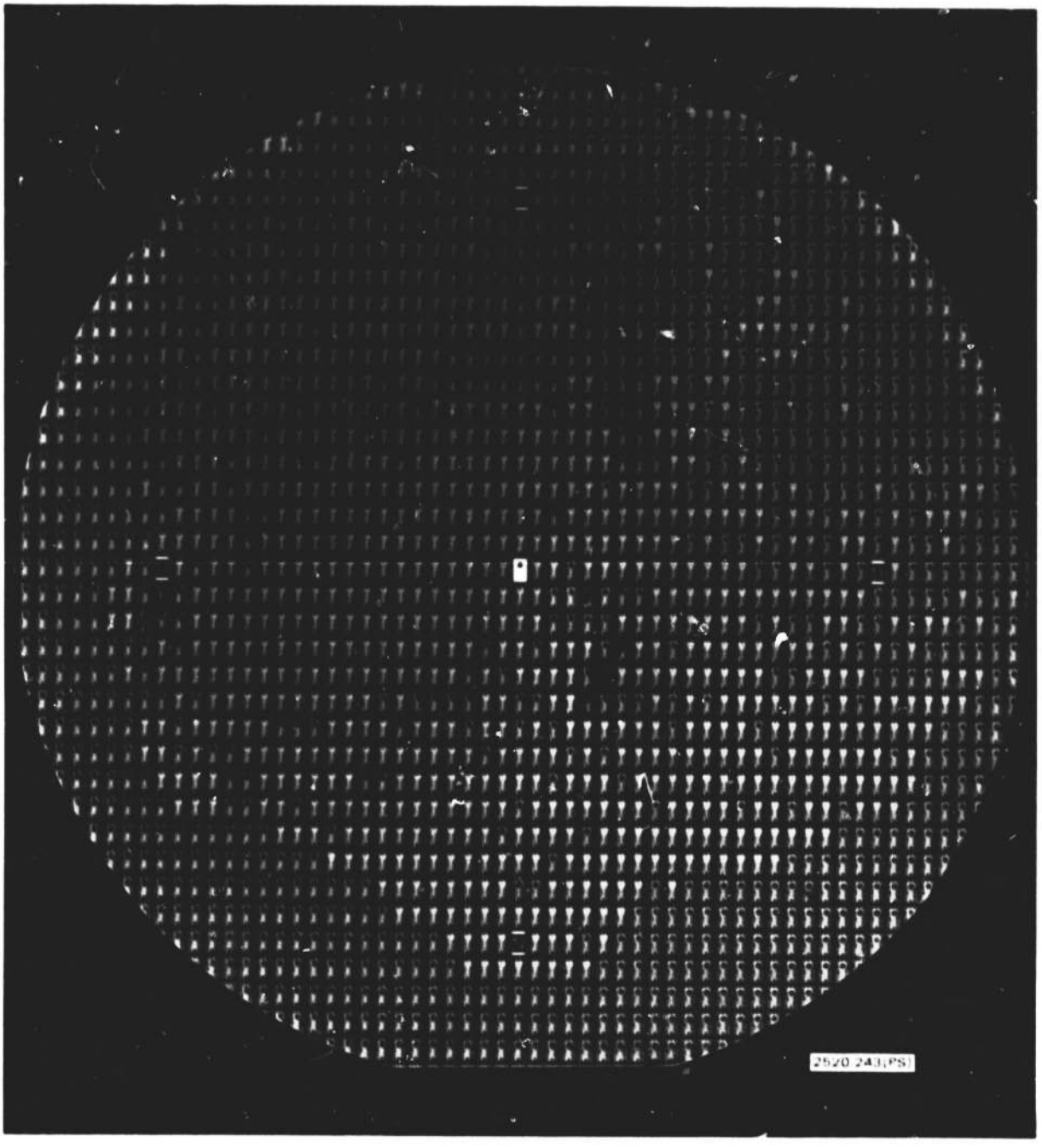
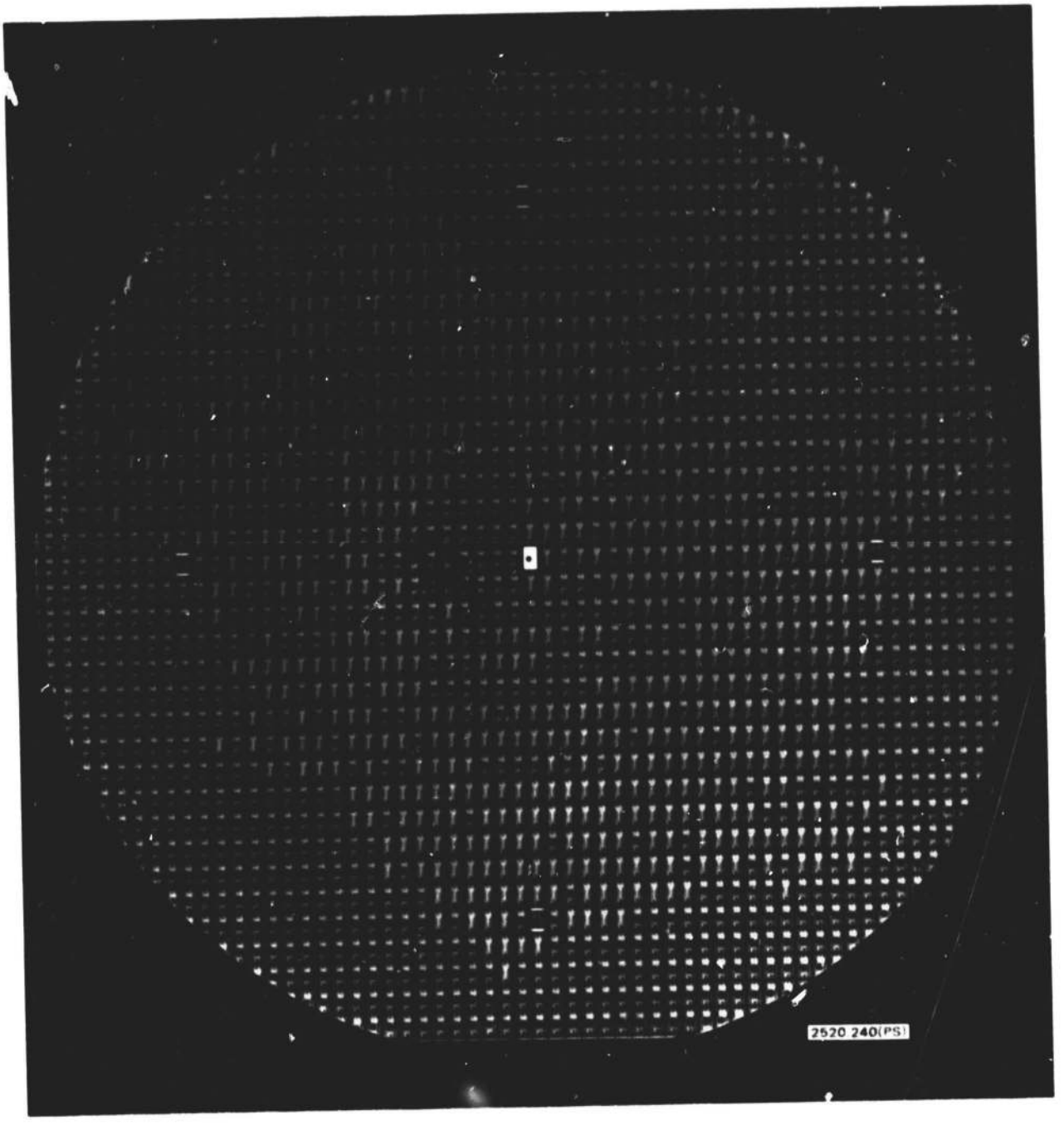


Figure 24. MM4601A Specifications






2520 240(PS)

The window mask for the CMOS wafers was obtained from National Semiconductor. However, the window mask was more complicated than was needed, in that an undesirable grid pattern of 0.075mm wide scribing lines was incorporated into the mask, in addition to the desired bonding pad window areas. After an attempt was made to blank out this grid pattern, it was decided that it would be easier to re-make the mask, with its simple pattern of fourteen bonding pads per device. The artwork was done at ATI, and the photoreduction and step-and-repeat was done at Micromask in Sunnyvale.

The wafers were processed as described in Section VI-B above.

The wafers were bumped with the indium/lead/silver bumps for two reasons. First, the gold/lead/silver bumping process requires exposing the passivation layer to the conversion gold plating bath. The commercial plating bath used contains potassium ions. It is not desirable to expose MOS devices to such an environment containing alkalai metal ions. While it is possible to prepare an alkalai ion-free conversion gold plating path, such a solution was not readily available. The second reason was that the gold/lead/silver process requires an alloying step at 350°C., whereas no elevated temperature pre-alloying step is required in the indium/lead/silver process.

The test parameters measured were:

- Data output swing (0, 1)
- Data input threshold
- Data input capacitance
- Propagation delay (0, 1)

The first two CMOS wafers processed and tested showed no data output from any of the devices.

The third wafer was handled much more carefully. In particular, static electricity from the dry film lamination step was suspect. The third wafer was heated on a hot plate within a laminar flow bench, with a grounded aluminum plate interposed between the wafer and the hot plate. The dry film resist was cut into a circle, and the polyethylene film was peeled off. The exposed resist was brushed with an anti-static brush, and then the resist was brought into contact with a clean grounded aluminum surface for about 15 minutes. Finally, the resist was laminated onto the silicon wafer on the hot plate with the aid of a grounded aluminum rod used as a roller, and the assembly was removed from the hot plate.

This third wafer produced some electrically good chips, but the yield was low. Clearly, more work must be done to define improved handling procedures. It is not certain, for example, that the modified dry film resist lamination procedure was responsible for the improved handling.

XI. FLUXLESS SOLDER-BUMP CONTACT TECHNOLOGY EVALUATION WITH RESPECT TO DEFINED CRITERIA

A. Evaluation with Respect to the Seven Criteria

1. Reliability of Electromechanical Interconnection of Semiconductor Chips

The solder-bump alloys tested are metallurgically compatible with gold and other common precious metal bonding surfaces. Neither scavenging nor the formation of undesirable intermetallic phases takes place at the bonding surface.

The entire bonding process is implemented without the use of flux, thus providing contamination control. This is important, because it is exceedingly difficult to assure the reliable removal of all traces of flux residues after soldering, especially in the close spacings between bonded devices and substrate; these flux residues can lead to device degradation and failure.

Centrifuge, temperature cycling, and high temperature storage data have demonstrated the high reliability of electromechanical interconnection, especially for iridium/lead/silver-bumped chips bonded using Method I. It is expected that gold/lead/silver-bumped chips would exhibit the same high electromechanical interconnection reliability with a thinner gold overcoat layer.

2. Low Cost Processing

It has been demonstrated that the fluxless solder-bumping process can be performed with no more than a single photomasking step. Competing processes require no less than two photomasking steps. The photomasking operation is generally the

single most expensive element in batch-processed production, and the number of required photomasking steps is widely employed in judging process complexity.

In addition, neither solder pads nor solder dams nor the application of flux nor the removal of flux residue is required for joining, thus reducing process complexity and cost.

3. Implementability by Both Manufacturers of Semiconductor Products and Purchasers of Those Products

Flip-chip device processing is more implementable by both manufacturers and users of semiconductor products than either beam-lead or beam-tape technology. Because of it's relative process simplicity, fluxless solder-bump technology is more readily implementable than any competing solder-bump flip-chip technology. The basic equipment required is as follows:

- Thin-film vacuum evaporation station.
- Mask aligner/printer in a light-controlled area.
- Spray development tank.
- Plating power supply, assorted electrodes, plating solutions and inexpensive plating vessels.
- Dry nitrogen/hot air oven.
- Wafer dicing saw.
- Microscope.
- Flip-chip bonding machine.

Special tooling consists of a window mask. Device layouts currently in production, in inventory, and on the drawing boards can be processed as described herein. Flip-chip bumps can be readily applied to the latest high performance

devices from any semiconductor device manufacturer.

When purchasing wafers, considerations of part quality control and quality responsibility could arise. However, it should not be much more difficult to purchase good wafers than to purchase good loose die in this regard.

4. Compatibility with Available Bonding Equipment and Materials

Suitable flip-chip bonding equipment is readily commercially available - notably the Unitek Model 8-149-01-02 flip-chip bonder.

5. Economy for Both Large and Small Volume Production

Because of its relative process simplicity, processing is more economical than competing technologies for both large and small volume production.

Regarding minimum quantity requirements, it is estimated that as few as a dozen wafers could be processed economically. However, the epoxy bump process explored briefly as part of this program must be unexcelled for low cost, low quantity processing.

6. Adaptability to Automatic Procedures

During attachment of devices to substrate bonding pads, all required mechanical and electrical interconnections to the devices are achieved in a single convenient, low-cost, reliable gang-bonding operation. Special tooling is not required to handle each device size.

Because of the physically accessable but rugged nature of the flip-chip terminals, device pre-testing and attachment is very compatible with relatively simple automated processing equipment. In addition, bumps with magnetic properties are readily provided to facilitate chip handling and storage.

It is possible to completely automate the entire flip-chip bonding process, including flip-chip die orientation, flip-chip die testing and classification, and flip-chip die bonding. Device burn-in could be similarly automated.

7. Compatibility with a Large Number of Bump Contacts Per Chip

Using the processes outlined, it is possible to form 0.1mm diameter bumps on 0.2mm centers. Thus, for example, a chip measuring 5mm on a side could accommodate nearly 100 bump contacts.

Well-controlled bump dimensions result from the process of forming bump metallization through windows in thick dry film resist - a simple, effective, low-cost technique.

XII. CONCLUSIONS AND RECOMMENDATIONS

The fluxless solder-bump materials and bonding techniques evaluated have proven to be an effective method for chip joining. The indium/lead/silver solder-bump process seems to be easier to implement than the gold/lead/silver process, and it appears to form joints which may be more reliable.

However, the conductive epoxy bump process represents a new technology which also holds much promise.

Some potential advantages of the conductive epoxy bump process are:

- o Simplified process. Fewer, faster, easier steps.
- o Essentially an all-additive process. Cleaner, easier. Minimum pre-cleaning required (can leave marking ink intact).
- o Lowest temperature processing.

Development of this process should include the following tasks:

1. Develop techniques for forming reliable conductive epoxy bump contacts.
2. Evaluate the feasibility of extending bumps to the edge of the chip for ease of alignment and bond inspection.
3. Define reliable bump contact and die attach materials and techniques.
4. Environmentally test conductive epoxy bumped and bonded CMOS devices.

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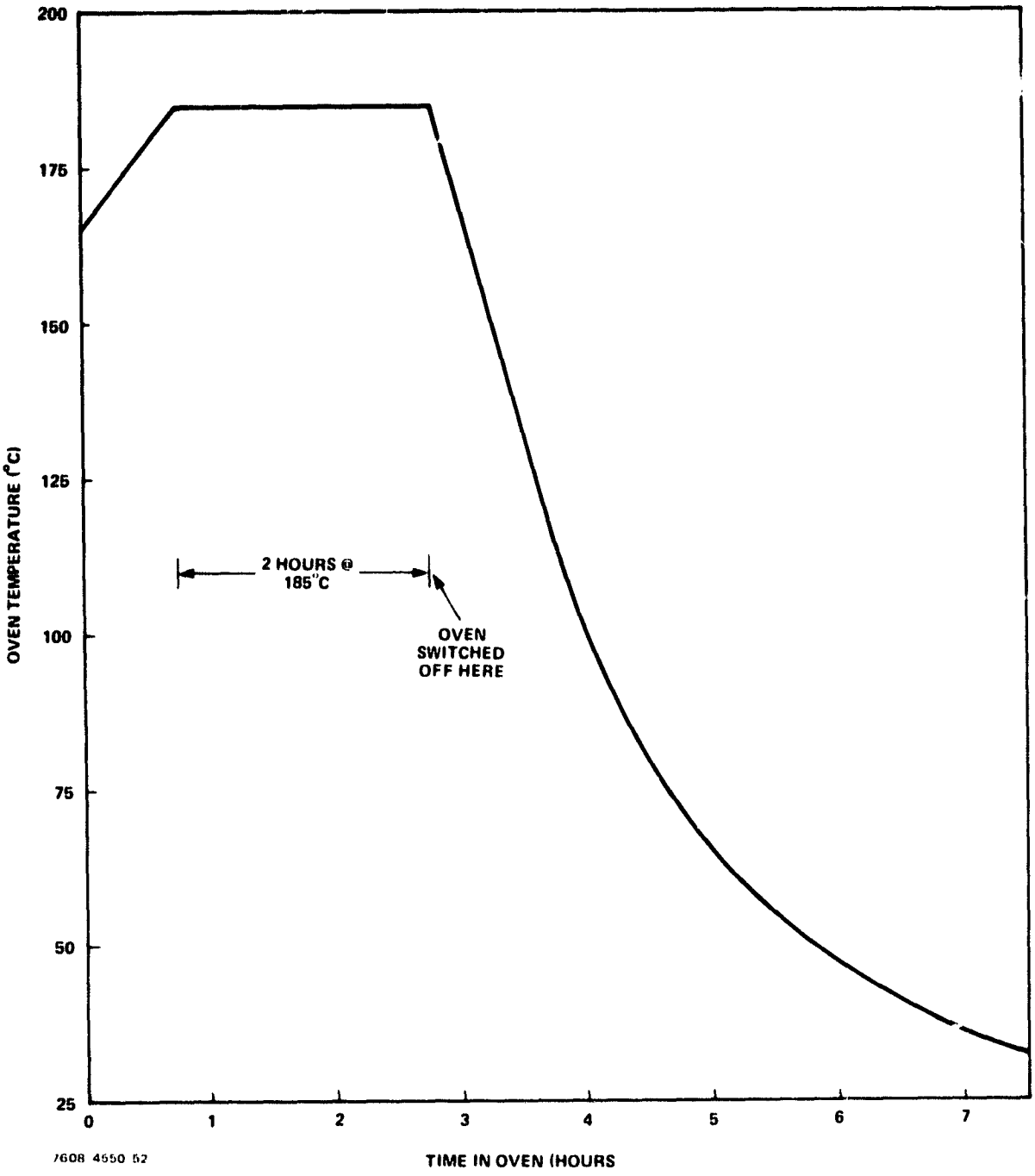
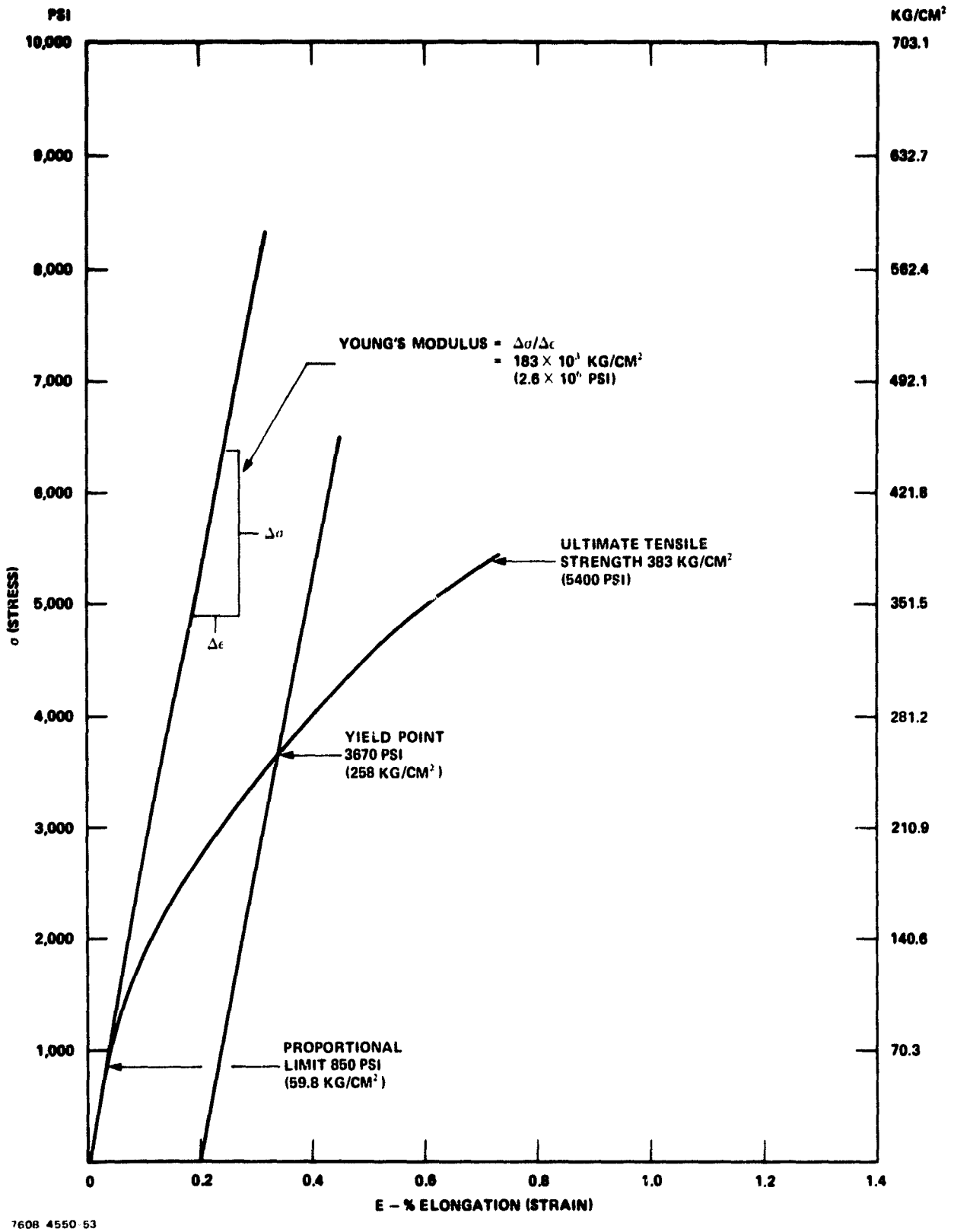
APPENDIX I

STRESS/STRAIN CURVES FOR SELECTED SOLDER ALLOYS

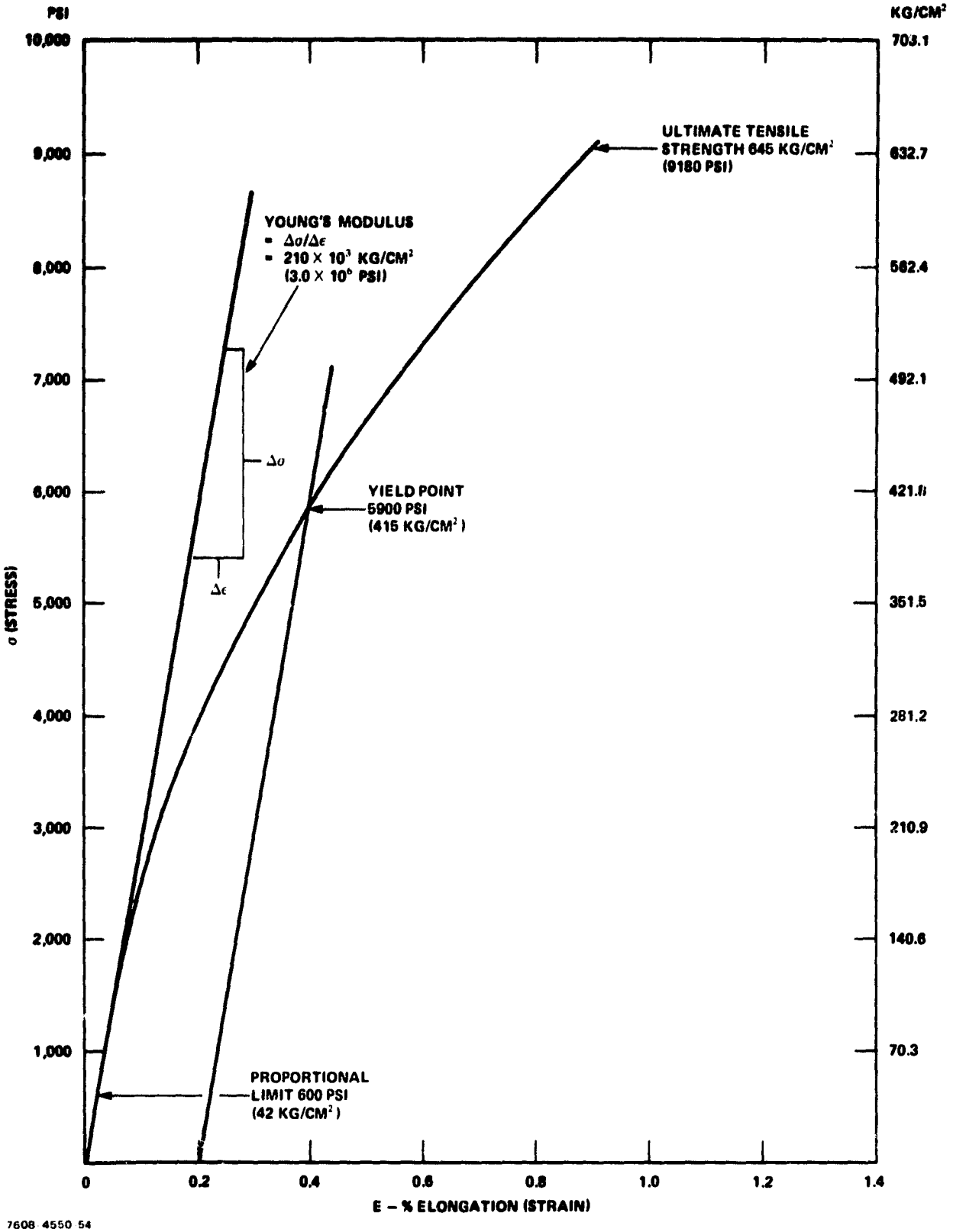
GRAPH A	ANNEALING OF METAL ALLOY SAMPLES IN VACUUM OVEN
GRAPH #1	STRESS/STRAIN CURVE FOR 82.9% Pb - 15.0% Au - 2.1% Ag ALLOY
GRAPH #2	STRESS/STRAIN CURVE FOR 84.7% Pb - 15.3% Au ALLOY
GRAPH #3	STRESS/STRAIN CURVE FOR 64.4% Pb - 32.9% In - 2.7% Ag ALLOY
GRAPH #4	STRESS/STRAIN CURVE FOR 66.2% Pb - 33.8% In ALLOY
GRAPH #5	STRESS/STRAIN CURVE FOR 85.0% Pb - 12.5% Au - 2.5% Ag ALLOY
GRAPH #6	STRESS/STRAIN CURVE FOR 90.0% Pb - 10.0% Sn ALLOY



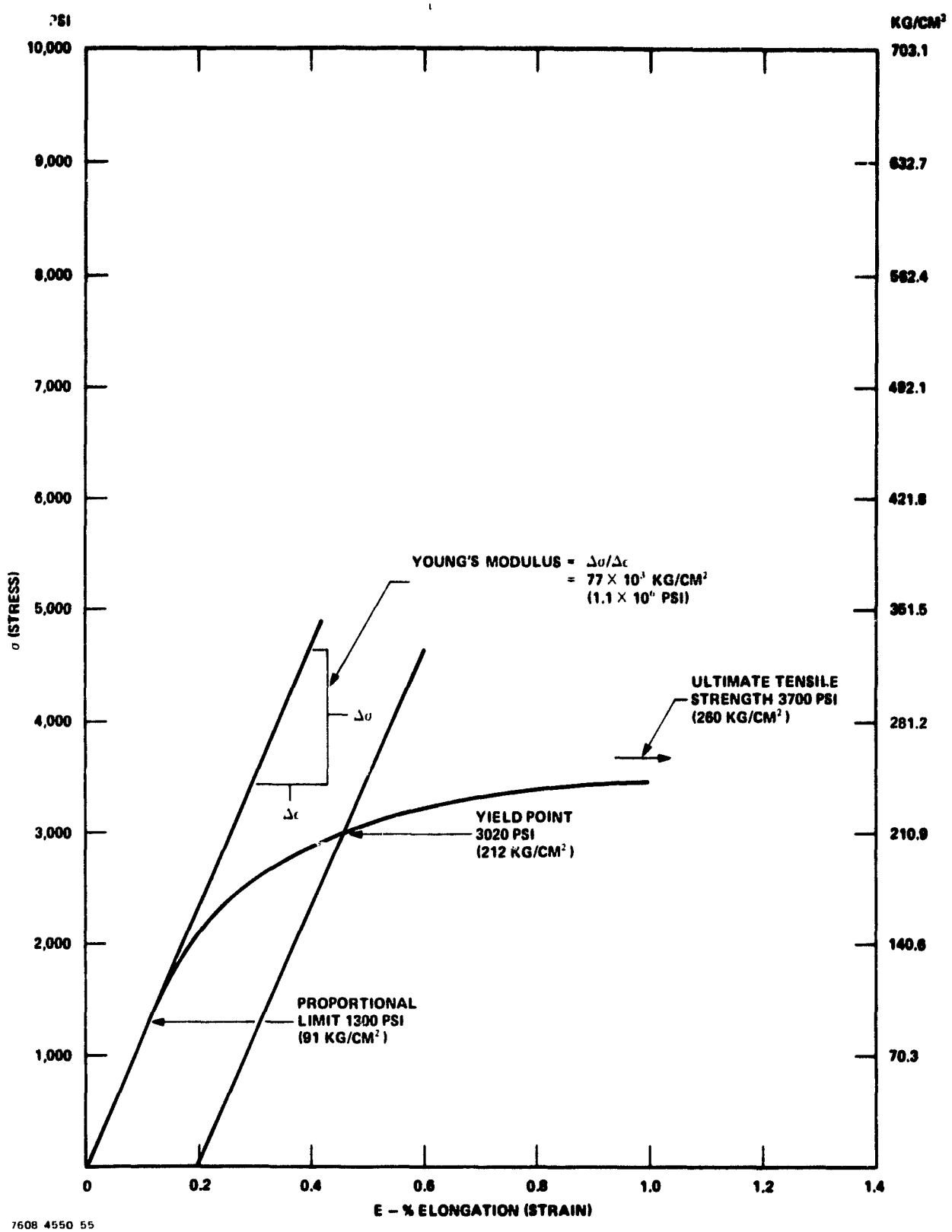
Graph A. Annealing of Metal Alloy Samples in Vacuum Oven



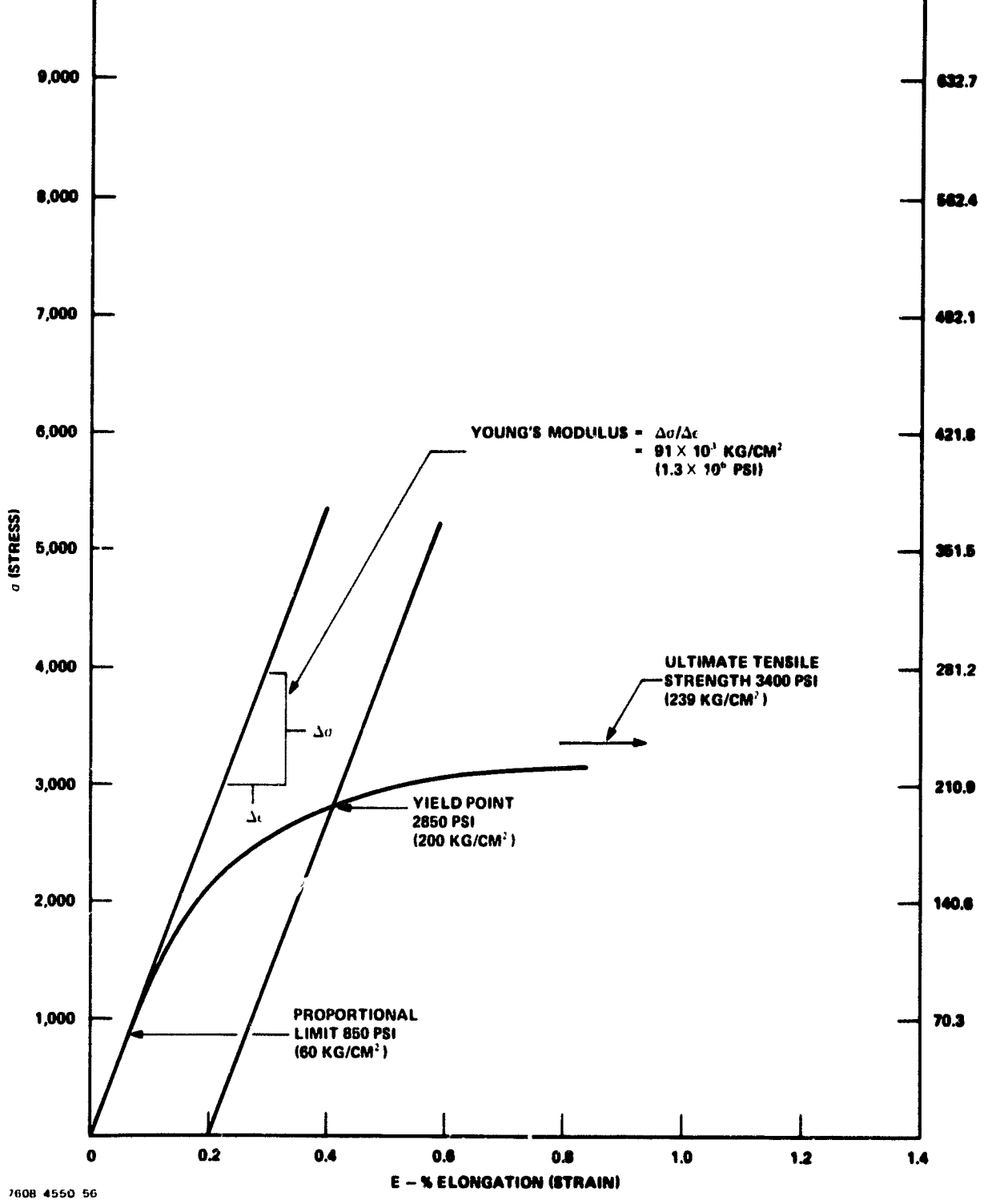
Graph 1. Stress/Strain Curve for 82.9% Pb, 15% Au, 2.1% Ag Alloy



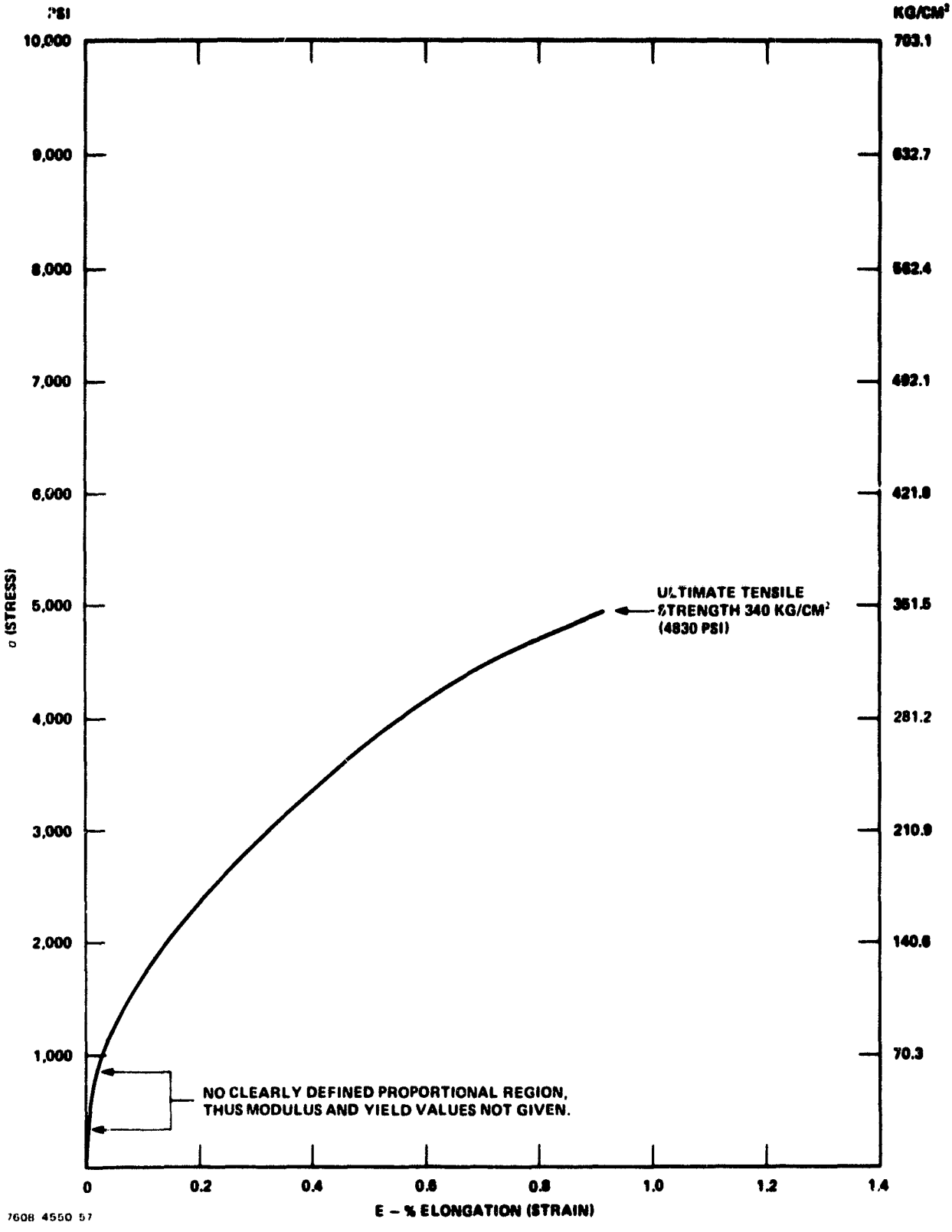
Graph 2. Stress/Strain Curve for 84.7% Pb, 15.3% Au Alloy



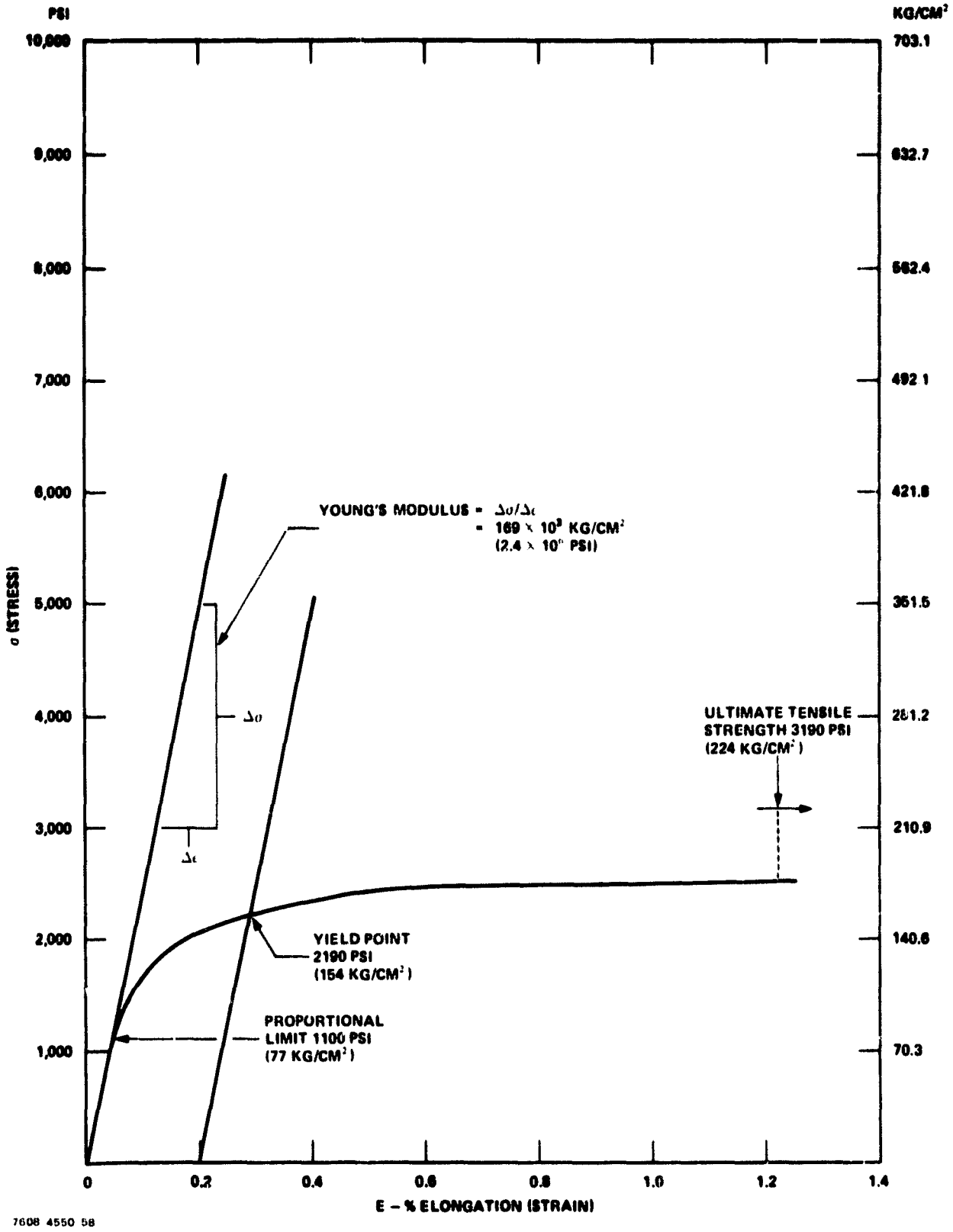
Graph 3. Stress/Strain Curve for 64.4% Pb, 32.9% In, 2.7% Ag Alloy



Graph 4. Stress/Strain Curve for 66.2% Pb, 33.8% In Alloy



Graph 5. Stress/Strain Curve for 85% Pb, 12.5% Au, 2.5% Ag Alloy



Graph 6. Stress/Strain Curve for 90% Pb, 10% Sn Alloy

APPENDIX II
DRY FILM PHOTOMASK APPLICATION PROCEDURE
SIMULATED INTEGRATED CIRCUIT WAFERS

1. Clean the wafers (TMC vapor degrease, DI water rinse, isopropyl alcohol boil (pull out slowly).

2. Place the wafers on a metal sheet carrier which is covered with a teflon film.

3. Mount a roll of Riston 30S dry film photoresist on the upper roller, and mount a roll of photocopy paper on the lower roller of a duPont HRL-24 laminator.

4. Pre-heat the duPont HRL-24 laminator rolls to 104°C., and the wafers to 140°C.

5. Laminate the dry film photoresist onto the wafers at a speed of 1.7 cm/second automatically peeling away the polyethylene surface film from the resist immediately prior to lamination.

6. Cut out the laminated wafers from the carrier. Let the wafers cool for at least one hour.

7. Align the mask pattern to the wafer, and print the mask pattern onto the laminated dry film resist (approximately a 25-second exposure using a Kasper mask aligner/ printer). Let the wafers sit for at least one hour.

8. Peel off the mylar protective film to expose the photoresist surface, and mount the wafers onto a holding fixture.

9. Place the wafers in a jet spray of 1,1,1-trichloroethane developer at room temperature, such that the spray is directed against the surface of the photoresist. Spray develop for 120 seconds.

10. After spray development, immediately immerse the parts in a tank of liquid 1, 1, 1-trichloroethane at room temperature for 10 seconds, using manual agitation.

11. After dip development, immediately rinse the wafers in a water spray at room temperature. After 20 seconds of exposure to the water spray, dry the wafers with a jet of filtered dry air or nitrogen.

12. Post-bake the wafers in a circulating hot air oven at 93°C. for 15 minutes.

APPENDIX III

PREPLATE PROCESS PROCEDURE FOR SIMULATED INTEGRATED CIRCUIT WAFERS

A. Preplate Procedure

1. Apply plater's tape to the back surface of the wafer.
2. Mask edges with Shipley AZ-119 resist or equivalent.
3. Ion mill or ion bombard for approximately 15 minutes (argon, 10^{-6} torr range).
4. Immerse in Neutra Clean 68 (see B1 below) for 5 minutes, agitating about 15 seconds each time.
5. Rinse thoroughly in a spray D.I. water rinse.
6. Immerse in 20% sulfuric acid solution (see B-2 below) for 15 to 30 seconds, with continuous agitation. Do not rinse; immediately transfer the wafer into the first plating solution.

B. Preplate Chemical Solution Parameters

1. Neutra Clean 68

   Manufacturer: Ship Company

   (1) Concentration: 100%

   (2) Temperature: Room

2. Sulfuric Acid Dip

   (1) Concentration: 20% H_2SO_4 by volume

   (2) Temperature: Room

APPENDIX IV

ELECTROFORM PROCEDURE

GOLD/LEAD/SILVER SOLDER-BUMPS AND INDIUM/LEAD/SILVER SOLDER-BUMPS

A. Electroform Procedure for Gold/Lead/Silver Solder-Bumps

(NOTE: It is essential that the plating surfaces be properly conditioned as described in the appropriate Preplate Procedure, immediately prior to using this electroform procedure.)

1. Nickel Plate - (Plating Solution IV-C-1)

Plating Time:	Approximately 1 hour 45 minutes
Current Density:	4.2 amps per square foot (4.5 ma/cm^2)
Thickness:	1.0 mil ± 0.1 mil (25 micrometers ± 2.5 micrometers)

(NOTE: A micrometer may be employed to aid nickel plating parameter calibration.)

2. D.I. water spray rinse.

3. Copper Strike - (Plating Solution IV-C-2)

Plating Time:	60 ± 10 seconds
Current Density:	8.3 amps per square foot (8.9 ma/cm^2)
Thickness:	Approximately 40 microinches (1 micrometer)

4. D.I. water spray rinse.

5. Silver Plate - (Plating Solution IV-C-3)

Plating Time:	55 ± 5 seconds
Current Density:	1.9 amps per square foot (2.04 ma/cm^2)
Thickness:	68 to 90 microinches (1.7 to 2.25 micrometers)

6. D.I. water spray rinse.

7. Gold Plate - (Plating Solution IV-C-4)

Plating Time:	Approximately 19 minutes
Current Density:	0.8 amps per square foot (0.86 ma/cm^2)
Thickness:	93 to 118 microinches (2.3 to 2.95 micrometers)

8. D.I. water spray rinse.

9. Lead Plate - (Plating Solution IV-C-5)

Plating Time:	Approximately 2 hours 20 minutes
Current Density:	5 amps per square foot (5.4 ma/cm^2)
Thickness:	1.79 mils ± 0.02 mils (4.55 ±0.05 micrometers)

10. D.I. water spray rinse and nitrogen dry.

B. Electroform Procedure for Indium/Lead/Silver Solder-Bumps

(NOTE: It is essential that the plating surfaces be properly conditioned as described in the appropriate Preplate Procedure, immediately prior to using this electroform procedure.)

1. Nickel Plate - (Plating Solution IV-C-1)

Plating Time:	Approximately 1 hour 45 minutes
Current Density:	4.2 amps per square foot (4.5 ma/cm^2)
Thickness:	1.0 mil ± 0.1 mil (25 micrometers ±2.5 micrometers)

(NOTE: A micrometer may be employed to aid nickel plating parameter calibration.)

2. D.I. water spray rinse.

3. Copper Strike - (Plating Solution IV-C-2)

Plating Time:	60 ± 10 seconds
Current Density:	8.3 amps per square foot (8.9 ma/cm^2)
Thickness:	Approximately 1 micrometer

4. D.I. water spray rinse.

5. Lead Plate - (Plating Solution IV-C-5)

Plating Time:	Approximately 2 hours 30 minutes
Current Density:	5 amps per square foot (5.4 ma/cm^2)
Thickness:	1.32 mils ± 0.13 mils (33.6 ± 3.4 μm)

6. D.I. water spray rinse.

7. Indium Plate - (Plating Solution IV-C-6)

Plating Time:	Approximately 1 hour
Current Density:	5 amps per square foot (5.4 ma/cm^2)
Thickness:	0.68 mil ± 0.07 mil (17.3 ± 1.7 μm)

8. D.I. water spray rinse.

9. Silver Plate - (Plating Solution IV-C-3)

Plating Time:	90 ± 10 seconds
Current Density:	1.9 amps per square foot (2.04 ma/cm^2)
Thickness:	27 microinches ± 3 microinches (6900 angstroms ± 690 angstroms)

10. D.I. water spray rinse.

11. Gold Plate - (Plating Solution IV-C-7)

Plating Time:	60 minutes
Thickness:	Approximately 2 microinches (500 Å)

12. D.I. water spray rinse and nitrogen dry.

C. Chemical Solution Parameters

1. Nickel Plate

Bath Type:	Sulfamate Nickel (Acid)
Manufacturer:	Udylite (Oxy Metal Industries Corp.)

Bath Preparation	Bath Parameters
Nickel Sulfamate	36 to 44 oz/gal (270 to 300 g/l)
Nickel Chloride	2 oz/gal (15 g/l)
Boric Acid	4 to 6 oz/gal (30 to 45 g/l)
Stress Reducer	0 to 2 oz/gal (0 to 15 g/l)
Wetting Agent 2A	0.1 to 0.2 oz/gal (0.75 to 1.5 g/l)

Operating Conditions

Temperature:	100 ± 20°F (38 ± 11°C.)
pH:	3.0 to 5.0
Current Density:	Up to 100 ASF (108 ma/cm^2)
Agitation:	Mechanical
Baume':	29 to 31 at 70°F (21°C.)
Tank Voltage:	6 to 10 Volts
Anodes:	Nickel Rolled Depolarized
Anode Bags:	Cotton or Dynel

2. Copper Plate

Bath Type: Cubath Sulfate (High Acid/Low Copper)

Manufacturer: Oxy Metals Industries Corp. (Sel Rex)

Bath Preparation	Range	Optimum
Copper Metal	2-2 1/2 oz/gal (15-19 g/l)	2 1/4 oz/gal (17 g/l)
Copper Sulfate	8-10 oz/gal (6-7.5 g/l)	9 oz/gal (67 g/l)
H_2SO_4	20-30 oz/gal (150-225 g/l)	23 oz/gal (170 g/l)
Chloride Ion	20-80 mg/l	30 mg/l

Operating Conditions

Temperature:	70-85°C (21-29°C)	75°F (24°C)
Filtration:	For classification purposes only	
Anodes:	Cubath anodes .040-.060% phosphorous (OFHC copper or electrolytic cannot be used)	
Anode Hooks:	Titanium	
Agitation:	Blower Air	
Current Density:	Up to 40 ASF Cathode (43 ma/cm^2)	
Cubath HY M Addition Agent	1/4 - 1/2 ml/amp hour	

3. Silver Plate

Bath Type: Cyanide Silver (Alkaline)

Manufacturer: Oxy Metals Industries Corp. (Sel Rex)

Operating Conditions	Nominal	Range
Metallic silver content	10.8 Tr. oz/gal (8.9 g/l)	(8-12 Tr. oz/gal)(6.6-9.9 g/l)
Potassium cyanide content	10.0 Av. oz/gal (75 g/l)	(8-12 Av. oz/gal)(6-9 g/l)
Potassium carbonate	2.0 Av. oz/gal (15 g/l)	(1-3 Av. oz/gal)(7.5-22.5 g/l)
Industrial silver brightener	4.0 cc/gal (1 cc/l)	(3-5 cc/gal) (0.8-1.3 g/l)
pH	12.5	(12-13)
Temperature	21°C (70°F)	(18-28°C) (68-85°F)
Agitation	Vigorous	
Anode to Cathode Ratio	2 to 1 or higher	
Anodes	Pure Silver	

Operating Conditions	Nominal
Cathode Current Density (Rack)	(Up to 80 ASF) (86 ma/cm^2)
Time to Deposit 0.0001" @ 30 ASF (Rack)	1.23 minutes

4. Gold Plate

Bath Type: Alkaline Non-Cyanide Bright Ductile Gold

Manufacturer: Oxy Metal Industries Corp. (Sel Rex), BDT 510

Physical Properties

Purity	99.9%
Hardness	130-190 Knoop
Contact Resistance	0.3 milliohms
Deposit Weight for 0.0001" Thickness	31.6 mg/sq.in. (5.0 mg/cm^2)

Materials Required

Materials required for this bath are:

BDT 510 Make-Up
BDT Replenisher
BDT Conducting Salts
Reagent grade sodium hydroxide (20%) and sulfuric acid (5%) for pH adjustment

Operating Conditions	Nominal	Range
Metallic Gold Content	12 g/l	8-16 g/l
pH (Electrometric)	8.5	8.0 - 9.0
Specific Gravity	10° Baume' minimum	8° - 35° Baume'
Temperature	50°C (120°F)	(95° - 130°F) (35-55°C)
Agitation	Vigorous at Anode and Cathode	
Anodes	Platinum or Permanode	
Anode-to-Cathode Ratio	2 to 1 or higher	
Cathode Current Density (Rack)	Up to 10 ASF (11 ma/cm^2)	

5. Lead Plate

Bath Type: Fluoborate Lead (Acid)

Manufacturer: Allied Chemical

Bath Composition

Lead Fluoborate	200 g/l
Lead Metal	108.8 g/l
Peptone	0.5 g/l
Baume' (at 80°F)	21.5 - 22.0
pH (maximum)	1.0
Temperature	75 - 100°F (24-38°C.)
Cathode Current Density	Up to 50 ASF (54 ma/cm^2)
Average Tank Voltage	1-3 V
Anodes	Lead

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6. Indium Plate

Bath Type: Sulfamic Acid

Manufacturer: Indium Corporation of America

Bath Composition

Indium Sulfamate	105.4 g/l
Sodium Sulfamate	150.0 g/l
Sulfamic Acid	26.4 g/l
Sodium Chloride	45.8 g/l
Dextrose	8.0 g/l
Triethanolamine	2.3 g/l

Operating Conditions

pH	Under 3.5
Temperature	Room Temperature
Current Density	Up to 100 ASF (108 ma/cm^2)
Anodes	Indium

7. Conversion Gold Plate

Bath Type: Ammonaic Cyanide Gold, Atomex

Manufacturer: Engelhard Minerals & Chemicals Corp.

Operating Conditions

Gold Concentration	1/2 ounce per gallon (3.8 g/l)
pH	7 to 8
Temperature	75°C ± 5°C with stirring

APPENDIX V
POSTPLATE PROCEDURE
SIMULATED INTEGRATED CIRCUIT WAFERS

A. Postplate Procedure for Gold/Lead/Silver Solder-Bumped Wafers

1. Strip away the plastic film. First, soak the wafer in a solution of 93% methylene chloride/7% methyl alcohol at room temperature until the resist film begins to loosen. Remove the resist film in a spray of 93% methylene chloride/7% methyl alcohol. Rinse in a water spray, then in methyl alcohol, and blow dry. Remove remaining traces of resist in Uresolve Plus (Dynaloy) at 65°C ± 5°C for 5 minutes or at room temperature overnight. Finally, rinse in D.I. water, then in methyl alcohol. Blow dry.

2. Etch away the interconnecting copper film with copper etchant (Solution V-C-1) (approximately 20 seconds). Water rinse in D.I. water (approximately 60 seconds), then in methyl alcohol. Blow dry.

3. Alloy the gold/lead/silver solder (60 seconds at 350°C in a forming gas or nitrogen atmosphere).

4. Etch away the interconnecting molybdenum film with molybdenum etchant (Solution V-C-2) (approximately 5 seconds). Water rinse in D.I. water (approximately 60 seconds).

5. Plate gold on the solder-bumps. First deoxidize the surface of the solder-bumps (aqueous ammonia, 15 seconds, room temperature). Immediately plate conversion gold (Solution V-C-3) for approximately 5 minutes.

6. Rinse in aqueous ammonia for 15 seconds, then in D.I. water for 1 minute, and finally in methyl alcohol. Blow dry.

B. Postplate Procedure for Indium/Lead/Silver Bumped Wafers

1. Strip away the plastic resist film. First, soak the wafer in a solution of 93% methylene chloride/7% methyl alcohol at room temperature until the resist film begins to loosen. Remove the resist film in a spray of 93% methylene chloride/7% methyl alcohol. Rinse in a water spray, then in methyl alcohol, and blow dry. Remove remaining traces of resist in Uresolve Plus (Dynaloy) at 65°C ± 5°C for 5 minutes or at room temperature overnight. Finally, rinse in D.I. water, then in methyl alcohol. Blow dry.

2. Etch away the interconnecting copper film with copper etchant (Solution V-C-1) (approximately 20 seconds). Water rinse in D.I. water (approximately 60 seconds).

3. Etch away the interconnecting molybdenum film with molybdenum etchant (Solution V-C-2) (approximately 5 seconds). Water rinse in D.I. water (approximately 60 seconds).

4. Rinse in aqueous ammonia for 15 seconds, then in D.I. water for 1 minute, and finally in methyl alcohol. Blow dry.

C. Chemical Solution Parameters

1. Copper Etchant

Bath Type: Oxidizing Alkaline Solution

Manufacturer: Southern California Chemical Corp. - AE-25

Composition

40% part "A" aqua ammonia solution (by volume)
20% part "B" alkaline oxidizing solution
40% deionized water

Operating Conditions

Room temperature with stirring in a plastic container.

2. Molybdenum Etchant

Bath Type: Alkaline Ferricyanide

Composition

184 grams potassium ferricyanide
40 grams potassium hydroxide
600 ml. deionized water

Operating Conditions

Room temperature with stirring in a plastic container.

3. Conversion Gold Plate

Bath Type: Ammonaic Cyanide Gold, Atomex

Manufacturer: Engelhard Minerals & Chemicals Corp.

Operating Conditions

Gold Concentration	1/2 ounce per gallon (3.8 g/l)
pH	7 to 8
Temperature	75° C ± 5°C with stirring

D. Discussion

Both the copper etchant and the molybdenum etchant are selective. The copper etchant does not attack lead, nickel, indium, silver or gold; copper is etched at the rate of approximately 500 Å/sec. The molybdenum etchant does not attack nickel, indium, gold, or copper; molybdenum is etched at the rate of approximately 200 Å/sec., while silver is etched at the rate of about 40 Å/sec., and lead forms a black oxidized surface which is easy to remove in ammonium hydroxide.

APPENDIX VI
WAFER SAWING PROCEDURE

Wafer sawing was done on a Lindberg-Tempress wafer dicing saw.

Since the wafers were to be sawed completely through, the wafers were first bonded to base plates. The base plates were comprised of graphite, 5 cm in diameter by approximately 3 mm thick, machined on both sides to a flatness of better than 25 μm. Before use, the graphite base plates were wiped clean of dust and precleaned by submersion in boiling trichloroethylene followed by thorough drying on a clean hot plate. The adhesive used was comprised of 99% Corning Quartz Wax: 1% pure mineral oil.

To bond the silicon wafers to the graphite base plates, the base plates were preheated to approximately 100°C on a hot plate. The base plates were then removed from the hot plate, and a thin layer of the wax preparation was applied from a heated source of the material with the aid of a Q-tip. Then the wafer was lowered onto the molten waxed surface, and the assembly was allowed to cool.

The wafers were sawed with a Lindberg-Tempress dicing saw, using a 38 μm-thick blade. This blade leaves a 40 to 48 μm kerf.

The sawed devices, still mounted to the graphite base plate, were then washed with D.I. water followed by methanol.

The bumped silicon chips were loosened from the graphite base plate by soaking in trichloroethylene at room temperature, thus dissolving the wax. The chips were then collected, and cleaned by immersion in boiling trichloroethylene (two separate applications), followed by rinsing in pure acetone, and then in pure methanol, and dried.

APPENDIX VII
PREPLATE PROCESS PROCEDURE FOR CMOS WAFERS

A. Preplate Procedure

1. Apply plater's tape to the back surface of the wafer.

2. Mask edges with Shipley AZ-119 resist or equivalent

3. Etch the copper film with copper etchant (Solution VII-B-1) (approximately 15 seconds). Water rinse in D.I. water (approximately 60 seconds). Blow dry.

4. Etch the nickel/cobalt film with nickel etchant (Solution VII-B-2) (approximately 30 seconds). Water rinse in D.I. water (approximately 60 seconds).

5. Immerse in Neutra Clean 68 (Solution VII-B-3) for 5 minutes, agitating about 15 seconds each minute.

6. Rinse thoroughly in a spray D.I. water rinse.

7. Immerse in 20% sulfuric acid solution (Solution VII-B-4) for 15 to 30 seconds, with continuous agitation. Do not rinse; immediately transfer the wafer into the first plating solution.

B. Preplate Chemical Solution Parameters

1. Copper Etchant

   Bath Type: Oxidizing Alkaline Solution

   Manufacturer: Southern California Chemical Corp. - AE-25

Composition

40% part "A" aqua ammonia solution (by volume)
20% part "B" alkaline oxidizing solution
40% deionized water

Operating Conditions

Room temperature with stirring

2. Nickel Etchant

Bath Type: Oxidizing Acidic Solution

Composition

1 part sulfuric acid (97%)
1 part hydrogen peroxide (30%)
8 parts glacial acetic acid

Operating Conditions

Room temperature with stirring

3. Neutra Clean 68

Manufacturer: Shipley Company

(1) Concentration: 100%
(2) Temperature: Room

4. Sulfuric Acid Dip

(1) Concentration: 20% H_2SO_4 by volume
(2) Temperature: Room

APPENDIX VIII
POSTPLATE PROCEDURE
CMOS WAFERS

A. Postplate Procedure for Indium/Lead/Silver Bumped Wafers

1. Strip away the plastic resist film. First, soak the wafer in a solution of 93% methylene chloride/7% methyl alcohol at room temperature until the resist film begins to loosen. Remove the resist film in a spray of 93% methylene chloride/7% methyl alcohol. Rinse in a water spray, then in methyl alcohol, and blow dry. Remove remaining traces of resist in Uresolve Plus (Dynaloy) at 65°C ± 5°C for 5 minutes or at room temperature overnight. Finally, rinse in D.I. water, then in methyl alcohol. Blow dry.

2. Etch away the interconnecting copper film with copper etchant (Solution VIII-C-1) (approximately 15 seconds). Water rinse in D.I. water (approximately 60 seconds). Blow dry.

3. Etch away the interconnecting nickel/cobalt film with nickel etchant (Solution VIII-C-2) (approximately 30 seconds). Water rinse in D.I. water (approximately 60 seconds).

4. Etch away the interconnecting copper film with copper etchant (Solution VIII-C-1) (approximately 10 to 15 seconds). Water rinse in D.I. water (approximately 60 seconds). Blow dry.

5. Etch away the interconnecting nickel/cobalt film with nickel etchant (Solution VIII-C-2) (approximately 45 to 60 seconds). Water rinse in D.I. water (approximately 60 seconds).

6. Etch away both the interconnecting aluminum and chromium films with aluminum etchant (Solution VIII-C-3) (approximately 10 to 15 seconds). Rinse in hot D.I. water in a plastic vessel (approximately 15 seconds).

7. Rinse in D.I. water in a plastic vessel at room temperature (approximately 5 minutes). Rinse in methyl alcohol (approximately 60 seconds). Blow dry.

B. Postplate Procedure for Gold/Lead/Silver Solder-Bumped Wafers

1. Strip away the plastic resist film. First, soak the wafer in a solution of 93% methylene chloride/7% methyl alcohol at room temperature until the resist film begins to loosen. Remove the resist film in a spray of 93% methylene chloride/7% methyl alcohol. Rinse in a water spray, then in methyl alcohol, and blow dry. Remove remaining traces of resist in Uresolve Plus (Dynaloy) at 65°C ± 5°C for 5 minutes or at room temperature overnight. Finally, rinse in D.I. water, then in methyl alochol. Blow dry.

2. Etch away the interconnecting copper film with copper etchant (Solution VIII-C-1) (approximately 15 seconds). Water rinse in D.I. water (approximately 60 seconds). Blow dry.

3. Etch away the interconnecting nickel/cobalt film with nickel etchant (Solution VIII-C-2) (approximately 30 seconds). Water rinse in D.I. water (approximately 60 seconds).

4. Etch away the interconnecting copper film with copper etchant (Solution VIII-C-1) (approximately 10 to 15 seconds). Water rinse in D.I. water (approximately 60 seconds). Blow dry.

5. Alloy the gold/lead/silver solder (60 seconds at 350°C in a forming gas or nitrogen atmosphere).

6. Etch away the interconnecting nickel/cobalt film with nickel etchant (Solution VIII-C-2) (approximately 45 to 60 seconds). Water rinse in D.I. water (approximately 60 seconds).

7. Etch away both the interconnecting aluminum and chromium films with aluminum etchant (Solution VIII-C-3) (approximately 10 to 15 seconds). Rinse in hot D.I. water in a plastic vessel (approximately 15 seconds).

8. Rinse in D.I. water in a plastic vessel at room temperature (approximately 5 minutes). Rinse in methyl alcohol (approximately 60 seconds). Blow dry.

9. Plate gold on the solder-bumps. Plate conversion gold (Solution VIII-C-4) for approximately 5 minutes.

10. Rinse in aqueous ammonia in a plastic vessel for 15 seconds. Rinse in D.I. water in a plastic vessel at room temperature (approximately 5 minutes). Rinse in methyl alcohol (approximately 60 seconds). Blow dry.

C. Chemical Solution Parameters

1. Copper Etchant

Bath Type: Oxidizing Alkaline Solution

Manufacturer: Southern California Chemical Corp. - AE-25

Composition

40% part "A" aqua ammonia solution (by volume)
20% part "B" alkaline oxidizing solution
40% deionized water

Operating Conditions

Room temperature with stirring in a plastic container.

2. Nickel Etchant

Bath Type: Oxidizing acidic solution

Composition

1 part sulfuric acid (97%)
1 part hydrogen peroxide (30%)
8 parts glacial acetic acid

Operating Conditions

Room temperature with stirring.

3. Aluminum Etchant

Bath Type: Acidic solution

Composition

1 part hydrochloric acid (37%)
4 parts D.I. water

Operating Conditions

At 80°C with stirring in a plastic vessel.

4. Conversion Gold Plate

Bath Type: Ammonaic Cyanide Gold, Atomex

Manufacturer: Engelhard Minerals & Chemicals Corp.

Operating Conditions

Gold Concentration	1/2 ounce per gallon (3.8 g/l)
pH	7 to 8
Temperature	$75^{\circ} \pm 5^{\circ}$C with stirring

D. Discussion

These etchants are selective.

The copper etchant does not attack lead, nickel, indium, silver, or gold. Copper is etched at the rate of approximately 500 Å/sec.

The nickel etchant does not attack lead, silver, gold, or aluminum. Attack on copper is extremely slow. Nickel or nickel/cobalt alloy is etched at the rate of approximately 100 Å/sec. Indium is attacked, but the etch rate is less than half that for nickel.

It is claimed that TFG proprietary nickel etchant (Transene, Inc., Rowley, Mass) will not attack indium.

The aluminum etchant does not attack gold, silver, copper, lead, indium, or nickel appreciably.