EVALUATION OF O_2 PLASMA AND XeF_2 VAPOR ETCH RELEASE PROCESSES FOR RF-MEMS SWITCHES FABRICATED USING CMOS INTERCONNECT TECHNOLOGY

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ABSTRACT

This paper evaluates two commercially available dry etch processes for releasing integrated RF MEMS devices. The first is an oxygen microwave plasma removal of a Diamond-Like Carbon (DLC) sacrificial layer and the second is a XeF_2 vapor phase removal of an amorphous silicon (a-Si) sacrificial layer. The studied techniques were selected for compatibility in fabricating monolithically integrated RF-MEMS devices within the interconnect levels of CMOS and Bi-CMOS technologies. To determine the etch rate of the sacrificial release layer, test wafers were fabricated using a simple 1-mask lithography level that allows direct observation of the release etch through a dielectric membrane. Effects relating to changes in the release etch rate are documented and discussed. Additionally, the ability of XeF_2 to extract sacrificial layers through small via holes, and bulk vs. thin-film etching of a-Si for MEMS release etches are presented. The results of this study demonstrate that both oxygen microwave plasma removal of DLC and XeF_2 vapor phase etch of a-Si can be used to manufacture RF-MEMS devices using high volume CMOS interconnect manufacturing processes.

INTRODUCTION

A common process element in the fabrication of MEMS devices is the removal of a sacrificial layer to release the micromechanical device from a substrate. Ideally the release process removes the sacrificial layer quickly and cleanly without altering the micromechanical element. In a more specific application, such as integrating RF-MEMS devices in CMOS interconnect levels [1-2], the release process must also not degrade the existing structure or devices. While many processes exist to remove sacrificial layers [3], we have studied XeF_2 etching of Si sacrificial layers and O_2 microwave plasma etching of Diamond-Like-Carbon (DLC) sacrificial layers. Both of these techniques work well in the aforementioned application where the sacrificial layer is typically less than 1.0 μm thick and the micromechanical beam is primarily SiO_2. In addition, Si and DLC are compatible with CMOS fabrication lines and can be deposited by many different techniques. The commercially available process tools used to perform the release etch are an Applied Materials APS + chamber for the O_2 microwave plasma process and a Xactix X3 Xetch ® system.

The efficiency of the release etch can be influenced by geometric relationships that evolve as micromechanical structures are being released. Even small displacements of the micromechanical beams during the release etch can have significant effects. In this report we have fabricated structures to facilitate evaluation of both XeF_2 and O_2 microwave plasma release etching processes. The test devices were made identical to compare the two processes and gain a general understanding of the etch behavior. Structures to evaluate release etching of a sacrificial layer through via holes and of bulk Si sacrificial layer etching were also explored. For demonstration purposes, fully integrated RF-MEMS CMOS integrated switches were fabricated and tested to verify compatibility of these processes with interconnect structures. Both techniques resulted in MEMS switches with insertion loss < 0.5 dB.

EXPERIMENTAL DETAILS

The test samples used to evaluate the two release etch processes are shown in Figure 1 with optical photographs of an example device before and after the release etch. The fabrication process for these samples is as follows: for the a-Si release samples, the Si wafer is first thermally oxidized to form a 100 nm thick SiO_2 layer to protect the Si wafer from being etched in the XeF_2 process. For the DLC samples the thermal oxide layer was not required. The next step is to form the sacrificial layer which for DLC was deposited by PECVD with post 400 °C annealing and the a-Si samples were deposited by DC sputtering. After the sacrificial layer deposition, the dielectric membrane was deposited. For the a-Si release structures a single layer of PECVD SiO_2 1000 nm thick was deposited at 400°C. In the case of the DLC a sandwich structure of SiN 35 nm/SiO_2 1000 nm/SiN 35 nm was deposited by PECVD at 400°C. SiN is required to gain good adhesion between the DLC and SiO_2. To minimize stress distortion a top layer of SiN was added to "balance" the stress gradient of the structure. Lastly, the samples are coated and patterned with photoresist, etched with RIE to open the dielectric stack down to the release layer and the resist is then stripped in-situ with an O_2 plasma. The O_2 resist strip process does remove the DLC in the open areas but is timed such that no detectable undercut occurs.

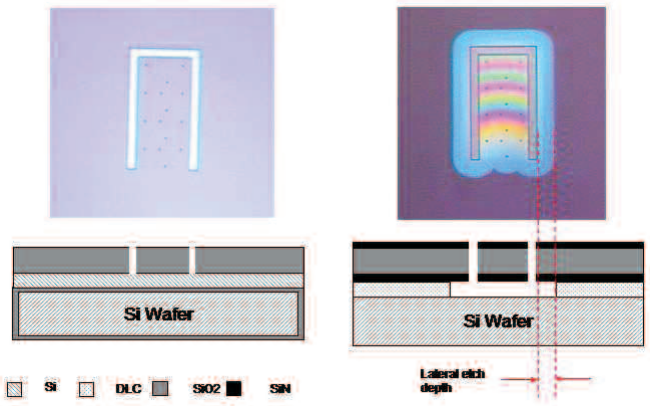

Figure 1. *Top: Optical photos of structures prior to release (left) and after release (right). Bottom: Schematic view of silicon test vehicle (left) and DLC release (right).*

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O_2 MICROWAVE PLASMA RELEASE ETCH

An Applied Materials APS+ microwave strip chamber was used to perform the O_2 microwave plasma release etches. The chamber uses IR lamps to directly heat the wafer which is placed slightly downstream of the waveguide that introduces the microwave into the chamber [4]. Key advantages to this platform for etching are the lack of ion bombardment to minimize sputtering effects and the application of heat to enhance the etch rate of the DLC. In these experiments wafer pieces were used and placed on a 200 mm wafer to allow for simultaneous processing on different structures. In all cases the gas chemistry was kept constant (O_2 3000 sccm and N_2 200 sccm) at a total pressure of 2 Torr.

Two sets of samples were fabricated to optimize the O_2 microwave plasma release process. The first set was made with a 300 nm DLC sacrificial layer. After release, the membrane was under slight tensile stress, and had very little stress related distortion. In the second set of samples, a range of DLC thicknesses was deposited (100 nm. 200 nm, 400 nm and 800 nm) to evaluate the release etch rate as a function of sacrificial layer thickness. However, the dielectric membrane for these samples was deposited using a different PECVD reactor and upon release were found to have highly distorted membranes. This was later determined to be from a temperature variation during the PECVD SiO_2 deposition that increased the compressive stress of the dielectric membrane and added a negative stress gradient within the SiO_2 layer.

As a result, upon release the membrane deflected downward towards the substrate, as shown for the device in Figure 2A. This deformation effectively narrows the release gap and causes an uneven removal of the sacrificial layer. High temperature annealing (450 ^oC) was used to minimize the stress magnitude and gradient to the point where the etch front was uniform. The stress effects were still apparent however as shown in Figure 2B. For comparison the device shown in Figure 2C is from the first sample set with a 3000 nm DLC sacrificial layer, and with a slightly tensile membrane and no stress gradient. White light interferometric measurements were used to measure the membrane deflection at mid length of the cantilever for samples after 10 min O_2 microwave plasma etch. A deflection of 10 nm to 50 nm towards the substrate was observed for the set of samples with stress related distortions, and no deflection was detected for the sample that was free of stress related distortions.

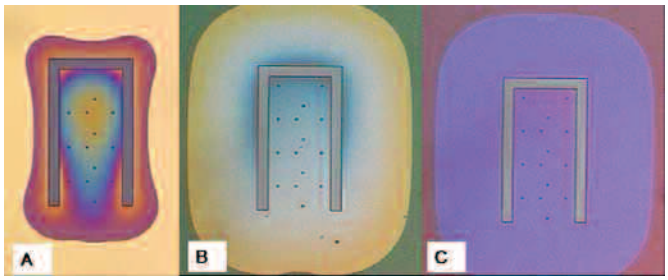

Figure 2. *Optical photograph of released test samples (cantilever 27 μm x 60 μm). Deformations in A shows a highly stressed membrane with uneven release front in as-deposited membrane. After annealing, sample B (with a 400 nm DLC sacrificial layer) demonstrates a reduced compressive stressed membrane. Sample C has a 300 nm DLC sacrificial layer, tensile membrane with no stress gradient and no stress related distortion.*

To optimize the O_2 microwave release process, wafer temperature and microwave power were varied. Shown in Figure 3 is a plot of the lateral undercut depth as a function of wafer temperature. As expected, the etch rate increases rapidly with increasing temperature, reaching rates as high as 6 μm/min. All the samples appear to have equal release etch rates until temperatures above 250 ^oC. The difference in lateral etch rate at higher temperatures may be due to diffusion limiting effects. In addition, deflection in the released membrane, which is larger for these deep undercuts, may play a significant role.

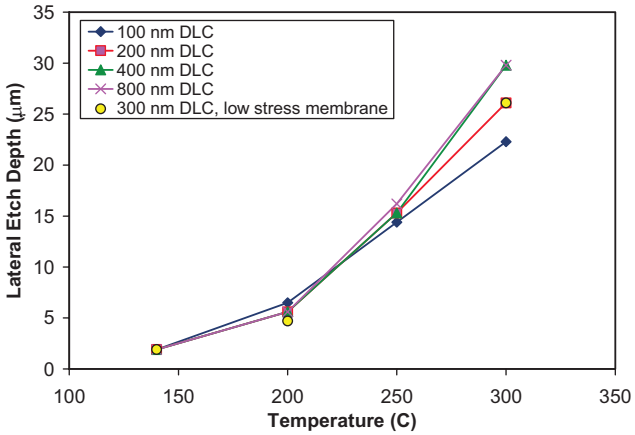

Figure 3. *Plot of lateral etch depth vs. wafer temperature during O_2 plasma microwave release at 1400 W for a 5 min. release etch.*

The effect of microwave power on the release etch rate is shown in Figure 4. A near linear increase in rate was observed up to 500 W, after which the release etch rate slowed and eventually remained constant. At this point the plasma may be at a critical density and not increase [5]. Another possible explanation for the release rate to level off would be if physical sputtering were occurring, acting as to mask the release layer. However no SiO_2 loss was observed for a 25 min 1400 W etch.

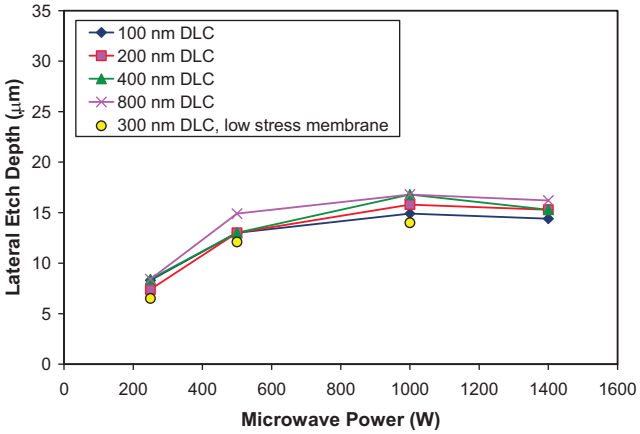

Figure 4. *Plot of release etch vs. microwave power for O_2 microwave plasma etch at 250 ^oC for 5 min.*

XeF_2 RELEASE ETCH

All Si etching experiments were performed using an X3 Series XeF_2 etching system manufactured by Xactix [6]. The XeF_2 etching is a gas phase process with no plasma and is performed at room temperature (although the Si etching process is exothermic in nature [7]). The XeF_2 release etch is a cyclical process where XeF_2 gas is introduced into a process chamber, allowed to react for a pre-determined dwell time, and pumped out. Gas pressure is established in a separate expansion chamber prior to introduction into the process chamber. The process chamber pressure is 3.4 times lower than the pressure reported here which is measured in the expansion chamber. The amount of Si etched can be controlled by the number of pulses, as well as XeF_2 pressure and concentration using N_2 as a dilutant. The samples etched for each experiment had Si exposed over 1.6% of the top surface dielectric area, and were 2x2 cm chips with the Si wafer edge exposed (a total of 0.66 μm^2). The a-Si sacrificial layers were 100, 200, 400, 600, 800 or 1000 nm thick. These samples were also annealed at 450 ^oC prior to release to reduce the as-deposited stress gradient. After release, the deflection for a 60 µm long cantilever was ~ 1 µm.

Due to the large selectivity between Si and SiO_2, all samples were etched in DHF (100:1) for 15 sec followed by a DI water rinse to remove any native oxide from the Si layer. Samples which did not receive this pre-processing step required an additional 20-30 cycles of XeF_2 in order to break through the native oxide before any etch could be observed [7]. The etch rate of thermal SiO_2 was measured to be ~60A for 20 cycles with 1.5T XeF_2 and 10T N2.

To study the effect of XeF_2 concentration on the release etch rate, two sets of samples were run at 1.5 and 3.0 Torr. A higher XeF_2 concentration is expected to lead to a faster etch rate as illustrated in Figure 5. However the release etch rate increased far more than expected. It is known that the XeF_2 etch is not 100 % efficient [7] and this data suggests the efficiency is pressure dependent. The decrease in release rate at high pressure for thinner sacrificial layers is likely diffusion related. Similar dependencies on aperture vs. lateral etch depth for thin film etching were reported for 3 Torr XeF_2 etches [7].

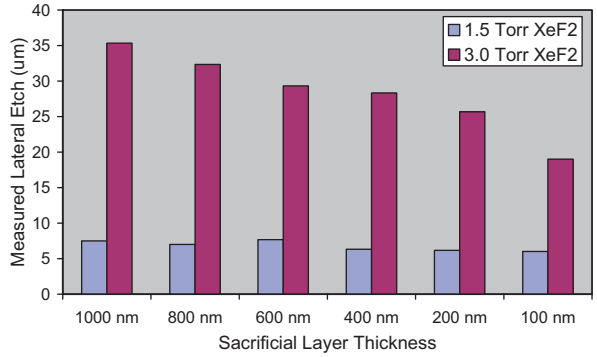

Figure 5. *Measured lateral etch rate with varying XeF_2 pressure. Both sets were run for 10 cycles, each 30 sec.*

Lateral etch rate was also measured as a function of dwell time by varying the dwell time from 5 to 60 sec for three sacrificial layer thicknesses. As seen in Figure 6, the amount of etching is relatively independent of dwell time. From this experiment is evident that the etch process happens in the first few seconds upon exposure of Si to XeF_2. The independence of exposure time was also observed for samples etched with 3.0 Torr XeF_2. This observation contradicts earlier reports on an increase in lateral etch of poly-Si with increasing pulse duration [7]. Furthermore, no pressure increase was observed in the process chamber during the etch process. As presented, this data supports a self-limiting effect or a reactant limited etch process. More experiments are in progress to determine this more accurately.

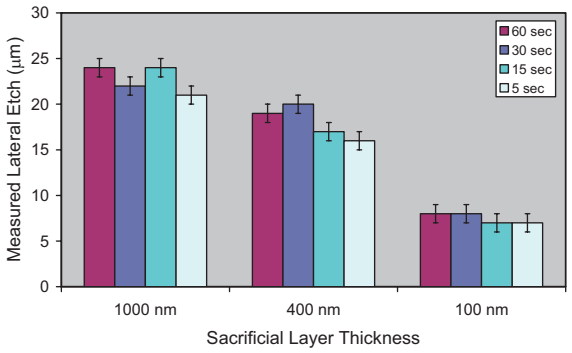

Figure 6. *Measurement on effect of cycle time on lateral etch rate. The cycle time was varied between 5 – 60 sec. for 40 cycles 1.5 Torr XeF_2.*

Adding nitrogen to raise the process pressure resulted in an increase in overall release etch rate with a maximum observed for 10 Torr N_2 and 1.5 Torr XeF_2 as shown in Figure 7. The additional nitrogen pressure increased the reaction rate of the physisorbed XeF_2 by as much as a factor of 3 while it also enhanced limited reactions.

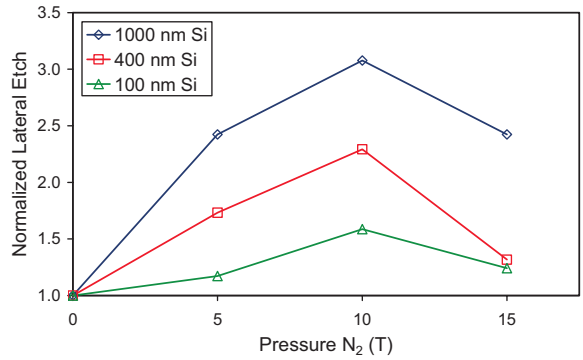

Figure 7. *Measured normalized effect of N_2 pressure on lateral etch rate. Maximum etch rate is obtained for with N_2 pressure of 10 Torr (10 cycles, 30 sec 1.5 Torr XeF_2)*

To compare bulk Si etching, samples were prepared with a single layer of patterned thermal SiO_2. Figure 8 shows a comparison between lateral etch rate for a thin film and bulk sacrificial layer. The lower undercut rate for a bulk release is not unexpected since more material is being removed, and should be factored in when releasing MEMS devices from a bulk Si-substrate. Thus, devices which depend on dielectrics and metals with low etch selectivity to Si should utilize a thin film over bulk release process as to minimize the exposure to XeF_2.

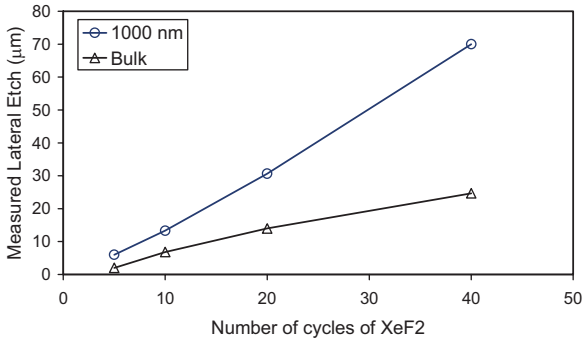

Figure 8. *Comparison of lateral etch rate of a thin-film to a bulk release process. 30 sec pulses, 1.5 Torr XeF_2 – 10 Torr N2*

COMPARISON OF RELEASE PROCESSES

Figure 9 shows a comparison between the O_2 and XeF_2 release process. For the O_2 release process, the effective etch rate decreases with lateral etch depth. This is caused by the effective surface area increase of DLC as the release etch depth increases. The flux of excited O_2 species entering the release area is determined by the geometry of the membrane cutout, which remains constant. Both release processes show a decrease in etch rate for a thin sacrificial layer, due to diffusion limitations and stress related deformation of the structural layer. It is important to note that most RF-MEMS devices typically need about 10 μm to 20 μm of a lateral etch to fully release all devices.

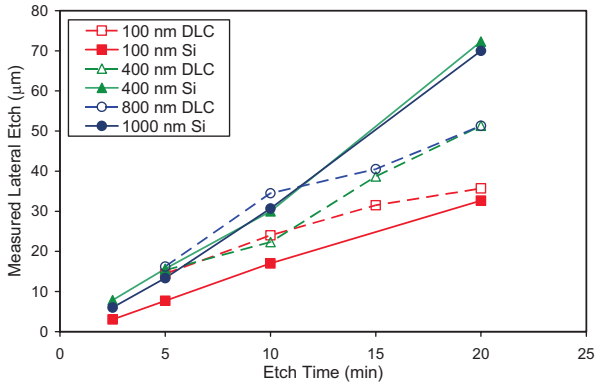

Figure 9. *Comparison of lateral etch depth vs. etch time for a 250 °C 1400 W O_2 microwave plasma and 30 sec pulsed 1.5 Torr XeF_2 – 10 Torr N_2 Si release process.*

Release can also be carried out through a dielectric film with small holes, which may subsequently be pinched off for wafer-level packaging by thin-film encapsulation. This was previously described in detail for the DLC process using the O_2 plasma release process [1]. Figure 10 shows SEM pictures of a sacrificial layer removal using XeF_2 dry etch to extract a 300 nm thick a-Si film through 0.25 μm diameter x 1.0 μm tall holes in a 1 μm thick SiO_2 film.

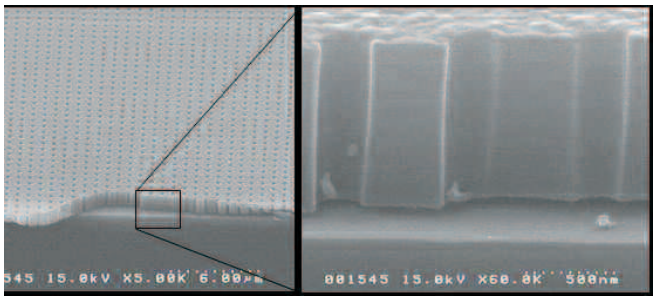

Figure 10. *SEM image of cleaved sample of hole grid pattern for XeF_2 a-Si release through a top dielectric layer with 0.25-um wide holes 1.0 μm tall. The nominal gap is 300 nm.*

SUMMARY

The results of this study demonstrate that both O_2 plasma removal of DLC and XeF_2 vapor phase etch of a-Si can be used to manufacture RF-MEMS devices using high volume CMOS interconnect manufacturing processes. Both techniques can extract a sacrificial release layer through small vias, which is a requirement for thin-film encapsulation packaging of RF-MEMS devices at wafer level. For large lateral undercuts (>20 μm), XeF_2 is superior as compared to microwave plasma etching as the release rate decrease is less pronounced. Measured RF performance of ohmic switches fabricated both with DLC and Si release layers have demonstrated excellent RF characteristics.

ACKNOWLEDGEMENTS

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