Evaluation of Level-Shifted and Phase-Shifted PWM Schemes for Seven Level Single-Phase Packed U Cell Inverter

Mohd Tariq, Mohammad Meraj, Abdul Azeem, Ali I. Maswood, Atif Iqbal, and Bharatiraja Chokkalingam

***Abstract*—An evaluation of level shifted and phase shifted triangular and sawtooth carrier modulation schemes for a seven level packed U cell (PUC) inverter is presented in this paper. The investigated PUC is the recently introduced topology for multilevel inverter having reduced switch count in comparison to the conventional topologies of multilevel inverters. The PUC inverter has six switches for 7 level inverter which is very less in comparison to the conventional topologies. In this paper, the level-shifted pulse width modulation (LS-PWM) and phase-shifted PWM (PS-PWM) for triangular and sawtooth carrier are presented and compared. A comparative harmonic analysis for all the cases is performed and results are presented in the paper. The difference in harmonics of the two modulation methods given by the theoretical approach for both the carrier is validated by the experimental results. DC voltage controller and load current controller of the PUC inverter are also designed and presented. The investigated PUC topology is tested in dynamic and steady state conditions and results obtained are presented. The analysis is done and validated using simulation in MATLAB® Simulink environment and experimental approaches using FPGA platform.**

***Index Terms*—Level shift, multilevel inverter, modulation, phase shift, PI controller, PUC inverter.**

I. Introduction

In the last two decades the risk and reality of environmental degradation have become more apparent. Fossil fuel which is the main source of energy, has led to the degradation of environment. For all these degradation and problem in environment, renewable energy sources can provide a solution [1], [2]. To meet the environmental challenges and depletion of fossil fuels, Photovoltaic (PV) source presents a highly attractive energy source during the last two decades. Multilevel inverter is required for connecting the PV sources which generates DC power to AC loads. Multilevel inverter circuits switch multiple DC sources in sequence at fundamental frequency to generate nearly sinusoidal stepped AC output voltage [3], [4].

In literature many traditional multilevel converters topologies like neutral point clamped converters (NPC), flying capacitors converters (FCC) and classic cascaded H-bridges [4]-[6] are available which enhanced the harmonic profile of the voltage and current but they offers high number of switching devices and capacitors which increases the cost and decreases the reliability. In [7], many new topologies of multilevel converter is given which offers less no. of switching device but the Packed U Cell (PUC) multilevel inverter topology is symmetrical and easy to control. For low and medium power applications where a PV panel installed at home is connected to local grid etc., a single-phase transformer-less DC-AC converter with minimum number of switch devices, capacitors and DC sources are required [8], [9]. PUC topology introduced in [10], [11] is working with only one DC source and having high power quality using a small number of passive and active components. The capacitors acts as auxiliary DC source in the PUC inverter. PUC inverter is suggested for PV application in [12] as it offers high efficiency. Many papers on control of PUC inverter are available in literature [13], [14], but a comparative analysis of different modulation carrier schemes is missing in the literature. Analysis of different carriers is essential as in local grid connected PV applications, the total harmonic distortion (THD) generated by the switching element should be minimum [15].

There are two modulation methods in the multicarrier PWM schemes: level shifted PWM (LS-PWM) [16] and phase shifted PWM (PS-PWM) [17]. Combination of the level-shifted PWM (LS-PWM) and the phase-shifted PWM (PS-PWM) is reported in [18]. It is called "level- and phase-shifted PWM (LPS-PWM)". The LPS-PWM realizes low voltage ripple on the capacitors. In [19], the comparison between the Phase-Shifted PWM and Level-Shifted PWM is done on a Modular Multilevel Single Delta Bridge Converter (SDBC) Inverter whereas in the proposed work the comparison is done on recently introduced Packed U Cell (PUC) Inverter. Since till date no such work is available on PUC inverter wherein different modulation techniques have been evaluated, hence in the proposed work, the authors wanted to investigate the effects of different modulation techniques/methods on the PUC inverter. In this paper a comparison between triangular and sawtooth carrier is done

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using level shifted and phase shifted PWM methods for PUC inverter. This study is important keeping in view the need to understand the operation of PUC inverter under different modulation schemes for achieving low THD.

The rest of the paper is organized as follows: In Section II operation of PUC inverter is explained. The generalized PWM spectral modeling is presented in Section III. Analysis of phase shifted and level shifted for triangular carrier is presented in Section IV whereas in Section V, analysis of phase shifted and level shifted for sawtooth carrier is presented. Section VI details the controller design for dc link and capacitor voltages and load current. Simulation and experimental results are presented in Section VII and VIII respectively. Conclusion is given in Section IX.

II. Operation of PUC Inverter

A seven level single-phase voltage source inverter with packed U-cell topology is shown in Fig. 1. This is called Packed U-cell because each unit of the inverter is of U shape. Depending upon the number of capacitors in the PUC topology different level of voltages can be achieved. In the PUC topology two capacitors (one is DC link capacitor and the second is the floating or flying or auxiliary capacitor) have been used to obtain seven levels (V_{dc}, $2V_{dc}/3$, $V_{dc}/3$, 0, $-V_{dc}/3$, $-2V_{dc}/3$, $-V_{dc}$). The Voltage across second capacitor (C_2) i.e. V_b must be maintained at one-third of the voltage of the first capacitor (C_1) i.e. V_a. The relation between number of voltages level achieved and number of auxiliary capacitors used can be represented by (1).

$$N_v = 2^{Nc+2} - 1 \tag{1}$$

Where: N_v is number of voltage levels and N_c is number of auxiliary capacitors used.

The numbers of devices for different types of inverters (NPC, FLC, CHB and PUC) are shown in TABLE I. Six IGBTs have been used in the PUC topology for achieving 7 levels. These 6 IGBTs are subdivided into two legs, hence only three switches form one leg. Number of possible states can be given by (2).

$$N_p = 2^{Ns} \tag{2}$$

Where, N_p is number of possible states and N_s is number of switches in one leg.

There are 8 possible switching states in a single-phase PUC inverter as shown in Fig. 2 and listed in TABLE II. It is seen that there are three positive levels and three negative levels while two states yield zero voltage, namely state 4 and state 5. Zero voltage is produced when load is short circuit either though main switches or complimentary switches.

The switching function of the PUC inverter can be defined by (3) and the inverter output voltage can be defined by (4). The points x, b, c and y are shown in Fig. 1.

Based on the switching function shown in TABLE II, each voltage can be represented as given in (5) to (8).

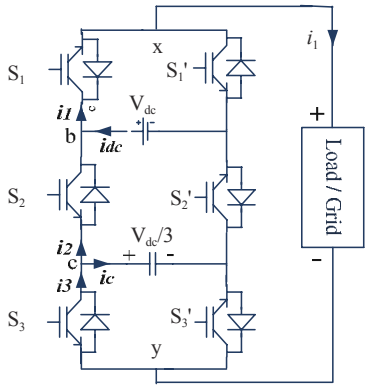

Fig. 1. Packed U-cell converter topology.

TABLE I
Seven Level Single Phase Inverter Topologies

Components	NPC	FLC	CHB	PUC
Power Switches (IGBTs)	24	24	12	6
Capacitors	6	30	3	2
Clamping Diodes	20	0	0	0

$$S_j = \begin{matrix} 0 \text{ if } S_j \text{ is Off} \\ 1 \text{ if } S_j \text{ is On} \end{matrix} \qquad j = 1, 2, 3 \tag{3}$$

$$V_{xy} = V_{xb} + V_{bc} + V_{cy} \tag{4}$$

$$V_{xb} = V_1 (S_1 - 1) \tag{5}$$

$$V_{bc} = (V_1 - V_2)(1 - S_2) \tag{6}$$

$$V_{cy} = V_2 (1 - S_3) \tag{7}$$

$$V_{xy} = V_1 (S_1 - S_2) + V_2 (S_2 - S_3) \tag{8}$$

III. Generalized PWM Spectral Modeling

The distortion in the output current or voltage waveform with respect to an ideal sine wave is often used in comparing the effectiveness of different modulation processes. Since the output voltage of an inverter is a periodic function having time period (T), the root-mean-square (RMS) value of the function can be defined as:

$$V_{rms} = V_{1,rms} \sqrt{1 + THD^2} \tag{9}$$

From (9), it is to be noted that if the THD is zero then the RMS value of the waveform is equal to the fundamental RMS voltage. Hence, it is clear that the modulation technique has to be designed in such a way so as to obtain the minimum THD or ideally zero THD. Moreover, when the inverter is connected to the induction motor operating pump for standalone solar PV pumping application, it is to be noted that the total copper loss

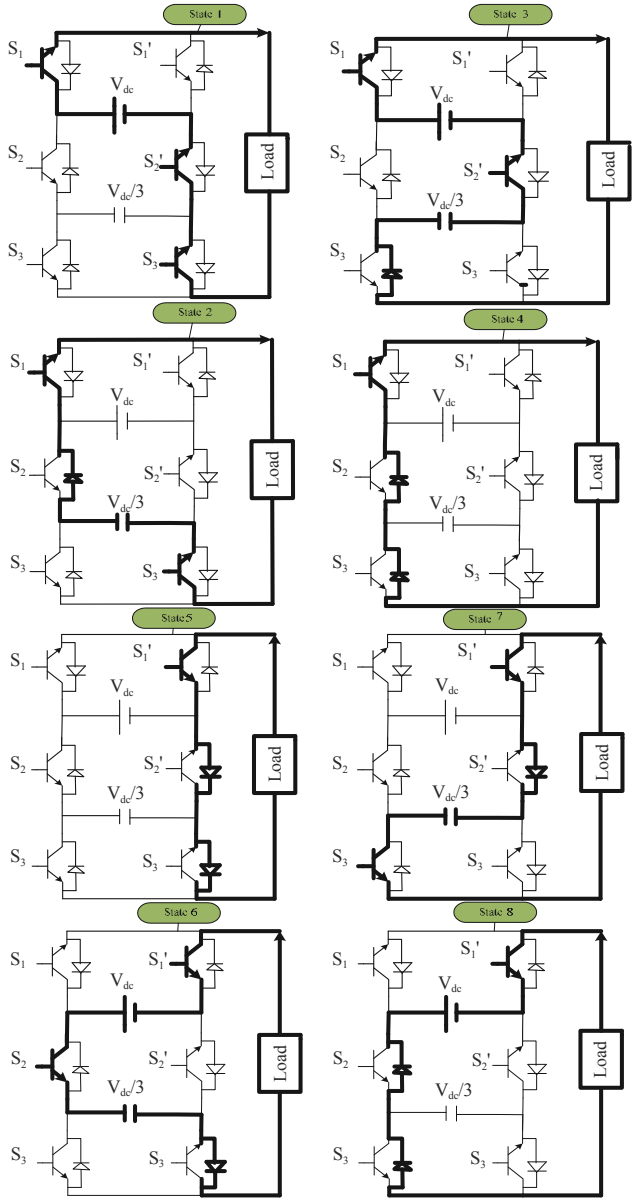

Fig. 2. Switching states for single-phase AFLC/PUC.

TABLE II
SWITCHING COMBINATION FOR ONE LEG OF PUC

State	Voltage	S_1	S_2	S_3
0	V_a	1	0	0
1	V_a - V_b	1	0	1
2	V_b	1	1	0
3	0	1	1	1
3'	0	0	0	0
4	-V_a	0	0	1
5	V_b - V_a	0	1	0
6	-V_b	0	1	1

due to the harmonic content in the quasi-square-wave inverter can be 0.5-1% of the rating. Hence all these leads to the formulation of modulation strategies for reducing the component of harmonics in the inverter output voltage.

The mathematical model is developed for PWM triangular and sawtooth carrier signals for the defined reference here for better understanding of the subject. The PWM output spectrum is described using the analytical models when different carrier signals (triangular/sawtooth) are used.

Fourier series is used to represent a periodic function. For the presented application, Fourier analysis is performed on the PWM waveform for 50 Hz (20 milliseconds period) which corresponds to one cycle of the reference. The switching point as shown in the pulse width modulation waveform of Fig. 6(I)(a), Fig. 6(I)(b), Fig. 6(I)(c), and Fig. 6(I)(d) is described using the trigonometry equation given in (10). The trigonometric equation involves both the linear function of time (which basically represent carrier signal) and a sinusoidal reference.

$$s(t) = S_0 + S_1 \cos(2\pi f_1 t + \theta_1) \tag{10}$$

In the next two sections, (10) is used for doing the spectral analysis of various pulse width modulation methods. Depending upon the application under study, in (10), S_0 and S_1 are set to zero. For solving (10), a new two-dimensional function (double Fourier series for decomposing the function) given in (11) is introduced in the literature wherein the reference fundamental and the carrier frequency are corresponding to an independent variable respectively [20]. A periodical 2 (two) dimensional function f (x, y) having periodicity in x and y both, with a time period equal to 2π for both the axes, is represented by a double Fourier series which is mathematically expressed here in (11).

$$\begin{aligned} f(x,y) = \frac{A_{00}}{2} + \sum_{n=1}^{+\infty} \left(A_{0n} \cos ny + B_{0n} \sin ny \right) \\ + \left(A_{m0} \cos mx + B_{m0} \sin mx \right) \\ + \sum_{m=1}^{+\infty} \sum_{n=\pm 1}^{\pm\infty} \left(A_{mn} \cos(mx+ny) + B_{mn} \sin(mx+ny) \right) \end{aligned} \tag{11}$$

Where the coefficients A_{mn} and B_{mn} are defined as follows in (11) and (12)

$$A_{mn} = \frac{1}{2\pi^2} \int_0^{2\pi} \int_0^{2\pi} f(x,y) \cos(mx+ny)\, dx\, dy, \tag{12}$$

$$B_{mn} = \frac{1}{2\pi^2} \int_0^{2\pi} \int_0^{2\pi} f(x,y) \sin(mx+ny)\, dx\, dy. \tag{13}$$

In (11), the PWM waveform contains the fundamental sine, the DC and many harmonics components described (grouped) as follows:

(i) Carrier frequency and its associated harmonics.
(ii) Sideband harmonics of the carrier and its associated harmonics. The sideband harmonics appears because of the modulated reference.

For sawtooth carrier modulation the sideband harmonic amplitude at frequency $f = mf_c + nf_1$ equals to as given in (14),

whereas for triangular carrier modulation it equals to as given in (15). In (14) and (15), the $J_n(z)$ which is a Bessel function is defined as given in (16):

$$\frac{J_n(m\pi M)}{m\pi} \tag{14}$$

$$\frac{2}{m\pi}J_n\left(\frac{m\pi M}{2}\right) \tag{15}$$

$$J_n(z)=\frac{j^{-n}}{\pi}\int_0^{2\pi} e^{jz\cos\theta}\, e^{jn\theta}\, d\theta \tag{16}$$

In (16), the argument z can be a complex or real number. If z is real, the function will also be real. Whereas, "n" will be an integer always. Bessel functions $J_0(x)$ through $J_{10}(x)$ is shown in the Fig. 3. The double Fourier series and Bessel functions are used in the analysis of the triangular and sawtooth carrier modulation techniques in the next two sections.

IV. Triangular Carrier Level Shifted and Phase Shifted PWM Analysis

The triangular carrier based modulation scheme is given in Fig. (4) wherein the formulation of double Fourier series is shown. Fig. 4(a) shows the triangular and reference signals. Fig. 4(b) shows the resulting PWM output which is expressed mathematically in (17). As shown in Fig. 4(c) the original carrier along with the reference are sequenced in the correct and inverted position alternatively. The stacked carriers are mathematically written as c(t), $2C_m-c(t)$, $2C_m+c(t)$, $4C_m-c(t)$, whereas the stacked references can be mathematically expressed as r(t), $2C_m - r(t)$, $2C_m + r(t)$, $4C_m - r(t)$. As seen in Fig. 4(c), line AB is the extension of the rising edge of the first triangle of the original carrier, c(t). It can be observed that the PWM generated by the interaction between the original carrier and reference signal and PWM generated with the intersection of the line AB with the references shifted (stacked).

$$\begin{aligned} b_{pwm}(t) = {} & D+\frac{M}{2}\cos(\omega_1 t+\theta_1) \\ & +\sum_{m=1}^{+\infty}\frac{2}{m\pi}J_0\left(\frac{m\pi M}{2}\right)\sin(Dm\pi)\cos\left[m(\omega_c t+\theta_c)\right] \\ & +\sum_{m=1}^{+\infty}\sum_{n=\pm1}^{\pm\infty}\frac{2}{m\pi}J_n\left(\frac{m\pi M}{2}\right)\sin\left(\frac{(2Dm+n)\pi}{2}\right) \\ & .\cos\left[m(\omega_c t+\theta_c)+n(\omega_1 t+\theta_1)\right]. \end{aligned} \tag{17}$$

The phase voltage of an inverter with natural sampled PWM and triangular carrier can be described by (18). (18) is derived in [21] using the expression given in the works of Black in [22]. The three terms in (18) are explained as: a) Term 1 is directly proportional to the modulation index and it represents the fundamental frequency amplitude; b) Term 2 represents the carrier frequency harmonics amplitude and multiples of the carrier frequency and it is due to the presence of the sin (mt/2); c) Term 3

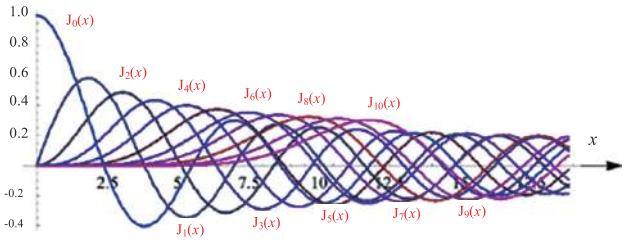

Fig. 3. Bessel functions plot for $J_0(x)$ to $J_{10}(x)$ [20].

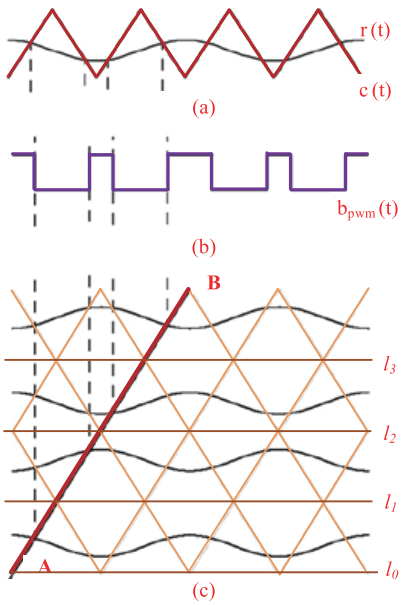

Fig. 4. Triangular carrier and development of a double Fourier series.

gives the amplitudes of the harmonics in the sidebands around each multiple of the carrier frequency.

$$\begin{aligned} F(t) = {} & \frac{MV}{2}\cos(\omega_F t)+\frac{2V}{\pi}\sum_{m=1}^{\infty}J_o\left(mM\frac{\pi}{2}\right)\sin\left(m\frac{\pi}{2}\right).\cos(m\omega_c t) \\ & +\frac{2V}{\pi}\sum_{m=1}^{\infty}\sum_{n=\pm1}^{\pm\infty}\frac{J_n\left(mM\frac{\pi}{2}\right)}{m}.\sin\left((m+n)\frac{\pi}{2}\right)\cos(m\omega_c+n\omega_F t) \end{aligned} \tag{18}$$

Fig. 6(I)(a), Fig. 6(I)(b), Fig. 6(I)(c), and Fig. 6(I)(d), shows level shifted and phase shifted triangular carrier and sinusoidal reference signal generation of PWM signals for IGBT switches of inverter.

V. Sawtooth Carrier Based Level Shifted and Phase Shifted PWM Analysis

The sawtooth carrier based modulation scheme is given in Fig. 5 wherein the formulation of double Fourier series is shown. Fig. 5(a) shows the triangular and reference signals. Fig. 5(b) shows the resulting PWM output which is expressed mathematically in (19). As shown in Fig. 5(c) the original carrier along with the reference are stacked equidistantly. The stacked carriers are

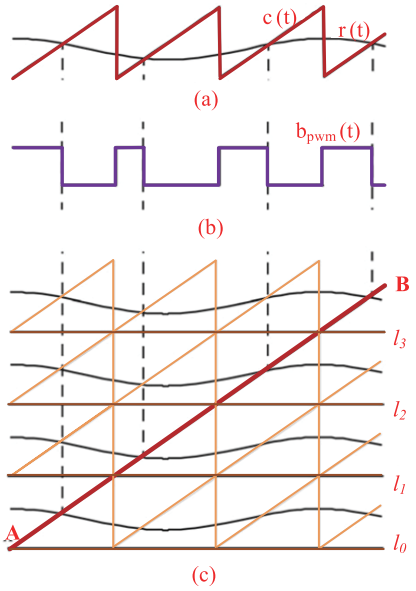

Fig. 5. Sawtooth carrier and development of a double Fourier series.

mathematically written as c(t), C_m + c(t), $2C_m$ + c(t), whereas the stacked references can be mathematically expressed as r(t), C_m + r(t), $2C_m$ + r(t). As seen in Fig. 5(c), line AB is the extension of the first slope of the original sawtooth signal. The lines l_1, l_2, l_3 and l_4 (shown horizontally) is separating the different stacked carriers with a spacing of C_m between them. It can be observed that the PWM generated by the interaction between the original carrier and reference signal and PWM generated with the intersection of the line AB with the references shifted (stacked).

The sawtooth carrier wavesas shown in Fig. 6(II)(a), Fig. 6(II)(b), Fig. 6(II)(c), and Fig. 6(II)(d) consists of sawtooth carrier as well as inverted sawtooth carrier. This arrangement is done so as to produce the trailing edge modulation in the positive cycle and to produce the leading edge modulation in the negative cycle. The trailing-edge modulation scheme has a wave having the leading (rising) edge of PWM output occurs at fixed instants in time while the position of the trailing (falling) edge is modulated as the reference signal level varies. Similarly, for leading edge modulation scheme has the trailing (falling) edge of PWM output occurs at fixed instants in time while the position of the leading (rising) edge is modulated as the reference signal level varies.

$$b_{pwm}(t) = D + \frac{M}{2}\cos(\omega_1 t + \theta_1) + \sum_{m=1}^{+\infty}\frac{1}{m\pi}\begin{Bmatrix}\sin\left[m(\omega_c t+\theta_c)\right] \\ -J_0(m\pi M)\sin\left[m(\omega_c t+\theta_c)-2mD\pi\right]\end{Bmatrix} + \sum_{m=1}^{+\infty}\sum_{n=\pm 1}^{\pm\infty}\frac{J_n(m\pi M)}{m\pi}\sin\begin{bmatrix}\frac{n\pi}{2}-m(\omega_c t+\theta_c) \\ -n(\omega_1 t+\theta_1)+2mD\pi\end{bmatrix} \quad (19)$$

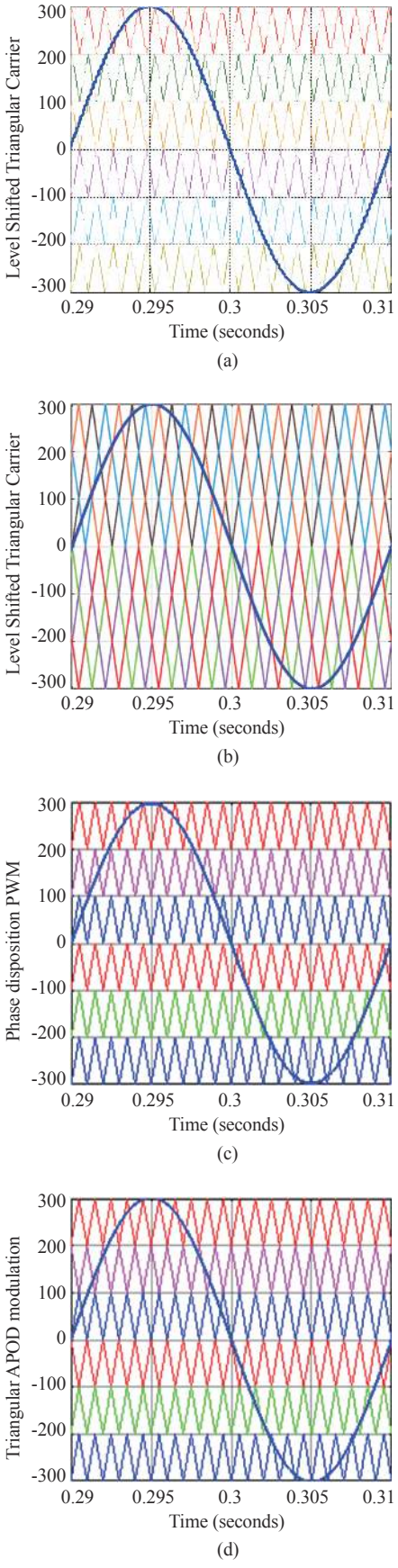

Fig. 6(I). Triangular carrier waves. (a) Phase opposition disposition. (b) Phase shifted. (c) Phase disposition. (d) Alternate phase opposition disposition.

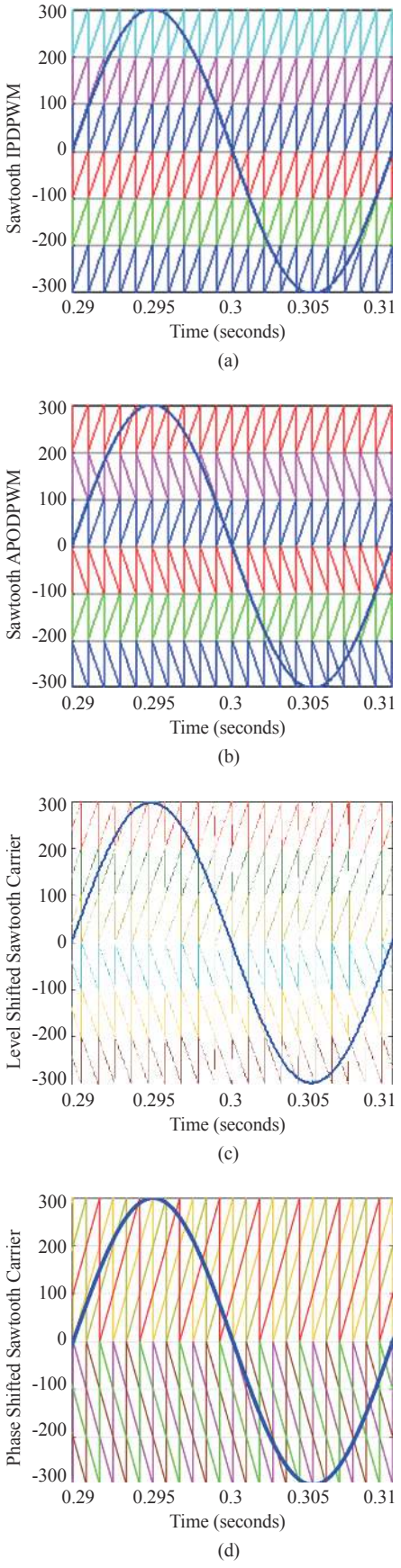

Fig. 6(II). Sawtooth carrier waves. (a) Phase disposition. (b) Alternate phase opposition disposition. (c) Phase opposition disposition. (d) Phase shifted.

$$F(t)=\frac{MV}{2}\cos(\omega_F t)+\frac{V}{\pi}\sum_{m=1}^{\infty}\frac{\sin(m\omega_c t)}{m} - \frac{V}{\pi}\sum_{m=1}^{\infty}\frac{J_o(mM\pi)}{m}\left[\cos(m\pi)\sin(m\omega_c t)\right] - \frac{V}{\pi}\sum_{m=1}^{\infty}\sum_{n=\pm1}^{\pm\infty}\frac{J_n(mM\pi)}{m}[\cos(m\pi+n\pi/2).\sin(m\omega_c+n\omega_F t) - \sin(m\pi+n\pi/2).\cos(m\omega_c t+n\omega_F t)]. \quad (20)$$

The phase voltage of an inverter with natural sampled PWM and sawtooth carrier can be described by (20).

(10) is derived in [21] using the expression given in the works of Black [22]. Here again, the amplitude of the fundamental is directly proportional to modulation index. Whereas the second and third term shows that all harmonics of the carrier frequency is existing in the phase voltage.

In (18) and (20):

ω_F = frequency of the fundamental (reference)

ω_c = frequency of the carrier signal (rad/s),

M = modulation index, V= value of the dc supply voltage,

J_o, J_n = Bessel functions of the first kind.

VI. Design of DC-Link Volatge, Auxiliary Capacitor Voltage and Load Curremt Controllers

A. Voltage Controllers

The solar PV is considered as the source (DC link) of the analysed PUC inverter. In PV applications, using capacitors of electrolytic type will be less desirable because of short lifetime mainly when installed in outdoor temperatures. Film capacitors have very long life time hence these can replace electrolytic capacitors, however they have very high prices. This makes practical limitation for dc link capacitor, establishing significant doubly frequency ripple on dc link and clamping capacitor voltages. This doubly frequency ripple further couples with control loop & causes distortions in output current.

Therefore, a notch filter (stop band filter) is placed on the feedback signal of DC voltage to attenuate ripple component. Notch filter is given as in (21).

$$H(s)=\frac{s^2+2\varepsilon_1\omega_n s+\omega_n^2}{s^2+2\varepsilon_2\omega_n s+\omega_n^2} \quad (21)$$

Where ω_n is double of fundamental frequency. For getting maximum number of output voltage levels from the inverter, the auxiliary capacitor or holding capacitor voltage should be held at one third of dc link voltage. A simple PI controller is used to control the voltage of the auxiliary capacitor voltage and dc link voltage. The load current is represented as in (22).

$$i_L = c\,\frac{dv_c}{dt} \quad (22)$$

Assuming a phase margin of 75° and critically damped system with damping factor ε=1.The transfer function of the sys-

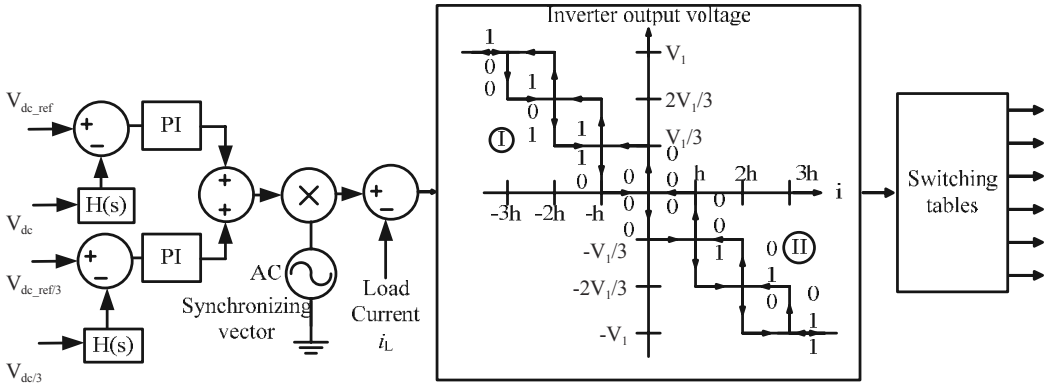

Fig. 7. Control block diagram for generation of gate pulses.

tem is given as in (23), (24):

$$G(s) = \left(K_p + \frac{K_I}{s}\right) * \left(\frac{1}{sC}\right) \tag{23}$$

$$G(j\omega) = \frac{K_I + j\omega K_p}{-\omega^2 C} \tag{24}$$

The phase of the system can be written as in (25):

$$Phase\,(G\,(j\omega)) = -180° + \tan^{-1}\left(\frac{\omega K_p}{K_I}\right) \tag{25}$$

$$\begin{aligned} -180° + 75° &= -180° + \tan^{-1}\left(\frac{\omega K_p}{K_I}\right) \\ (3.73^2 + 1)\,K_I^2 &= (10)^4 * 2.2^2 * 10^{-6} \end{aligned} \tag{26}$$

The phase margin of the system is 75°. Thus, $K_I = 0.06$, $K_p = 0.02$ as calculated from (26).

B. Current Controller

From Fig. 1, on applying KVL on the load or grid side, (27) and (28) are achieved:

$$\text{For RL load: } V_{an} = R * i_L + L\frac{di_L}{dt} \tag{27}$$

$$\text{For grid load: } V_{an} = R_f * i_L + L_f\frac{di_L}{dt} + V_{ac} \tag{28}$$

Here R & L are load resistor & reactor and R_f & L_f are filter inductor internal resistance & inductance. For generationof seven level output voltage, one should control the DC-link & auxiliary capacitor voltages to V_{dc} and $V_{dc}/3$, respectively. This has been done by voltage controllers as shown in Fig. 7. When actual injected current into grid or load is lower than reference (current error) then positive voltage across the load is applied thus Fig. 7 sector I are applied.When actual injected current into grid or load is greater than reference (current error) then negative voltage across the load is applied thus Fig. 7 sector II are applied.

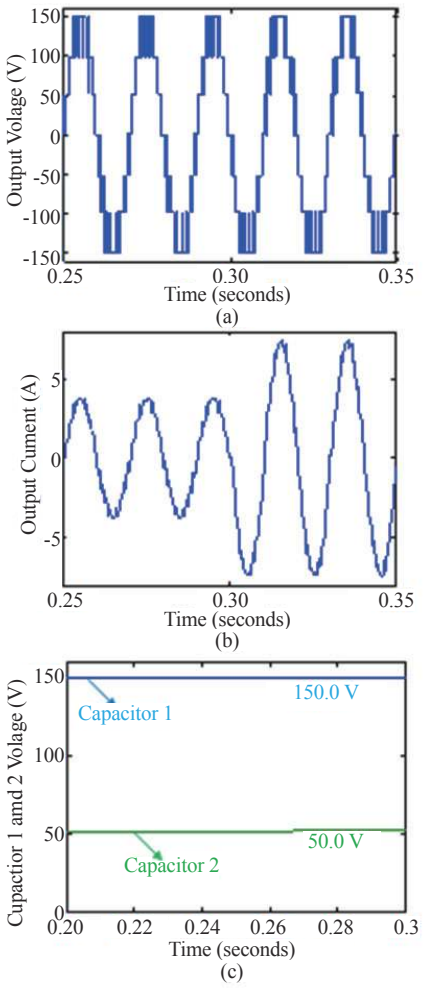

Fig. 8. (a) Output voltage; (b) Output current; (c) Capacitor voltage.

VII. Simulation Results and Discussion

The PUC inverter model is built using MATLAB®/Simulink simulation software package to verify the performance of different triangular and sawtooth carrier-based PWM modulation schemes. In line to the above, single DC source is selected of 150 V. The second capacitor has the voltage rating of 1/3rd of the DC source. Fig. 8(c) shows the capacitor voltages to be 150 V

TABLE III
THE OPERATING CONDITIONS FOR SIMULATION

Simulation Set up Parameters	Rating
Capacitors	4700 μF
Load Resistance	40 Ω
Load Inductance	12 mH
Modulating Frequency	1 kHz
Load Change (at time)	0.3 seconds

Fig. 9. Experimental set up.

and 50 V. Seven level output voltage (shown in Fig. 8 (a)) is obtained using TABLE II switching combination. TABLE III outlines the operating condition of PUC inverter for simulation. The value of inductor andresistance at the load is 12 mH and 40 ohm respectively. At 0.3 seconds the load was doubled, hence the current doubles at 0.3 seconds (as shown in Fig. 8(b)). At 0.3 seconds, two 40 ohm resistors were connected in parallel to make 20 ohm effective resistance. It can be observed that the output voltage is unchanged at 0.3 seconds thus verifying the effectiveness of the closed loop control.

VIII. EXPERIMENTAL RESULTS AND DISCUSSION

Experimental investigation is done to validate the theoretical findings and simulation results presented in the paper so far. Experiment is conducted with customised hardware comprising of Semikron modules SKM75GB12T4 as shown in Fig. 9. Control code is written in system generator and processed using FPGA board Vortex 5. Fluke 42B power analyser is used to to record the total harmonic distortion (THD) in the voltage and current waveform.The experimental parameters is presented in TABLE IV where the parameters are chosen to match with the available components. Fig. 10 shows the experimental result showing 7 level waveform and sinusoidal fundamental of PUC inverter output voltage and sinusoidal load current. It can be observed from the figure that the load current is in phase with the fundamental output of the PUC waveform. The dynamics of DC link voltage control loop and load current loop is tested and the resulting waveforms are presented in Fig. 11, Fig. 12, Fig. 13. The DC link voltage is ramped down from 54 V to 36 V (33% decrease in the initial value) and the transients are recorded in Fig. 11. The DC link voltage is seen to quickly drops to the new value and correspondingly the auxiliary capacitor voltage follows the change. The output voltage level drops and the current magnitude drops accordingly. Further test is conducted by increasing the DC link voltage value and the corresponding results are shown in Fig. 13. The DC link voltage is ramped up from 36 V to 54 V (50% increase in the initial value). The auxiliary capacitor voltage is seen to follow the change and settle to the new value and the voltage and current follows the change quickly. Hence it is concluded that both the DC voltage control loop and load current loop have large control bandwidth with fast dynamics. The THD is calculated using Fluke 42B power analyser for different modulation schemes and are shown in Fig. 12(a) to Fig. 12(p). The THD obtained are tabulated in TABLE V wherein the THD for voltage and current both are shown to be minimum for the case of level shifted triangular carrier.

TABLE IV
EXPERIMENTAL SET UP PARAMETERS

Parameter	Value
Auxiliary Capacitor	4700 μF
Load Resistance	4 Ω
Load Inductance	10 mH
Modulating Frequency	1 kHz
Sinusoidal Reference Frequency	50 Hz
DC link voltage	54 V
Dead-band period	2μS

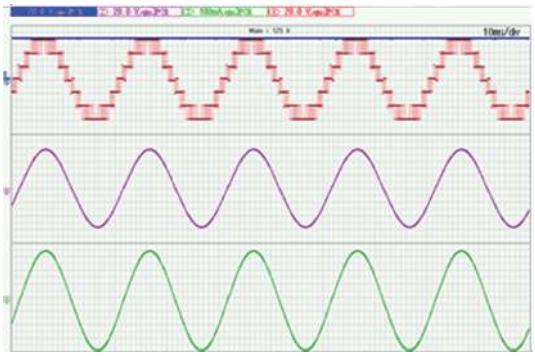

Fig. 10. Experimental result showing 7 level waveform and sinusoidal fundamental of PUC inverter output voltage and sinusoidal load current.

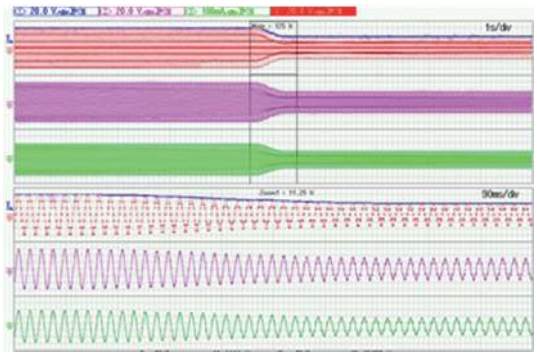

Fig. 11. Experimental result showing dynamic condition when load current is decreased.

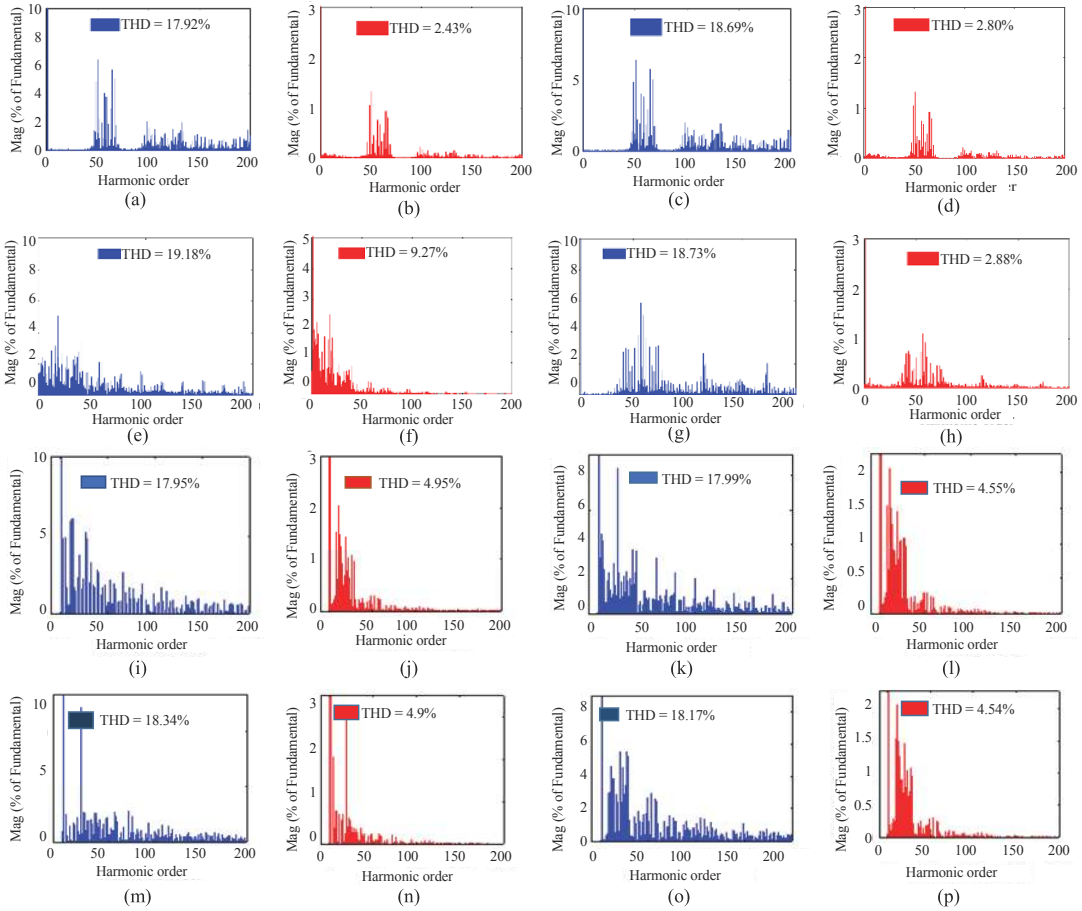

Fig. 12 (a) FFT of voltage for triangular PD-PWM scheme; (b) FFT of current for triangular PD-PWM scheme; (c) FFT of voltage for triangular phase shifted scheme; (d) FFT of current for triangular phase shifted scheme; (e) FFT of voltage for sawtooth PD-PWM scheme; (f) FFT of current for sawtooth PD-PWM scheme; (g) FFT of voltage for sawtooth phase shifted scheme; (h) FFT of current for sawtooth phase shifted scheme; (i) FFT of voltage for sawtooth AOPD; (j) FFT of current for sawtooth APOD; (k) FFT of voltage for sawtooth IPD; (l) FFT of current for sawtooth IPD; (m) FFT of voltage for triangular IPD; (n) FFT of current for triangular IPD; (o) FFT of voltage for triangular APOD; (p) FFT of current for triangular APOD.

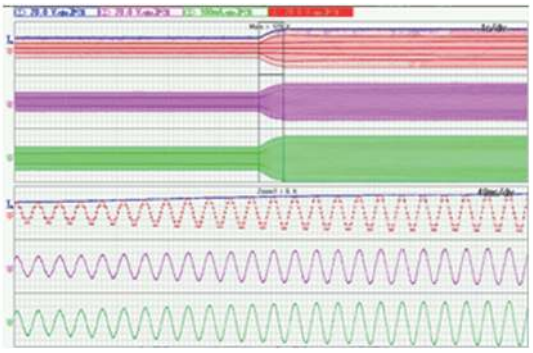

Fig. 13. Experimental result showing dynamic condition when load current is increased.

TABLE V
FFT Results for Different Modulation Schemes

Particulars	THD (in %)	
	Triangular Carrier	
PWM Schemes	*Voltage*	*Current*
PD-PWM	18.34	4.90
POD-PWM	17.92	2.43
APOD-PWM	18.17	4.54
Phase-Shifted	18.69	2.80
	Sawtooth Carrier	
PD-PWM	17.99	4.54
POD-PWM	19.18	9.27
APOD-PWM	17.95	4.54
Phase-Shifted	18.73	2.88

IX. Conclusion

The paper has presented the comparison of different PWM schemes which can be applied to the PUC inverter. Investigating the suitable modulation schemes is very essential with respect to local grid integration, as the power quality is directly dependent on THD. Triangular carrier based PWM schemes is exhibiting the better result than the sawtooth carrier based PWM schemes as the triangular level shifted carrier PWM scheme is better as compared to sawtooth level shifted carrier because in triangular level shifted carrier both edges (falling and rising) of pulses are modulated which improves the harmonic spectrum. However, in the sawtooth level shifted carrier only rising edges are mod-

ulated. Hence triangular level shifted carrier PWM scheme can be applied for integrating the PUC inverter with PV and local grid systems. Triangular level shifted carrier PWM scheme for PUC inverter has been suggested based on observing the THD in voltage and current which are respectively just 17.92% and 2.43%. The whole system i.e. solar panel, boost converter with PUC inverter will be very cost effective, besides having good reliability and power quality as it has the minimum number of power electronics devices compared to previously introduced multilevel inverter topologies. With reduced number of capacitors and power switches seven levels of voltages have been achieved for PUC inverter.

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