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Evaluation Procedures for Wafer Bonding and Thinning of Interconnect Test Structures for 3D ICs

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Abstract -- Electrical and mechanical impacts of wafer bonding and thinning processes required for three-dimensional (3D) IC fabrication have been evaluated with interconnect structures. In addition to the bonding and thinning required for a two-level 3D IC stack, an additional bonding and thinning process is used along with dielectric glue ashing to expose the previously tested interconnect structures. This procedure permits evaluation of bonding and thinning integrity without inter-wafer interconnect processing. Promising results on wafers with oxide inter-level dielectric (ILD) have been obtained, while some damages observed with the porous low-k ILD.

I. Introduction

One of the emerging architectures/technologies for future chips is wafer-level three-dimensional (3D) integration [1,2], i.e., fabrication of functional components (e.g., logic and memory) on separate wafers, followed by wafer aligning, bonding, thinning and vertical inter-wafer interconnection [3]. The 3D integration offers high interconnect performance by reducing delays of global interconnects [2] and high functionality with heterogeneous integration of materials, devices, and signals [1-4]. Initial focus of the 3D integration has been on microprocessors, application specific ICs (ASICs), and memories, but extensions to RF, analog, optical, and micro-electro-mechanical systems (MEMS) are also being pursued [1-5].

One of the fundamental issues in all 3D IC implementations [2-11] is the 3D processing compatibility with advanced semiconductor processing protocols. We have developed procedures to evaluate the impact of wafer bonding and thinning processes on the performance and yield of wafers without requiring inter-wafer interconnect processing. Wafers with state-of-the-art two-level back-end copper interconnect test structures with two types of inter-level dielectrics (ILDs) are evaluated. Promising results are obtained on wafers with oxide ILD, while wafers with porous low-k ILD show some damage. Both the types of wafers were provided by International SEMATECH.

II. Experimental Results and Discussion

The experimental procedures to evaluate the wafer bonding and thinning processes are based on our 3D integration approach, which is also referred to as monolithic high density multifunctional integration (HDMI) or hyper-integration (see [3] for more details). Fig. 1 is a schematic of our approach, where fully processed wafers (with multilevel on-chip interconnects) are aligned and bonded with a dielectric glue, followed by top-wafer thinning and inter-wafer interconnection. Among other process steps, wafer bonding and thinning involve thermal and mechanical processes; their impacts on the processed wafers need to be evaluated to qualify the process.

Various procedures are developed for specific evaluation purposes. Three evaluation procedures are discussed in this paper: (1) visual inspection using thermal-coefficient-of-expansion (TCE) matched glass wafers, (2) mechanical bonding strength tests using four-point (4-pt) bending/delamination technique, and (3) electrical tests of the processed wafers using a procedure that involves additional bonding, thinning and dielectric glue ashing.

In order to visually evaluate the bonding and thinning integrity, an interconnect test structure wafer with 900 nm topological features across the Al test pads was bonded onto a TCE-matched glass wafer using benzocyclobutene (BCB). The use of TCE matched glass allows visual inspection of the bonding and thinning integrity through the glass wafer. The Si substrate was then completely removed by a three-step thinning process: grinding, polishing and tetramethyl-ammonium hydroxide (TMAH) wet etching. Typically the grinding and polishing processes thin the Si substrate to 30 – 50 μm. Subsequent wet etching stops at the oxide layer, leaving a transparent Cu/oxide interconnect structures on the glass wafer. Fig. 2 shows an image of transparent Cu/oxide interconnect structures on a TCE-matched glass wafer. Detailed optical microscopy inspection indicates a defect-free bonding interface with damage-free interconnect patterns maintained. For similarly processed wafers with

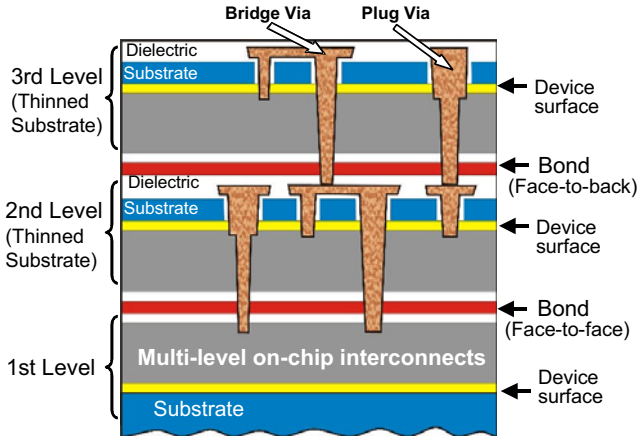

Fig. 1. Schematic of a monolithic 3D IC test vehicle using wafer bonding, showing bonding interface, vertical inter-chip vias (plug- and bridge-type), and "face-to-face" and "face-to-back" bonding.

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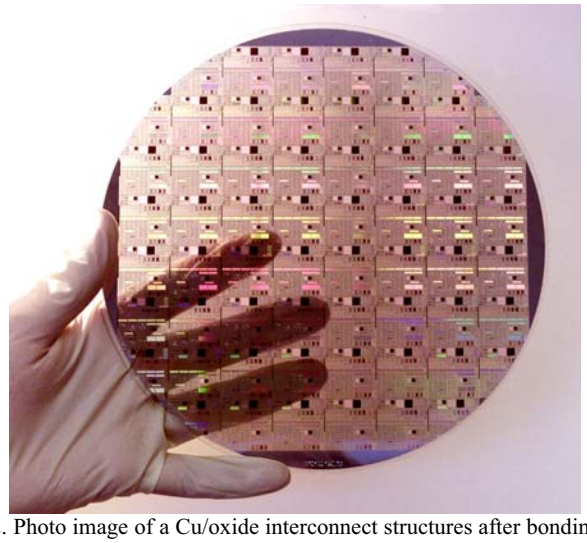

Fig. 2. Photo image of a Cu/oxide interconnect structures after bonding to a glass wafer using BCB and removing the Si substrate by grinding, polishing and TMAH etching.

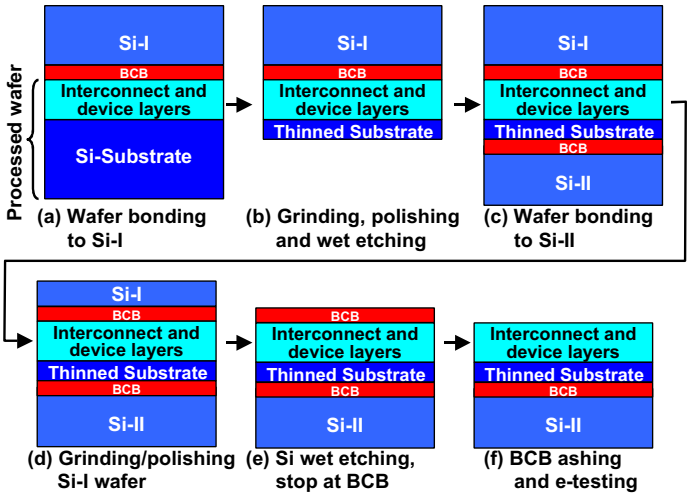

Fig. 4. Process flow of a typical double bonding/thinning procedure, permitting bonding and thinning integrity evaluation without inter-wafer interconnect processing.

porous low-k ILDs, results are not uniform across the wafer, indicating that ILD damage occurs during bonding and/or thinning.

To evaluate the bonding integrity, a four-point (4-pt) bending technique is used. With this technique, the weak interface of the bonded structures can be identified and the critical adhesion energy of the interface can be determined. Two sets of bonded wafer pairs are compared. Set A consists of two thermally oxidized prime silicon wafers (called "blanket" wafer) bonded using our baseline BCB bonding process. Set B consists of interconnect test wafers bonded to a "blanket" wafer. The wafer with porous low-k two-level copper interconnect structures is of particular interest because of the relatively weak mechanical strength of the porous low-k ILD. The bonded wafer pair is diced into specimens with nominal dimensions of 40 mm x 4 mm x 1.5 mm, followed by pre-crack creation and chemical treatments. The measured critical adhesion energy of the weakest interface is ~ 30 J/m^2 for wafer set A and ~ 6 J/m^2 for wafer set B.

Fig. 3 represents optical microscopic images of the surfaces on the interconnect wafer (Fig. 3a) and the "blanket" wafer (Fig. 3b) in the same lateral position after 4-pt bending test with a set B wafer. A layer of the interconnect structures and some traces of the Al pads adhered to the "blanket" wafer. These images show that

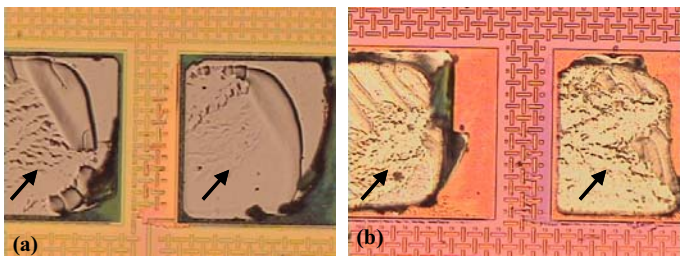

Fig. 3. Surfaces of a delaminated bonded wafer pair (a) on Cu/low-k wafer, and (b) on "blanket" wafer after 4-pt bending tests. Arrows indicate Al features in bond pad area (originally bond pad only on interconnect wafer).

delamination of the wafer from set B occurs in the porous low-k interconnect structure rather than at the BCB bonding interface. Considering the difference in the adhesion energy between sets A and B, we conclude that the BCB bond strength is higher than that of porous low-k interconnect structures.

A more aggressive evaluation procedure with a double bonding and thinning process is depicted in Fig. 4. Wafer Si-I and/or Si-II can be either a prime silicon wafer with or without a SiO_2 layer, a prime silicon-on-insulator (SOI) wafer, or a TCE matched glass wafer. If the processed wafer is an SOI wafer, the thinned substrate can be the buried oxide layer (BOX) in step (b) of Fig. 4. The Si substrate of the processed wafer can be completely wet-etched (the etch stops on the BOX) after backside grinding/polishing due to high Si-to-SiO_2 etch selectivity with TMAH.

The common processing steps in this evaluation procedure include additional bonding and thinning, along with dielectric glue ashing to expose the previously tested interconnect structures. This procedure permits bonding and thinning integrity evaluation without requiring inter-wafer interconnect processing.

The interconnect test wafers, either with oxide or porous low-k ILDs, experience two bonding and thinning processes, plus a top silicon (Si-I) removal (wet-etch) and a BCB RIE ashing in order to re-expose the Al test pads for electrical testing. Void-free bonding interface and damage-free patterns can be visually observed after this procedure, even with the weak mechanical strength of the low-k interconnect. This result with a bonded structure of three wafers (three-wafer level bonding) demonstrates that our approach of 3D integration can preserve the mechanical integrity of the Cu/low-k interconnect structures when silicon wafers are bonded (as opposed to silicon-to-glass bonding, where some damage was observed).

Electrical characteristics of the interconnect structures are measured and compared before and after this evaluation

procedure. Fig. 5 shows the electrical test results: (a) via-chain resistance and (b) comb-to-comb bridging current with interconnect wafers with oxide and porous low-k ILDs. The resistance with oxide ILD has not changed after the double bonding/thinning and BCB ashing processes, while a slight resistance shift is observed for porous low-k ILD. Another observation is the yield loss with Cu/low-k wafer after the double bonding/thinning process (Fig. 5a).

Fig. 5a also shows the probability distribution of the via-chain resistances with porous low-k ILD before and after a "single bonding/thinning" process, i.e., without steps (b) and (c) depicted in Fig. 4. Similar resistance shift to that in the double bonding/thinning case is observed, but the yield is preserved. Comparing results obtained from Cu/oxide and Cu/low-k wafers after a full procedure as depicted in Fig. 4 indicates that the yield loss may occur during mechanical thinning and/or bonding of the interconnect wafer due to the weak mechanical strength of the porous low-k ILD.

Changes in comb-to-comb bridging current have been observed with both Cu/oxide and Cu/low-k interconnect test structures (Fig. 5b). For the Cu/oxide interconnect structures, the change after a double bonding/thinning process is comparable to that of a single bonding/thinning, the latter was reported previously [3]. For the Cu/low-k interconnect structures, the change after a double bonding/thinning process is close to that of a single bonding/thinning. However, the change in the bridging current for Cu/oxide interconnects is less compared to that for Cu/low-k interconnects.

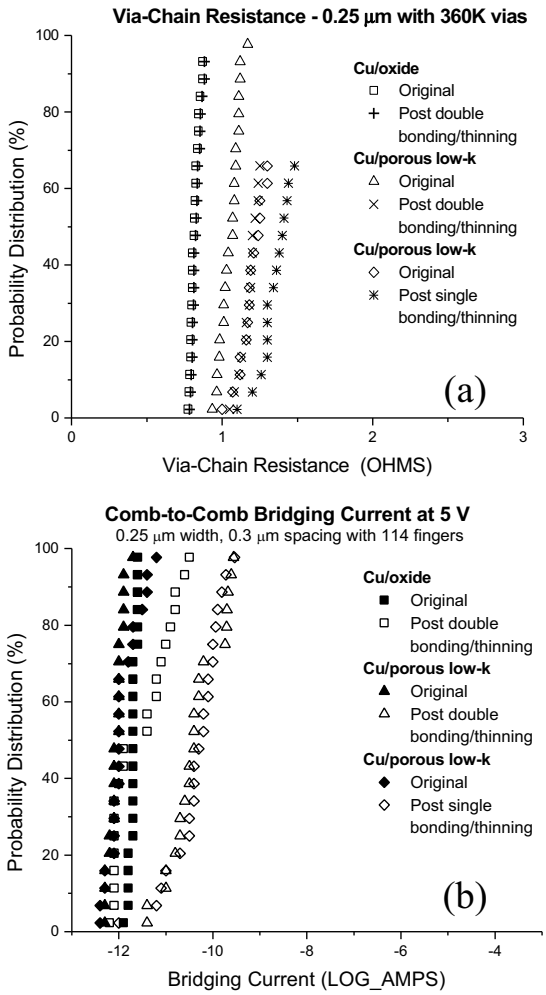

Fig. 5. Electrical test results on interconnect wafers with oxide and porous low-k ILDs.

III. Summary and Conclusions

Procedures to evaluate the mechanical and electrical impacts of wafer bonding and thinning processes required for 3D IC fabrication have been discussed. Wafer bonding and thinning processes with our 3D approach can preserve the mechanical integrity of the interconnect test structures with oxide or porous low-k ILDs, although the bonding and thinning process is marginal and needs improvement with porous low-k ILDs. Promising electrical testing results are obtained with oxide ILDs, but the porous low-k interconnect results indicate some mechanical failure across the wafer. The applicability of the experimental procedures to quantify bonding and thinning processed with multilevel test wafers has been demonstrated.

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