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Excess-loop-delay compensation technique for CT ΔΣ modulator with hybrid active–passive loop-filters

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Abstract The design and optimization methodology for CT ΣΔ modulators with hybrid Active–Passive (AP) loop-filters is indicated in this work. From the discussion, by appropriately scaling the passive filter gain and cooperating with a single-bit quantizer, the hybrid AP loop filtering can achieve an approximated noise-shaping function as a fully active ΔΣ modulator with the same order. The ELD effect in the hybrid AP CT ΔΣ modulator which influences the poles and zeros locations of the Noise Transfer Function (NTF) in the modulator is depicted. This paper also investigates the feasibility of applying the ELD compensation techniques that were used to be implemented in the active integrator's case to the hybrid AP CT ΔΣ modulator; however, some of them cannot be practically applied since the passive loop-filter cannot perform proportional feedback signal summation. After the discussion and analysis, the technique similar to Vadipour et al. (In: Symposium on VLSI circuits digest of technical papers, 2008) can be easily implemented at circuit-level and after applying it, there is one additional zero to compensate the peak in the NTF. With the help of this technique, the maximum quantizer delay tolerance can be a full clock period. The mentioned ELD compensation technique was applied in a 2nd order CT ΔΣ modulator with an active-RC integrator as the 1st stage and a passive RC filter as the 2nd stage, which was verified by transistor-level simulations in 65 nm CMOS. The circuit exhibits either 67.3 dB or 65.3 of SNDR, under the effect of half clock period or one clock period ELD, respectively; by contrast, without compensation, the system is unstable with both half or one clock period ELD effect. The designed hybrid CT ΔΣ modulator achieves 2 MHz signal bandwidth and consumes 2.54 mW of power.

Keywords CT ΔΣ modulator · Hybrid active–passive loop-filter · Excess-loop-delay for hybrid active–passive loop-filter · Excess-loop-delay compensation techniques for hybrid active–passive loop-filter

1 Introduction

Continuous-Time (CT) ΔΣ modulators have been extensively used in wideband telecommunication systems thanks to their merits in terms of low power consumption, small silicon area, large signal bandwidth, and also inherent anti-aliasing function. Three main elements: integrator, quantizer and feedback DAC compose a CT ΔΣ modulator. The integrator is the core component of the modulator and it can be either active or passive. Active integrators can be implemented with diversified circuit structures [1], being the active RC the most commonly used, since it produces higher linearity when compared with other structures, though consuming larger power. Furthermore, power dissipation is a crucial factor to have into consideration in current state-of-art telecommunication systems [1]. Hence,

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the CT ΔΣ modulator with hybrid Active–Passive (AP) integrators becomes an interesting circuit alternative.

Although the CT ΔΣ modulator with hybrid AP integrators profits from low power consumption, it is still sensitive to the effect of Excess Loop Delay (ELD). ELD is normally caused by the nonzero switching time of the transistors in the quantizer and the DAC [2, 3]. Due to ELD, when Non-Return-to-Zero (NRZ) feedback is used, a part of the feedback pulse will be shifted into the next clock cycle which may lead to system instability [4–7]. In order to reduce the serious effect of ELD in the CT ΔΣ modulator a diversified range of compensation methods have been proposed [1, 4–9], where in [10, 11] the amount of the delay is larger than one clock period and it can also be compensated. However, they are applied in full-active modulators due to the lack of isolation in passive integrators [12, 13]. Even though [14] focused on the ELD compensation for hybrid AP filters as well, the technique cannot tolerate a delay amount larger than half clock cycle. A passive ELD compensation technique similar to [15] is then analyzed and implemented for the hybrid AP CT ΔΣ modulator. The corresponding simulation results show that the ELD effects of half or one clock period can be compensated.

2 CT ΔΣ modulator with hybrid active–passive loopfilters

To increase the rate of signal processing, CT loop-filters are the most suitable candidates for the implementation of ΔΣ loop-filtering. A general procedure of CT ΔΣ loop-filter design starts from its Discrete-Time (DT) counterpart. A 2nd order DT ΔΣ modulator with a Cascade of Integrators in Feedback (CIFB) loop structure is shown in Fig. 1(a). By knowing the DT loop-filter coefficients, a_1 and a_2, and the impulse response of the selected proper CT feedback DAC pulse, the corresponding CT loop coefficients can be obtained through Impulse-Invariant Transform (IIT).

2.1 Alternative circuit structures for the CT loop-filter

The block diagram of a CT ΔΣ modulator transformed from the DT counterpart in Fig. 1(a) is shown in Fig. 1(b); with k_1 and k_2 as the CT loop-filter coefficients. Different from the DT ΔΣ modulator, loop-filters in the CT case do not sample data; data sampling operation is in front of the quantizer, and in most cases is embedded in the quantizer itself. In Fig. 1(b), both CT integrators are active, where the most commonly adopted circuit structure is the active-RC integrator whose circuit implementation and input–output transfer function are illustrated in Fig. 2(a). The integrator is constituted by an operational amplifier (op-amp), a feedback capacitor and an input resistor. Due to the

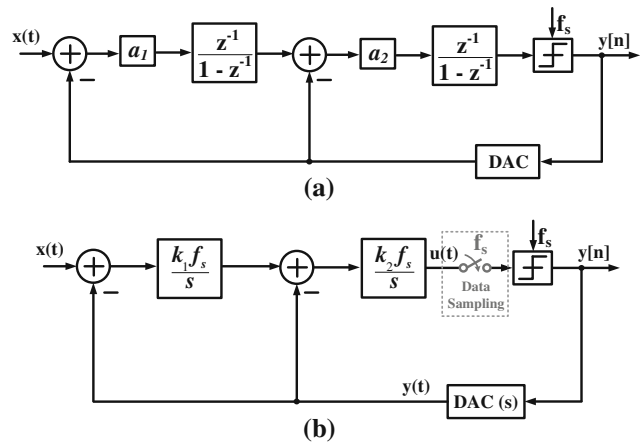

Fig. 1 Block diagrams of **a** discrete-time and **b** active continuous-time ΔΣ modulator

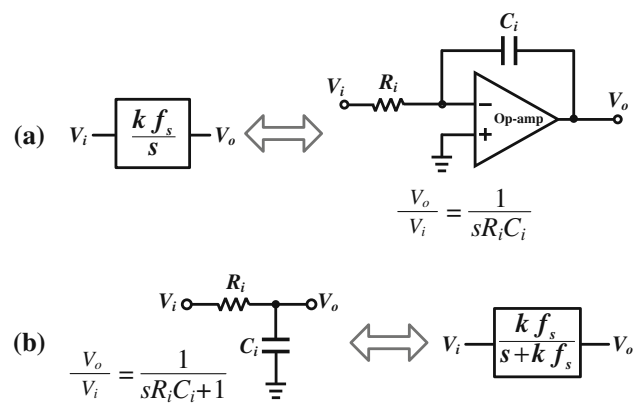

Fig. 2 Mathematical models and circuit implementations of **a** active-RC integrator and **b** passive RC filter

charge supply function of the op-amp, the integrator can ideally realize perfect low pass filtering. The integrator gain is controlled by the RC time-constant, and the expression of the integrator gain in terms of the circuit parameters is

$$kf_s = \frac{1}{R_i C_i} \tag{1}$$

The presence of an op-amp implies a significant increase in static power dissipation; and in practice op-amp's power consumption would be dominant in the whole ΔΣ modulator.

Another alternative structure for the CT loop-filter configuration is the passive RC filter, with circuit and transfer function illustrated in Fig. 2(b). From the filter transfer function, the filter gain is dependent of the RC time-constant and satisfies (1); its pole location is determined by the RC time-constant as well. When compared with the active integrator, the passive RC filter cannot implement a pole at DC. The mathematical model of the passive RC filter is also illustrated in Fig. 2(b), which

shows that to approximate the pole location like in an active RC integrator the filter gain must be minimized. Hence, in order to acquire better low-pass characteristics, input signal attenuation will be the tradeoff.

Another important drawback of the passive RC filter is that its gain at DC is 1 while for the active integrator it's infinite; on the other hand, the ΔΣ modulator requires a high loop gain to suppress In-Band-Noise (IBN), then, it will be difficult for the passive loop filter to achieve a loop function similar to that of the active integrator. In fact, this issue can be minimized by the optimization method presented hereinafter. Besides the DC gain difference, when compared with the passive structure, the active-RC integrator can provide much better suppression of the circuit noise together with a stable virtual ground node, which is crucial for accurate signal summation. In practice, due to the critical Signal-to-Noise-and-Distortion-Ratio (SNDR) requirement of the input stage in a ΔΣ modulator, the active-RC integrator is normally the preferred choice. Owing to the 1st order noise-shaping function achieved by the 1st stage, the loop-filter in subsequent stages can adopt an optimized passive structure to reduce system power. A mathematical system model for a CT ΔΣ modulator with hybrid AP loop-filter is shown in Fig. 3.

2.2 Loop function optimization with single-bit quantizer

The Loop transfer Function (*LF*) of the active CT ΔΣ modulator shown in Fig. 1 can be derived as (2). The expressions of k_1 and k_2 are for the NRZ rectangular feedback case where a_1 and a_2 are the integrator gain of the corresponding DT counterpart. Because the output is a quantized signal in the DT domain, the CT *LF* describes the signal transferred from the DAC output y(t) to the front of the quantizer u(t). Thus, the CT DAC response is considered within the calculation of the loop-filter gain.

$$LF_a(s) = -\frac{k_2 f_s(s + k_1 f_s)}{s^2}$$
$$k_1 = \frac{2a_1}{2 - a_1} \tag{2}$$
$$k_2 = a_2\left(1 - \frac{1}{2}a_1\right)$$

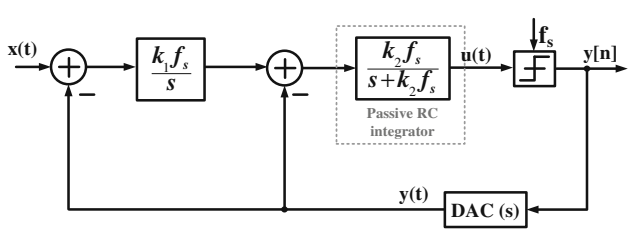

Fig. 3 System architecture of the hybrid AP CT ΔΣ modulator

The *LF* for the hybrid AP CT ΔΣ modulator shown in Fig. 3 is

$$LF_{ap}(s) = -\frac{k_2 f_s(s + k_1 f_s)}{s(s + k_2 f_s)} \tag{3}$$

where k_1 and k_2 are determined like in (2). To observe the relocated pole-zero of the Noise-Transfer-Function (NTF) for the hybrid AP CT ΔΣ modulator, the CT *LF* should be transformed into the $\mathcal{Z}$-domain since both the quantization error and the output signal are discrete in time. The equations presented in (4) can be applied to determine the corresponding NTF of a hybrid AP CT ΔΣ modulator [12]. Plus, here, all the discussed feedback DAC pulses are rectangular.

$$NTF(z) = \frac{1}{1 - LF(z)}$$
$$LF(z) = Z\left\{L^{-1}\{LF(s)DAC(s)\}_{t=nT_S}\right\} \tag{4}$$
$$DAC_{NRZ}(s) = \frac{1 - e^{-T_s s}}{s}$$

The expression to transform an ideal rectangular feedback waveform is exhibited in (4), and with the modified $\mathcal{Z}$-transformation method [12] the *LF* in the $\mathcal{Z}$-domain (Fig. 3) would be:

$$LF_{ap}[z]|_{CT-DT} = Z\left\{L^{-1}[LF(s)DAC_{NRZ}(s)]_{t=nT_S}\right\}$$
$$= -\frac{k_1}{z-1} + \frac{k_2 - k_1}{k_2}(e^{-k_2} - 1)\frac{1}{z - e^{-k_2}} \tag{5}$$

By applying (5), the pole-zero locations for the NTF of the active and the hybrid CT ΔΣ modulator are shown in Fig. 4. Without losing generality, the sampling frequency is normalized to 1. The DT integrator coefficients are $a_1 = 0.5$, $a_2 = 2$ to achieve a standard 2nd order noise shaping.

In Fig. 4, for the active CT ΔΣ modulator, there are 2 double-poles at 0 and 2 double-zeros at 1; the pole-zero locations conform with the ideal 2nd order NTF, $(1 - z^{-1})^2$. By contrast, for the hybrid AP CT ΔΣ modulator, one zero moves within the unit-circle, and it indicates that the NTF is only a 1st order differentiation in a certain low frequency band. The separated poles affect the out-band response of the NTF. The analytical NTFs over frequency for the active and the hybrid AP CT ΔΣ modulator are shown in Fig. 5. Because one zero moves to high frequency, the hybrid AP modulator achieves only a 1st order in-band noise-shaping function.

To approximate the *LF*, for the hybrid AP modulator, to the ideal active form given in (2), a feasible way would be to move the non-DC pole in (3) to as lower frequency as possible. However, scaling down k_2 also decreases the filter gain which will increase IBN floor. In a general case, this issue should be compensated by increasing the quantizer

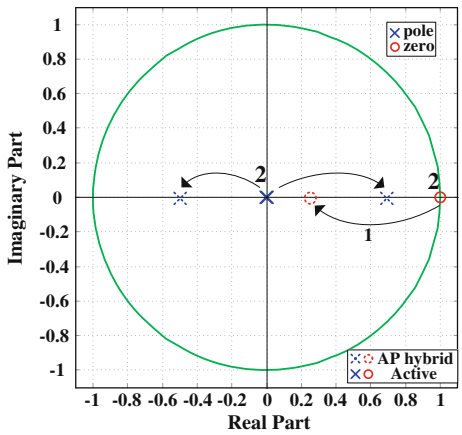

Fig. 4 NTF pole-zero locations for the 2nd order active CT ΔΣ modulator and the hybrid AP modulator without optimization

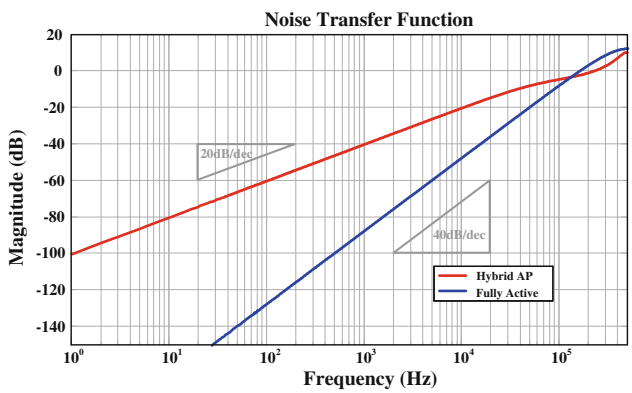

Fig. 5 Calculated NTF for the un-optimized hybrid AP and the active CT ΔΣ modulator

gain to fix the total loop gain. In the modulator, by employing a single-bit quantizer, the loop gain scaling issue can be automatically compensated through the arbitrary gain characteristics of the quantizer itself.

The analytical model for the loop function optimization of the hybrid AP CT ΔΣ modulator is shown in Fig. 6 where the scaled passive filter gain is described as k_2'.

Gain c describes the inherent gain of the single-bit quantizer, which can have an arbitrary value between 0 and 1. In practice, the following equations can be obtained:

$$\left.\begin{aligned} \text{Passive filter gain}: k_2' &= a \cdot k_2 \\ \text{Loop gain}: k_2' \cdot c &= k_2 \end{aligned}\right\} \rightarrow a \cdot c = 1 \qquad (6)$$

where a is the scaling factor of the passive filter gain that will ensure that the passive filter will approximate the ideal active RC filter. The value of c can automatically satisfy (6) to compensate the loop gain. The NTFs plotted in Fig. 7 represent the effect under different values of a.

It can be observed that the smaller the value of a is the closer the NTF is to an ideal modulator. However, (1)

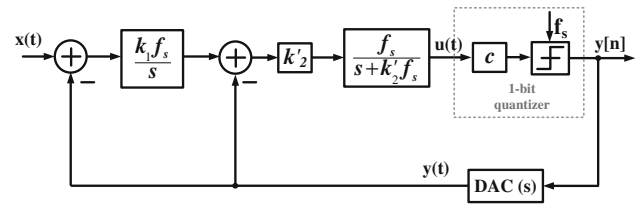

Fig. 6 Analytical model for the loop function optimization of the AP CT ΔΣ modulator

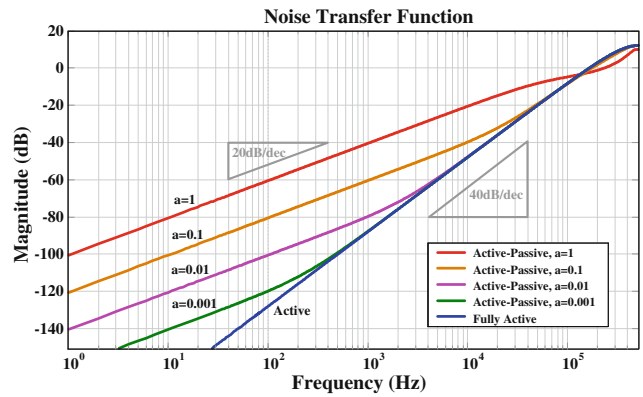

Fig. 7 Calculated NTFs for the hybrid AP CT ΔΣ modulator with different passive loop filter gain scaling values

shows that for an extremely small value of the passive filter gain (i.e. extreme small value of a as in above (6) and Fig. 7) the RC time-constant should be very large which increases circuit area. Moreover, if the loop-filter gain is scaled down too much, from (6), the equivalent quantizer gain c will be quite high which means that the quantizer is processing an extremely small input, thus further increasing the accuracy requirement of the single-bit quantizer to the comparator. The scaling factor a should be determined based on the desired signal band. The NTF's zero and pole locations variation as a function of the decreasing value of a are shown in Fig. 8.

From the previous analysis, to optimize a hybrid AP CT ΔΣ modulator as an approximate standard active modulator, it is preferable to use a single-bit quantizer for its arbitrary conversion gain in the system. A suitable scaling value for the passive filter gain can be determined based on the desired signal bandwidth.

3 ELD compensation for a CT ΔΣ modulator with hybrid active–passive loop-filters

Due to the effect of ELD the SNDR of the modulator may drop significantly in the CT ΔΣ modulator with hybrid AP integrators. Hence, the coming section will analyze the effect of ELD and the implementation as well as the possibilities of some compensation methods which used to be

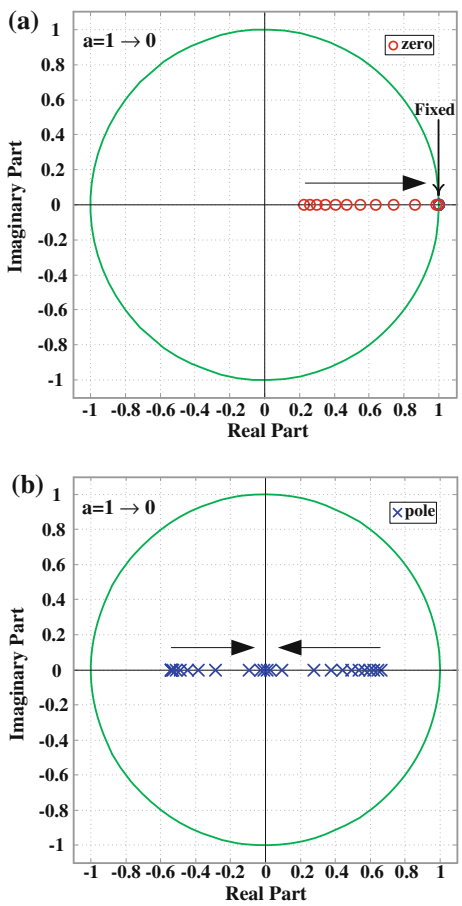

Fig. 8 NTF pole-zero location variation for the AP CT ΔΣ modulator with the passive loop filter gain scaling from 1 to 0

commonly utilized in the full-active integrator case. In particular, in a 2nd order CT ΔΣ modulator with hybrid AP integrators, namely, an active RC integrator as the 1st stage of the loop filter, and a passive RC circuit as the 2nd stage.

3.1 ELD effect in the hybrid AP CT ΔΣ modulator

Figure 3 and (3) depict the model and transfer function of a 2nd order hybrid AP CT ΔΣ modulator in the continuous-time domain. As mentioned before, all of the continuous-time transfer functions (with/without delay) should be transformed into the $\mathcal{Z}$-domain. Then, a standard *LF* of the hybrid AP CT ΔΣ modulator should be achieved firstly. As mentioned, the NRZ rectangular feedback DAC will be used in our analysis due to its higher sensitivity to the ELD effect.

When comparing (5) with the corresponding *LF* of the ideal 2nd order fully active modulator (which has two identical poles with values $z_1 = z_2 = 1$, as in Fig. 4), it can be noticed that one pole of (5) has been shifted from 1 to e^{-k2}. Besides, different k_2 will lead to different pole locations of the NTF, as presented in Fig. 8.

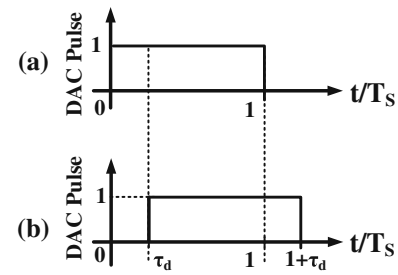

Fig. 9 NRZ DAC feedback pulse **a** ideal case and **b** with delayed τ_d

Meanwhile, the ELD effect will shift the NRZ feedback waveform from the current period to the subsequent period [1], as it can be shown in Fig. 9,

According to the equation of the ideal NRZ DAC feedback pulse (4) and the methodology to get the DAC expression with delay, as referred in [16], the expression of the NRZ DAC with delay τ_d ($0 \le \tau_d \le 1$) is,

$$DAC_{NRZ_\tau_d}(s) = \frac{e^{-\tau_d s T_S} - e^{-(1+\tau_d)sT_S}}{s} \tag{7}$$

Based on (7), as well as on (4), which expresses the methodology to achieve the *LF* in the $\mathcal{Z}$-domain, the *LF* due to the ELD effect can be obtained, as below, where the new *LF* is obviously dominated by the shifted delayed DAC pulse,

$$\begin{aligned} LF[z]_{ap_\tau_d}|_{CT-DT} &= Z\left\{L^{-1}[LF(s)DAC_{NRZ_\tau_d}(s)]_{t=nT_S}\right\} \\ &= Z\left\{L^{-1}\left[-\frac{k_2 f_s(s+k_1 f_s)}{s(s+k_2 f_s)}\frac{e^{-\tau_d s T_S} - e^{-(1+\tau_d)sT_S}}{s}\right]_{t=nT_S}\right\} \end{aligned} \tag{8}$$

With the help of [16] and after simplification the *LF* with delay τ_d will become,

$$\begin{aligned} LF[z]_{ap_\tau_d}|_{CT-DT} &= z^{-1}(1-z^{-1}) \\ &\times Z\left\{L^{-1}\left[-\frac{k_2 f_s(s+k_1 f_s)}{s(s+k_2 f_s)}\frac{1}{s}\right]_{t=(n+1-\tau_d)T_S}\right\} \end{aligned} \tag{9}$$

From (9) it can be observed that the ELD increases the order of the *LF* and the amount τ_d affects the expressions of *LF*, which matches well with the statements of ELD effect in [1–3, 12, 16]. For instance, let us consider the excess loop delay with an amount $\tau_d = 1$. According to (9), the *LF* when $\tau_d = 1$ is

$$\begin{aligned} LF[z]_{ap_\tau_d=1} &= z^{-1}(1-z^{-1}) \\ &\times Z\left\{L^{-1}\left[-\frac{k_2 f_s(s+k_1 f_s)}{s(s+k_2 f_s)}\frac{1}{s}\right]_{t=(n+1-1)T_S}\right\} = (z^{-1}-z^{-2}) \\ &\times \left[\frac{-k_1 z}{(z-1)^2} + \left(-1+\frac{k_1}{k_2}\right)\frac{z}{z-1} + \frac{k_2-k_1}{k_2}\frac{z}{z-e^{-k_2}}\right] \\ &= \frac{-k_1}{z-1} + \frac{1}{z}\left(k_1 - 1 + \frac{k_1}{k_2} - \frac{k_1}{k_2}e^{k_2} + e^{k_2}\right) \\ &+ \frac{1}{z-e^{-k_2}}\left(-\frac{k_1}{k_2} + 1 + \frac{k_1}{k_2}e^{k_2} - e^{k_2}\right) \end{aligned} \tag{10}$$

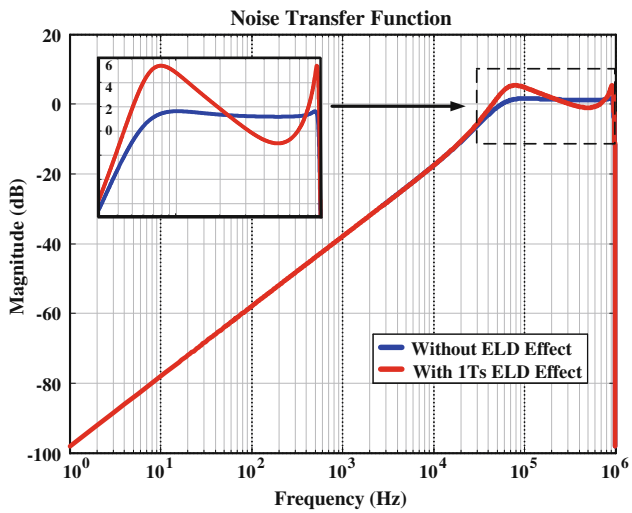

Fig. 10 The NTF when the hybrid AP modulator either contains or not one clock cycle delay effect with $a = 0.25$

And, when comparing (10) with the ideal AP case from (5), there will be one additional pole which may affect the performance of the modulator.

Figure 10 exhibits the comparison of the NTF in an example of a hybrid AP modulator with $a = 0.25$ as in (6) with or without 1 clock cycle ELD effect. Without ELD effect the noise shaping is quite smooth; however, whenever there is 1 clock cycle delay in the modulator, a peak will appear which represents the instability of the system. This figure also highlights the importance of ELD compensation and the trend to compensate the ELD effect, which will imply the introduction of a suitable zero in the NTF appropriate to compensate the peak in the NTF.

3.2 Traditional ELD compensation method

Because of the significant effect of ELD, there are many methods proposed to compensate its effect in CT ΔΣ modulators [1, 10, 12, 14]. However, some of them have limitations, which will be highlighted in the coming section as well as the comparison with the proposed technique.

The classical technique with one additional feedback path to compensate the ELD effect can also be used in the hybrid AP case, as shown in Fig. 11.

It consists of a delay τ_d, and, in practice, it is usually set to be 1/2 or 1 period of clock cycle, placed before the feedback DAC and which is normally implemented by a D Flip–Flop. The signal delay can be locked by the DFF within a certain time in order that a smaller delay amount can be tolerated within it.

According to the classical compensation structure in Fig. 11, the corresponding *LF* with delay can be obtained using (8). And, for the simplicity of the analysis, 1 clock

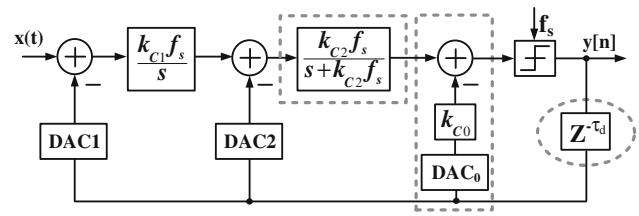

Fig. 11 Traditional ELD compensation method for a 2nd order CT ΔΣ modulator with hybrid AP integrators

cycle delay is set as the example. With 1 cycle delay and based on (7) the Laplace Transform of the rectangular NRZ feedback can be obtained. Thus, by combining the equation which represents the *LF* with 1 clock cycle delay effect and inserting on it the delayed DAC effect, the *LF* with $\tau_d = 1$ of Fig. 11 can be expressed as,

$$\begin{aligned} LF[z]\big|_{ClassicalComp_\tau_d=1} &= -\frac{k_{C1}}{z-1} \\ &+ \frac{1}{z}\left(k_{C1} - k_{C0} + 1 - \frac{k_{C1}}{k_{C2}} + \frac{k_{C1}}{k_{C2}}e^{-k_{C2}} - e^{-k_{C2}}\right) \\ &+ \frac{1}{z-e^{-k_{C2}}}\left(\frac{k_{C1}}{k_{C2}} - 1 - \frac{k_{C1}}{k_{C2}}e^{-k_{C2}} + e^{-k_{C2}}\right) \end{aligned} \tag{11}$$

In order to compensate the effect of ELD, (11) should be equal to (5). Then, the additional term $\frac{1}{z}$ should be zero, meaning that its coefficient should be zero. Finally, the coefficients of Fig. 11, with $\tau_d = 1$ matching with Fig. 3, will be:

$$\begin{aligned} k_{C0} &= k_1 + \frac{k_2 - k_1}{k_2}(1 - e^{-k_2}) \\ k_{C1} &= k_1 \\ k_{C2} &= k_2 \end{aligned} \tag{12}$$

From Fig. 10, one clock cycle delay will mean that the peak of the NTF leads to instability of the modulator. To verify the efficiency of the compensation method, with the coefficients from (12), different NTFs are depicted, and can be compared, in Fig. 12, with a value of a equal to 0.25, as in Fig. 10.

3.3 Simple resistor adder method

Usually, an analog adder can accomplish such a function. In order to reduce power dissipation the analog adder can be implemented with passive elements in a general active CT ΔΣ modulator similar with the technique in [17]. As shown in Fig. 13(a), the feedback current flows through the adder resistor and produces a voltage drop; the final output is equal to the integrator output added to the voltage drop on the resistor. The feedback current will not affect the original integrator output due to the op-amp's low output impedance.

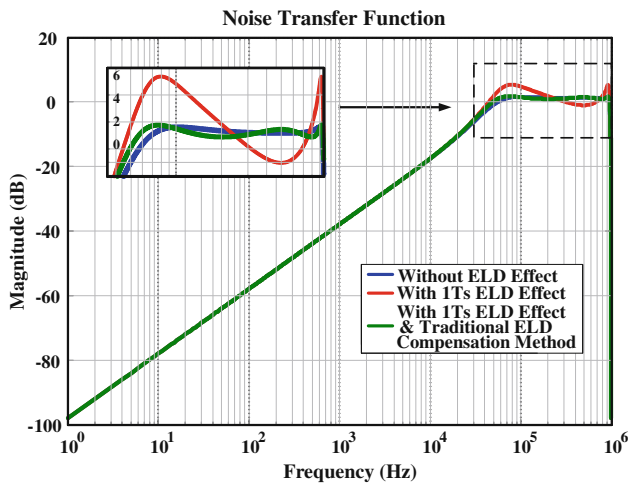

Fig. 12 The ideal NTF (without ELD effect), the NTF for the modulator with 1 clock cycle delay effect, and the NTF with delay after traditional compensation with $a = 0.25$

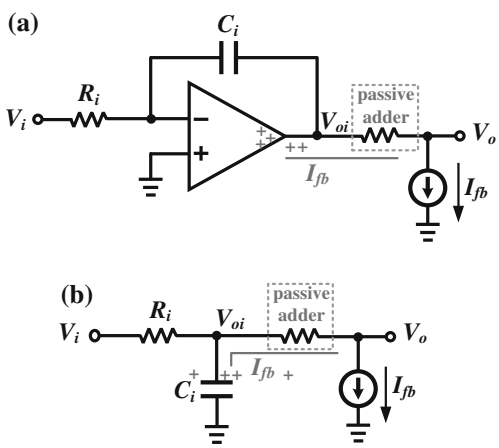

Fig. 13 Passive analog adder current feedback in **a** active and **b** passive loop-filters

By contrast, if the same method as in [17] is applied to a passive RC filter, as shown in Fig. 13(b), the only source of charges is the energy storage element, i.e. the integrating capacitor C_i. The charges forming the feedback current come from capacitor C_i (equivalent to the integration of the feedback current), and, consequently, the final output includes the integration of the sum of the input and the feedback simultaneously, and the constant k_{C0} feedback cannot be realized. Then, the passive simple resistor adder compensation method as illustrated in Fig. 13(a) cannot be implemented when the passive loop-filter is in the last stage. On the other hand, if an active adder is employed to implement the compensation, the low power benefit of the hybrid AP loops filtering will be lost. Therefore, low power compensation and highly efficient techniques for ELD compensation are required for the hybrid AP CT ΔΣ modulator.

3.4 Passive ELD compensation technique for hybrid active–passive integrators

Comparing the model of the traditional ELD compensation method in Fig. 11 with the ideal AP model in Fig. 3, the additional path with constant k_{C0} (as depicted in Fig. 11) is introduced to compensate the delay. Thus, the effect of the ELD can be equivalently compensated by additional feedback with a constant in front of the quantizer and in the eyes of the *LF*. In order to reduce the additional constant path (Fig. 11) and save power consumption, combining the constant term with the preceding passive integrator similar with the technique in [15] will be implemented, as shown in the following Fig. 14.

According to Fig. 14, and with the passive integrator of Fig. 2(b), the ELD effect in the hybrid AP CT ΔΣ modulator can be compensated if the constant K (Fig. 14) is obtained by a ratio of resistors or capacitors, leading to the implementation of the technique. This is based on the structure of a passive RC integrator and similar with that from [7, 15].

To compensate the ELD effect the *LF* of the passive compensation structure should match with that of the ideal hybrid AP CT ΔΣ modulator, as expressed by (5). The passive technique imposes the additional resistor R_0 in series with C_2, as shown in Fig. 15. For this structure, after simplification, the constant K (Fig. 14) can be determined by the ratio of resistors. The whole 2nd loop-stage (highlighted as the gray dashed block in Fig. 14) can be implemented by the structure in Fig. 15, with the transfer function given by,

$$\frac{V_{out}}{V_{in}} = \frac{sR_0C_2 + 1}{sC_2(R_0 + R_2) + 1} = \frac{k_{P2}s + k_{P0}k_{P2}f_s}{s(k_{P0} + k_{P2}) + k_{P0}k_{P2}f_s} \quad (13)$$

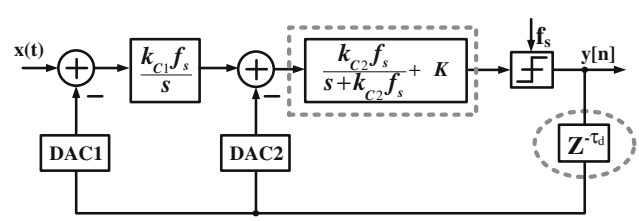

Fig. 14 The model of the passive technique to compensate the ELD effect in the hybrid AP modulator

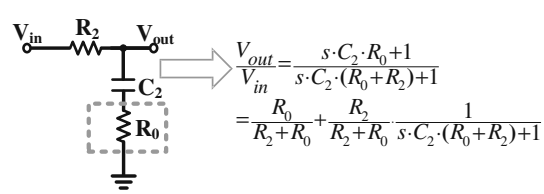

Fig. 15 Circuit implementation of the passive ELD compensation technique for a passive RC integrator

Figure 16 represents the structure of the proposed technique for a 2nd order CT ΔΣ modulator with hybrid AP integrators and excess loop delay τ_d. (as before, τ_d is set to be 1 clock cycle). The corresponding *LF* should be equal to that of Fig. 3, to compensate the ELD effect. Since the *LF* with ELD effect of Fig. 11 is also identical to that of Fig. 3, the equivalence of the *LF* between Figs. 11 and 16 implies that the compensation is achievable. After some calculation, the new coefficients that turn equivalent the structures of Figs. 16 and 11 are,

$$k_{P0} = \frac{k_{C2}}{k_{C0}}$$
$$k_{P2} = \frac{k_{C2}}{1 - k_{C0}} \tag{14}$$
$$k_{P1} = k_{C1}$$

And for the figure about NTF as demonstrated in Fig. 12, since this methodology is identical to that of the traditional compensation technique, the same condition will lead to the same curve as illustrated in Fig. 12 (green line).

When comparing both structures (from Figs. 11, 16), the modified passive RC integrator (Fig. 15) operates as an adder plus an additional feedback path, simplifying the whole circuit structure and reducing power dissipation. Furthermore, the extra elements in Fig. 11 can be implemented by only one additional resistor. Plus, when compared with the method from [7, 14, 15], this passive technique can compensate the delay up to 1 clock cycle.

Although the compensation method presented in [14] (as illustrated in its Fig. 8) also did not contain an additional feedback path in front of the quantizer (traditional compensation technique), that additional path was efficiently added together with the input of the last stage integrator which was implemented by an $G_m - C$ integrator so that summation could be accomplished more easily (as depicted in Fig. 9 of [14]). In addition, also from [14], the feedback shapes of DAC1 and DAC2 are different: DAC1 was NRZ feedback but DAC2 was Return-to-Zero (RZ) feedback. In contrast, the last integrator here is the passive RC integrator which consumes no power and the feedback shapes of DAC1 and DAC2 are the same, which are NRZ.

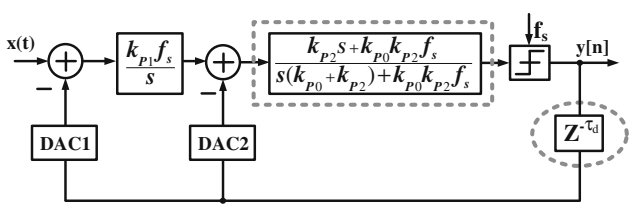

Fig. 16 Passive ELD compensation technique with hybrid AP integrators

4 Design example of hybrid AP CT ΔΣ modulator

In order to verify the passive ELD compensation technique, shown in Fig. 15, a 2nd order, single-bit, low-pass CT ΔΣ modulator with hybrid AP integrators was designed based on the system diagram of Fig. 16, with a sampling rate of 250 MS/s. The input bandwidth is 2 MHz corresponding to the standard of 3G WCDMA receivers and the OSR is 64. The input amplitude of the signal is $P_{in} = -2$ dBFS and NRZ feedback was chosen. The transformed CT coefficients were scaled down to guarantee that the signal swing will not reach the saturation level of the loop filter. However, since the second integrator is passive, which will reduce the signal swing, the input swing of the second integrator should not be too small (small input swing will increase the requirement of the quantizer). The overall circuit schematic of the modulator is given in Fig. 17, which was implemented in 65 nm CMOS with 1 V supply voltage. The circuit of Fig. 15 was employed in the second loop filter to obtain the compensation.

Based on Fig. 3 and previous analysis, the performance (SNDR) of a hybrid AP CT ΔΣ modulator can approximate that of an active structure whenever the coefficient of the passive integrator is properly selected. If the structure of Fig. 3 is taken as an example, in order to get the expected performance, a suitable value of k_2 is required.

In this design and to match with Fig. 3, taking the swing reduction of the second passive integrator into account, for a hybrid AP 2nd order CT ΔΣ modulator without delay, $k_1 = 0.25$ is selected. Since the coefficient of the 2nd integrator affects the performance of the system it should be carefully chosen, leading here to $k_2 = 0.01$. Then, after calculation, the system coefficients with ELD compensation (as in Fig. 16) can be obtained. Additionally, based on (13) and the working principle of the active and passive RC integrator, the values of all circuit elements in Fig. 17 can be determined: $R_1 = R_{f1} = 16$ kΩ, $C_1 = 1$ pF, $R_2 = R_{f2} = 400$ kΩ, $C_2 = 1$ pF and $R_0 = 2$ kΩ. Comparing this passive ELD compensation method with the traditional compensation technique which needs active circuit

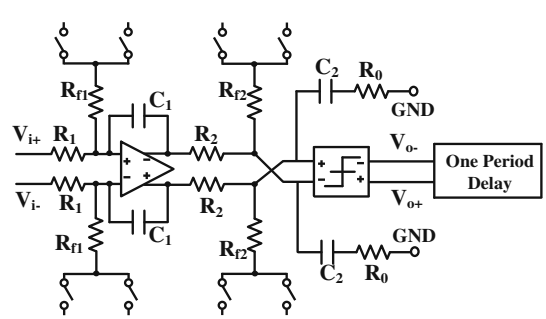

Fig. 17 Circuit schematic of the passive ELD compensation structure in a 2nd order, 1-bit, CT ΔΣ modulator with hybrid AP integrators and NRZ DAC

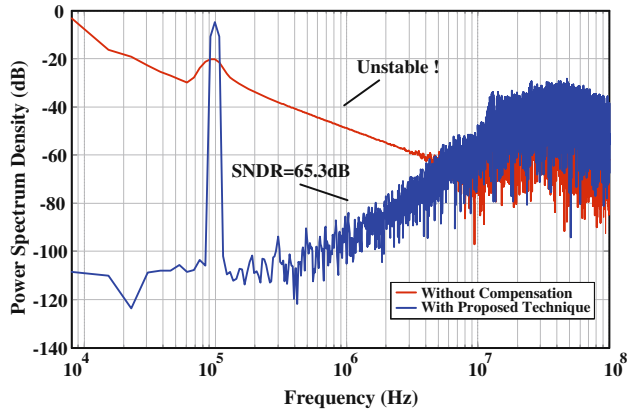

Fig. 18 Comparison of simulation results for 2 different cases (Pin_red = −20 dBFS, Pin_blue = −2 dBFS) when there is 1Ts delay in the quantizer

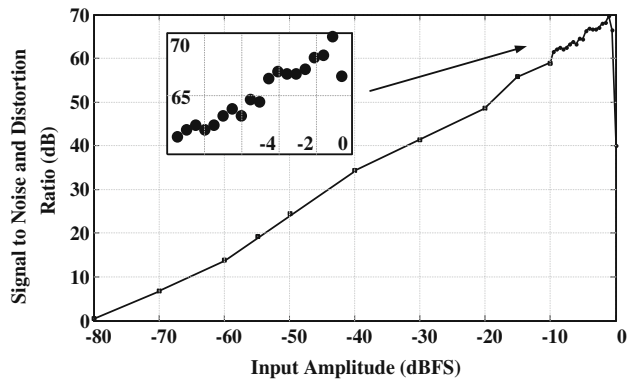

Fig. 19 SNDR versus input signal amplitude

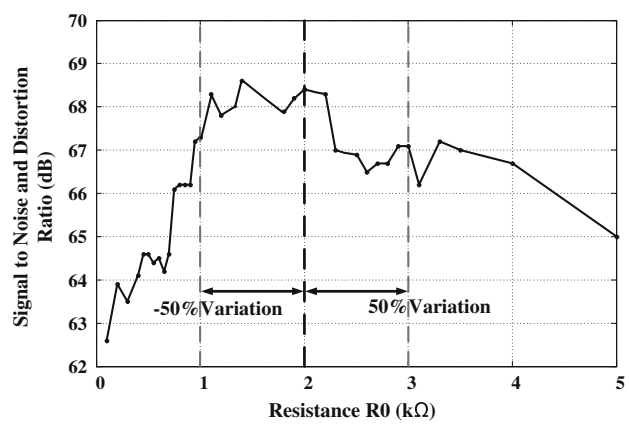

Fig. 20 The value of R0 vesus SNDR of the system

elements, clearly this will reduce the power consumption of the overall system.

Figure 18 shows the simulation results (when 1 clock cycle delay is added) of the same modulator in two different cases, with and without the passive ELD compensation. The red curve is with input amplitude Pin = −20 dBFS and blue one is Pin = −2 dBFS. Since without compensation, the input amplitude Pin = −2 dBFS leads to un-stability as well, here it is shown the low input amplitude to allow a comparison. The results demonstrate that the in-band noise floor of the red curve (without ELD compensation) is much higher than that of the system employing the passive ELD compensated technique (blue

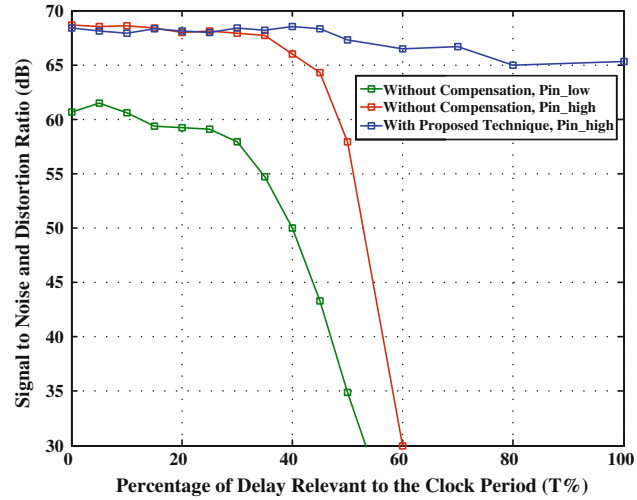

Fig. 21 Simulation results for system sensitivity to ELD in a 2nd order Hybrid AP CT ΔΣ modulator with and w/o the proposed compensation technique, with Pin_low = −20 dBFS and Pin_high = −2 dBFS

Table 1 Comparison of performance of different structures

CT ΔΣ modulator	OSR	SNDR (dB)	Power (mW)	Delay (% T_S)
A	256	69.6	6	–
B	64	70	5.3	–
B	64	30	5.3	50
B	64	Unstable	–	100
C	64	69.4	6.1	50
C	64	67.1	6.1	100
D	64	68.7	2.5	–
D	64	57.9	2.5	50
D	64	Unstable	–	100
E	64	67.3	2.54	50
E	64	65.3	2.54	100

A 1st Order CT ΔΣ modulator with active RC integrator

B 2nd Order CT ΔΣ modulator where both stages are active RC integrators

C 2nd Order CT ΔΣ modulator where both stages are active RC integrators and with traditional ELD compensation

D Hybrid AP with 1st stage as an active RC integrator and 2nd stage as a passive RC integrator

E Hybrid AP with 1st stage as an active RC integrator and 2nd stage as a passive RC integrator with the *passive ELD compensation technique*

curve); and also the noise shaping function has been distorted due to the change of the NTF. Obviously, the system is unstable and cannot work normally under $1T_S$ loop delay without ELD compensation, in particular also because of the NRZ feedback. The dynamic range of the system is 77 dB, and Fig. 19 depicts the SNDR versus the input signal amplitude. The variation of R0 versus SNDR is also depicted in Fig. 20, showing that the technique is not sensitive to process variations. The efficiency and delay tolerance of the passive technique is plotted and compared with the structure without compensation, as described in Fig. 21. By contrast, after applying the proposed technique, if there is 1/2 clock period delay, the SNDR is 67.3 dB; on the other hand, with 1 clock period ELD effect compensated the SNDR is 65.3 dB; both of them close to the ideal 69 dB case. Theoretically, the passive scheme can compensate the loop delay if not larger than 1 clock period. The comparison of the performance of the different structures analyzed is shown in Table 1.

5 Conclusions

This paper discussed the ELD effect in hybrid AP CT ΔΣ modulators and the feasibility of implementing different compensation techniques which commonly used full-active integrators. The passive ELD effect compensation technique and its corresponding circuit scheme, to be used in hybrid AP CT ΔΣ modulators, was verified as exhibiting very high efficiency and low power consumption. Its application allows the tolerance of up to 1 clock period of loop delay. This passive method is simpler in terms of circuit implementation and does not consume active power. Its behavior was verified both mathematically and through the design of a 2nd order CT ΔΣ modulator with hybrid AP integrators and NRZ feedback. Simulation results show that with 1/2 of clock period delay the performance of the hybrid AP CT ΔΣ modulator without ELD compensation was poor (57.9 dB); by contrast, the proposed modulator achieved 67.3 dB SNDR; when there is 1 clock period delay, the structure without compensation is unstable; after using the compensation method, the SNDR is 65.3 dB, which is close to the ideal active case, further demonstrating the effectiveness of this passive scheme.

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References

1. Cherry, J. A., & Snelgrove, W. M. (2000). *Continuous-time delta–sigma modulators for high-speed A/D conversion*. Norwell, MA: Kluwer Academic.
2. Cherry, J. A., & Snelgrove, M. (1999). Excess loop delay in continuous-time delta–sigma modulators. *IEEE Transactions on Circuits Systems II: Analog Digital and Signal Processing, 46*(4), 376–389.
3. Pavan, S. (2008). Excess loop delay compensation in continuous-time delta–sigma modulators. *IEEE Transactions on Circuits Systems II: Analog Digital and Signal Processing, 55*(11), 1119–1123.
4. Mitteregger, G., et al. (2006). A 20-mW 640-Hz CMOS continuous-time ΣΔ ADC with 20-MHz signal bandwidth, 80-dB dynamic range and 12-bit ENOB. *IEEE Journal of Solid-State Circuits, 41*(12), 2641–2649.
5. Fontaine, P., Mohieldin, A. N., & Bellaouar, A. (2005). A low-noise low-voltage CT ΔΣ modulator with digital compensation of excess loop delay. In *IEEE International Solid-State Circuits Conference (ISSCC)—Digest of Technical Papers*, Feb. 2005 (pp. 498–613).
6. Weng, C. H., Lin, C. C., Chang, Y. C., & Lin, T. H. (2011). A 0.89-mW 1-MHz 62-dB SNDR continuous-time delta–sigma modulator with an asynchronous sequential quantizer and digital excess-loop-delay compensation. *IEEE Transactions on Circuits Systems II: Analog Digital and Signal Processing, 58*(12), 867–871.
7. Cai, C. Y., Jiang, Y., Sin, S. W., Seng-Pan, U., & Martins, R. P. (2011). A passive Excess-Loop-Delay compensation technique for Gm-C based continuous-time ΣΔ modulators. In *IEEE International Midwest Symposium on Circuits and Systems (MWSCAS)* (Aug. 2011), pp. 1–4.
8. Alamdari, H. H., El-Sankary, K., & El-Masry, E. (2009). Excess loop delay compensation for continuous-time ΔΣ modulators using interpolation. *IEEE Transactions on Circuits Systems II: Analog Digital and Signal Processing, 45*(12), 609–610.
9. Keller, M., Buhmann, A., Sauerbrey, J., Ortmanns, M., & Manoli, Y. (2008). A comparative study on excess-loop-delay compensation techniques for continuous-time sigma–delta modulators. *IEEE Transactions on Circuits and Systems I: Regular Papers, 55*(11), 3480–3487.
10. Krighnapura, N., Pava, S., Vigraham, B., Nigania, N., & Behera, D. A 16 MHz BW 75 dB DR CT ΔΣ ADC compensated for more than one cycle excess loop delay. In *Proceedings of the IEEE Custom Integrated Circuits Conference (CICC)*, Sept. 2011 (pp. 1–4).
11. Singh, V., Krishnapura, N., Pavan, S., Vigrahm, B., Behera, D., & Nigania, N. (2012). A 16 MHz BW 75 dB DR CT ΣΔ ADC compensated for more than one cycle excess loop delay. *IEEE Journal of Solid-State Circuits, 47*(8), 1–12.
12. Ortmanns, M., & Gerfers, F. (2005). *Continuous-time delta–sigma A/D conversion*. Berlin: Springer.
13. Schreier, R., & Temes, G. C. (2005). *Understanding delta–sigma data converters*. Piscataway, NJ: IEEE Press.
14. Song, T., Cao, Z., & Yan, S. (2008). A 2.7-mW 2-MHz continuous-time ΣΔ modulator with a hybrid active–passive loop filter. *IEEE Journal of Solid-State Circuits, 43*(2), 330–341.
15. Vadipour, M., Chen, C., Yazdi, A., Nariman, M., Li, T., Kilcoyne, P., & Darabi, H. (2008). A 2.1 mW/3.2 mW delay-compensated GSM/WCDMA ΣΔ analog–digital converter. In *Symposium on VLSI Circuits Digest of Technical Papers*, June 2008 (pp. 180–181).

16. Loeda, S., Reekie, H. M., & Mulgrew, B. (2006). On the design of high-performance wideband continuous-time sigma–delta converters using numerical optimization. *IEEE Transactions on Circuits and Systems I: Regular Papers, 53*(4), 802–810.
17. Matsukawa, K., Mitani, Y., Takayama, M., Obata, K., Dosho, S., & Matsuzawa, A. (2009). A 5th-order delta–sigma modulator with single-opamp resonator. In *Symposium on VLSI Circuits Digest of Technical Papers*, Jun. 2009 (pp. 68–69).

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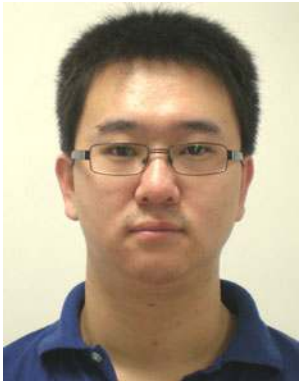

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