Experimental Efficiency Comparison between a Direct Matrix Converter and an Indirect Matrix Converter using both Si IGBTs and SiC MOSFETs

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Abstract— This paper presents an experimental efficiency comparison study between two different direct AC-AC converter topologies: a direct matrix converter (DMC) and an indirect matrix converter (IMC). The evaluation is performed under variable load conditions using both discrete Silicon (Si) IGBTs and Silicon Carbide (SiC) MOSFETs working at power levels up to 9 kW. Each loss measurement is carried out using two power analyzers: one placed at the input and one at the output of the converter under study. To facilitate this measurement an output filter was necessary in addition to the normal input filter. Both converters are modulated the same traditional symmetrical space vector approach and feature an identical input/output filter design.

I. INTRODUCTION

Matrix Converters perform direct AC-AC, bi-directional, power conversion and have received substantial attention in the past two decades from the academic community and from industry. They are employed in different applications and particularly in variable speed drive systems [1-9] where the application demands a more compact and robust solution [10] in place of the traditional two-level, rectifier/voltage source inverter (VSI) circuit [11-13]. Matrix converter technology has been considered more recently for aerospace applications [14-18] because of the potential for higher volumetric and gravimetric power density with improved reliability [19] when compared to a back-to-back converter employing large DC-link electrolytic.

Two basic types of AC-AC matrix converter structure have been proposed in the literature, the Direct Matrix Converter (DMC) and the Indirect Matrix Converter (IMC) whose circuit schematics are shown in Figures 1a and 1b respectively. It can be immediately noted that both converters use the same number of power devices. Additionally, they can both achieve the same quality of input current and output voltage when controlled using the same type of modulation. Consequently they require identical input filtering to achieve comparable performance with respect to the line current and the output filtering requirement is also the same. Some common limitations also exist for both converters, mainly regarding the maximum output voltage available and power factor correction especially at very low output power. Figures 2a and 2b show photographs of the experimental prototypes, with labels to show the physical positions of each of the devices with respect to the circuit schematics shown in figure 1.

The main differences between the two converters are:

- Efficiency
- Loss distribution among the devices

This paper focusses on the first issue, by carrying out an efficiency evaluation and analysis and by comparing the two converters using experimental data. The losses in the two converters have different distributions among the devices because the topologies of the circuits are different; this also leads to different total conduction losses. Furthermore, this paper also investigates and compares the use of Silicon Carbide MOSFETs and Silicon IGBTs to implement the power circuits.

Silicon Carbide devices have received increased attention in recent years and with many devices now commercially available; their potential advantages are being exploited by design engineers. Silicon Carbide is classed as a wide bandgap material and the blocking voltage capability is superior to Si for similar structures. Whilst IGBT structures are needed to achieve a 1200V blocking voltage in Si devices, this can be readily achieved by MOSFET structures using SiC. Silicon Carbide also has higher charge mobility than Si and a higher thermal conductivity. These features create the possibility of significantly increasing switching speeds and reducing losses.

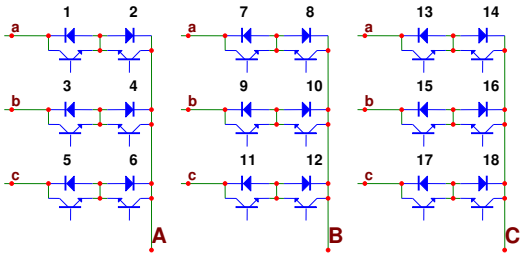
An earlier paper [20] reported a comparison between the use of Si IGBTs and SiC MOSFETS when employed in the DMC topology and operated under the same conditions. Another paper [21] focused on an efficiency comparison of the DMC versus the IMC using Si devices. The contribution of this paper is the experimental comparison between the DMC and the IMC using different devices, both Si IGBTs and SiC MOSFETS. In addition, this paper also investigates the performance of the IMC when using a hybrid solution of Si IGBTs on the input stage and SiC MOSFETS at the output stage.

The loss distribution between the devices of the input stage and the output stage of the IMC is also highlighted as this has significant implications when using the hybrid Si-SiC solution.

II. MEASUREMENT SYSTEM CONFIGURATION

The comparison study in this work is based on experimental measurements taken on converter prototypes expressly built (figure 2) for this purpose. The converters have been assembled using the following power devices:

- Si IGBT (IKW15T120) rated at 1.2k[V] and 30[A] at 25[°C]
- SiC MOSFET (C2M0080120D) rated at 1.2k[V] and 31.6[A] at 25[°C]



a)

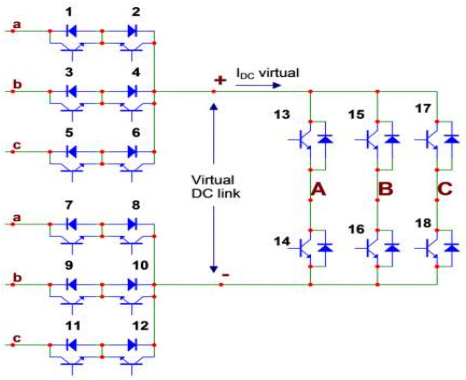


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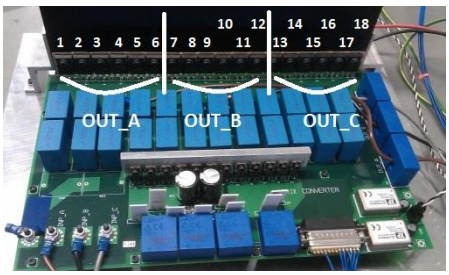
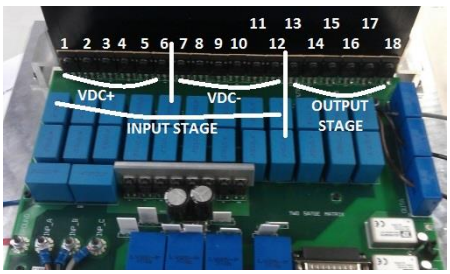
Fig. 1 Schematic circuits of the DMC (a) and the IMC (b), where a,b,c are the input connections and A,B,C are the output connections



a)



b)

Fig. 2 a) DMC prototype and b) IMC prototype showing the functional regions and individual devices w.r.t. figure 1

As mentioned previously the IMC has also been configured using Si IGBTs in the input stage and SiC devices in the output stage for some of the tests. The converters are fed by a standard 3-phase mains supply 240 V_{rms} phase to neutral at 50 Hz.

In order to measure the efficiency of the converters using two (input, output) power analyzers, an output filter was required in order to avoid noisy measurements and remove the high frequency components which are unmeasurable by the power analyzer. These types of converter do not need an output filter for the majority of applications (drives) but it is necessary if the converter is used as a power supply. Figure 3 shows the measurement system configuration, the topology of the input/output filters used and the location of the two power analyzers. The input/output filter parameters are given in Table I.

Table I. Input /output filter parameters

Rf	20 [Ω]	L4	1.2 [mH]
L1	145 [μH]	C4	10.8 [μF]
C1	12 [μF]		
L2	850 [μH]	RL	30-15-10-7.5-4.2 [Ω]
C2	10 [μF]		
C3	660 [nF]		

III. CONVERTER MODULATION FOR COMPARISON

For comparison purposes, both the IMC and DMC prototypes were modulated using an identical, symmetrical space vector modulation (SVM) scheme as described fully in [22] and [23]. This uses 4 active vectors and 3 different null vectors during each switching period (T_p) with a converter switching frequency ($F_{sw}=1/T_p$) [20], this method results in there being 12 hard commutations per switching period for both types of converter. Table II shows the modulation scheme in more detail for each converter where the hard and soft commutations are highlighted using red and blue lines respectively. In general, there are many different ways in which the converters could be modulated which result in different switching losses and spectral performance. For example, the 3 zero SVM used within this study (with the switching sequence shown in Table II) is symmetrical whereas if it was made asymmetrical, the number of hard commutations per period would reduce from 12 to 6. Furthermore, if only 2 null vectors are used, the number of commutations is reduced to 5 and if only one zero vector is used; the number of commutations can be reduced to 4. These reductions in the number of commutations benefits the efficiency of the power stage but the waveform quality is poorer and larger filters are needed. The losses in the filters are likely to be higher as the waveform quality diminishes. The important issue for this study is that the same technique is used for both converters and hence the filter circuits and input/output waveforms are identical, resulting in identical filter losses. This allows a proper comparison of the losses in each of the power circuits. In the case of the IMC, there are three different strategies to control the switching devices when implementing the chosen SVM technique. The methods differ from one another in the way that the zero vectors are applied to the output and are referred to within the rest of the paper as modulations one, two and three.

It is also worth noting that in the IMC there are two different ways to apply the null vector:

- Using only the output stage(this is indicated on the paper as modulation one) [24]

- Using only the input stage, (this is indicated on the paper as modulation two) [25],[26]

Note that the time domain waveforms of the input current and the output voltage (and hence their spectra) are independent of which of the two different modulations are used. This is because, at the output, the same line-to-line voltage is applied to the load in both cases and also during either zero vector, the input current is zero in both instances. Furthermore the total switching losses are equal for the two modulation techniques.

It is clear that, using modulation one, all the switching losses are located on the output stage and the switching frequency of a single device is double F_{sw}; however using modulation two the switching losses are distributed between the input and output stages. Since there is the possibility to change the balance of losses between the input and output stages, the work in this paper considers the possibility of using different types of devices for both the input and output stages. In this case, it is assumed that devices which exhibit improved switching losses are used in the output stage and those which favour conduction losses in the input stage. In addition it should be realized that, using modulation two, the input stage conducts current also during the null vectors, which is not the case using modulation one. These effects become important as the power factor of the load is changed.

There is also the possibility when using the IMC to use a third modulation technique (in this paper referred to as modulation three) [26] that combines the benefits of modulation two regarding the switching loss distribution together with the advantages of modulation one regarding the minimization of the conduction losses of the input stage during the null vector. Table II shows the switching sequences of a symmetrical SVM for a particular input/output sector for the DMC and for the IMC. The red line indicates a hard commutation (four for each output phase), while the blue line indicates a soft commutation (at zero current for modulation one and at zero voltage for modulations two and three). The gate signal patterns for the input stage when using modulation three is the same as that in modulation two, while that of the output stage is the same as in modulation one. Using this last modulation strategy, two commutations occur at the same time; therefore to make sure that the hard commutation happens in the input stage, a delay time between the two commutations must be introduced. In this work this time was chosen to equal 500ns when using the Si IGBT, and 250ns while using the SiC MOSFET. For comparison, in this paper, seven different combinations of converters, devices and modulation techniques were used (note that all experimental result use the same legend reported below to identify the different test conditions):

- DMC using 18 Si IGBTs(♦ continuous line)
- DMC using 18 SiC MOSFETS (♦ dot line)
- IMC using 18 Si IGBTs with modulation one (■ continuous line)
- IMC using 18 Si IGBTs with modulation two (● continuous line)
- IMC using 18 Si IGBTs with modulation three (o continuous line)
- IMC using 12 Si IGBTs and 6 SiC MOSFETs with modulation one (■ dot line) like suggest in [5]
- IMC using 18 SiC MOSFETs with modulation three (o dot line)

In the case of 18 SiC MOSFETs in the IMC, using modulation one was not considered because there is no point in using SiC devices if they are not switching.

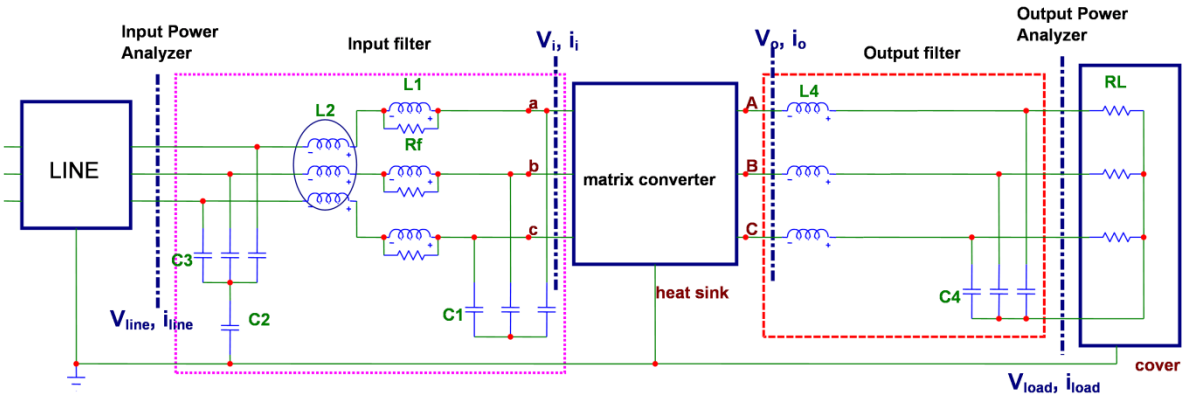


Fig.3 Measurement system configuration, where the matrix converter box can be either the DMC or the IMC

	Direct MC			Indirect MC																	
	Output phases			MODULATION ONE						MODULATION TWO						MODULATION THREE					
				virtual dclink		IDC_vir	inverter status			virtual dclink		IDC_vir	inverter status			virtual dclink		IDC_vir	inverter status		
time	A	B	C	+	-		A	B	C	+	-		A	B	C	+	-		A	B	C
T0/8	c	c	c	c	a	0	H	H	H	c	c	(IA+IB)=-IC	H	H	L	c	c	0	H	H	H
T1/2	c	c	a	c	a	(IA+IB)=-IC	H	H	L	c	a	(IA+IB)=-IC	H	H	L	c	a	(IA+IB)=-IC	H	H	L
T3/2	c	a	a	c	a	IA=-(IB+IC)	H	L	L	c	a	IA=-(IB+IC)	H	L	L	c	a	IA=-(IB+IC)	H	L	L
T0/4	a	a	a	c	a	0	L	L	L	a	a	IA=-(IB+IC)	H	L	L	a	a	0	L	L	L
				b	a	0															
T4/2	b	a	a	b	a	IA=-(IB+IC)	H	L	L	b	a	IA=-(IB+IC)	H	L	L	b	a	IA=-(IB+IC)	H	L	L
T2/2	b	b	a	b	a	(IA+IB)=-IC	H	H	L	b	a	(IA+IB)=-IC	H	H	L	b	a	(IA+IB)=-IC	H	H	L
T0/4	b	b	b	b	a	0	H	H	H	b	b	(IA+IB)=-IC	H	H	L	b	b	0	H	H	H
				b	a	0				b	b					b	b				
T2/2	b	b	a	b	a	(IA+IB)=-IC	H	H	L	b	a	(IA+IB)=-IC	H	H	L	b	a	(IA+IB)=-IC	H	H	L
T4/2	b	a	a	b	a	IA=-(IB+IC)	H	L	L	b	a	IA=-(IB+IC)	H	L	L	b	a	IA=-(IB+IC)	H	L	L
T0/4	a	a	a	b	a	0	L	L	L	a	a	IA=-(IB+IC)	H	L	L	a	a	0	L	L	L
				c	a	0															
T3/2	c	a	a	c	a	IA=-(IB+IC)	H	L	L	c	a	IA=-(IB+IC)	H	L	L	c	a	IA=-(IB+IC)	H	L	L
T1/2	c	c	a	c	a	(IA+IB)=-IC	H	H	L	c	a	(IA+IB)=-IC	H	H	L	c	a	(IA+IB)=-IC	H	H	L
T0/8	c	c	c	c	a	0	H	H	H	c	c	(IA+IB)=-IC	H	H	L	c	c	0	H	H	H

Table II Switching sequences for input current sector K_i=4 and output voltage sector K_V=1, for the DMC and for the IMC using three different ways to obtain the null vector

IV. ANALITICAL MODEL OF THE LOSSES

In this section, converter loss models are developed based on the data that is typically found in the power device data sheets. These models are initially populated with information from the relevant data sheets. Due to variability between the device operating conditions in the converter and those used in the data sheet measurements, the resulting loss values can be subject to considerable error. Accordingly the models are further developed to use data based on average values found during experimentation; this model is similar to [25]-[27] and it does not consider the effect of dead time and the commutation delay time on the conduction losses since this is a very small part of the conduction period for any particular switch. For the DMC the complete analysis is done in [20] so it is not reported here.

A. *The switching losses*

In theory, both converters should have the same total switching loss (1), because they use the same modulation technique; i.e. have the same number of commutations at the same voltage and current (see table II). In practice this is not always the case due to the differences in commutation loop areas, and the associated stray inductances; these effects will be addressed later in the paper. Switching energy loss values can be found in the data sheets and it is assumed that they are linear with voltage and current (2). For all cases the average voltage across all commutations (V_{AVc}) is the same (3) and is a function of the line voltage, which was assumed to have a constant rms value. Note that the effect of the displacement angle φ_i between the input voltage vector Vi and the input current vector Ii is not considered, since it is always maintained at zero in the experimental tests (following normal practice). The average current (I_{AVc}) of all the commutations is a function of the output current $I_{O(rms)}$ (4).

$$P_{sw} = 3F_{sw}\left[2E_{on} + 2E_{rec} + 2E_{off}\right] \quad (1)$$

$$E = E^* \frac{V_{AVc}}{V_{data\_sheet}} \frac{I_{AVc}}{I_{data\_sheet}} \quad (2)$$

$$V_{AVc} = \frac{3\sqrt{2}\sqrt{3}V_{i_{rms}}}{\pi}\int_0^{\pi/3}\cos(\omega t)\,dt \approx 466[V] \quad (3)$$

$$I_{AVc} = \frac{2}{\pi}\int_0^{\pi/2} i_o dt = \frac{2\sqrt{2}}{\pi} I_{o,RMS} \quad (4)$$

According to the data sheets of the IGBT the energy losses are also function of the gate drive resistor and the junction temperature of the IGBT.

B. *Conduction losses of the IMC*

The conduction losses of the IMC are more complex to calculate compared to the DMC, because the losses are a function of m_I and also of the load power factor (displacement angle φ_o). The conduction losses also vary depending on how the null vector is applied (see Table II).

Modulation one with Si IGBTs and Diodes

The input stage conducts current only when the active vectors are applied (time intervals T1,T2,T3,T4, see table II). During the time intervals T1&T2, the virtual dc link current has the value of $I_{DC\_1,2}$ (6) and during the time T3&T4 the virtual dc link current is equal to $I_{DC\_3,4}$ (7); those values are functions of the output current and of φ_o.

$$I_{DC\_1,2} = \sqrt{2}I_{oRMS}\sqrt{\frac{3}{\pi}\int_{\varphi_o-\frac{\pi}{3}}^{\varphi_o}[cos(\varphi)]^2\,d\varphi} \quad (6)$$

$$I_{DC\_3,4} = \sqrt{2}I_{oRMS}\sqrt{\frac{3}{\pi}\int_{\varphi_o}^{\varphi_o+\frac{\pi}{3}}[cos(\varphi)]^2\,d\varphi} \quad (7)$$

These two dc link current values could also be a function of the input sector; however since the input phase displacement angle was considered to be zero that is not the case here. The timing of the active vectors is a function of the modulation index (m_I) and the least common multiple (t_lcm) of input and output fundamental frequency periods (8)(9)

$$d_{AV1,2} = lcm\int_0^{t\_lcm}(d^I + d^{II})dt \quad (8)$$

$$d_{AV3,4} = lcm\int_0^{t\_lcm}(d^{III} + d^{IV})dt \quad (9)$$

Where $d^i = \frac{T_i}{T_p}$ for i=1..4 .

The conduction losses of the input stage are hence equal to:

$$P_{COND\_inp\_stage\_IGBT\_mod1} = 2I_{DC\_1,2}\left(V_{ce}(I_{DC\_1,2}) +\right.$$

$V_F(I_{DC\_1,2})\big)d_{AV1,2} +$
$2I_{DC\_3,4}\big(V_{ce}(I_{DC\_3,4}) + V_F(I_{DC\_3,4})\big)d_{AV3,4}$ (10)

To calculate the conduction losses of the output stage it is possible to consider only one sector of the output voltage, since the losses are equal in all the sectors. The equivalent rms value of the output currents can be calculated as in (11)-(13); noting that these values are a function of φ_o. The average duty cycles (for i=0,1,2,3,4) are shown in (14), while the losses for all of the three output legs of the converter can be calculated as in (15),(16) and (17).

$$I_{AS,RMS} = \sqrt{2}I_{oRMS}\sqrt{\frac{3}{\pi}\int_{\varphi_o}^{\varphi_o+\frac{\pi}{3}}[cos(\varphi)]^2\, d\varphi} \quad (11)$$

$$I_{BS,RMS} = \sqrt{2}I_{oRMS}\sqrt{\frac{3}{\pi}\int_{\varphi_o}^{\varphi_o+\frac{\pi}{3}}\left[cos\left(\varphi-\frac{2\pi}{3}\right)\right]^2 d\varphi} \quad (12)$$

$$I_{CS,RMS} = \sqrt{2}I_{oRMS}\sqrt{\frac{3}{\pi}\int_{\varphi_o}^{\varphi_o+\frac{\pi}{3}}\left[cos\left(\varphi-\frac{4\pi}{3}\right)\right]^2 d\varphi} \quad (13)$$

$$d_{avi} = lcm\int_0^{t\_lcm} d^i dt \quad (14)$$

$$P_{con_{outstage_{IGBT_{mod1}}}}^{legA} = I_{AS,RMS}V_{ce}\big(I_{AS,RMS}\big)\left(1-\frac{d_{av0}}{2}\right) + I_{AS,RMS}V_F\big(I_{AS,RMS}\big)\left(\frac{d_{av0}}{2}\right) \quad (15)$$

$$P_{con_{outstage_{IGBT_{mod1}}}}^{legB} = \frac{1}{2}I_{BS,RMS}V_{ce}\big(I_{BS,RMS}\big) + \frac{1}{2}I_{BS,RMS}V_F\big(I_{BS,RMS}\big) \quad (16)$$

$$P_{con_{outstage_{IGBT_{mod1}}}}^{legC} = I_{CS,RMS}V_{ce}\big(I_{CS,RMS}\big)\left(1-\frac{d_{av0}}{2}\right) + I_{CS,RMS}V_F\big(I_{CS,RMS}\big)\left(\frac{d_{av0}}{2}\right) \quad (17)$$

Modulation one with the hybrid solution (Si IGBTand diode at the input and siC MOSFETs at the output stage)

In this case the conduction losses of the input stage are the same as those shown in (10), while the conduction losses of the output stage are shown in (18)

$$P_{con_{outstage_{MOS_{mod1}}}} = 3R_{DS}(t)I_{o,RMS}^2 \quad (18)$$

Modulation two with Si IGBTs and Diodes

Using this method, unlike in modulation one, current flows in the input stage also during the null vector (time interval T_0). The two average times for the duty cycles are calculated in (19) and (20), and the conduction losses of the input stage are calculated in (21).

$$d_{AV1,2,0} = lcm\int_0^{t\_lcm}(d^I + d^{II} + d^0/2)dt = \frac{1}{2} \quad (19)$$

$$d_{AV3,4,0} = lcm\int_0^{t\_lcm}(d^{III} + d^{IV} + d^0/2)dt = \frac{1}{2} \quad (20)$$

$$P_{COND\_inp\_stage\_IGBT\_mod2} = I_{DC\_1,2}\big(V_{ce}(I_{DC\_1,2,0}) + V_F(I_{DC\_1,2,0})\big) + I_{DC\_3,4}\big(V_{ce}(I_{DC\_3,4,0}) + V_F(I_{DC\_3,4,0})\big) \quad (21)$$

From Table II, it is clear that there is always one positive current (leg_A) and one negative current (leg_C) flowing through the Si IGBTs (assuming $|\varphi_o| < \pi/6$). If the current is in the positive direction, it will flow through the upper IGBT, if it is negative, through the lower IGBT of the same inverter leg and not through the antiparallel diode. This means that the losses for leg_A and leg_C are identical (22). For one phase, the current can be either positive or negative and the losses are the same as for modulation method one (16).

$$P_{con_{outstage_{IGBT_{mod2}}}}^{legA\_and\_C} = I_{AS,RMS}V_{ce}\big(I_{AS,RMS}\big) \quad (22)$$

Modulation two with SiC MOSFETs

The losses of the output stage are calculated in the same way as described in (18), while calculations for the input stage are shown in (23)

$$P_{COND\_inp\_stage\_MOS\_mod2} = 2R_{DS}(t)(\, I_{DC_{0,1,2}}^2 + I_{DC_{0,3,4}}^2) \quad (23)$$

Modulation three

Theoretically the conduction losses of this modulation method should be identical to modulation one. In reality due to the introduction of the "dead time" to move the commutation from the output stage to the input stage the real losses are slightly higher than in modulation one. However, as mentioned earlier, dead times were not considered in this study.

Consideration of the load power factor

Within this paper all tests were carried out with a load power factor close to unity. In most applications however, e.g. motor drives, this is not a real condition. The load power factor does change the efficiency, but not the losses of the converter for the same output current. This statement is true for the matrix converter even using Si IGBTs and SiC MOSFETs; it is also true for the two stage converter if the SiC MOSFETs are used in the output stage, while for the input stage of the IMC it doesn't matter if SiC MOSFETs or Si IGBT/Diode are used. The conduction losses of the output stage will change if Si IGBT/Diode are used, because the distribution of the current between the IGBT and the Diode is also a function of the load power factor; however, considering that there is a similar voltage drop for both the IGBT and Diode, the total losses of the converter should be similar.

V. EXPERIMENTAL RESULTS

Using the system set up shown in figure 3 it is possible to measure the total input and output power of the two converters. This approach is hence able to determine losses and efficiency of both converters, measuring the total losses in the power electronic devices and filters at the same time. Since the same modulation technique is used for both converters and since the output voltage and input current waveforms are unaffected by way in which the zero vectors are applied in the IMC, the harmonic characteristics at both the input and output are identical between the DMC and IMC regardless of switching sequence selection in the IMC. This means that the losses in the filters are the same for both

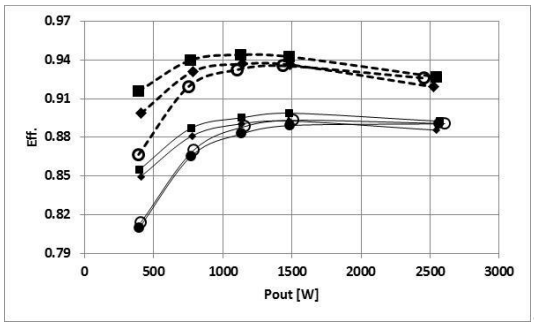
converters because they implement the same modulation technique. This will lead to an identical ripple of the input current and of the output voltage in both converters. The converters were tested for three different value of m_i (cases a, b & c), and for several different switching frequency values (F_{sw}): 10kHz in figure 4, 15 kHz in figure 5, 20 kHz figure 6, 25kHz in figure 7 and 30 kHz, in figure 8. In figures 6, 7 and 8 the MCs were tested using only the SiC MOSFETs configuration.

Important points to note about the results presented:

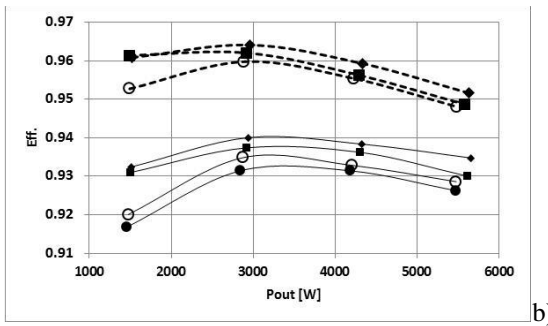
- When using the full Si solution, the DMC is more efficient in every test point compared with the IMC; only at low modulation index, when using modulation one, is the IMC is more efficient than the DMC due to the very low conduction losses during the null vector. However this solution presents other types of problems.
- At 15 kHz the IMC using modulation one and full Si solution is not able to perform the entire range of tests since all of the switching losses are concentrated in the output stage and the converter failed. So it is reasonable to conclude that if modulation one is used with the IMC when using only Si devices, the size of the IGBTs should be different between input and output stage. For example, if the devices within the output stage were replaced by the 40 A version (IKW40T120) the conduction losses would be reduced by a factor of approximately 27% at 25^{O}C and almost 40% at 150^{O}C according to the datasheets and all of the per volt-amp switching energies are also slightly reduced. The 40A version is also more able to dissipate higher losses and would enable a wider range of operating points to be used compared to the 15A versions used in the tests. This would have the effect of increasing the efficiency of the converter but at an increase in cost.
- Due to the increased switching speed of the SiC devices (SiC MOSFETs) the efficiencies of both types of MCs is improved when compared to the IGBT based converters due to the lower switching losses. It is therefore possible to increase the switching frequency without compromising the total efficiency too much (ie DMC with Si at 10 kHz has very similar in performance to the 30kHz SiC MOSFET version)
- The efficiency of the SiC MOSFET converters is improved at low current levels due to the low value of $R_{DS.}$ hence the SiC MOSFETs exhibits a low conduction loss when compared to the losses generated within the IGBT due to Vce at low current levels.
- The IMC using the hybrid solution (modulation one with Si devices at the input and SiC at the output) always performs better when compared with the IMC using a full SiC solution and modulation 3.
- The DMC using the full SiC solution is better than the IMC using the hybrid solution when operated at high modulation index, while at low modulation index the IMC has better performance. The point where they have similar performance is where the modulation index is around 0.5. Considering that, at present, the SiC devices are much more expensive than the Si devices (for low quantities and standard distribution routes the price ratio is around 3), it seems that the best way to improve the efficiency and limit the cost is to use the IMC with the hybrid solution and modulation method one although the switching performance seems to be highly dependent on the physical implementation of the converter and the commutation loop inductance plays an important role in achieving the best performance from the devices. The packages used by the semiconductor manufacturers are the ultimate driver for the physical size of the converter and hence commutation loop sizes which can be realized. Further explanation and examples regarding the layout of the converters used in this study is given later in the text.

VI. ESTIMATION OF THE POWER ELECTRONIC LOSSES FROM EXPERIMENTAL MEASUREMENTS

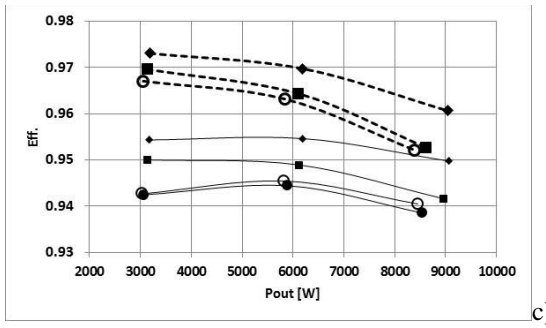
As mentioned in the previous section the experimental results are based on the losses of the full converter i.e. including the power electronics and the input/output filters. The main losses within the filters are in the differential mode inductors. The measured spectrum of the inductor current is used to calculate the resistive losses, including the effect of measured AC resistance variation [20]. Core loss is determined using the datasheet loss characteristics in conjunction with the harmonic fluxes (also calculated from the current harmonic measurements).



a)

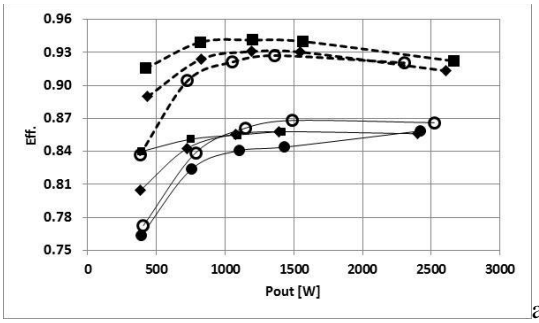


b)

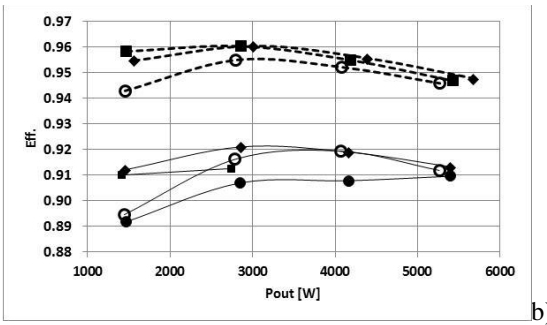


c)

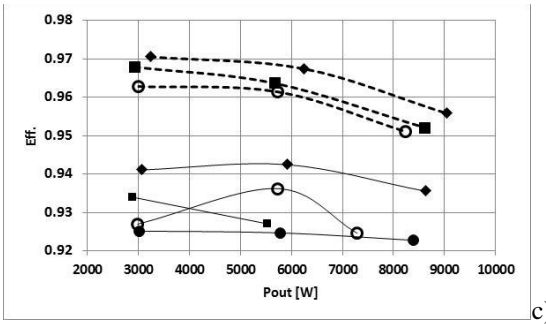
Fig. 4 Efficiency of the converters with Fsw=10 Khz, a) $m_I \approx 0.25$, b) $m_I \approx 0.5$, c) $m_I \approx 0.8$. (♦)DMC-18 IGBTs; (♦---)DMC-18 SiC MOS; (■)IMC 18 IGBTs-Mod1; (●)IMC-18 IGBTs-Mod2; (o)IMC 18 IGBTs-Mod3; (■---) IMC 12 IGBTs 6 SiC MOS-Mod1; (o---); IMC 18 SiC MOS-Mod3



a)

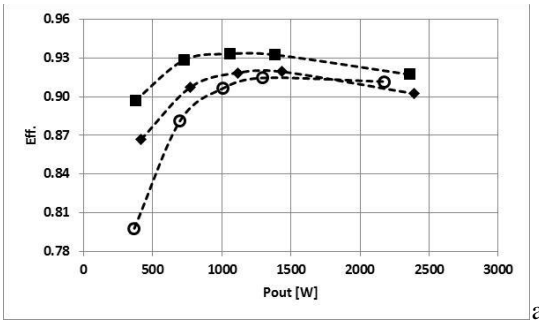


b)

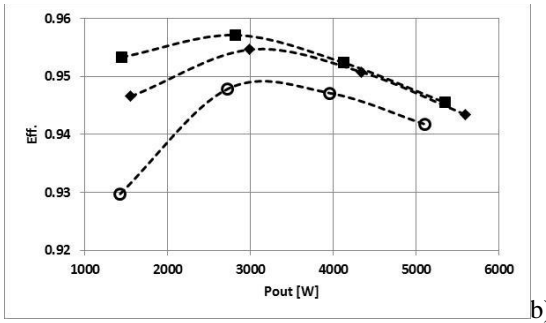


c)

Fig. 5 Efficiency of the converters with Fsw=15Khz, a) $m_I \approx 0.25$, b) $m_I \approx 0.5$, c) $m_I \approx 0.8$. (♦)DMC-18 IGBTs; (♦---) DMC-18 SiC MOS; (■)IMC 18 IGBTs-Mod1; (●)IMC-18 IGBTs-Mod2; (o)IMC 18 IGBTs-Mod3; (■---)IMC 12 IGBTs 6 SiC MOS-Mod1; (o---); IMC 18 SiC MOS-Mod3



a)



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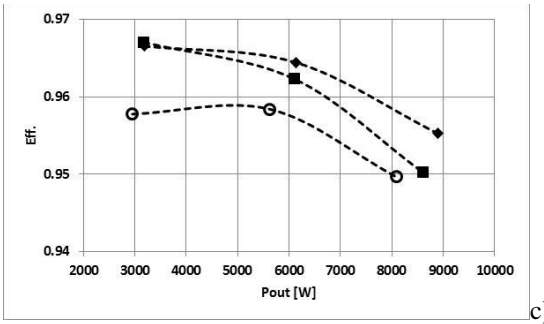
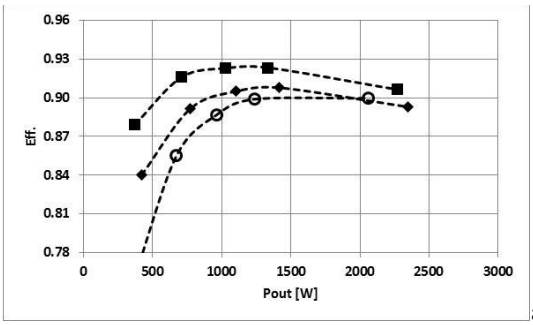
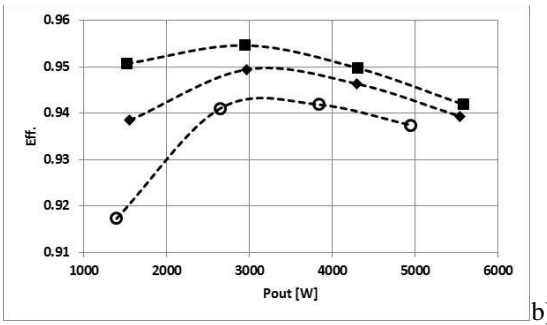


c)

Fig. 6 Efficiency of the converters with Fsw=20Khz, a) $m_I \approx 0.25$, b) $m_I \approx 0.5$, c) $m_I \approx 0.8$.



a)



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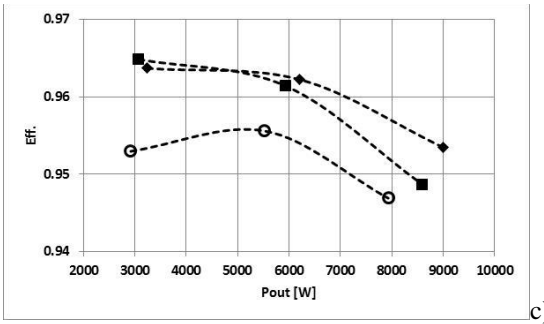
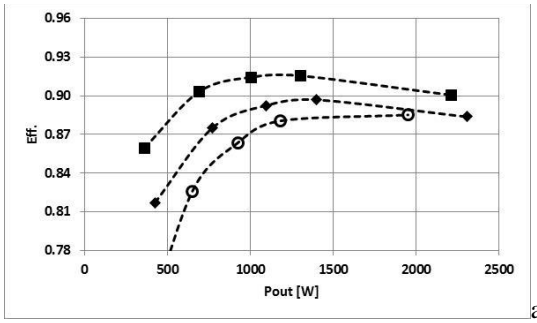


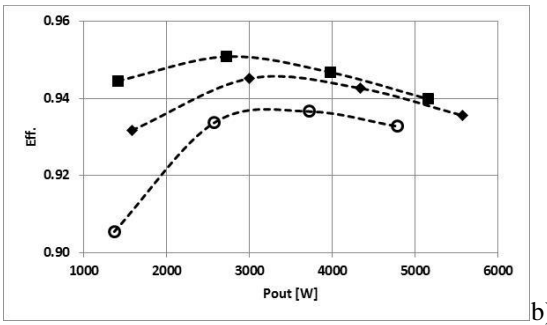
c)

Fig. 7 Efficiency of the converters with Fsw=25Khz, a) $m_I \approx 0.25$, b) $m_I \approx 0.5$, c) $m_I \approx 0.8$.

By removing the losses of the input/output inductors from the total losses, it is possible to estimate the losses of the power electronic devices since the losses within the film capacitors were assumed to be almost negligible. Figure 9 shows the losses of the power electronics for the DMC using a full SiC solution and for the IMC with the hybrid solution for $m_I \approx 0.5$ and a load current around 12Arms. It is important to notice on figure 9 that the losses are proportional to the switching frequency as one would expect.



a)



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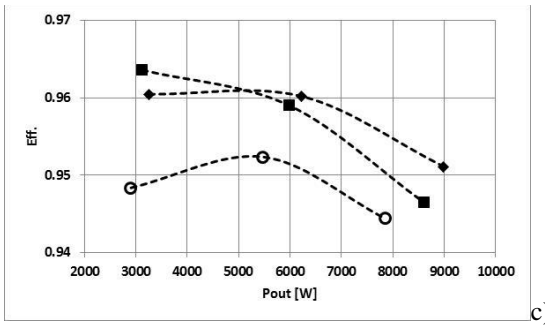


c)

Fig. 8 Efficiency of the converters with Fsw=30Khz, a) $m_I \approx 0.25$, b) $m_I \approx 0.5$, c) $m_I \approx 0.8$. (♦)DMC-18 IGBTs; (♦---) DMC-18 SiC MOS; (■)IMC 18 IGBTs-Mod1; (●)IMC-18 IGBTs-Mod2; (o)IMC 18 IGBTs-Mod3; (■---)IMC 12 IGBTs 6 SiC MOS-Mod1; (o---); IMC 18 SiC MOS-Mod3

However, while in theory the switching losses should be identical for each converter as all of the commutations are performed at the same voltages and currents, the switching losses of the DMC are measured to be higher than those of the IMC. This occurs even when using the same gate driver with the same gate resistor. This is due to the fact that the distance between the devices involved in a commutation is much smaller on the IMC due to the layout; this means the parasitic loop inductances are much lower and it is possible to switch faster, A simple example to illustrate this practical difference between the converters can be seen if we look at the switching sequences in Table II. Take for example the beginning of the sequence where output phase leg C commutates from input phase c to phase a using the labeling system introduced in Figure 2, this corresponds to a commutation between device numbers 13 and 14 for the IMC (fig 2b) and device numbers 13 and 17 for the DMC (fig2a). There is clearly a much smaller distance for the current to commutate with this implementation of the IMC compared to the DMC which increases the inductance in the commutation path.

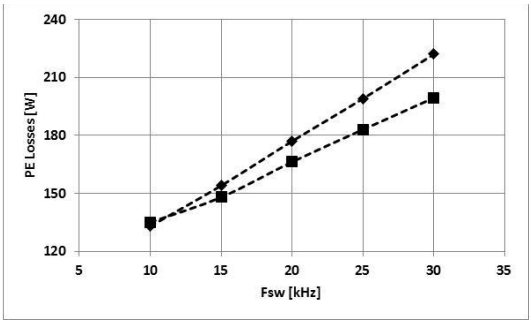


Fig. 9 Estimation of the power electronic losses based on measurements with respect to the switching frequency, with $m_I \approx 0.5$, and ≈12Arms load current

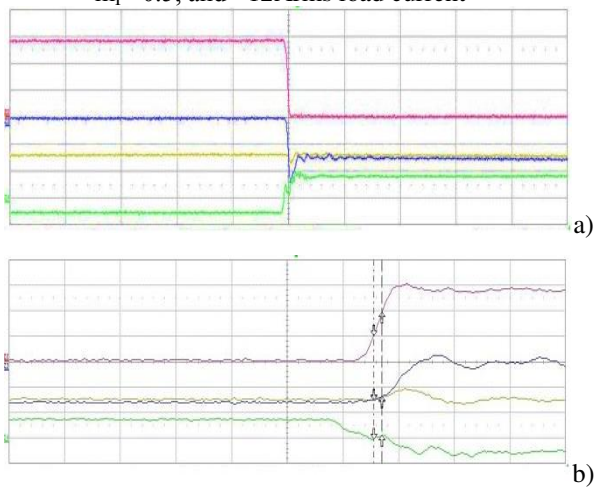

a)
b)

Fig. 10 switching performance of the SiC MOSFEST on the output stage of the IMC. a) turn on (500nsec/div) b) turn off (50nsec/div). (Red V_{DS} 200V/div, Green V_{GS} 20V/div, yellow current output phase 20A/div, blue devices current 20A/div)

This allows the IMC, as implemented in this study, to switch faster than the DMC even though the same gate drive components are used in both.

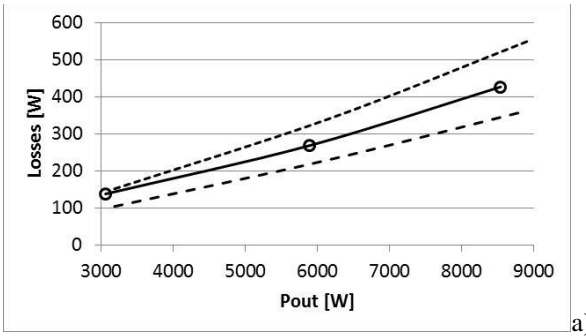
Figure 10 shows the switching performance of the SiC MOSFETS on the output stage of the IMC, while paper [20] shows the switching performance of the same devices in the DMC. In the DMC the average dv/dt is around 11kV/µsec, while for the IMC it is around 20kV/µsec.

VII. COMAPRISON

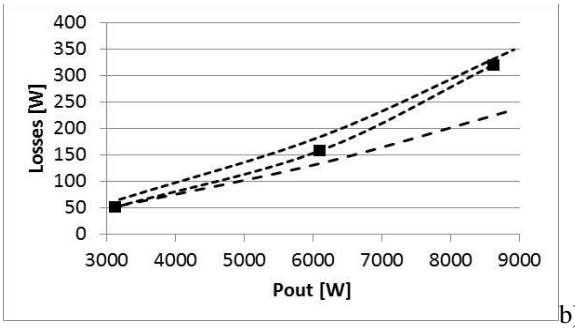
Figure 11 a) shows the extrapolated losses of the power electronic devices of the IMC using Si devices and modulation 3 together with the loss curves calculated by the analytical loss model at both 25°C and 150°C.

Figure 11 b) shows the extrapolated losses of the power electronic devices of the IMC when using the hybrid solution and modulation 1 together with the losses calculated by the analytical loss model at 25°C and 150°C.

All the experimental results for the two converter structures at the different operating conditions are within the limits identified by the analytical model for both high and low temperatures. For simplicity only two pictures are reported here.



a)



b)

Fig.11 Extrapolated Power Electronic losses of the IMC and the calculated losses at 25°C(-) and 150°C (--), at 10kHz, and $m_I \approx 0.8$ a) full Si converter, b) hybrid converter, modulation 1

The loss calculation with a T_j equal to 25°C does not represent a real operating condition since that is more likely to be the ambient temperature and the junction will always be at a higher temperature. On the contrary the loss calculation at T_j equal to 150°C represents an "extreme condition" because this is the maximum allowed temperature of the junction.

It is worth remembering that the junction temperature is not just a function of the device losses, but also of the cooling system. For the specific Si devices used in this study, the switching losses increase significantly as Tj increases, while the conduction losses, even if they are function of Tj, do not however change substantially when compared to the SiC devices. In these devices, the switching losses are almost constant with an increasing Tj, while the conduction losses increase a great deal as Tj increases. For example; if the data for V_{CE} for the IGBT[28] is used to determine the voltage drop at 20A for example using a 15V gate voltage, at 25^{O}C, V_{CE} ~=1.9V and ~=2.5V at 150^{O}C corresponds to a 30% increase. Similarly for the diode, at 20A, a 5% increase can be observed when the temperature increases from 25 to 150^{O}C, For the SiC MOSFET[29], R_{DS} increases by 60% for the same temperature rise. The detail of these observations is of course specific to the particular devices used and there may be variations with other devices which should be taken into account at the design stage.

VIII. CONCLUSIONS

This paper has presented an efficiency comparison between two topologies of matrix converter, the direct (DMC) and indirect (IMC) using different technologies of switching devices, both silicon (IGBT, diodes) and silicon Carbide based (SiC MOSFETs). The IMC was tested using three different ways of applying the null vector, indicated within the paper as modulation 1, 2 and 3. The tests have been carried out using the same load and supply conditions using the same modulation technique to ensure a like-for-like comparison of the loss performance of the different topologies and switch configurations. It can be said that the total switching losses should be the same in both topologies, but as shown within the results presented here, the switching losses also depend on the parasitic inductances present in the commutation loops and hence the converter layout, irrespective of topology, plays an important role in loss creation where high speed devices are concerned.

It is also not possible to come to an ultimate conclusion as to which configuration is the 'best' as this depends heavily on the load duty and application to which the converter will be subjected to during its lifetime. However having said that, some general conclusions can be drawn based on the presented data. At high modulation index, the DMC is in general more efficient than the IMC, this is due to the fact that in the DMC there are only two active devices which provide the load current path from the grid to the load whereas the IMC has three devices and hence the conduction losses are higher in the IMC in this case. The opposite is true at low modulation index where the null vector of the IMC can be implemented to cause only two devices to conduct the load current where the DMC will have four devices in series for the re-circulating current.

Further degrees of freedom are offered in the IMC in that the null vector can be implemented in three different ways which can change the balance of losses between input stage and output stage. This can offer a further advantage in the implementation of a hybrid solution where high speed SiC devices are used on the output stage. Here, the SiC devices offer a lower loss and the modulation pattern can then be changed to favor the input stage creating the possibility of using a low cost Si IGBT/diode solution for the input stage and a higher cost, but higher performance stage at the output.

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