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Research Article

Experimental Evaluation on the Influence of RCD Snubbers in a 3-Level Thyristor Based MLCR CSC

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Multilevel current reinjection (MLCR) concept provides self-commutation capability to thyristors, enabling thyristor based current source converters (CSC) to operate under negative firing angle. It also lowers the input current harmonic distortion. This is achieved by using an auxiliary reinjection bridge. Extensive experimental results are presented in this paper to analyse the performance of the 3-level MLCR CSC for different snubber components across the reinjection bridge. The trade-off in the choice of the snubber circuit is illustrated, with its influence on the AC side line current and DC side output voltage of the 3-level MLCR CSC.

1. Introduction

In order to reduce the harmonic content in the line current caused by High Voltage Direct Current (HVDC) converters, different strategies have been proposed. These are (i) multipulse methods, (ii) multilevel methods, and (iii) pulse-width modulation (PWM) methods.

Different methods for increasing the number of pulses using multipulse converters have been investigated [1]. The simplest method is by increasing the pulse number by using phase-shifting transformers. Multipulse converters such as 12-, 18-, 24-, and 36-pulse converter are used nowadays and the total harmonic distortion (THD) of the input line current of these converters has been reduced to around 15.2%, 10.1%, 7.5%, and 5.3%, respectively. Many modelling techniques for phase-shifting converter transformers have been also proposed in [2–4] to meet the IEEE 519 standards. However, the weakness of these methods is the increase in size and complexity of the transformer and the high costs involved due to multiple 6-pulse bridges. A DC side current injection method [5] improves the quality of the AC side line currents by using a three-phase current-controlled inverter which injects compensation currents in the AC side of the converter. However, this method uses a complex 18-pulse phase-shifting transformer.

Multilevel converters give significantly lower switching losses and better harmonic performance [6–8] than equivalent series-connected converters operating at the same rating and carrier frequency but advantages of multilevel converter are counterbalanced by the need for self-commutated switches instead of thyristors, balancing of capacitors, and so forth. Modular current source converters (MCSC) utilise PWM techniques just like the PWM-voltage source converters (VSC). Two-level PWM-VSC or Modular Multilevel Converter (MMC) [9] has been used by the industry, for example, HVDC-light and HVDC-plus, respectively. However, they are only being used for medium voltage HVDC transmission. MCSC utilise selective harmonic elimination [10] as the PWM strategy but the use of thyristors in the main bridge is still not possible. Ongoing research in the field of MMC converters includes direct power control [11], neural network based sliding mode control [12], and fuzzy logic based control [13].

It is now established that PWM-VSC/MMC/MCSC technology is well suited for the medium voltage levels but will not be able to catch up with the thyristor based technology in terms of high power handling capacity in the very near future. Thus, there is a clear incentive for research in the thyristor based HVDC technology to achieve the following:

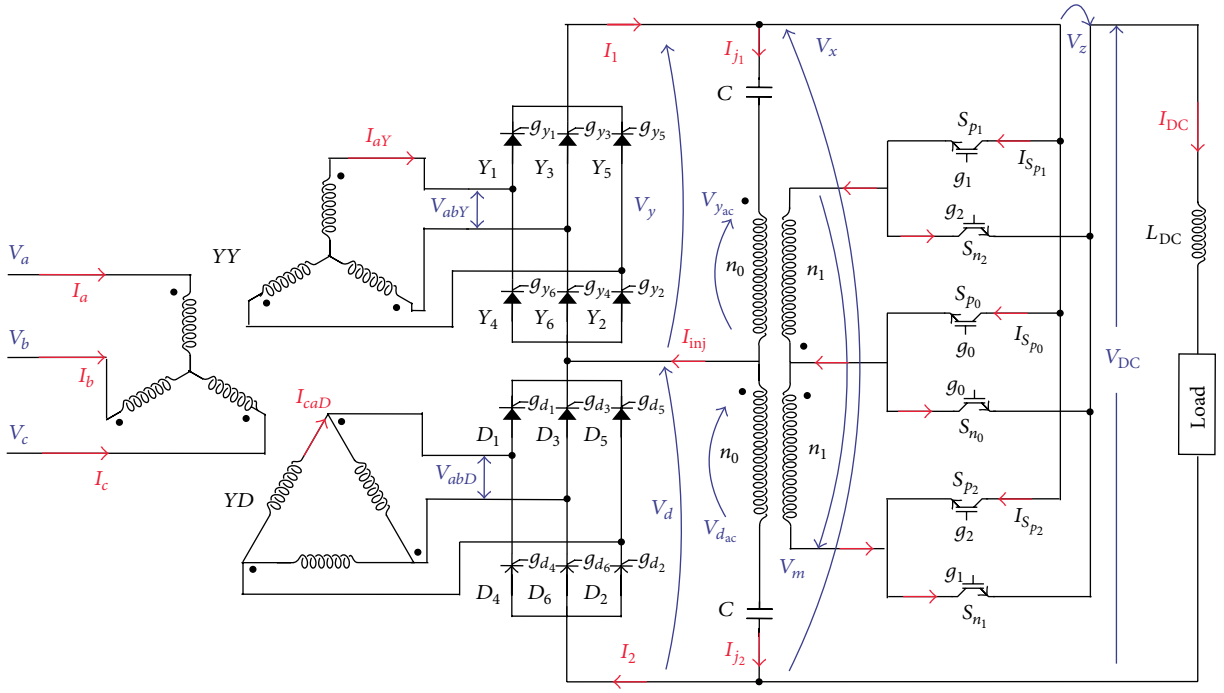


Figure 1: Three-level thyristor based MLCR CSC with Linear Reinjection.

(i) Achieve force commutation with thyristors.

(ii) Operate at negative firing angles enabling reactive power export.

(iii) Operate the thyristors under zero-current switching lowering the switching losses, voltage stress, and costs.

(iv) Reduce harmonic distortion caused by thyristor based systems.

The new concept of multilevel current reinjection (MLCR) [14] combines the advantages of DC-ripple reinjection [15, 16] and multilevel conversion and soft switching technique. Thyristor based MLCR current source converter (CSC) was proposed in [17] where the magnitude and duration of the reinjection current, used to minimize the harmonic content, were adjusted to ensure that the currents through the main bridge thyristors are forced to zero during the main bridge commutations instants. This possibility had the important implication that the thyristors do not need to rely on the line voltage to commutate and are capable of operating with firing angles that provide leading power-factor just like self-commutating switches. Based on this, the self-commutated HVDC MLCR CSC was introduced in [18].

However, questions have been raised about the ability to force the main thyristors off using the reinjection bridge. In a real world implementation, there are inevitable stray capacitance and inductances which may influence the thyristor turn-off and simulation switching model may not fully represent the switching characteristics accurately. The question that needed answering was whether these would hinder the self-commutation ability with thyristors. For this proof of concept, a small-scale prototype of a 3-level MLCR CSC has been built in the laboratory. The experimental investigation (under steady-state conditions), presented here, shows that the line currents in AC side of MLCR CSC follow the theoretical current wave-shape well. This has clearly demonstrated that self-commutation ability is achievable in a practical system by the use of an auxiliary reinjection bridge.

RCD snubber is necessary across the reinjection bridge switches to limit the sharp rise in voltage across it due to the sudden interruption of current flowing through it. This paper presents the experimental investigation of the influence of the RCD snubber across the reinjection switches in a 3-level thyristor based MLCR CSC performance. This paper is divided into the following sections: Section 2 provides the brief introduction to the 3-level thyristor based MLCR CSC; Section 3 provides the PSCAD/EMTDC simulation results, with and without the RCD snubber circuit, of the performance of the 3-level MLCR CSC. Section 4 presents some of the main hardware modules while Section 5 presents the experimental results obtained. The trade-off in choice of the snubber circuit is explained clearly with respect to AC side line current and DC side voltage waveforms.

2. Three-Level Thyristor Based MLCR CSC

Figure 1 shows the 3-level thyristor based MLCR CSC along with the reinjection circuit. The reinjection transformer is a single-phase two-winding transformer with 1:1 turns ratio. The primaries of the two single-phase transformers are connected across the DC bus through DC blocking capacitors (C). The DC current (I_{DC}) flows through the reinjection IGBTs and load inductance (L_{DC}) and the load. It is chopped into AC waveforms in the secondary windings

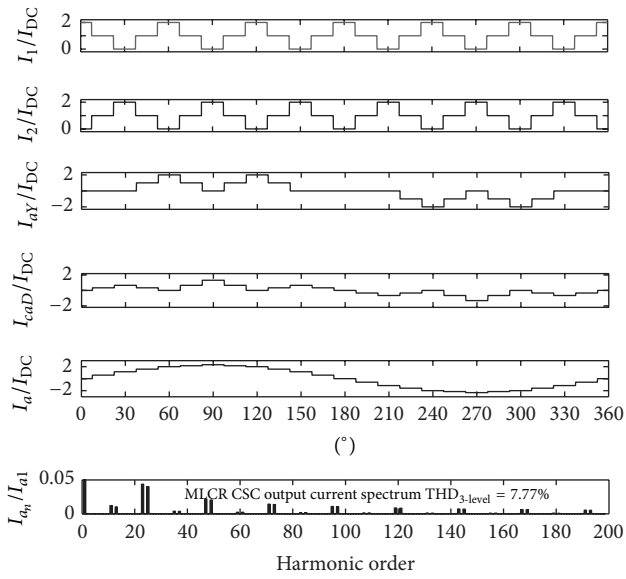


Figure 2: Current waveforms for 3-level thyristor based MLCR CSC with Linear Reinjection.

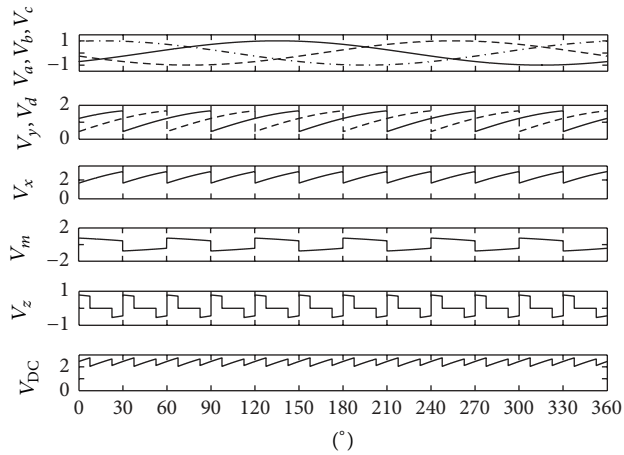


Figure 3: Theoretical DC voltage waveforms for 3-level thyristor based MLCR CSC for $\alpha = -45^\circ$.

of the reinjection transformer with the help of reinjection switches (S_{p_1}/S_{n_1}, etc.). These currents are coupled to the reinjection transformer primary winding to form multilevel currents I_{j_1} and I_{j_2} which combine with I_{DC} to shape the DC bus currents I_1 and I_2 into multilevel waveforms. This reinjection circuit generates three current steps in I_1 and I_2. Two levels are generated due to reverse connected switches (S_{p_1}/S_{n_1} and S_{p_2}/S_{n_2}) and one additional level is obtained by firing S_{p_0}/S_{n_0} when I_{j_1} and I_{j_2} are both zero.

2.1. AC Side Current Waveforms. The theoretical analysis of the circuit shown in Figure 1 allows $I_a(\omega t)$ to be determined from the time domain components of the AC side secondary currents $I_{aY}(\omega t)$ and $I_{caD}(\omega t)$. This gives

$$I_a(\omega t) = \frac{1}{k_n}\left[I_{aY}(\omega t) + \sqrt{3} I_{caD}(\omega t)\right], \quad (1)$$

where k_n is interface transformer turns ratio. The corresponding current waveforms are shown in Figure 2 where the resulting current (I_a) $THD_{3\,level}$ of 7.77% is obtained.

2.2. DC Side Voltage Waveforms. The DC side voltage waveforms (Figure 3) are time referenced with respect to the AC side current waveform I_a (Figure 2). The DC side voltages across the individual bridges ($V_y(\omega t)$ and $V_d(\omega t)$) are plotted in Figure 3 with respect to the peak phase source voltage (V_{p_k}) and can be expressed as for the first $\pi/6$ interval as

$$\begin{aligned} V_y(\omega t) &= \frac{\sqrt{3}}{k_n} V_{p_k} \cos(\omega t + \alpha), \\ V_d(\omega t) &= \frac{\sqrt{3}}{k_n} V_{p_k} \cos\left(\omega t + \alpha - \frac{\pi}{6}\right), \\ V_x(\omega t) &= V_y(\omega t) + V_d(\omega t), \end{aligned} \quad (2)$$

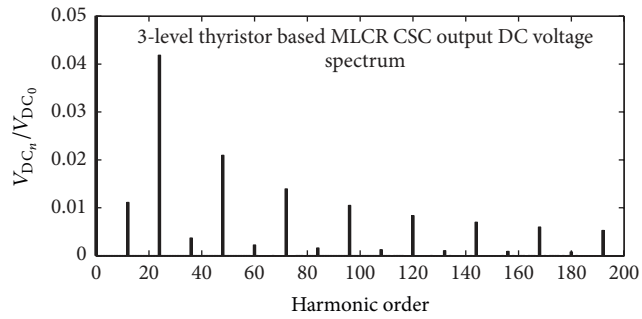


FIGURE 4: Harmonic spectrum of V_{DC} of 3-level thyristor based MLCR CSC for $\alpha = -45^{\circ}$.

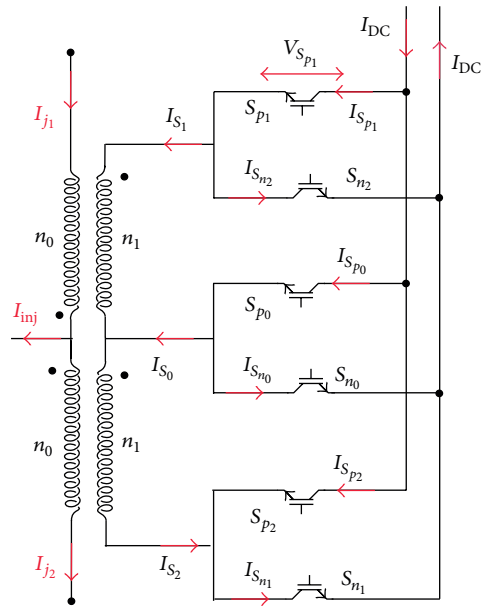


FIGURE 5: Reinjection current flow for a 3-level MLCR CSC.

where α is firing angle. The DC load voltage (V_{DC}) is calculated as

$$V_{DC}(\omega t) = V_x(\omega t) + V_z(\omega t) \approx 3.39 \frac{V_{p_k}}{k_n} \cos \alpha. \quad (3)$$

The harmonic spectrum of V_{DC} is shown in Figure 4. It can be clearly seen that the dominant harmonics are 24th, 48th, 72nd, 96th, and 120th which represents 24-pulse operation. A small amount of 12-pulse related harmonics such as 12th, 36th, and 60th can also be seen but the magnitude is negligible.

2.3. Reinjection Current Waveforms. Figure 5 labels the various current waveforms in the reinjection circuit. The "chopping" of load current I_{DC} occurs with the help of the reinjection IGBTs. The injection current I_{inj} is a 3-level waveform composed of the following:

(i) When reinjection IGBT pair $S_{p_1} - S_{n_1}$ conducts, $I_{j_1} = (n_1/n_0)I_{DC} = I_{DC}$.

(ii) When reinjection IGBT pair $S_{p_0} - S_{n_0}$ conducts, $I_{j_1} = 0$.

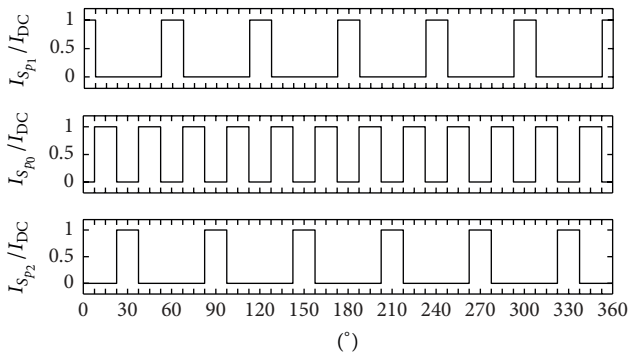
(iii) When reinjection IGBT pair $S_{p_2} - S_{n_2}$ conducts, $I_{j_1} = -(n_1/n_0)I_{DC} = -I_{DC}$.

Reinjection currents I_{j_1} and I_{j_2} add up to form I_{inj} which is injected back to the midpoint of the 12-pulse converter. The theoretical current waveforms in the reinjection circuit are shown in Figure 6.

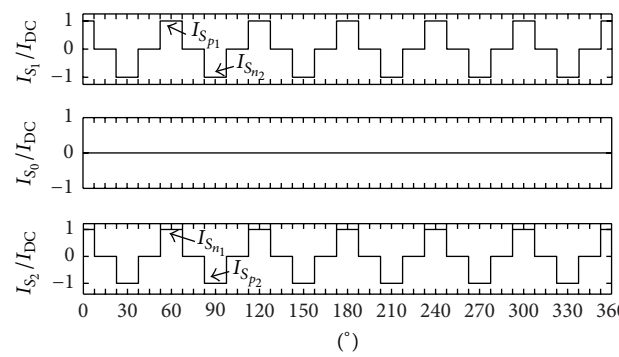
3. PSCAD/EMTDC Verification

This section presents the PSCAD/EMTDC simulation results of the thyristor based 3-level MLCR CSC. The converter is directly connected to a balanced 3-phase voltage source with series resistance and series inductance. The simulation is carried out under the conditions listed in the Appendix.

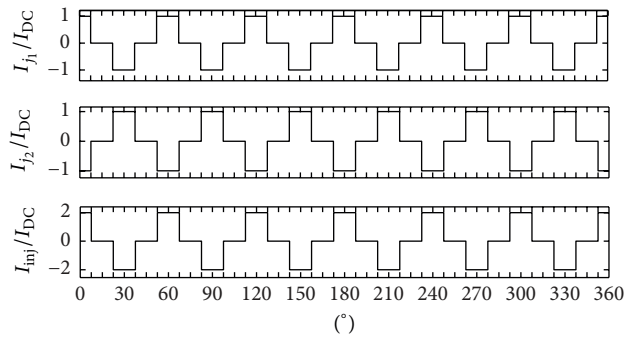
3.1. Waveforms without RCD Snubber. The voltage waveform across the reinjection IGBT S_{p_1} as well as the current flowing through it, without the RCD snubber, is shown in Figure 7. It can be clearly seen that there is a sharp rise in voltage across $V_{S_{p_1}}$ whenever there is a current transition through



(a) $I_{S_{p1}}$, $I_{S_{p0}}$, and $I_{S_{p2}}$ waveforms



(b) I_{S_1}, I_{S_0}, and I_{S_2} waveforms



(c) I_{j_1}, I_{j_2}, and I_{inj} waveforms

Figure 6: Theoretical waveforms in the reinjection circuit.

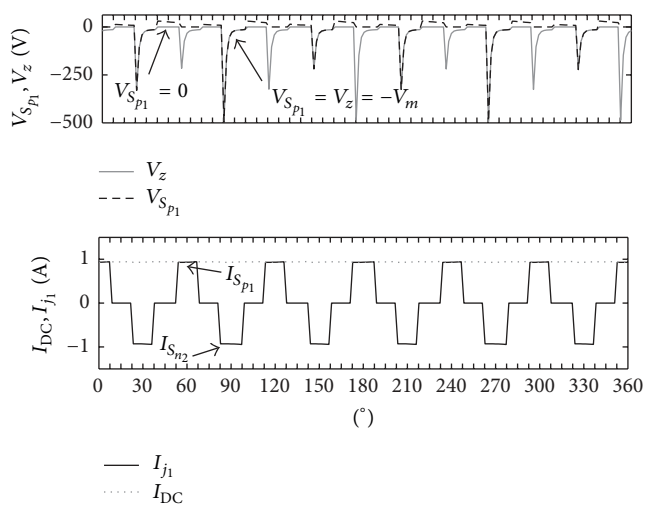


Figure 7: $V_{S_{p1}}$ and I_{S_1} with no snubber.

it, that is, current transition from 0 to $-I_{DC}$ or 0 to I_{DC}. This effect was not considered while deriving the theoretical waveforms. As seen from Figure 8, these voltage spikes occur across the individual DC voltage waveform of the two 6-pulse bridges which in turn affect the voltages V_m and V_z. The spikes occur exactly 7.5° before and after the theoretical main bridge switching instant. Thus there is a need to limit the voltage dv/dt using RCD snubber to an acceptable value so that the voltage across the main bridge switches and DC blocking capacitor and the reinjection transformer are within their rated values.

The simulated AC side current waveforms are shown in Figure 9. The simulated line current THD of 7.8% is very close to the calculated theoretical value.

3.2. Waveforms with RCD Snubbers. As illustrated in Figure 10(b), the snubber capacitor size is a trade-off between dv/dt across the reinjection switches and switching

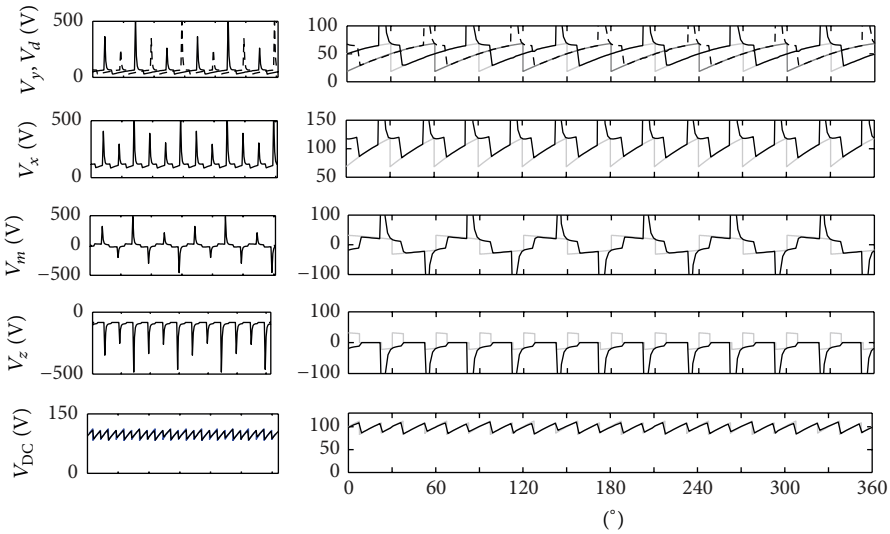


Figure 8: Simulated DC voltage waveforms for 3-level thyristor based MLCR CSC for $\alpha = -45^\circ$ without RCD snubber.

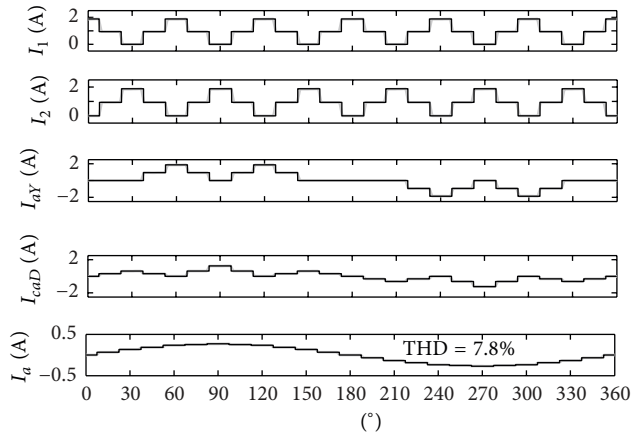


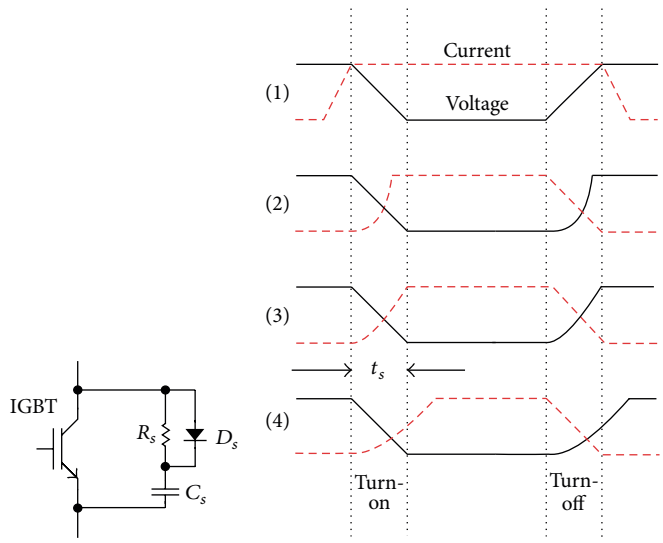
Figure 9: Simulated AC current waveforms for 3-level thyristor based MLCR CSC for $\alpha = -45^\circ$ without RCD snubber.

time. A "normal" snubber is defined as the one which allows the current to reach the rated level at the same time the voltage reaches zero. A small snubber allows the current to rise faster while a large snubber slows the current rise rate. However, large capacitor values will provide overclamping. When the RCD snubber is used to control the rate of voltage rise at the IGBT, the capacitor must be completely charged and discharged during each cycle to be able to control the rate-of-rise of the drain voltage. The RC time constant of the snubber should be much smaller than the switching period. Usually, the time constant (τ_{RC}) should be (1/10)th of the switching period. The value of snubber capacitor C_{sn} is given by the following equation [19]:

$$C_{sn} = \frac{It_s}{2E}, \tag{4}$$

where I is maximum IGBT current (assumed) = 2 A, t_s: ≈1.65 μs (3 times the value given in the datasheet of the IGBT), and E is the maximum expected voltage across IGBT: $\approx 0.9(V_{p_k}/k_n) \approx 36.72$ V for the present application. Substituting these values in (4) gives $C_{sn} = 0.045\,\mu$F. The value of R_{sn} is determined by allowing the switching time constant (τ_{RC}) to be less than 166.66 μs ((1/10)th of 600 Hz). With $C_{sn} = 0.05\,\mu$F and $R_{sn} = 1\,\text{k}\Omega$, $\tau_{RC} = 50\,\mu$s.

Three different cases are considered in this study, small $C_{sn} = 0.01\,\mu$F, large $C_{sn} = 0.1\,\mu$F, and very large $C_{sn} = 1\,\mu$F. The PSCAD/EMTDC results are presented in Figures 11–15. From Figure 11, with $C_{sn} = 1\,\mu$F the voltage across $V_{S_{p_1}}$ is closest to its calculated value; however the rate of current rise for the switch S_{p_1} is slowest. $C_{sn} = 0.01\,\mu$F provides higher rate of current rise in S_{p_1} and the current reinjection current resembles the theoretical current more closely. THD for line current I_a is obtained as 7.9%, 8.1%, and 8.7%, respectively, with $C_{sn} = 0.01\,\mu$F, 0.1 μF, and 1 μF (Figures 12–14). The effectiveness of the MLCR scheme depends on the modification of the constant DC bus current into a 3-level DC bus current using reinjection current I_{inj}. The use of small C_{sn} is found to be the best even though it requires overrated reinjection switches as shown in Figure 11.



(a) RCD snubber for reinjection IGBT

(b) Voltage and current waveforms for (1) ideal and (2) small snubber and (3) normal snubber and (4) large snubber

FIGURE 10: Snubber consideration for reinjection switches.

4. Hardware Modules

The major components of the experimental set-up consist of voltage sensing, thyristor driver circuit, IGBT driver circuit, and so forth. Each will be discussed in the following sections.

4.1. Voltage Transducer Circuit. Voltage sensors LEM LV25-P [20] are used to convert power level voltage into low voltage signals by scaling down the measured voltage to 5 V_{RMS} The Hall effect transducers provide the isolation between the high power system and the control electronic circuit. For a 12-pulse converter, six voltage sensors are used. The line voltages sensed are V_{an}, V_{bn}, V_{cn}, V_{ab}, V_{bc}, and V_{ca}. The triggering signals for the Y-Y and Y-D connected converters are derived from the low voltage sensed signals V_{ca_Y} and $-V_{an_Y}$, respectively.

The LV25-P scales down the power level voltage into low level signal when a current proportional to the measured voltage is passed through the resistor R_{in} (Figure 16(a)). For the best accuracy of LV25-P, R_{in} should be so selected that the voltage measured corresponds to a primary current ($I_{\text{in}_{\text{RMS}}}$) of 10 mA. The current conversion ratio is 2.5; hence, the nominal secondary current is 25 mA. This secondary current flows through an output series resistance R_{out} to give the scaled down voltage. The fabricated PCB for this purpose is shown in Figure 16(b). The maximum and minimum value of the series resistance R_{out} with a ±15 V supply are between 100 Ω and 350 Ω.

The 12-pulse interface transformer rating is ($V_{\text{LL}_{\text{RMS}}}$) 400 V : 50 V. The primary side input resistance is calculated as

$$R_{\text{in}} = \frac{400\,\text{V}}{10\,\text{mA}} \approx 40\,\text{k}\Omega. \tag{5}$$

A fixed value resistor of 40 kΩ/5 W is used.

The output voltage is fixed at 5 V_{RMS}. Therefore, the output resistance R_{out} is calculated as

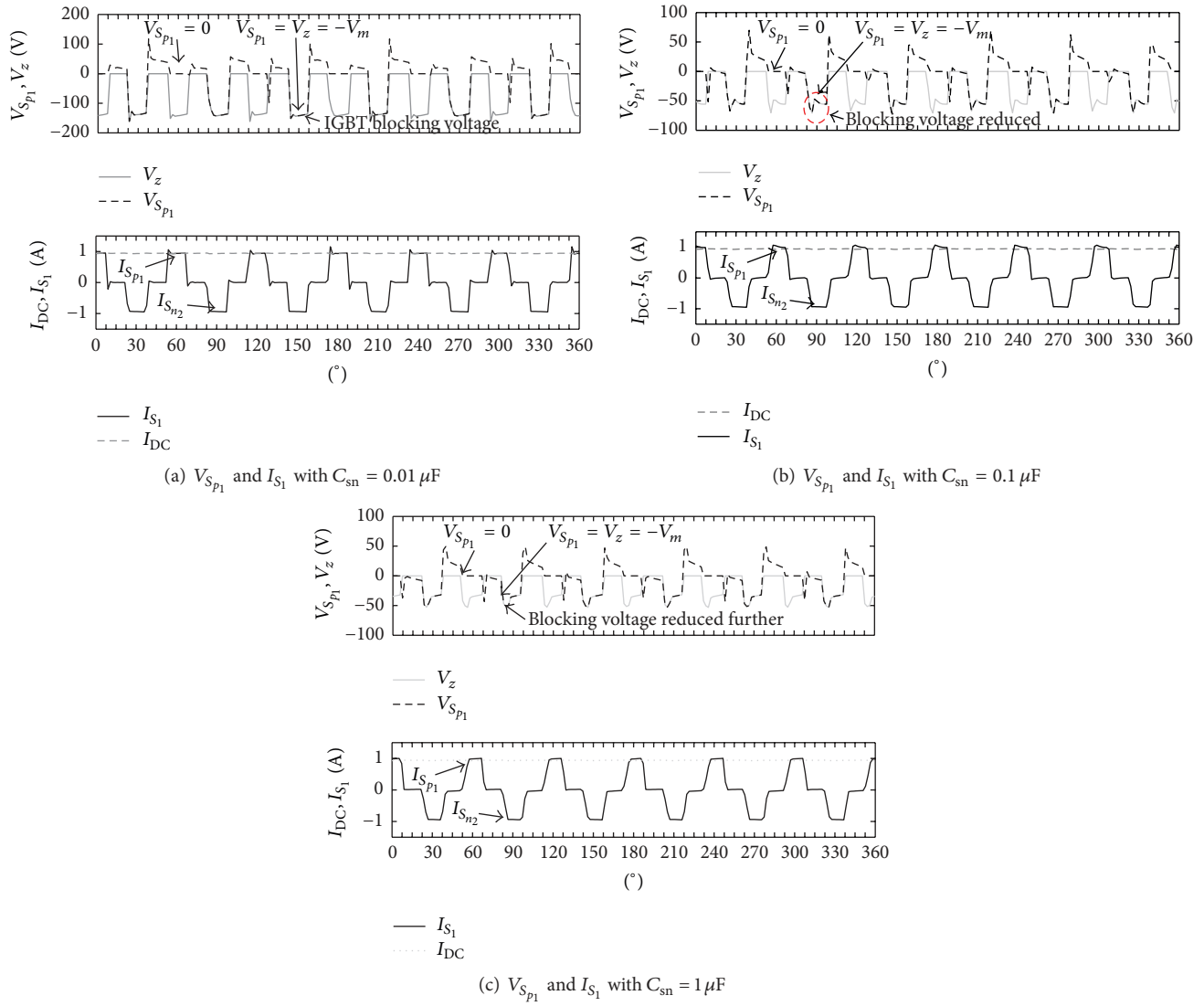
$$R_{\text{out}} = \frac{5}{25\,\text{mA}} \approx 200\,\Omega. \tag{6}$$

A variable 500 Ω/0.6 W resistor is used.

4.2. Forward Converter Based Thyristor Driver Circuit. The thyristor driver circuit is based on the forward converter topology with isolation between the control and power circuit being provided by the 77205C pulse transformer [21] (Figure 17(a)).

When the MOSFET is on, diode D_2 conducts and V_{sec} = 5 V is available across the secondary winding of the pulse transformer. V_{sec} drives gate current I_g in the gate-cathode junction of the thyristor to turn it on. For $I_g \approx 200$ mA, the gate drive resistor $R_g = 12.5\,\Omega$. When the MOSFET is off, diode D_1 returns the energy stored in the pulse transformer back to the supply. The 6-pulse thyristor PCB is shown in Figure 17(b) which uses BT152800R thyristors [22].

4.3. Generating of Reinjection Pulses for 3-Level MLCR. In order to produce the firing sequence needed to generate the 3-level I_{inj}, the firing sequences of the reinjection IGBTs are synchronised with the main bridge switching. In Figure 18 it is shown that each reinjection turn-on pulse is delayed from the main bridge switching pulse by 52.5° and the width of the turn-on pulse is 15°. Based on the six main bridge switching pulses, six reinjection turn-on pulses are derived and these are added together from the reinjection pulse for reinjection IGBT pair S_{p_1}/S_{n_1}. Following a similar procedure, the reinjection pulse for reinjection IGBT pair S_{p_2}/S_{n_2} is also derived as shown in Figure 19. A minimum dead time of 10 μs is selected between S_{p_1}/S_{n_1} and S_{p_0}/S_{n_0} and S_{p_2}/S_{n_2} and the



(a) $V_{S_{p_1}}$ and I_{S_1} with $C_{sn} = 0.01\,\mu$F

(b) $V_{S_{p_1}}$ and I_{S_1} with $C_{sn} = 0.1\,\mu$F

(c) $V_{S_{p_1}}$ and I_{S_1} with $C_{sn} = 1\,\mu$F

Figure 11: Voltage across reinjection IGBT S_{p_1} for different C_{sn}.

derivation of the reinjection pulse for S_{p_0}/S_{n_0} is shown in Figure 20.

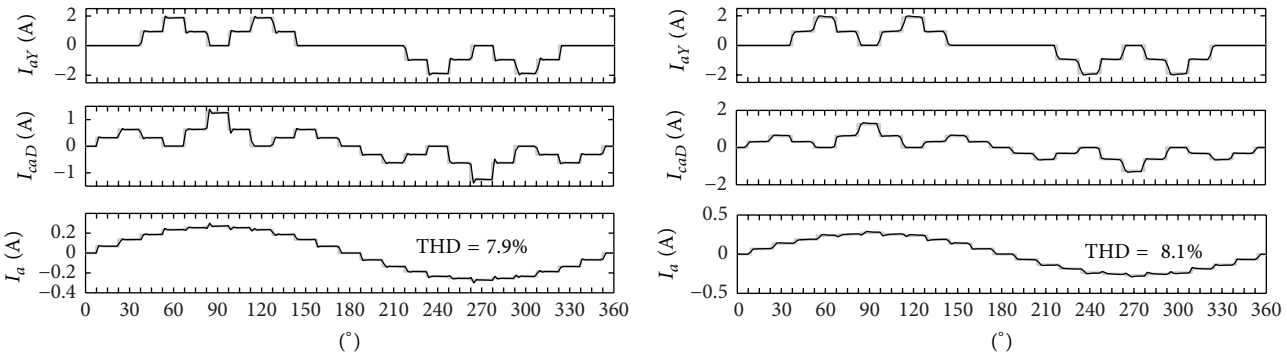
4.4. Optocoupler Based IGBT Driver Circuit. The isolated gate driver ACPL-312T [23] is used for this purpose. The response of optocoupler depends on the value of gate resistance (R_g). R_g is calculated from the peak gate current ($I_{G_{peak}}$) of 2.5 A (from ACPL-312T datasheet). V_{OL} is obtained from Figure 6 in the ACPL-312T datasheet, assuming temperature = 25°. Consider

$$R_g \geq \frac{V_{cc} - V_{OL}}{I_{G_{peak}}} = \frac{15 - 3.5}{2.5} = 4.6\,\Omega. \tag{7}$$

The value of the gate resistance has a significant impact on the dynamic performance of IGBTs. A smaller gate resistor charges and discharges the power transistor input capacitance faster, reducing switching times and switching losses. The trade-off is that this could lead to higher voltage oscillations. At lower R_g values, the voltage supplied by the ACPL-312T is not an ideal voltage step. Since the maximum peak gate current of the driver must be equal to or lower than $I_{G_{peak}}$, choosing $R_g = 10\,\Omega$ is a good trade-off.

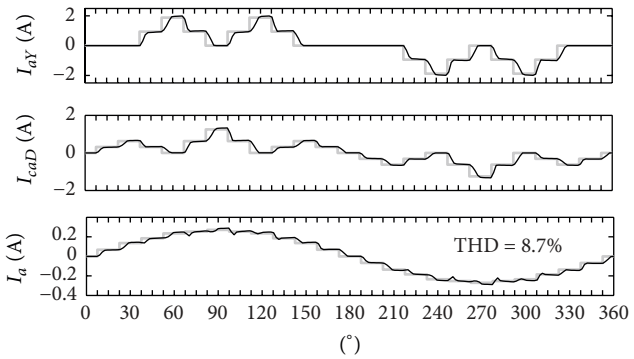
Once the logical signals (reinjection pulses for reinjection switches) are available, these are fed to the IGBT driver circuit. The driver circuit is shown in Figure 21. Since there are six reinjection switches (IXGP20N [24]) for a 3-level MLCR CSC, six isolated DC-DC converters are required for the ACPL-312T. The isolated DC-DC converter 0515S [25] from Tracopower is used here. $V_{cc} = 15\,$V is chosen because the output voltage (V_o) of ACPL-312T goes high when $V_{cc} - V_{ee}$ is between 13.5 V and 30 V. Input resistance for ACPL-312T, R_{in}, is calculated as follows (input current I_{in} of ACPL-312T needs to be limited between 7 mA and 16 mA):

$$R_{in} = \frac{15 - 1.5}{10\,\text{mA}} \approx 1.5\,\text{k}\Omega. \tag{8}$$



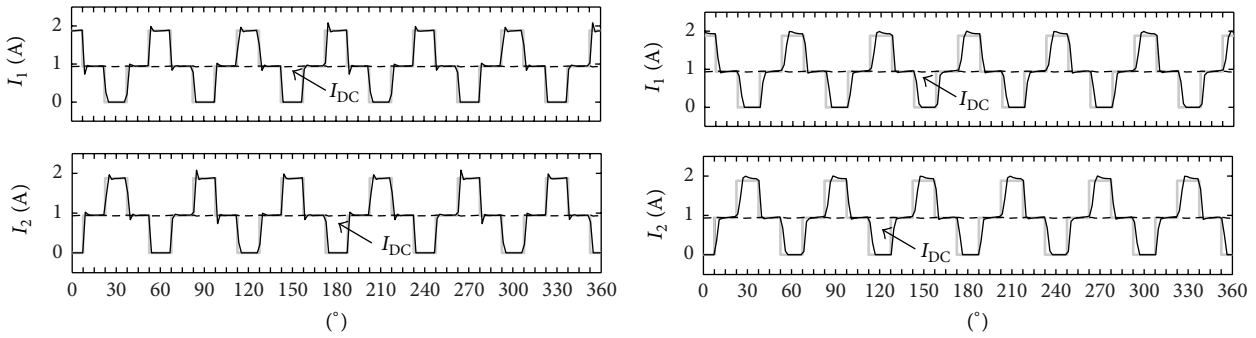
(a) I_{ay}, I_{caD}, and I_a for $C_{sn} = 0.01\,\mu$F

(b) I_{ay}, I_{caD}, and I_a for $C_{sn} = 0.1\,\mu$F



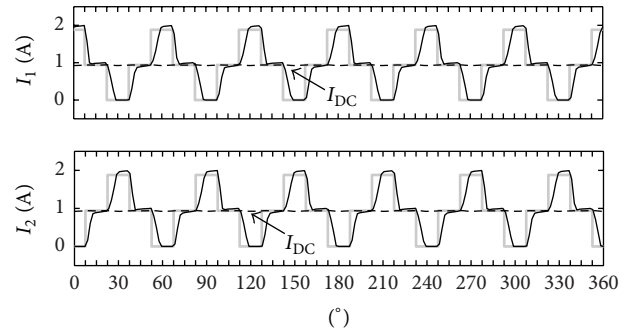
(c) I_{ay}, I_{caD}, and I_a for $C_{sn} = 1\,\mu$F

Figure 12: Simulated AC side current and DC bus waveforms for the 3-level thyristor based MLCR CSC.



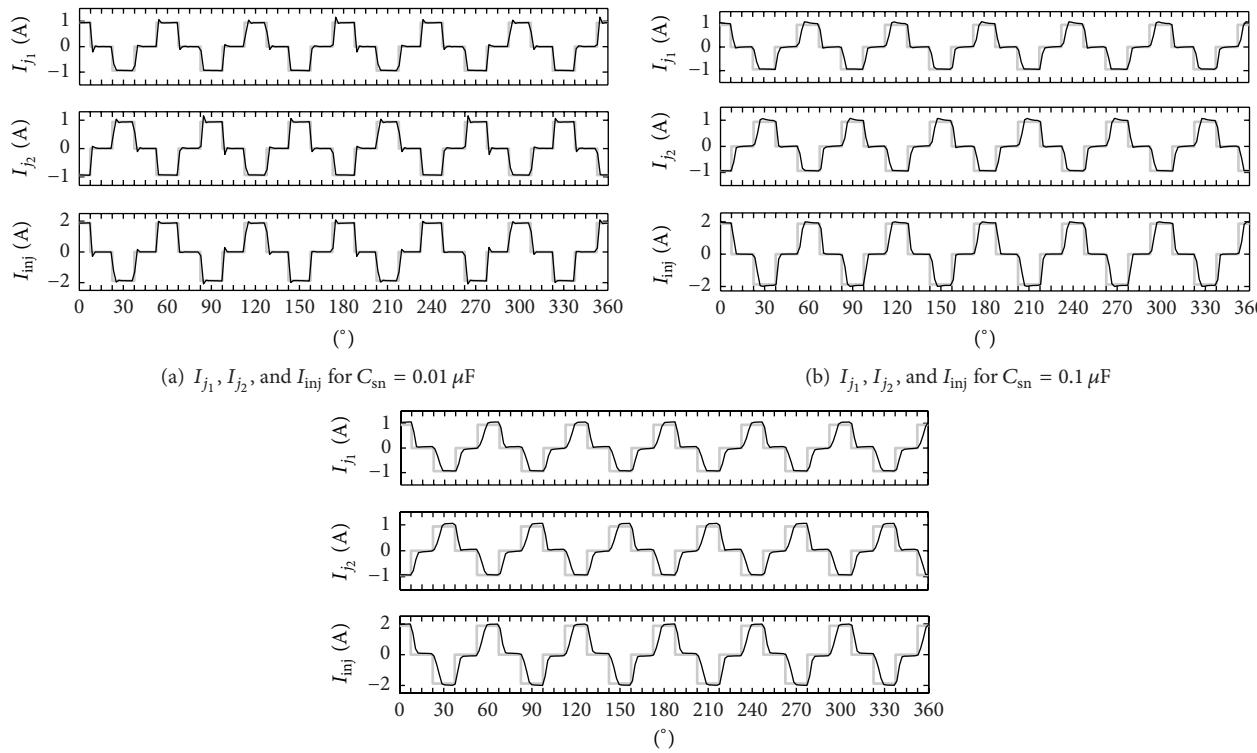
(a) I_1 and I_2 for $C_{sn} = 0.01\,\mu$F

(b) I_1 and I_2 for $C_{sn} = 0.1\,\mu$F



(c) I_1 and I_2 for $C_{sn} = 1\,\mu$F

Figure 13: Simulated AC side current and DC bus waveforms for the 3-level thyristor based MLCR CSC.

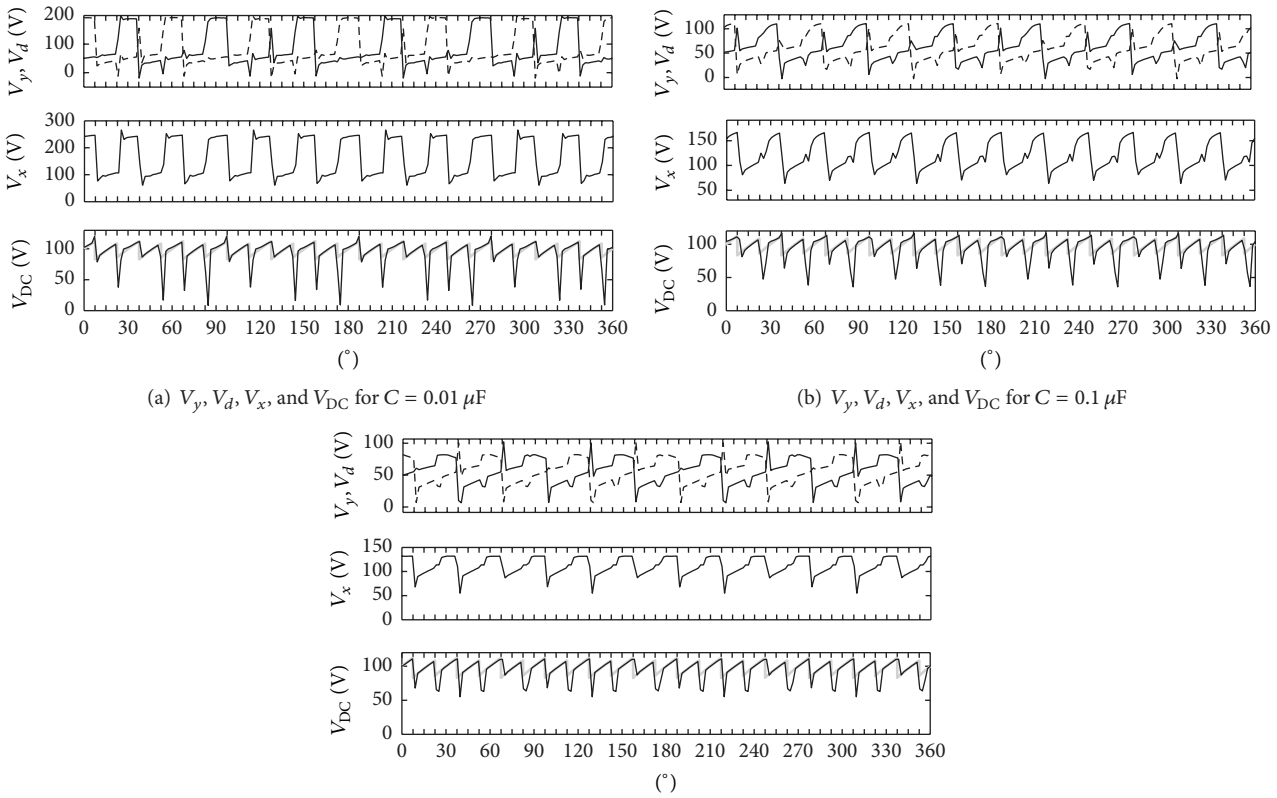


(a) I_{j_1}, I_{j_2}, and I_{inj} for $C_{\text{sn}} = 0.01\,\mu\text{F}$

(b) I_{j_1}, I_{j_2}, and I_{inj} for $C_{\text{sn}} = 0.1\,\mu\text{F}$

(c) I_{j_1}, I_{j_2}, and I_{inj} for $C_{\text{sn}} = 1\,\mu\text{F}$

Figure 14: Simulated Reinjection current and DC side voltage waveforms for the 3-level thyristor based MLCR CSC.

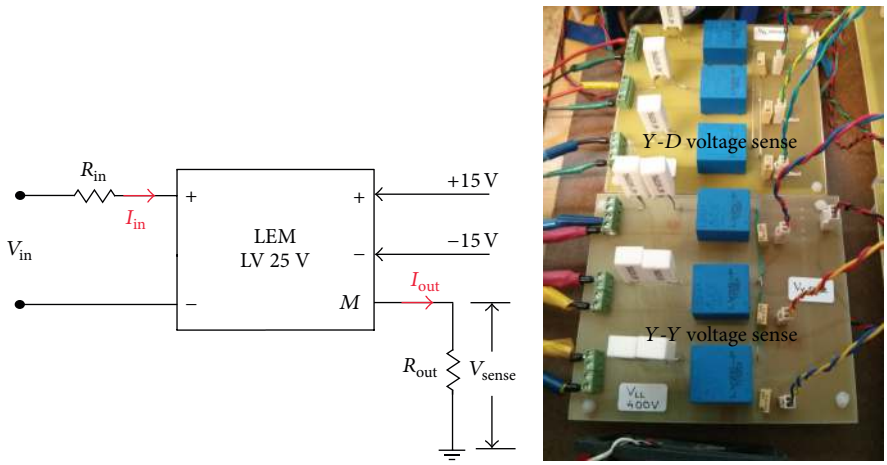


(a) V_y, V_d, V_x, and V_{DC} for $C = 0.01\,\mu\text{F}$

(b) V_y, V_d, V_x, and V_{DC} for $C = 0.1\,\mu\text{F}$

(c) V_y, V_d, V_x, and V_{DC} for $C = 1\,\mu\text{F}$

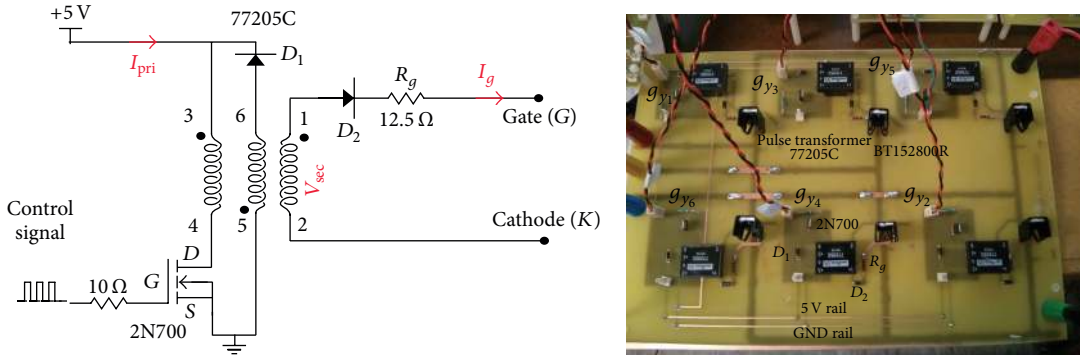
Figure 15: Simulated Reinjection current and DC side voltage waveforms for the 3-level thyristor based MLCR CSC.



(a) Hall effect voltage transducer

(b) Voltage sensor PCBs for Y-Y and Y-D voltage sensing

Figure 16: Voltage transducer circuit and fabricated PCB.



(a) Forward converter based thyristor driver circuit

(b) Six-pulse phase controlled thyristor converter PCB

Figure 17: Forward converter based thyristor driver circuit and PCB detail.

A decoupling capacitor of 0.1 μF is placed across V_{cc} and V_{ee}, very close to the optocoupler itself to filter out any noise coming from the isolated DC-DC converter.

4.5. DC Blocking Capacitor. A 400 V/1 mF (PEH200 Series, ±20%) electrolytic capacitor is used as the DC blocking capacitor. This unit is rated for a total of 5.9 A based on an equivalent series resistance (ESR) of 76 mΩ at a frequency of 100 Hz and equivalent series inductance (ESL) of 16 nH which gives $Z_{100\,\mathrm{Hz}} = 1.59\,\Omega$. The maximum average steady-state DC voltage for this 3-level MLCR CSC prototype is ≈138 V, $I_{DC} = 1.38$ A. The RMS value of reinjection currents I_{j_1} and $I_{j_2} = 0.707 \times 1.38 = 0.975$ A ≈ 1 A which is well under the rating of PEH200 capacitor. Figure 22 shows the set-up for the reinjection transformer along with the DC blocking capacitors.

5. Experimental Results

Real world capacitors often have ±1%–±20% variation in the capacitance values while resistors also have ±1%–±5% variation; thus exact DC bus currents (I_1 and I_2) may not be possible in hardware implementation. However, for comparison with the theoretical waveforms, the experimental and theoretical waveforms are overlapped together. Two different types of PCBs with C_{sn}: 0.01 μF and 1 μF (Figure 23) are fabricated and the results are summarized in this section. The experimental V_{DC} obtained from the prototype is 96.3 V and $I_{DC} = 0.97$ A with $\alpha = -45^{\circ}$.

5.1. Current through Reinjection IGBTs. Figure 24 shows the current flowing through reinjection IGBTs S_{p_1}, S_{p_0}, and S_{p_2}. For $C_{sn} = 0.01\,\mu$F (Figure 24(a)), these waveforms follow the theoretical waveform closely with $I_{S_{p_1}} \approx I_{DC}$ for almost the entire theoretical duration of 15°. As observed from Figure 24(b), with $C_{sn} = 1\,\mu$F, $I_{S_{p_1}} \approx I_{DC}$ for less than half of the theoretical duration. These waveforms constitute the "chopping" of I_{DC} and formation of the reinjection currents.

5.2. Reinjection Currents Waveforms. Figure 25 shows the reinjection currents I_{j_1}, I_{j_2}, and I_{inj} on the primary side of the

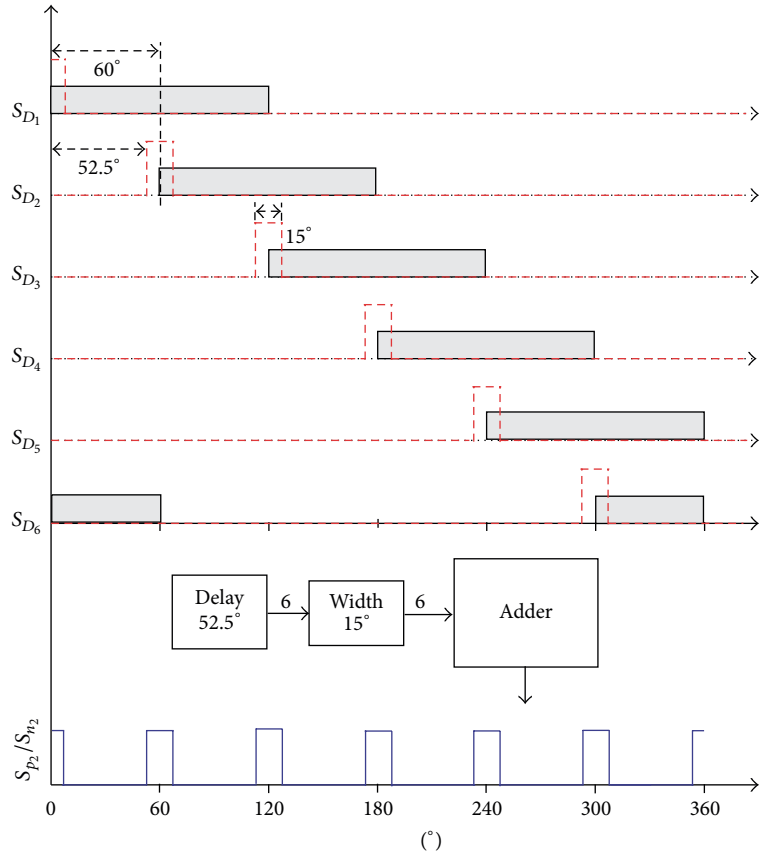


Figure 18: Generation of reinjection pulse for reinjection IGBT S_{p_1}/S_{n_1}.

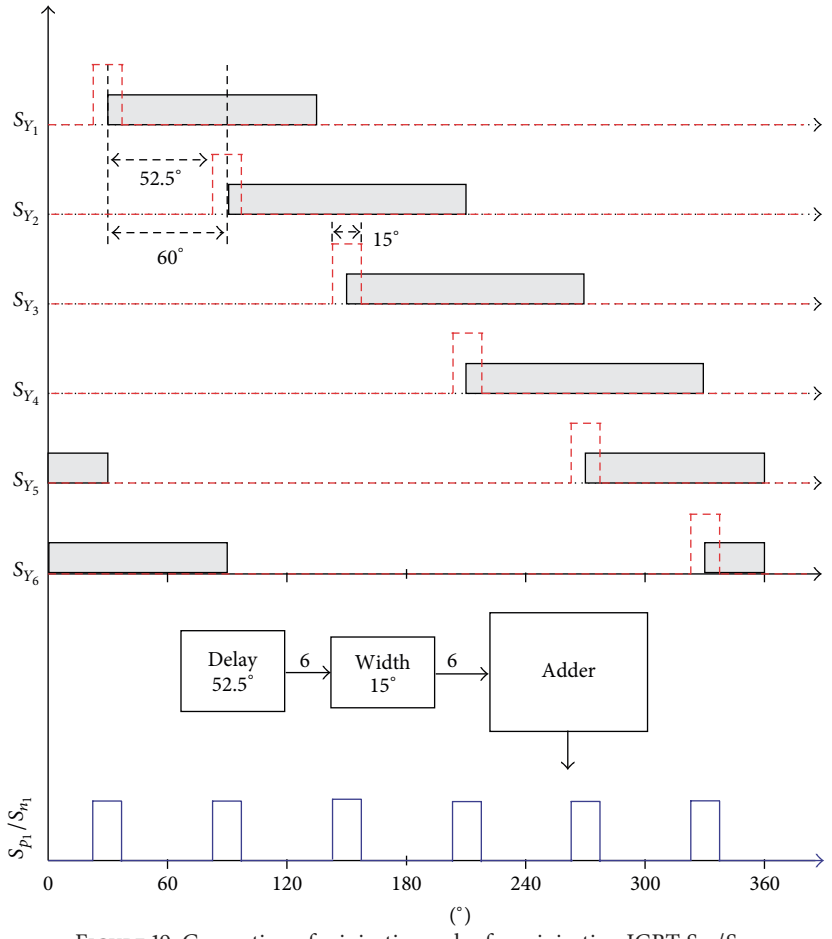


Figure 19: Generation of reinjection pulse for reinjection IGBT S_{p_2}/S_{n_2}.

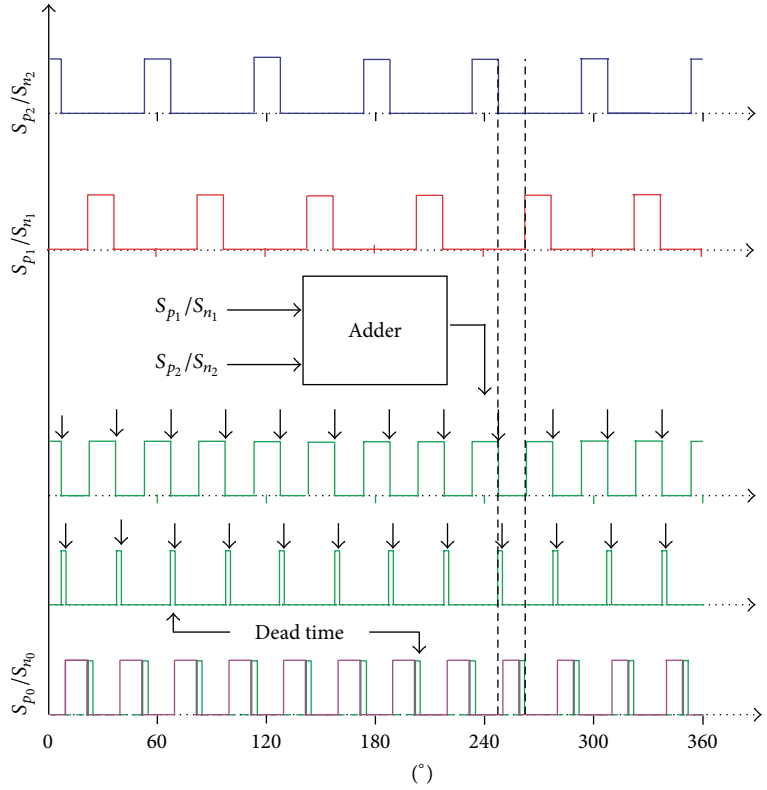


Figure 20: Generation of reinjection pulse for reinjection IGBT S_{p_0}/S_{n_0}.

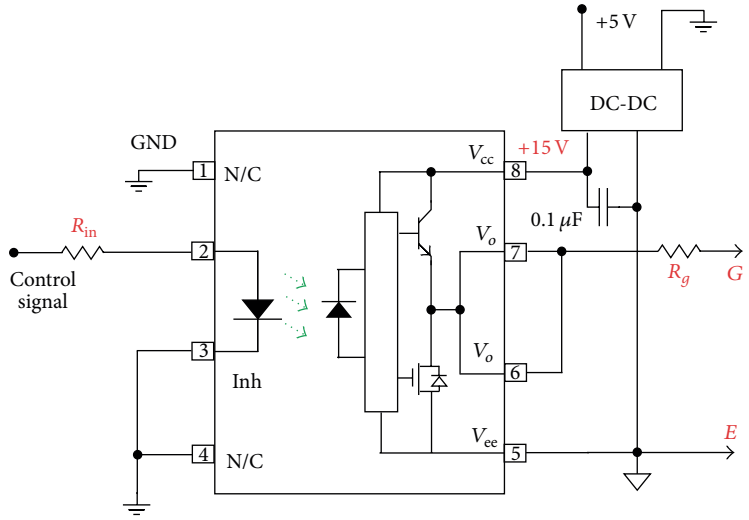


Figure 21: ACPL-312T IGBT driver circuit.

reinjection transformer. I_{inj} is composed of I_{j_1} and I_{j_2}. Again, with $C_{sn} = 1\,\mu$F reinjection current I_{inj} is not following the theoretical I_{inj} "perfectly" whereas, with $C_{sn} = 0.01\,\mu$F, I_{inj} follows the theoretical wave-shape.

5.3. DC Bus Currents Waveforms. The injected current waveform I_{inj} modifies the DC bus currents as shown in Figure 26. This DC bus current is a 3-level waveform with $I_{1,2} = 0$, $I_{1,2} = I_{DC}$, and $I_{1,2} = 2I_{DC}$ as the three different levels of DC bus current waveform.

5.4. AC Side Secondary Line Current Waveforms. The modified AC side secondary line currents I_{aY} and I_{aD} are shown in Figure 27. With $C_{sn} = 0.01\,\mu$F, experimental I_{aY} and I_{aD} follow the theoretical current wave-shape. Current spikes are observed in I_{aY} and I_{aD} with $C_{sn} = 1\,\mu$F. These spikes are

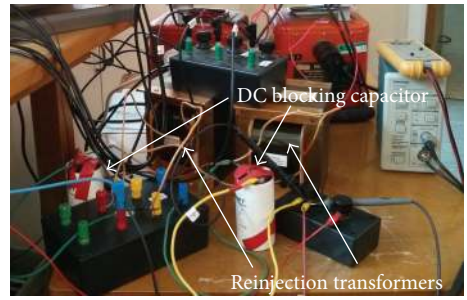
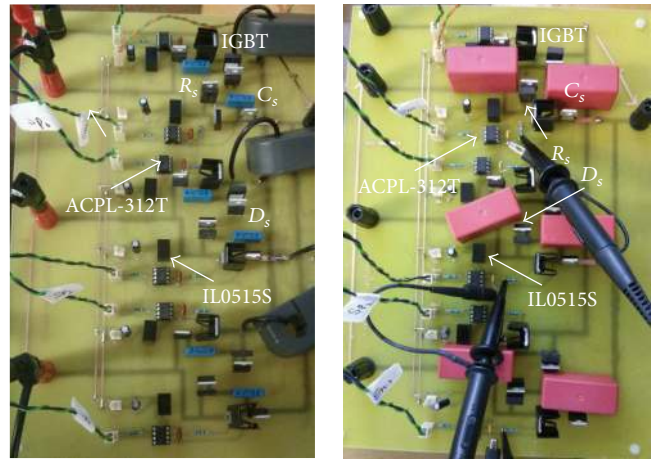


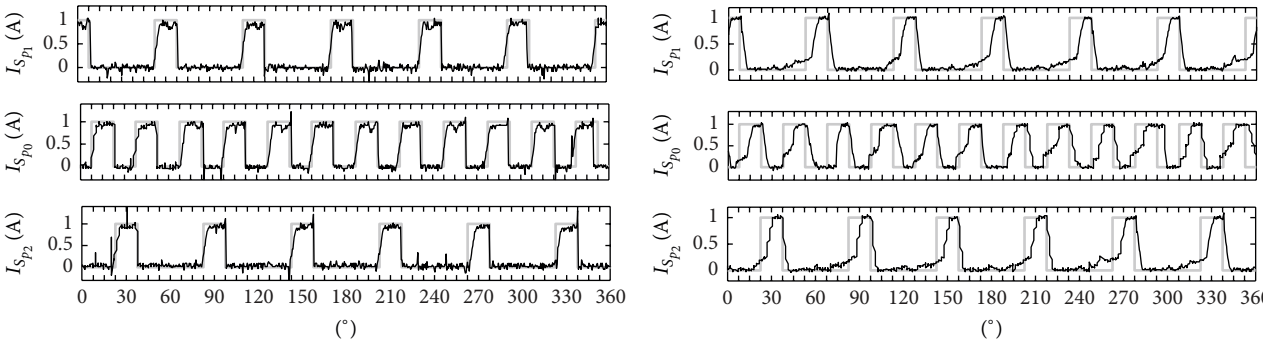
Figure 22: Three-level MLCR CSC prototype and associated auxiliaries: the DC side reinjection transformer.



(a) Three-level reinjection PCB, C_{sn}: 0.01 μF

(b) Three-level reinjection PCB, C_{sn}: 1 μF

Figure 23: Two reinjection PCBs used in the prototype.



(a) $I_{S_{P1}}$, $I_{S_{P0}}$, and $I_{S_{P2}}$, C_{sn} = 0.01 μF

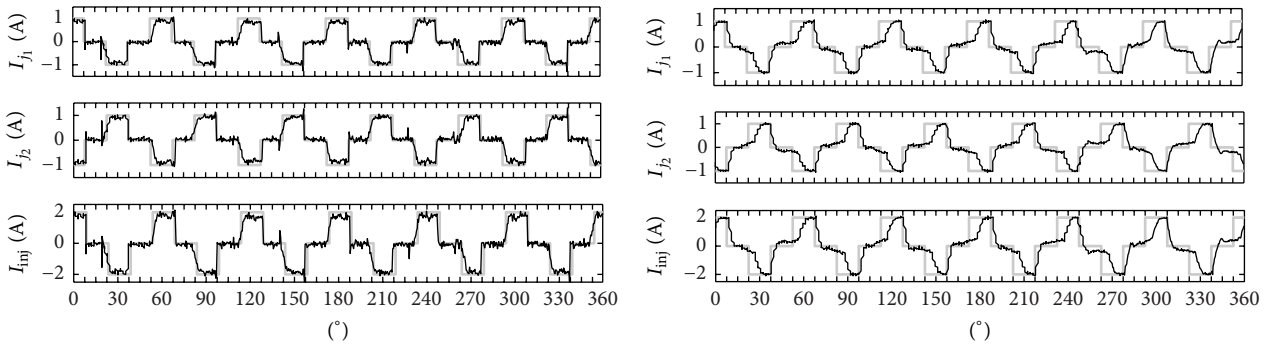
(b) $I_{S_{P1}}$, $I_{S_{P0}}$, and $I_{S_{P2}}$, C_{sn} = 1 μF

Figure 24: Experimental currents $I_{S_{P1}}$, $I_{S_{P0}}$, and $I_{S_{P2}}$ through reinjection IGBTs.

observed at the same instants when the main bridge thyristors are triggered. However, these spikes are not observed with C_{sn} = 0.01 μF.

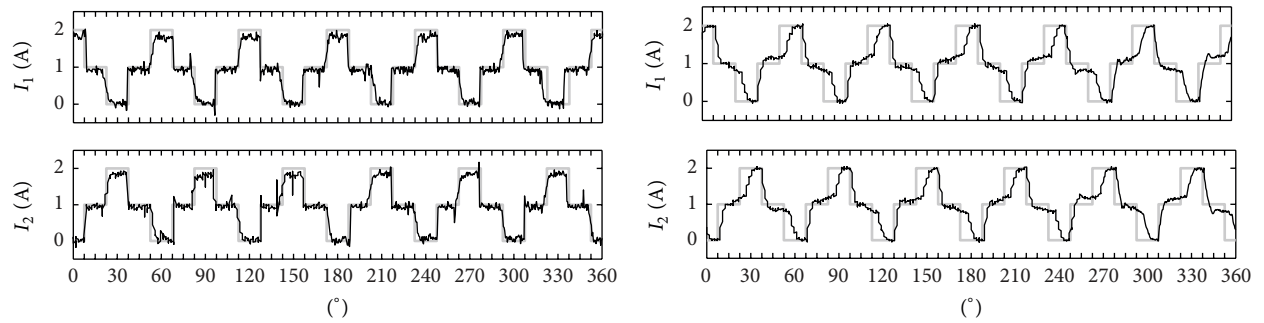
5.5. AC Side Primary Line Current Waveform. The modified primary side line current I_a is shown in Figure 28. The effect of using a "very large" C_{sn} is clearly observed (Figure 28(b)). I_a with C_{sn} = 1 μF is highly distorted although a multistep waveform can be observed. With C_{sn} = 0.01 μF, I_a follows the theoretical waveform closely and a 24-step I_a is obtained.

5.6. Y-Y and Y-D Connected DC Voltage Waveform. The DC voltage waveforms for both *Y-Y* and *Y-D* connected 6-pulse bridges are shown in Figure 29. With C_{sn} = 0.01 μF, the experimental waveform follows the theoretical one while,



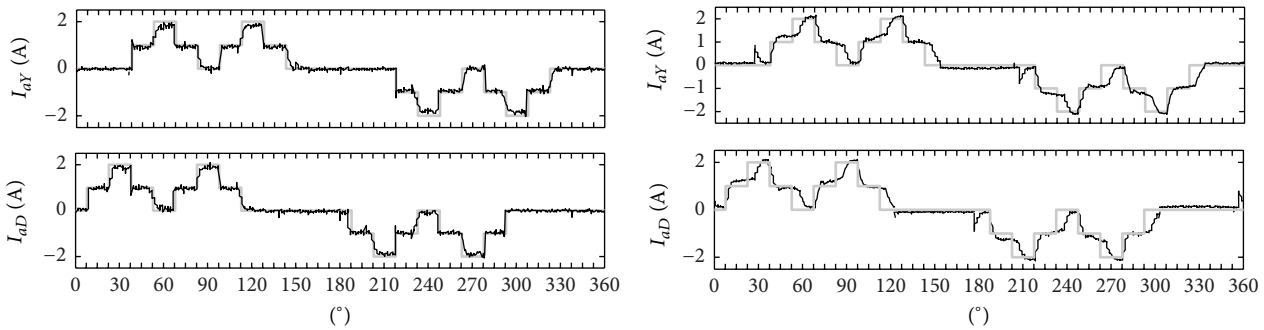
(a) I_{j_1}, I_{j_2}, and I_{inj}, $C_{\text{sn}} = 0.01\,\mu\text{F}$ (b) I_{j_1}, I_{j_2}, and I_{inj}, $C_{\text{sn}} = 1\,\mu\text{F}$

Figure 25: Reinjected current waveforms I_{j_1}, I_{j_2}, and I_{inj}.



(a) I_1, I_2, and I_{DC}, $C_{\text{sn}} = 0.01\,\mu\text{F}$ (b) I_1, I_2, and I_{DC}, $C_{\text{sn}} = 1\,\mu\text{F}$

Figure 26: Experimental DC bus currents I_1, I_2, and I_{DC}.



(a) I_{aY} and I_{aD}, $C_{\text{sn}} = 0.01\,\mu\text{F}$ (b) I_{aY} and I_{aD}, $C_{\text{sn}} = 1\,\mu\text{F}$

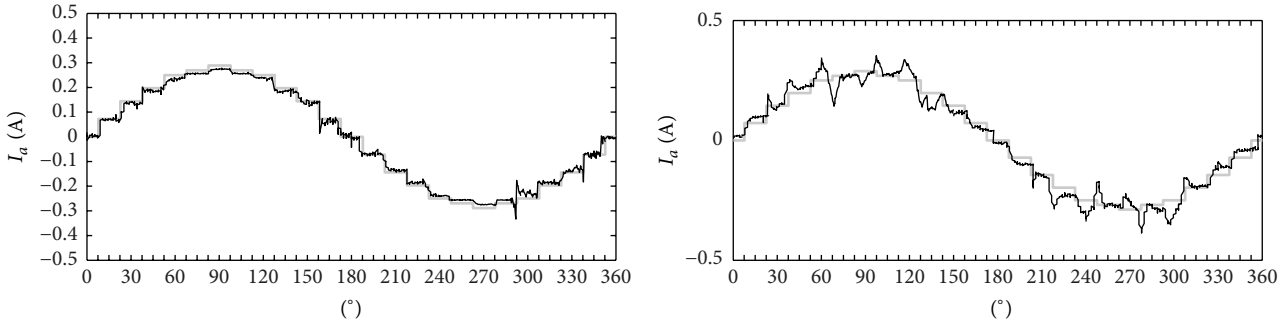
Figure 27: Secondary side line currents I_{aY} and I_{aD}.

with $C_{\text{sn}} = 1\,\mu\text{F}$, the transitions are delayed by about 7.5° which is also observed in PSCAD/EMTDC simulation result. However, very large voltage dv/dt, as predicted by PSCAD/EMTDC, is absent.

5.7. 12-Pulse DC Voltage Waveform. The 12-pulse DC voltage obtained for both the values of C_{sn} is shown in Figure 30.

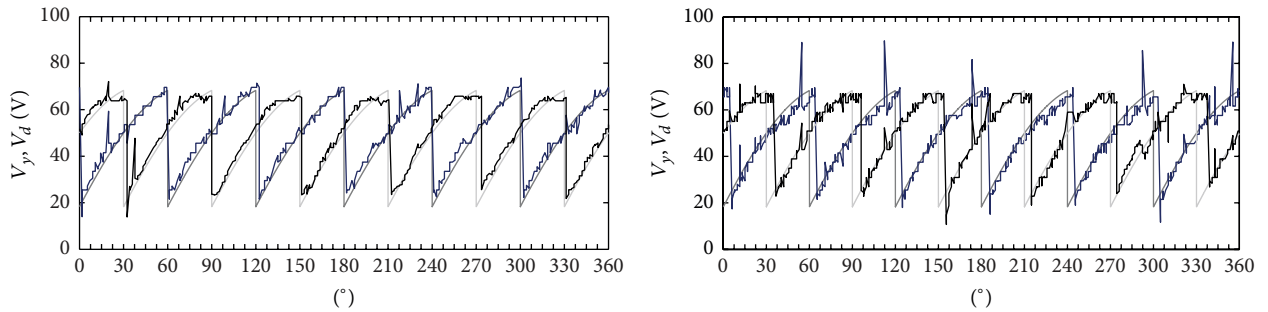
5.8. Reinjection Transformer Secondary Side Voltage Waveform. The reinjection transformer secondary side voltage V_m obtained is shown in Figure 31. V_m with $C_{\text{sn}} = 1\,\mu\text{F}$ follows the theoretical V_m more closely but is delayed by about 7.5°. V_m with $C_{\text{sn}} = 0.01\,\mu\text{F}$ has higher dv/dt during transitions (Figure 31(a)).

5.9. Three-Level MLCR CSC DC Voltage Waveform. The DC voltage waveform V_{DC} is shown in Figure 32. Voltage dv/dt observed in V_m with $C_{\text{sn}} = 0.01\,\mu\text{F}$ is clearly reflected across V_{DC} whereas the voltage dv/dt transitions are not observed in V_{DC} with $C_{\text{sn}} = 1\,\mu\text{F}$. Nevertheless, V_{DC} has 24 pulses in both the cases which implies that ripple voltage is getting added to V_x giving it 24-pulse characteristics.



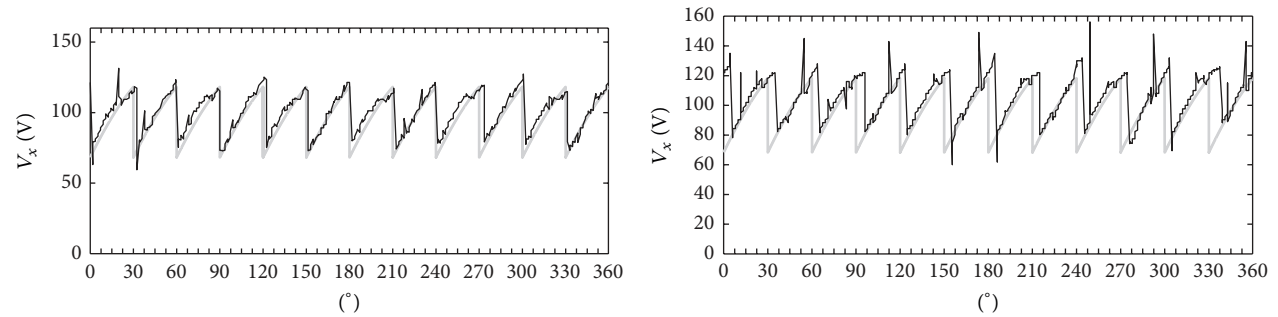
(a) I_a, C_{sn} = 0.01 μF (b) I_a, C_{sn} = 1 μF

Figure 28: Primary side line current I_a.



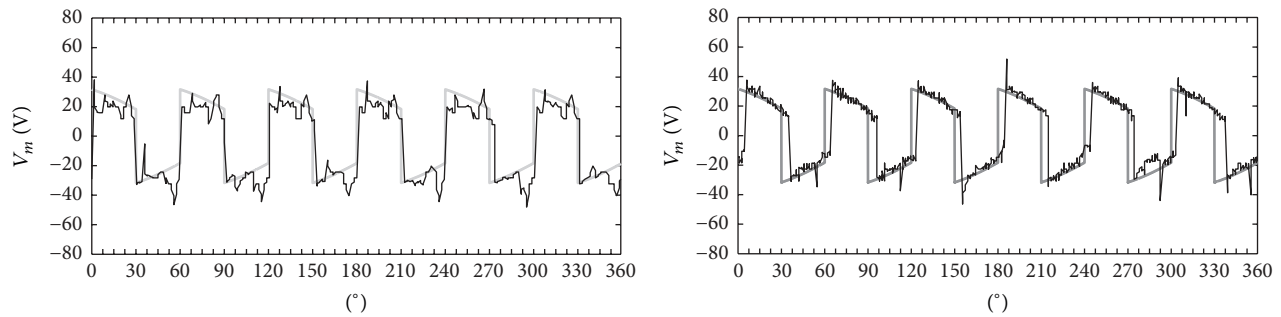
(a) V_y and V_d, C_{sn} = 0.01 μF (b) V_y and V_d, C_{sn} = 1 μF

Figure 29: DC voltage waveforms V_y and V_d.



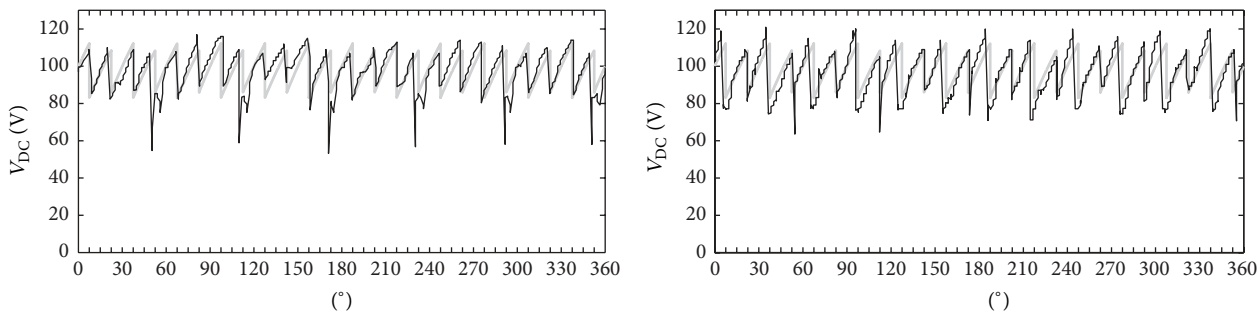
(a) V_x, C_{sn} = 0.01 μF (b) V_x, C_{sn} = 1 μF

Figure 30: 12-pulse DC voltage waveform V_x.



(a) V_m, C_{sn} = 0.01 μF (b) V_m, C_{sn} = 1 μF

Figure 31: Reinjection transformer secondary side voltage V_m.



(a) V_{DC}, C_{sn} = 0.01 μF (b) V_{DC}, C_{sn} = 1 μF

Figure 32: Three-level MLCR CSC DC voltage waveform V_{DC}.

6. Conclusion

The theory, PSCAD/EMTDC simulation results, hardware prototype, and experimental results of a 3-level thyristor based MLCR CSC have been presented in detail in this paper. The reinjection current forces the main bridge thyristor to commutate under zero current thereby allowing it to be switched at negative firing angles. It is possible to achieve self-commutation for thyristors using an auxiliary reinjection bridge.

From experimental investigation, it is observed that the deviation of the actual waveforms from the theoretical waveforms is mainly due to the use of a "very large" snubber capacitor. With a "very large" snubber capacitor value, interface transformer secondary side current showed current di/dt which happened exactly 7.5° before the current passed through that particular thyristor. This is when the thyristor is switched on. The voltage transitions were also delayed by 7.5° with a "very large" snubber capacitor. With a "small" snubber capacitor value, current waveform follows the theoretical waveforms very closely; however voltage dv/dt can be observed in the output DC voltage waveform.

The use of "small" snubber capacitor value is recommended to reduce line current distortion, as the modification of DC bus current is the key to achieve both self-commutation for thyristors and lower harmonic distortion.

Appendix

Experimental/Simulation Parameters

Source specification is as follows:

(i) Voltage rating: 415 V @ 50 Hz.
(ii) Source impedance: 0.1 Ω + 5 mH.

Interface transformer is as follows:

(i) Type: 3-phase, 3-winding @ 50 Hz.
(ii) Power rating: 2 kVA.
(iii) Voltage rating: 415 V : 50 V (1 : 1 for Y-Y and 1 : $\sqrt{3}$ for Y-D).

Reinjection transformer is as follows:

(i) Type: 1 phase and 2 windings @ 300 Hz.
(ii) Nominal impedance: 5%.
(iii) Power rating: 1 kVA.
(iv) Voltage rating: 400 V : 400 V.

Load specification is as follows:

(i) Load resistance: 100 Ω.
(ii) Load inductance: 400 mH.

Firing angle (α) = −45°.

Competing Interests

The authors declare that they have no competing interests.

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