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Experimental evidence of ferroelectric negative capacitance in nanoscale heterostructures

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We report a proof-of-concept demonstration of negative capacitance effect in a nanoscale ferroelectric-dielectric heterostructure. In a bilayer of ferroelectric $Pb(Zr_{0.2}Ti_{0.8})O_3$ and dielectric $SrTiO_3$, the composite capacitance was observed to be larger than the constituent $SrTiO_3$ capacitance, indicating an effective negative capacitance of the constituent $Pb(Zr_{0.2}Ti_{0.8})O_3$ layer. Temperature is shown to be an effective tuning parameter for the ferroelectric negative capacitance and the degree of capacitance enhancement in the heterostructure. Landau's mean field theory based calculations show qualitative agreement with observed effects. This work underpins the possibility that by replacing gate oxides by ferroelectrics in nanoscale transistors, the sub threshold slope can be lowered below the classical limit (60 mV/decade). © *2011 American Institute of Physics*. [doi:10.1063/1.3634072]

Complementary metal-oxide-semiconductor (CMOS) scaling is facing a fundamental barrier stemming from the Boltzmann statistics which dictate that a minimum voltage must be applied to effect an-order-of-magnitude increase in the current.[1] This means that CMOS voltage and transistor power dissipation cannot be downscaled arbitrarily. Therefore, it has been suggested that without introducing fundamentally new physics in transistor operation, an end to scaling is inevitable.[2] In that pursuit, it was proposed[3] that the minimum voltage requirement could be overcome if the ordinary gate oxide could be replaced by another stack that provides an effective negative capacitance (NC). The key to overcoming the Boltzmann limit by negative capacitance lies in the fact that, in a series combination of a negative and a positive capacitor, the total capacitance becomes larger than its constituent positive capacitor. Notably, this is just the opposite of what happens in a classical series combination of two positive capacitors, where the total capacitance is always reduced. For a MOSFET, a negative gate capacitance can make the total capacitance, looking into the gate, larger than the semiconductor capacitance. To induce the same amount of charge in the channel, one would require a smaller voltage than what would be required classically. This, in turn, means that the gate voltage could be reduced below the classical limit.

Capacitance (C) can be defined as the inverse of the radius of curvature of energy (U) vs. charge (P) profile of the capacitor (in other words, $C = [d^2U/dP^2]^{-1}$). For a nonlinear capacitor, the energy can be expanded as $U = \alpha P^2 + \beta P^4 + \gamma P^6$, where α, β, and γ are material dependent constants. The coefficient α is negative for a ferroelectric (FE) capacitor.[4] Leveraging on this fact, it can be shown that ferroelectric capacitance is indeed negative in a certain range of P, around $P = 0$. By putting a dielectric (DE) capacitor of proper capacitance in series with the FE capacitor, the FE can be biased in the negative capacitance state[3] and in that case, the FE-DE capacitance will be larger than that of the constituent DE capacitor. Properties of a ferroelectric material can be strongly modulated by the temperature. Within the phenomenological Landau model, this dependence is captured by the fact that $\alpha = \alpha_0(T - T_c)$ is strongly temperature dependent and α is negative only up to the Curie temperature, T_c. Based on this physics, the negative capacitance and degree of capacitance enhancement in FE-DE heterostructure can be tuned by changing the temperature. Figure 1(b) shows the simulated capacitance of a FE-DE heterostructure as a function of temperature and compares it to that of the constituent DE. Also shown in Fig. 1(b) is the FE capacitance in the heterostructure as well as the voltage amplification factor[5] at the FE-DE interface, $(1 + C_{DE}/C_{FE})^{-1}$. Capacitance of the heterostructures is numerically simulated using Landau Devonshire formalism[4] self-consistently with Poisson's equation in a 1D FE-DE structure. $Pb(Zr_{0.2}Ti_{0.8})O_3$ (PZT) and $SrTiO_3$ (STO) are considered as the FE and the DE, respectively, and the anisotropy constants of the materials are taken from Ref. 4. To be noted in Fig. 1(b) is that only at a certain temperature range, the FE capacitance is stabilized in the NC region and capacitance enhancement occurs in that temperature range. The details of the models, simulations, and the physics of this temperature dependence are further elaborated in supplementary material.[19] Figure 1(c) compares the simulated C-V characteristics of a PZT-STO heterostructure with that of the constituent STO at different temperatures.

FE-DE bilayer capacitors with PZT as the ferroelectric and STO as the dielectric were fabricated to test this hypothesis. Details of the synthetic approaches, device fabrication, and measurements are described in the supplementary materials.[19]

We first focus on the capacitance of a 28 nm PZT-48 nm STO bi-layer capacitor. Fig. 2(a) shows the C-V characteristics at 100 kHz of a PZT (28 nm)-STO (48 nm) bilayer capacitor at different temperatures and compares it to the

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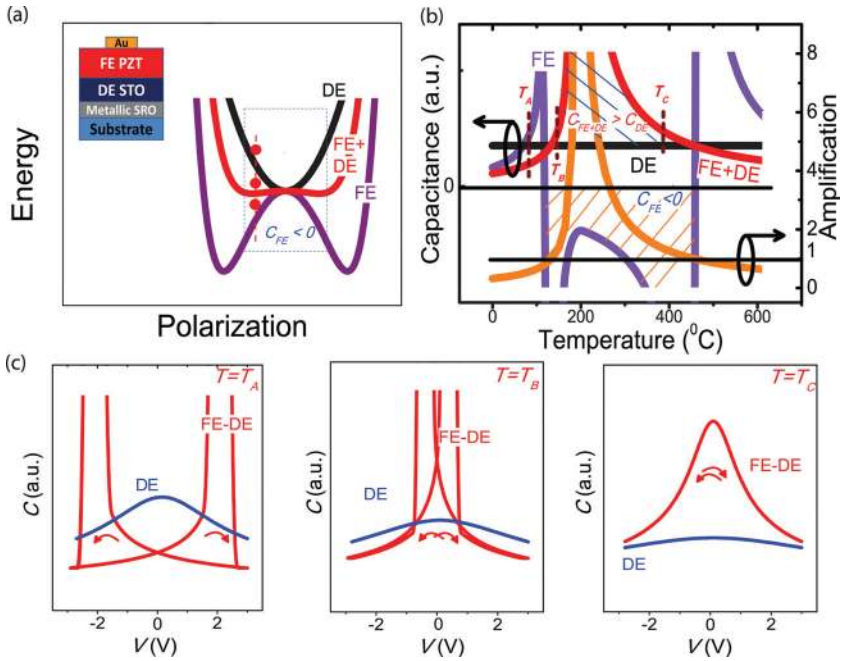

FIG. 1. (Color) (a) Energy landscapes of a DE, a FE and their series combination. The negative capacitance region of the FE energy landscape (curve 1) is shown inside the dotted rectangular box. The FE negative capacitance state is an unstable one, which is stabilized by putting a DE capacitor in series with it. The negative curvature of the FE makes the curvature of the FE-DE bilayer smaller than that of the dielectric material, which makes the bilayer capacitance larger than the constituent DE capacitance. Inset shows schematic of the experimental bilayer stack. (b) Capacitance of a FE (PZT)-DE ($\varepsilon_r = 200$) bi-layer capacitor (thickness ratio 4:1) as a function of temperature. Also shown in this figure is the capacitance of the constituent DE and FE in the heterostructure as well as the voltage amplification factor at the FE-DE interface. (c) Calculated *C-V* characteristics of a STO capacitor and a PZT-STO bi-layer capacitor (thickness ratio 4:1) at $T = T_A$, T_B, and T_C.

capacitance of a 48 nm STO. As predicted from the simulation, the capacitance of PZT-STO sample is larger than that of the STO capacitor at elevated temperatures. The evolution of *C-V* curves of the PZT-STO and the STO capacitors with temperature has similar trends when compared to those obtained by simulation (Fig. 1(c)). Fig. 2(b) shows the capacitance of the PZT-STO bi-layer and the isolated dielectric STO as a function of temperature. Shown in Fig. 2(c) are the extracted capacitance of the PZT in the bilayer and the calculated voltage amplification factor at the PZT-STO interface. At around 225 °C, the bi-layer capacitance exceeds the STO capacitance. This means that beyond this temperature, the capacitance of the 76 nm thick bi-layer (STO: 48 nm + PZT: 28 nm) becomes larger than that of 48 nm STO itself. Fig. 2(d) shows the enhancement in capacitance is retained even at 1 MHz, thereby indicating that defect mediated processes are minimal, if any and, therefore, the enhanced capacitance cannot be attributed to such effects.

A comparison of the dielectric constant of the bi-layer and the isolated STO is shown in Fig. S4(b) in supplementary section.[19] Also shown in Fig. S4(b) is the calculated dielectric constant of STO in that temperature range using Landau model. It is important to note that although the measured ε_r for the STO layer is smaller than the highest reported ε_r in unstrained thin film STO (Ref. 6) as well as the simulated STO ε_r at room temperature, at high temperatures, our measured STO ε_r is as high as the theoretical limit. Hence, the fact that the bilayer capacitance enhancement is observed at elevated temperatures precludes the possibility that the capacitance of the bilayer structure is unduly compared to that of a STO thin film that has lower ε_r due to undesired "dead layer" at the Au-STO interface that is otherwise absent in the bilayer structures. Calibration of STO dielectric constant and issue of a possible dead layer at the interface are further elaborated in the supplementary materials.[19]

Figs. 3(a) and 3(b) show the permittivity and capacitance, respectively, of three different samples (sample nos

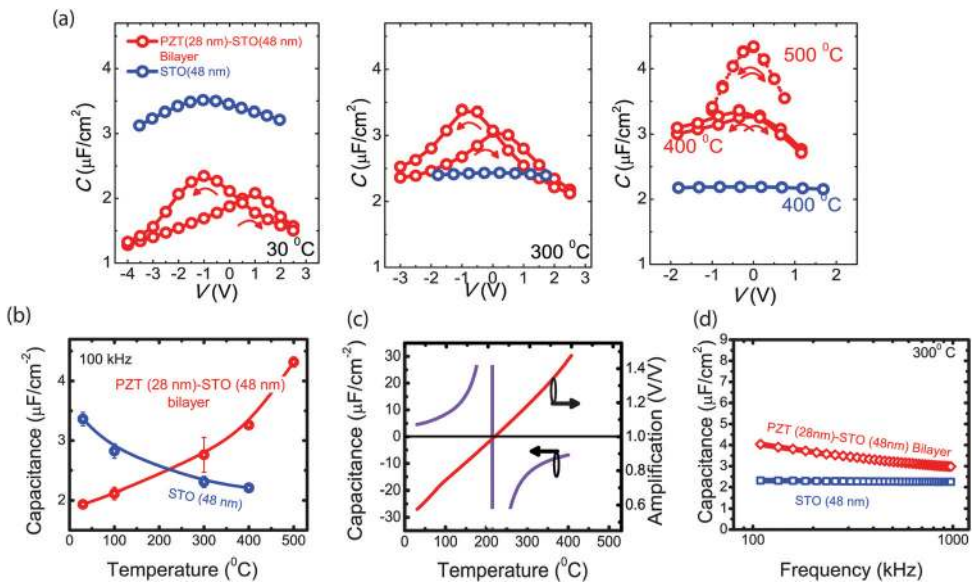

FIG. 2. (Color) (a) Comparison of *C-V* characteristics of a PZT (28 nm)-STO (48 nm) and an STO (48 nm) sample at different temperatures. (b) Capacitances of the samples at the symmetry point as functions of temperature measured at 100 kHz. Symmetry point refers to the cross point of the *C-V* curves obtained during upward and downward voltage sweeps. (c) Extracted PZT capacitance in the bilayer and the calculated amplification factor at the FE-DE interface. (d) Capacitances of the samples as functions of frequency at 300 °C.

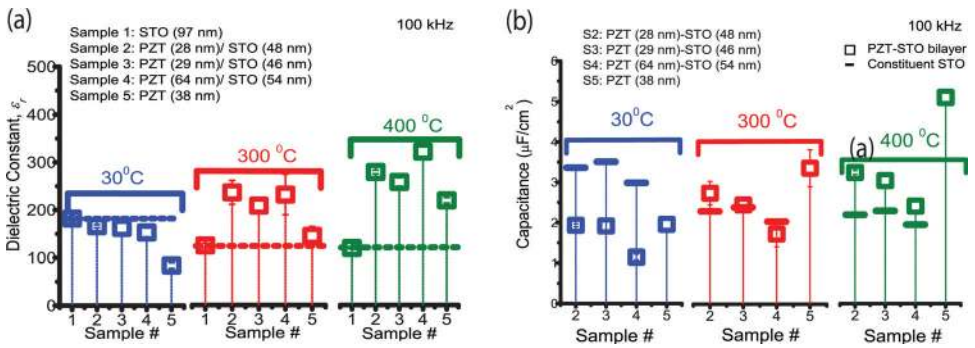

FIG. 3. (Color) Comparison of dielectric constant (a) and capacitance (b), of several PZT-STO samples with those of STO and PZT at 100 kHz at different temperatures. In (b), the capacitance of the constituent STO in each of the bilayers is shown by small horizontal line.

2-4) of PZT-STO bi-layers of different thicknesses, an isolated STO (sample 1) and an isolated PZT sample (sample 5). All the bi-layer samples show an enhancement in overall permittivity and capacitance as the temperature is increased. Fig. S5 shows the admittance angle θ of the same samples.[19] The dissipation factor D ($=\cot\theta$) in all the devices remains reasonably low confirming that capacitance measurements are not compromised by leakage.

As far as electrostatic boundary conditions are concerned, FE-DE bi-layers studied here are analogous to FE-DE superlattices, where similar enhancement in dielectric constant has been observed in $BaTiO_3/SrTiO_3$ (Ref. 7) and $PbTiO_3/SrTiO_3$ heterostructures.[8] Maxwell-Wagner (MW) effect was suggested as a possible origin of the enhanced dielectric constant in the super lattices.[9] This dielectric enhancement was shown to depend on the number of interfaces in the superlattice and to die out at reasonably low frequencies.[9,10] In view of the fact that our heterostructures have just one FE-DE interface, it is unlikely that MW effects can cause dielectric enhancement at frequencies as high as 1 MHz in our heterostructures. Analyzing our sample properties using established M-W models,[11] we conclude that the enhancement in permittivity in our samples is unlikely to have come from leakage mediated effects (see supplementary section for further discussions[19]). The contribution of domain dynamics to the overall enhancement of capacitance[9] needs to be studied carefully.

A number of other physical systems can be imagined that have negative terms in their energy profile and can behave as negative capacitance. One example is the exchange correlation between two closely spaced 2D electron gases (2DEGs). Experimentally, a negative compressibility was measured between two closely spaced 2DEGs in a modulation doped GaAs/AlGaAs heterostructure at cryogenic temperature.[12] Enhanced capacitance has recently been measured in epitaxial $LaAlO_3$/STO heterostructure also at cryogenic temperature[13] and was explained in terms of a negative capacitance that could arise due to similar exchange correlation.[13,14] The advantage of ferroelectric material based systems comes from the fact that the negative energy terms are reasonably large at room temperature, thereby removing the need for cryogenic operation.

Recently, a demonstration of <60 mV/decade has been achieved in a FET by putting a polymer ferroelectric on the gate.[15] In addition, multiple theoretical analysis[16,17] have investigated the design space of a negative capacitance FET. Our demonstration in a simple capacitor structure and in a different material system (crystalline perovskite oxide) underpins the concept of negative capacitance and also provides new insights into the effect.

To summarize, we have experimentally demonstrated the effect of ferroelectric negative capacitance. While integration of ferroelectrics into the silicon processes is a major technology challenge, crystalline $SrTiO_3$ can be used as a perovskite template for growing crystalline FE on silicon.[18] Going beyond overcoming the "Boltzmann limit" of transistor power dissipation, the enhancement in capacitance can be useful for ultra-dense dynamic random access memory (DRAM) applications. Increased capacitance beyond the classical limit can also lead to novel super capacitor structures. Finally, low Curie temperature ferroelectric materials can make it possible to obtain a robust enhancement at room temperature.

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[1]Y. Taur and T. K. Ning, *Fundamentals of Modern VLSI Devices* (Cambridge University Press, Cambridge, England, 2005).
[2]T. N. Theis and P. M. Solomon, Science **327**, 1600 (2010).
[3]S. Salahuddin and S. Datta, Nano Lett. **8**, 405 (2008).
[4]*Physics of Ferroelectrics: A Modern Perspective, Topics in Applied Physics*, edited by K. Rabe, C. H. Ahn, and J.-M. Triscone (Springer, Berlin, 2007), Vol. 105.
[5]Voltage amplification ratio at the FE-DE interface is the ratio of the voltage across the DE to the total voltage applied across the FE-DE.
[6]H. W. Jang, A. Kumar, S. Denev, M. D. Biegalski, P. Maksymovych, C. W. Bark, C. T. Nelson, C. M. Folkman, S. H. Baek, N. Balke, C. M. Brooks, D. A. Tenne, D. G. Schlom, L. Q. Chen, X. Q. Pan, S. V. Kalinin, V. Gopalan, and C. B. Eom, Phys. Rev. Lett. **104**, 197601 (2010).
[7]H. Tabata, H. Tanaka, and T. Kawai, Appl. Phys. Lett. **65**, 1970 (1994).
[8]P. Zubko, N. Stucki, N. Lichtensteiger, and J.-M. Triscone, Phys. Rev. Lett. **104**, 187601 (2010).
[9]G. Catalan, D. O'Neill, R. M. Bowman, and J. M. Gregga, Appl. Phys. Lett. **77**, 3078 (2000).
[10]B. D. Qu, M. Evstigneev, D. Johnson, and R. H. Prince, Appl. Phys. Lett. **72**, 1394 (1998).
[11]A. von Hippel, *Dielectrics and Waves* (Wiley, New York, NY, 1960), pp. 228–230.
[12]J. P. Eisenstein, L. N. Pfeiffer, and K. W. West, Phys. Rev. Lett. **68**, 674 (1992).
[13]L. Li, C. Richter, S. Paetel, T. Kopp, J. Mannhart, and R. C. Ashoori, Science **332**, 825 (2011).
[14]M. S. Loth, B. Skinner, and B. I. Shklovskii, Phys. Rev. E **82**, 056102 (2010).
[15]A. Rusu, G. A. Salvatore, D. Jiménez, and A. M. Ionescu, in IEDM 2010, San Francisco, USA, 06-08 December 2010.
[16]D. Jiménez, E. Miranda, and A. Godoy, IEEE Trans. Electron Devices **57**, 2405 (2010).
[17]A. Cano and D. Jiménez, Appl. Phys. Lett. **97**, 133509 (2010).
[18]R. A. McKee, F. J. Walker, and M. F. Chisholm, Phys. Rev. Lett. **81**, 3014 (1998).
[19]See supplementary material at http://dx.doi.org/10.1063/1.3634072 for further discussion.