

# Experimental Implementation of Delta Sigma AD Modulator Using Dynamic Analog Components With Simplified Operation Phase

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**Abstract** A proof-of-concept delta sigma AD modulator using dynamic analog components with simplified operation mode is designed and fabricated in 90nm CMOS technology. The measurement results of the experimental prototype demonstrate the feasibility of the proposed modulator architecture which can guarantee the reset time for ring-amplifier and relax the speed requirement on the asynchronous SAR quantizer. The peak SNDR of 77.93 dB and SNR of 84.16 dB are achieved while a sinusoid -4 dBFS input is sampled at 14 MS/s with signal bandwidth of 109 kHz. The total analog power consumption of the prototype modulator is 720  $\mu$ W under the supply voltage of 1.2 V.

**key words:** delta-sigma modulator, ring-amplifier, switched-capacitor circuit, successive-approximation-register ADC (SAR ADC)

**Classification:** Integrated circuits

## 1. Introduction

High SNDR ADCs are widely used in mixed-signal system-on-chip (SoC) in the fields of both the industrial and the consumer applications. The SAR ADC is well known as a high energy efficiency ADC architecture for medium resolution, low or medium speed applications [1, 2, 3, 4, 5, 6, 7]. However, because the resolution of SAR ADC depends on the offset of comparator and the accuracy of capacitor array matching, it is difficult to realize the high resolution ADC in nanoscale CMOS technology. On the other hand, the  $\Delta\Sigma$ AD modulator can reduce the quantization noise in the desired signal band by using the oversampling and noise-shaping technique, without the high resolution analog components. Thus, it is suitable to realize the high resolution ADC in nanometer CMOS technology [8, 9]. Normally, it is necessary that the high-order noise-shaping and the higher oversampling ratio (OSR) for the high performance  $\Delta\Sigma$ AD modulator. However, the implementation of high-order noise shaping need to use the multiple integrators with power hungry amplifier. In order to maximize the power-efficiency of the amplifier in the ADC, the use of the dynamic amplifier (eg. ring-amplifier or logic-inverter) instead of operational-transconductance-amplifier (OTA) has been proposed [10, 11, 12, 13, 14, 15, 16]. Nonetheless,

the dynamic amplifier has the drawback which the conversion speed of ADC is limited by the additional reset operation[17, 18, 19].

In our previous work, we have proposed a  $\Delta\Sigma$ AD modulator using ring-amplifier and passive adder embedded SAR quantizer. SPICE simulation results show that the proposed modulator can be realized with simplified operation phase[20, 21]. In this work, we report the detail of the circuit implementation and the experimental results of the proposed modulator. Measurement results show that the proposed prototype  $\Delta\Sigma$ AD modulator can relax the speed requirement on the asynchronous SAR quantizer and guarantee the reset time of ring-amplifier.

## 2. Proposed $\Delta\Sigma$ AD Modulator Architecture

Figure 1(a) shows the block diagram of conventional 2nd-order feed-forward  $\Delta\Sigma$ AD modulator using SAR quantizer and ring-amplifier [17]. The ring-amplifier is used for realizing the switched capacitor integrator in the  $\Delta\Sigma$ AD modulator. The behaviour of ring-amplifier is different from that of the traditional OTA. The ring-amplifier requires to generate the operating point by performing the reset operation before the amplification. Since the output of ring-amplifier is disabled in the process of the reset, the load capacitance must be unconnected to the output of the ring-amplifier in the reset operation. Furthermore, since SAR ADC is used as an internal quantizer in the proposed  $\Delta\Sigma$ AD modulator, unlike flash ADC, SAR ADC requires an extra phase for the signal sampling. Because of the above two factors, the clock timing design of  $\Delta\Sigma$ AD modulator using SAR ADC and ring-amplifier is more difficult than that of the  $\Delta\Sigma$ AD modulator using traditional amplifier and flash ADC. Considering the above factors, in order to correctly implement the transfer function of conventional 2nd-order feed-forward  $\Delta\Sigma$ AD modulator, the  $\Delta\Sigma$ AD modulator must be designed according to Fig. 1(b) and Fig. 1(c). Figure 1(b) shows the simplified circuit implementation of  $\Delta\Sigma$ AD modulator using ring-amplifier (R-AMP) and SAR ADC, its timing diagram is shown in Fig. 1(c). Because the  $\Delta\Sigma$ AD modulator operates in 4 phases, the speed of operation is limited, and the circuit implementation is complicated.

In order to improve the operation speed of the above  $\Delta\Sigma$ AD

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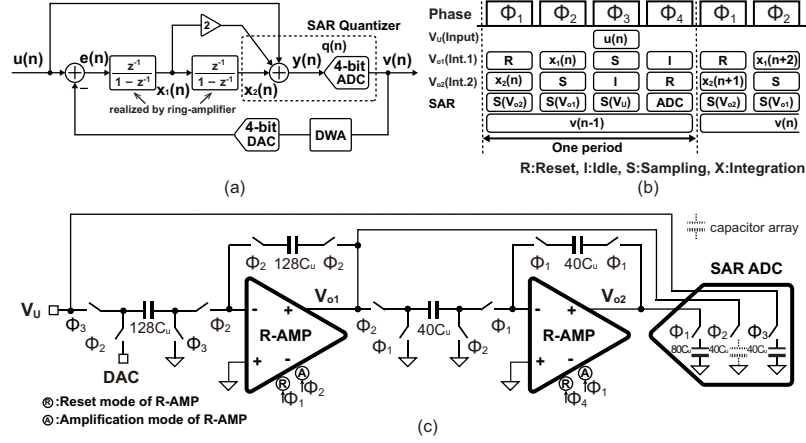


Fig. 1: Conventional 2nd-order feed-forward  $\Delta\Sigma$ AD modulator using SAR quantizer and ring-amplifier. (a) Block diagram. (b) Timing diagram. (c) Simplified circuit schematic.

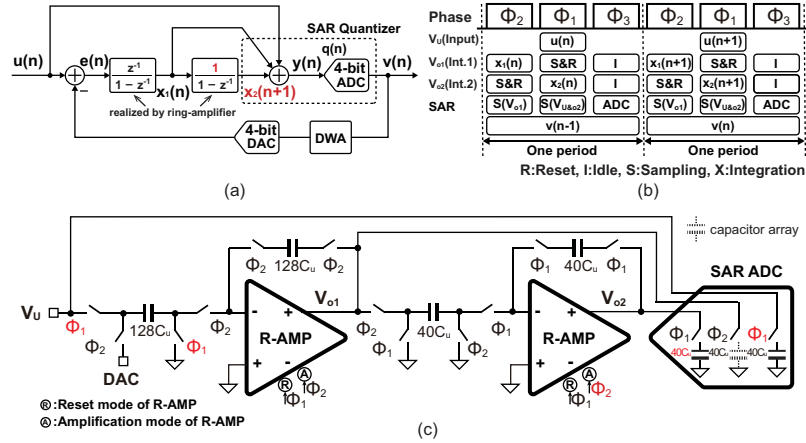


Fig. 2: Proposed  $\Delta\Sigma$ AD modulator using SAR quantizer and ring-amplifier with simplified operation phase. (a) Block diagram. (b) Timing diagram. (c) Simplified circuit schematic.

modulator, we propose a modified  $\Delta\Sigma$ AD modulator architecture using ring-amplifier and SAR ADC for simplifying the operation phase [20]. As shown in Fig. 2(a), the modified  $\Delta\Sigma$ AD modulator only requires 3 phases for once AD conversion. Its timing diagram and simplified circuit schematic are shown in the Fig. 2(b) and Fig. 2(c), respectively. Although the clock timing of two kinds of  $\Delta\Sigma$ AD modulator (Fig. 1(b) and Fig. 2(b)) are different, the modified  $\Delta\Sigma$ AD modulator (Fig. 2) can still realize the 2nd-order noise shaping as same as the traditional 2nd-order  $\Delta\Sigma$ AD modulator. That can be proved as the following. In Fig. 2(a),  $u(n)$  and  $v(n)$  are the input analog signal and the output digital signal of the  $\Delta\Sigma$ AD modulator, respectively. The input signal of the 4-bit sub-ADC can be given as

$$y(n) = u(n) + 2x_1(n) + x_2(n), \quad (1)$$

where  $x_1(n)$  is the 1st-integrator's output signal,  $x_2(n)$  is the 2nd-integrator's output signal.

Since the 2nd-integrator's output signal obeys the following relationship

$$x_2(n+1) = x_1(n) + x_2(n) \quad (2)$$

by combining it with (1) and (2) will lead to

$$y(n) = u(n) + x_1(n) + x_2(n+1) \quad (3)$$

Consequently, the  $\Delta\Sigma$ AD modulator in fig. 1 can be changed as shown in fig. 2. The output signal of the  $\Delta\Sigma$ AD modulator shown in fig. 2 is obtained as

$$v(n) = u(n) + q(n) + x_1(n) + x_2(n+1). \quad (4)$$

The z-domain expression of Eq.(4) can be given as

$$V(z) = U(z) + Q(z) + X_1(z) + X_2(z)z. \quad (5)$$

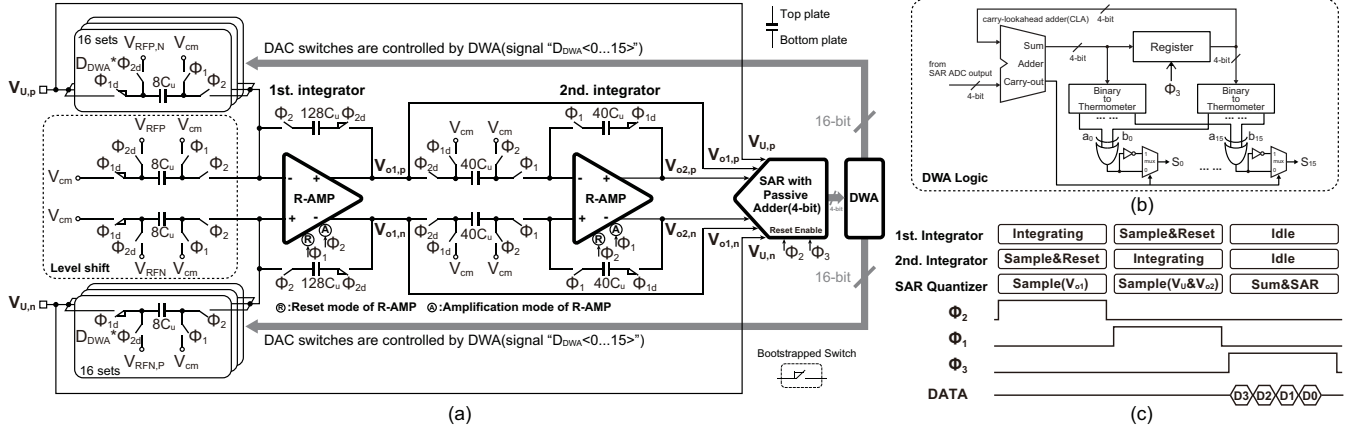


Fig. 3: Circuit implementation of the proposed  $\Delta\Sigma$ AD modulator using SAR quantizer and ring-amplifier with simplified operation phase. (a) Circuit schematic diagram. (b) DWA logic. (c) Clock timing chart.

In fig. 2, the z-domain expression of the 1st and the 2nd integrator's output signal are written as

$$X_1(z) = [U(z) - V(z)] \frac{z^{-1}}{1 - z^{-1}} \quad (6)$$

$$X_2(z)z = \frac{X_1(z)}{1 - z^{-1}} \quad (7)$$

Substituting Eq.(6) and (7) into Eq.(5) we get

$$V(z) = U(z) + (1 - z^{-1})^2 Q(z) \quad (8)$$

It can be concluded that the transfer function of the modified  $\Delta\Sigma$ AD modulator still has the 2nd-order noise shaping characteristic as expressed in Eq.(8). Hence, the equivalence of two kinds of the  $\Delta\Sigma$ AD modulator architecture (Fig. 1 and Fig. 2) is confirmed. The modified  $\Delta\Sigma$ AD modulator only requires three operation phases, so that the operation speed can be optimized to 1.33 (4/3) times compared with the previous work [17] (four operation phases are required in the the previous work), theoretically.

### 3. Proposed $\Delta\Sigma$ AD Modulator Implementation

Figure 3(a) shows the circuit schematic diagram of the proposed 2nd-order  $\Delta\Sigma$ AD modulator using ring-amplifier and SAR ADC with simplified operation phase. Its clock timing chart is shown in Fig. 3(c) [21]. Because the signal  $V_U$  and  $V_{o2}$  are sampled during the same phase by SAR quantizer as shown in Fig. 3, in contrast to Fig. 1, once AD conversion of the modified  $\Delta\Sigma$ AD modulator can be completed in three phases. The modified  $\Delta\Sigma$ AD modulator operation is simplified. In addition, a high-speed SAR ADC is used as an internal 4-bit quantizer. It not only relaxes the requirement on the amplifier's slew-rate, but also improves the stability of the  $\Delta\Sigma$ AD modulator. The 4-bit SAR quantizer has 3 inputs terminal ( $V_U$ ,  $V_{o1}$  and  $V_{o2}$ ), benefit from the SAR quantizer converts the summation of them to digital code by the capacitor array, the adder using active analog components (eg.

OTA or current-mirror) is not required. Moreover, the ring-amplifier performs dynamically the amplification without the static current, so that the high energy efficiency can be maintained.

#### 3.1 SAR ADC with Passive Adder

The block diagram and schematic diagram of proposed SAR ADC with the passive adder are shown in Fig. 4(a) and Fig.4(b), respectively. It consists of capacitive DAC, double tail dynamic comparator [22, 23] (Fig.4(d)) and asynchronous SAR logic circuits. The clock timing chart is represented in Fig. 4(c). Figure 5(a)~(c) show the equivalent circuit of proposed SAR ADC at three kinds of operation mode. In the sampling mode ( $\Phi_2$  and  $\Phi_1$ ), the bottom plates of the sampling capacitors are connected to input signals of  $V_U$ ,  $V_{o1}$  and  $V_{o2}$  and the top plates of the sampling capacitors are connected to  $V_{cm}$  as shown in Fig. 5(a), the ratio of capacitance for 3 input signals is 1:1:1. When the sampling operation is finished, the bottom plates of the sampling capacitors are connected to  $V_{cm}$  in the summation mode (at the beginning of  $\Phi_3$ ) as shown in Fig. 5(b). According to charge conservation law, the voltage at the input port of comparator  $V_x$  can be expressed as:

$$V_x = \frac{V_U + V_{o2} + V_{o1}}{3} \quad (9)$$

Equation (9) means that the summation of 3 input analog signals is realized by reconstituting the capacitor array of the SAR ADC. In the successive approximation conversion mode ( $\Phi_3$ ), the SAR ADC carried out the AD conversion from MSB to LSB as same as a traditional SAR ADC as shown in Fig. 5(c). As above mentioned, the proposed SAR ADC not only achieved an internal 4-bit quantizer, but also realized an analog adder without any active analog components.

#### 3.2 Pseudo-Differential Ring Amplifier

In this work, for maintaining the high energy efficiency of

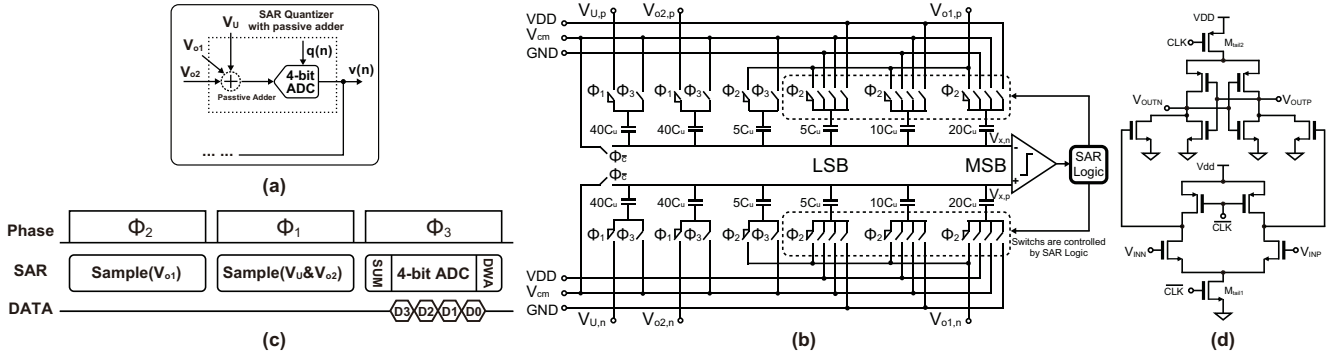


Fig. 4: Circuit implementation of proposed charge redistribution SAR quantizer with passive adder. (a) Block diagram. (b) Schematic diagram. (c) Clock timing chart. (d) Dynamic comparator used in the SAR quantizer.

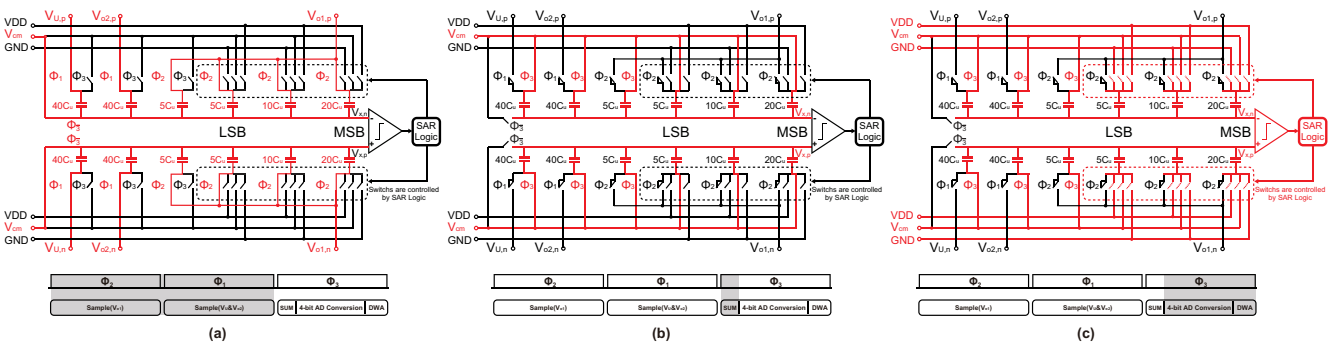


Fig. 5: Equivalent circuits of proposed charge redistribution SAR quantizer with passive adder. (a) Sampling mode. (b) Summation mode. (c) Successive approximation mode.

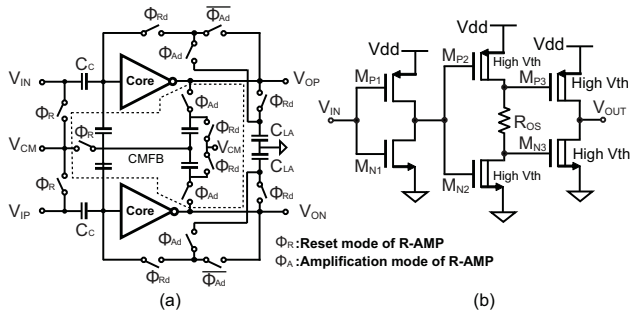


Fig. 6: Schematic of pseudo-differential R-AMP. (a) R-AMP (Ring-Amplifier). (b) Core of R-AMP.

$\Delta\Sigma$ AD modulator, the pseudo-differential ring-amplifier is used to realize the integrator. Fig. 6(a) shows the pseudo-differential ring-amplifier and the common mode feedback (CMFB) circuit [15]. Fig. 6(b) shows the core of the ring-amplifier. It consists of three inverters in series. Because the input referred noise of switched-capacitor (SC) integrator using the ring-amplifier depends on the class-AB amplifier which consists of  $M_{P1}$  and  $M_{N1}$  mainly, the power of the input referred noise is obtained as

$$\overline{V_n^2} = \frac{GB}{f_s} \times \frac{4kT}{3g_m} \approx \frac{20kT}{3g_m} \quad (10)$$

where the ratio of the unit-gain-bandwidth (GB) and the sampling frequency ( $f_s$ ) is set as 5 in the  $\Delta\Sigma$ AD modulator. The noise level of the ring-amplifier-based SC integrator is better than that of the traditional SC integrator using an OTA [14]. Moreover, high threshold voltage  $M_{P2,3}$  and  $M_{N2,3}$  are used for extending the dynamic range of ring-amplifier.

### 3.3 Multi-bit DAC and DWA Logic

A 5-bit capacitor DAC are used for the 1st integrator as shown in Fig. 3(a), the mismatches among the unit elements in a multi-bit DAC cause the harmonic distortion in the signal band [24, 25], the DWA logic circuit [26] is applied to the  $\Delta\Sigma$ AD modulator to reduce the influence of DAC non-linearity errors. The element rotation algorithm and an implementation of the DWA logic are shown in the Fig. 3(b). In addition, a level shift circuit is used for compensating the skew equal to  $LSB/2$  included by DAC's output signal as shown in Fig. 3(a).

## 4. Measurement Results

The proposed  $\Delta\Sigma$ AD modulator was fabricated in TSMC 90nm 1P9M CMOS technology. Fig. 7 shows the chip microphotograph and layout of the proposed  $\Delta\Sigma$ AD modulator,



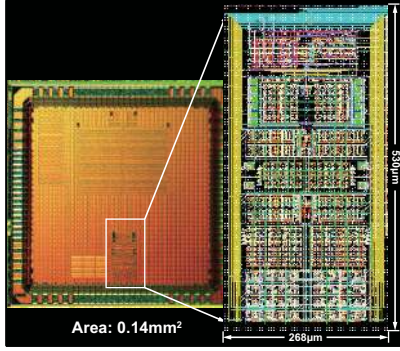


Fig. 7: Chip microphotograph and layout of the prototype modulator.

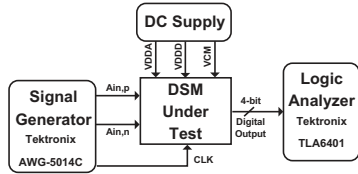


Fig. 8: Measurement setup for the prototype modulator testing.

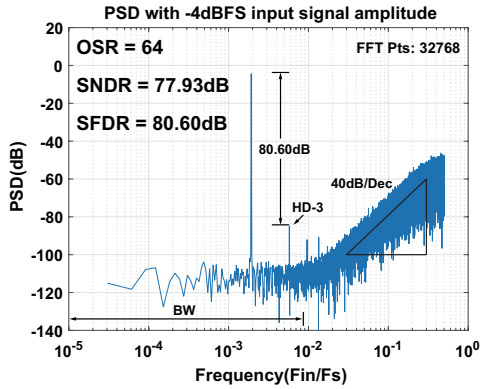
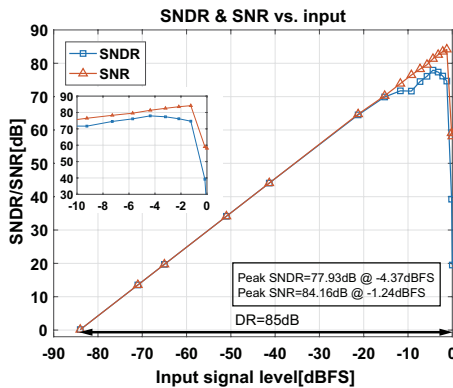
Fig. 9: Measured output spectrum for  $f_{in} \approx 26.92$  kHz and -4 dBFS input signal amplitude.

Fig. 10: Measured results of SNDR and SNR vs. Input signal level [dBFS].

its active area is  $0.14 \text{ mm}^2$ . In order to measure the performance of prototype  $\Delta\Sigma\text{AD}$  modulator, a 26.92 kHz differential sinusoid wave and a 14 MHz square wave created by the AWG are input to the  $\Delta\Sigma\text{AD}$  modulator as shown in Fig. 8. The output digital signal of prototype  $\Delta\Sigma\text{AD}$  modulator detected by logic analyzer is transferred to the power spec-

Table I: Performance summary and comparison with previous works

Specification	[27]	[28]	[29]	[30]	[31]	[17]	This work	
Technology (nm)	180	180	180	180	90	90	90	
Supply voltage (V)	5	1.8	0.7	1.2	1.2	1.1	1.1	1.2
Sampling rate (MS/s)	2.56	6.1	5	25	60	12	14	
OSR	64	152.5	100	8	15	64	64	
Signal BW (MHz)	0.02	0.02	0.025	1.56	2	0.094	0.109	
SNDR (dB)	99.3	97.7	95	75	N/A	77.51	77.82	77.93
SNR (dB)	99.5	98.6	100	N/A	56	80.08	84.05	84.16
DR (dB)	101.3	100.5	100	78	N/A	84	85	
Power (mW)	1.1	0.3	0.87	6.35	1.56	0.37	0.42	0.72
FOMW(pJ/conv.-step)	0.36	0.12	0.38	0.44	0.75	0.32	0.30	0.51
FOMS <sub>SNDR</sub> (dB)	171.9	175.9	169.5	158.9	147.1	161.5	162.0	159.7
FOMS <sub>DR</sub> (dB)	173.9	178.7	174.6	161.9	N/A	168.0	169.2	166.8
Active area (mm <sup>2</sup> )	0.38	0.31	2.16	3.79	N/A	0.16	0.14	

$$\text{FOMW} = \text{Power} / (2 \times \text{BW} \times 2^{(\text{SNDR}-1.76)/6.02})$$

$$\text{FOMS}_{\text{SNDR}} = \text{SNDR} + 10 \times \log_{10}(\text{BW}/\text{Power})$$

$$\text{FOMS}_{\text{DR}} = \text{DR} + 10 \times \log_{10}(\text{BW}/\text{Power})$$

trum by FFT procedure. Fig. 9 shows the power spectrum of output signal of the prototype modulator for a 26.92 kHz sinusoid differential -4 dBFS input being sampled at 14 MS/s. The peak SNDR=77.93 dB is achieved for 109 kHz bandwidth (OSR=64). The measured SFDR is 80.60 dB. Due to the influence of the bootstrapped switch's non-linearity, when a full dynamic range signal is input, the 3rd-order harmonics distortion imposes some performance issue that is verified by the SPICE simulation. Fig. 10 shows the measured SNR and SNDR versus input signal level. Peak SNDR of 77.93 dB and SNR of 84.16 dB at -1.24 dBFS and -4.37 dBFS are achieved, respectively. The measurement results show that linear SNDR responses up to the full scale, and the dynamic range of 85 dB is achieved. The total power consumption is  $720 \mu\text{W}$ . The supply voltages of both analog and digital circuit are 1.2 V. The Schreier FOMS<sub>SNDR</sub> is 159.7 dB. The performance of the proposed  $\Delta\Sigma\text{AD}$  modulator is summarized in Table I in comparison with the previous works.

## 5. Conclusions

A 2nd-order  $\Delta\Sigma\text{AD}$  modulator with simplified operation mode using ring-amplifier and asynchronous SAR ADC has been designed and fabricated in 90nm CMOS technology. Benefit from the reduction of the number of the  $\Delta\Sigma\text{AD}$  modulator operation phase, comparing with the previous work [17], the speed and bandwidth of proposed  $\Delta\Sigma\text{AD}$  modulator are improved by 16.7% ( $((14-12)/12=16.7\%)$ ) for the same performance level. Although, the speed and bandwidth can be improved by 33.3% ( $((4-3)/3=33.3\%)$ ) theoretically, due to the effects of parasitic parameters on wiring, the measurement results is not as expected. Nonetheless, the availability of proposed optimization method is confirmed. Because the integrator is realized by the pseudo-differential ring-amplifier without the static current, and the passive-adder

embedded SAR quantizer not only achieved the 4-bit internal quantizer, but also realized the analog adder without the active analog component, the energy efficiency of the proposed  $\Delta\Sigma$ AD modulator can be kept at high level. Measurement results show the feasibility of the proposed  $\Delta\Sigma$ AD modulator.

## 6. Acknowledgments

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