

# Newcastle University ePrints

Appleby DJR, Ponon NK, Kwa KSK, Zou B, Petrov PK, Wang T, Alford NM, O'Neill A. [Experimental Observation of Negative Capacitance in Ferroelectrics at Room Temperature](#). *Nano Letters* 2014, 14(7), 3864-3868.

**Copyright:**

Copyright © 2014 American Chemical Society.

This article is licensed under a Creative Commons Attribution 4.0 International Public License. For more information and terms of use see:

[http://pubs.acs.org/page/policy/authorchoice\\_ccby\\_termsfuse.html](http://pubs.acs.org/page/policy/authorchoice_ccby_termsfuse.html)

**DOI link to article:**

<http://dx.doi.org/10.1021/nl5017255>

**Date deposited:** 17<sup>th</sup> September 2014



This work is licensed under a [Creative Commons Attribution 4.0 International License](#)

ePrints – Newcastle University ePrints

<http://eprint.ncl.ac.uk>

# Experimental Observation of Negative Capacitance in Ferroelectrics at Room Temperature

Daniel J. R. Appleby,<sup>†</sup> Nikhil K. Poon,<sup>†</sup> Kelvin S. K. Kwa,<sup>†</sup> Bin Zou,<sup>‡</sup> Peter K. Petrov,<sup>‡</sup> Tianle Wang,<sup>‡</sup> Neil M. Alford,<sup>‡</sup> and Anthony O'Neill<sup>\*†</sup>

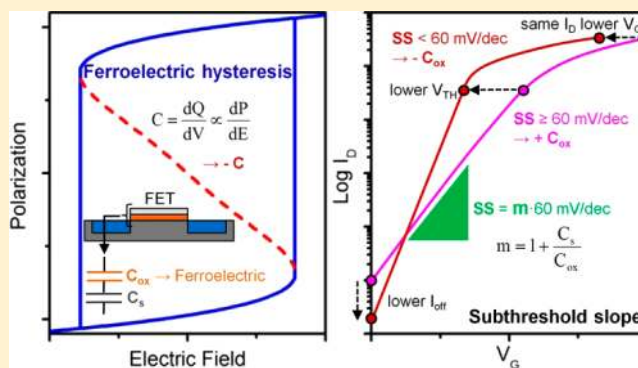
<sup>†</sup>School of Electrical and Electronic Engineering, Newcastle University, Newcastle upon Tyne NE1 7RU, United Kingdom

<sup>‡</sup>Department of Materials, Imperial College London, Royal School of Mines, Exhibition Road, London, SW7 2AZ, United Kingdom

## Supporting Information

**ABSTRACT:** Effective negative capacitance has been postulated in ferroelectrics because there is a hysteresis in plots of polarization-electric field. Compelling experimental evidence of effective negative capacitance is presented here at room temperature in engineered devices, where it is stabilized by the presence of a paraelectric material. In future integrated circuits, the incorporation of such negative capacitance into MOSFET gate stacks would reduce the subthreshold slope, enabling low power operation and reduced self-heating.

**KEYWORDS:** Negative capacitance, ferroelectric, BaTiO<sub>3</sub>, SrTiO<sub>3</sub>



The concept of ferroelectrics displaying effective negative permittivity has led to the speculation that its inclusion in the gate stack of a metal oxide semiconductor field effect transistor (MOSFET) will reduce the subthreshold swing of complementary metal oxide semiconductor (CMOS) devices below 60 mV/dec.<sup>1</sup> For a gate stack comprising a thin ferroelectric layer on top of a thin insulator layer, the channel potential ( $\Psi_s$ ) can change more than the gate voltage ( $V_g$ ) thus providing a step-up voltage transformer and  $S < 60$  mV/dec. If this can be engineered, it heralds a transformation of future integrated circuits (ICs), reducing the off-state current ( $I_{off}$ ) and/or supply voltage ( $V_{DD}$ ) that otherwise limits Moore's Law as heat generated during switching cannot be removed. The idea has led to the search for unambiguous experimental evidence of negative capacitance in candidate ferroelectrics at room temperature as a step toward this ambition. Alternative solutions under investigation for low energy devices include the use of impact ionization (requiring high  $E$  fields so unlikely to be useful at small geometries)<sup>2</sup> and tunneling currents (involving high series resistance which will slow devices).<sup>3</sup>

Ferroelectric materials display spontaneous electric polarization, which can be aligned by an applied electric field. A permanent dipole moment remains when the electric field is removed. An unstable region of negative  $dP/dE$  accompanies  $P$ - $E$  hysteresis corresponding with negative capacitance, but it is energetically unstable in isolation.<sup>4</sup> Experimental evidence for negative capacitance has proved elusive,<sup>5,6</sup> although proposals to stabilize it, in series with positive capacitance, have been put forward.<sup>1</sup> Here we demonstrate experimentally effective

negative capacitance in devices consisting of the ferroelectric BaTiO<sub>3</sub> in series with the paraelectric SrTiO<sub>3</sub> at room temperature. The low Curie temperature of BaTiO<sub>3</sub> allows room temperature stabilization of negative capacitance in a perovskite for the first time. It is repeatable and demonstrated at high frequencies.

Attempts have been made to observe experimentally the characteristics of negative capacitance in ferroelectrics.<sup>5</sup> However, this has proven elusive for ferroelectrics in isolation, because it corresponds with a negative energy density and so is unstable. In order to observe negative capacitance, it must be incorporated into a device with overall positive capacitance (and therefore positive energy density). Specifically, negative capacitance can be stabilized by using a bilayer metal-insulator-metal (MIM) parallel plate capacitor, as shown in Figure 1a.

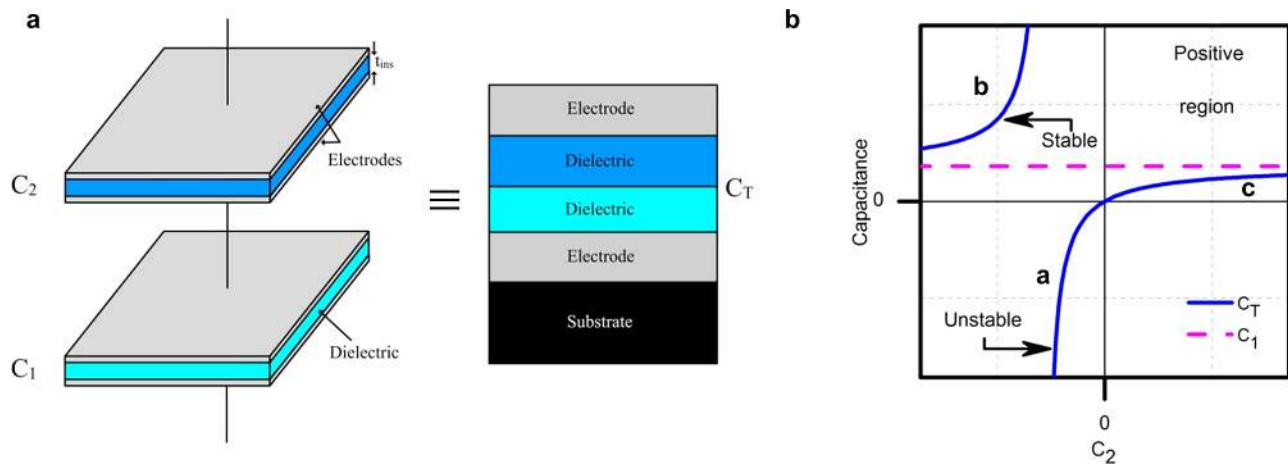
The total capacitance  $C_T$  is the sum of the inverse capacitances of each layer

$$\frac{1}{C_T} = \frac{1}{C_1} + \frac{1}{C_2} \quad (1)$$

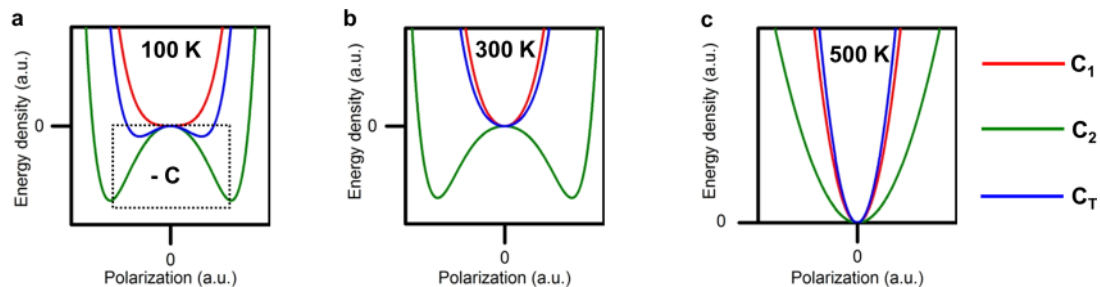
where  $C_1$  is the capacitance from a paraelectric material and  $C_2$  is the capacitance of a ferroelectric material. Figure 1b shows the theoretical relationship between  $C_T$ ,  $C_1$ , and  $C_2$  based on eq 1. It is observed that as  $C_2$  varies from positive to negative,  $C_T$  undergoes different changes to its overall stability. Region b is

Received: March 19, 2014

Published: June 10, 2014



**Figure 1.** Series capacitance configuration and plot of two capacitors. (a) The series capacitance is modeled using a metal–insulator–metal stack on a substrate. (b) The solid line (blue) represents the total capacitance of the system with the dashed line showing the positive capacitor in the series. Data is given as a function of the remaining capacitor contribution  $C_2$ , which is allowed to become negative. Standard analysis for the total capacitance is representative of the right half of the figure. Marked regions, a, b, and c correspond to Figure 2



**Figure 2.** Energy density functions of single and bilayer structures. (a) At 100 K, the BaTiO<sub>3</sub> capacitor  $C_2$  (thickness 50 nm) is in its ferroelectric phase, the SrTiO<sub>3</sub> capacitor  $C_1$  (25 nm) is paraelectric, and total capacitance of the two layers  $C_T$  displays ferroelectric properties. The dashed box encloses the negative capacitance region of the ferroelectric and is unstable in isolation using standard measurements. (b) At 300 K,  $C_2$  and  $C_1$  stay ferroelectric and paraelectric, respectively, while  $C_T$  is stabilized in a paraelectric phase with a shallower energy function than that shown in  $C_1$ . Capacitance enhancement will be seen in the bilayer at this operating temperature. (c) At 500 K, the total capacitance is now a contribution of two paraelectric capacitors,  $C_1$  and  $C_2$ . The resulting energy function displays a sharper characteristic, and hence smaller capacitance than either of the constituent layers.

identified as the design window where effective negative capacitance is stabilized, corresponding with a positive total energy density. Moreover, the total capacitance  $C_T$  is larger than the constituent positive capacitance  $C_1$  due to the negative capacitance  $C_2$ . Region a is unstable, as it has a total energy density that is negative, while region c comprises two positive capacitances in series that combine to have a reduced total capacitance.

In order to provide a better understanding of this phenomenon, the relationship between the total energy density and negative capacitance is described. The ability of a body to store electrical charge,  $Q$ , is defined by its capacitance,  $C$ . It can be described in terms of a change in energy density,  $U$ , as a function of changes in stored charge,  $Q$

$$C = \left[ \frac{d^2U}{dQ^2} \right]^{-1} \quad (2)$$

Thus, for a conventional dielectric there is a quadratic relation between energy density and charge, or polarization. For paraelectric material, where the relation between polarization and applied electric field is nonlinear, the relation between energy density and polarization still has a single turning point when  $P = 0$ . Ferroelectric materials exhibit a spontaneous

electric polarization below a critical temperature,  $T_c$ . Hysteresis is seen in plots of polarization versus applied electric field. It arises from an increasing alignment of electric dipoles as the applied electric field increases, which increases the polarization; when the field is removed there is a nonzero remnant polarization. This is manifested in plots of energy density versus polarization by two minima, as shown in Figure 2a for  $C_2$ . The stabilized minima ensure capacitance is always positive for a ferroelectric under the critical temperature, and polarization switching occurs when the field is reversed (Supporting Information, Figure S1a,b). The negative capacitance region (dashed box in Figure 2a) described by eq 2 due to the negative energy curvature is unstable in isolation.<sup>4</sup> Hence, negative capacitance is never measured for single layer ferroelectrics and should be stabilized in a series capacitance system.<sup>1</sup>

Effective negative capacitance may only be inferred from experiment using specific bilayer MIM device designs and conditions, as described above. Figure 2 shows energy density as a function of polarization for a bilayer  $C_T$  of SrTiO<sub>3</sub>, which is paraelectric and has a capacitance  $C_1$ , and BaTiO<sub>3</sub>, which is ferroelectric below the Curie temperature,  $T_c$ , and has a capacitance  $C_2$ . The relationship between  $C_T$ ,  $C_1$ , and  $C_2$  has been shown previously in eq 1. The series configuration of capacitances allows the summation of the constituent energy

functions to create an overall energy density for  $C_T$  (details in Supporting Information, Figure S1).

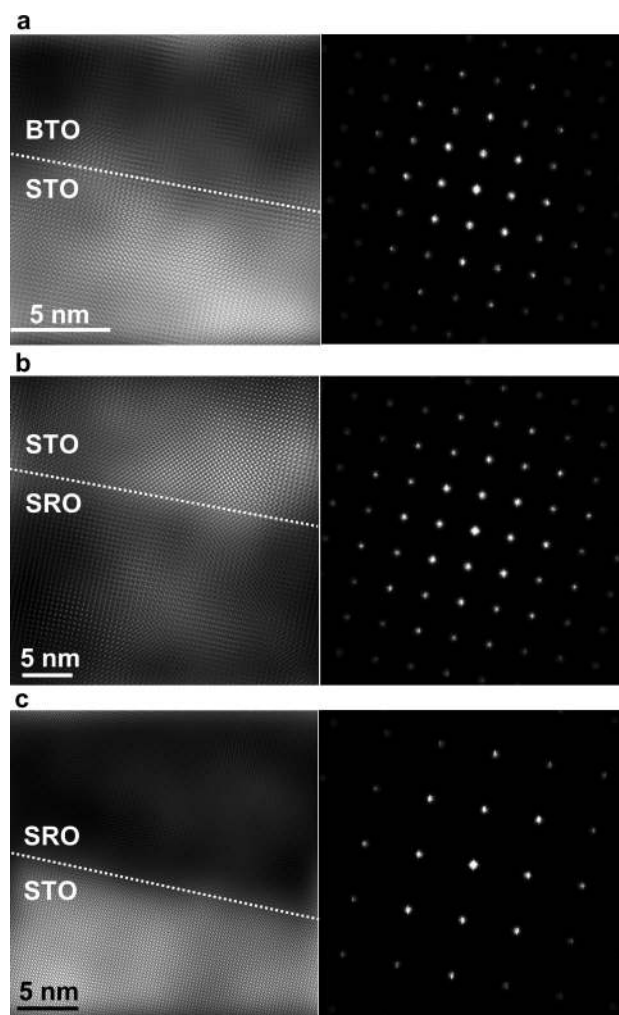
At a low temperature of 100 K (Figure 2a), the total capacitance displays ferroelectric properties as seen by the double minima for the total capacitance  $C_T$ . As a result, the negative capacitance will be energetically unstable and not observable. This corresponds to operations in region a, as shown in Figure 1b. At room temperature (Figure 2b), this bilayer design shows an overall positive capacitance as seen by the single minimum in  $C_T$  at  $P = 0$  and so negative capacitance could be observed. This is the ideal stable operation window, as described in region b in Figure 1b. At a temperature of 500 K (Figure 2c), above  $T_C$  the  $\text{BaTiO}_3$  layer has become paraelectric and so the overall capacitance comes from two paraelectric contributions. In this case, it follows that the total capacitance  $C_T$  is less than  $C_1$  or  $C_2$ , corresponding to region c in Figure 1b.

For the capacitor shown in Figure 2b where  $C_2$  is negative, then  $C_T$  can become larger than  $C_1$ . In this study, experimental evidence is presented to demonstrate effective negative capacitance at room temperature in a thin film of the ferroelectric  $\text{BaTiO}_3$ . The  $\text{BaTiO}_3$  is fabricated in a bilayer stack in series with  $\text{SrTiO}_3$ , which is paraelectric at room temperature. The MIM stack is formed on a  $\text{SrTiO}_3$  substrate and using  $\text{SrRuO}_3$  as the bottom conducting electrode, which is lattice matched to the substrate.

$\text{SrTiO}_3$ ,  $\text{BaTiO}_3$ , and  $\text{SrRuO}_3$  layers used for this study were all deposited by pulsed laser deposition (PLD) technique with a KrF excimer laser from Lambda Physik. Prior to PLD, commercially available, one side polished, single crystal [100] oriented  $\text{SrTiO}_3$  substrates of  $1\text{ cm} \times 1\text{ cm}$  were cleaned. The cleaning procedure involved an ultrasonic bath in acetone, isopropanol, and deionized water for 3 min each. The bottom electrodes ( $\text{SrRuO}_3$ ) were deposited at  $700\text{ }^\circ\text{C}$  at an oxygen pressure of 75 mTorr. A corner of the sample was covered with a small drop of  $\text{TiO}_2$  solution in acetone and was allowed to dry at room temperature. The purpose of this was to give access to the bottom electrode for electrical measurements.  $\text{SrTiO}_3$  and  $\text{BaTiO}_3$  layers were deposited at a substrate temperature of  $850\text{ }^\circ\text{C}$  and 75 mTorr oxygen pressure without breaking the vacuum of the PLD chamber.  $\text{TiO}_2$  was then gently scratched away and the sample was again rinsed in acetone, isopropanol, and deionized water. Circular patterns for top electrodes were created by spinning photoresist AZ-5214E, exposing using Karl-Suss MJB3 aligner and developing in AZ-326 MIF. A 60 nm thick Pt was deposited using a BOC-Edwards electron-beam evaporator and lifted-off in *N*-methylpyrrolidone. Electrodes of sizes ranging from 50 to  $300\text{ }\mu\text{m}$  were thus fabricated to complete the MIM capacitor structure. The  $\text{SrTiO}_3$  thickness is 25 nm and capacitors having  $\text{BaTiO}_3$  thicknesses of 0, 20, 30, and 50 nm were investigated. An additional  $\text{BaTiO}_3$  capacitor of thickness 30 nm was deposited without a 25 nm  $\text{SrTiO}_3$  layer.

Capacitance–voltage (CV) measurements on an Agilent 4294A system were taken at room temperature at a frequency of 10 kHz. Frequency was also varied between 1 kHz and 1 MHz to measure capacitance across a wide frequency range. XRD spectra were acquired using Panalytical x'pert Pro with  $\text{Cu K}\alpha$  X-ray radiation having a characteristic wavelength of  $1.5418\text{ \AA}$ . Transmission electron microscopy was conducted on a JEOL-2100F microscope operating a 200 kV Schottky field emitter. Electron diffractions were processed using Fourier transforms in the Gatan DigitalMicrograph software.

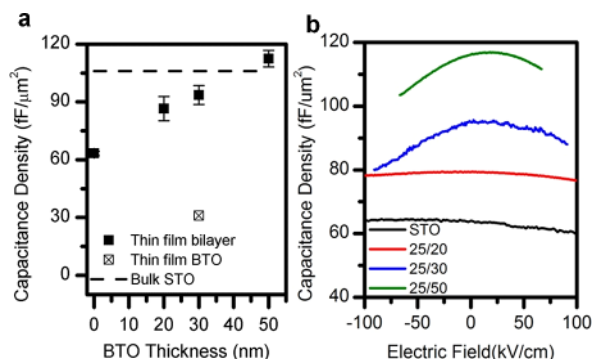
Cross sections of each interface of the capacitor having a  $\text{BaTiO}_3$  thickness of 20 nm are shown in Figure 3. Each layer is



**Figure 3.** TEM of the bilayer structure. Bright-field cross section of one the heterostructures under investigation at each interface. (a)  $\text{BaTiO}_3/\text{SrTiO}_3$  film, (b)  $\text{SrTiO}_3/\text{SrRuO}_3$ , and (c)  $\text{SrRuO}_3/\text{SrTiO}_3$  (100) substrate. Dashed line shows interface between each thin film. Corresponding electron diffraction pattern is also shown indicating the single crystal nature.

perovskite and grown epitaxially, lattice matched to the  $\text{SrTiO}_3$  (100) substrate. Electron diffraction (EDX), and X-ray diffraction (Supporting Information, Figures S2, S3) confirm a single crystal orientation throughout the MIM stack. Atomic force microscopy confirms the smooth interface due to the lattice-matched materials (Supporting Information, Figure S4). Reciprocal space mapping of the EDX pattern in Figure 3a indicates a lattice constant ratio of the perpendicular and in-plane parameters,  $c/a = 1.07$ . An elongation of the  $c$  lattice parameter favors the ferroelectric phase in the  $\text{BaTiO}_3$  film and is necessary for the negative capacitance observed in each structure. The remaining  $\text{SrTiO}_3$  and  $\text{SrRuO}_3$  films were cubic,  $c/a = 1$ .

In Figure 4a, the total capacitance for each capacitor is plotted as a function of their  $\text{BaTiO}_3$  layer thickness. A data point representing the single  $\text{BaTiO}_3$  capacitor  $C_2$  of thickness 30 nm without the 25 nm  $\text{SrTiO}_3$  layer is also shown for comparison. As the  $\text{BaTiO}_3$  layer thickness increases then the



**Figure 4.** Capacitance density in the heterostructures. The capacitance is measured using a parallel-plate relationship. (a) Zero bias capacitance in each structure. At 0 nm, the system is a sole SrTiO<sub>3</sub> capacitor ( $C_1$ ). At 30 nm, an additional data point is shown representing the single BaTiO<sub>3</sub> capacitor ( $C_2$ ) without a SrTiO<sub>3</sub> layer. The error bars correspond to the standard deviation of measurements across each sample. The dashed line represents bulk capacitance density in SrTiO<sub>3</sub>. (b) Full capacitance-bias scans. Measured capacitance increases as a function of BaTiO<sub>3</sub> thickness.

total capacitance is seen to increase, which is consistent with the ferroelectric capacitance being negative ( $C_2$  being negative in eq 1 and so  $C_T$  increases). The increase in ferroelectric layer thickness corresponds with  $C_2$  decreasing in magnitude, so the trend in experiment is consistent with Figure 1b. In each case, the bilayer capacitance exceeds the SrTiO<sub>3</sub> capacitance alone. Any hysteresis behavior is absent from the capacitance measurements in these bilayer devices, which show tunable paraelectric capacitance properties (Figure 4b), consistent with the single minimum energy function in Figure 1b. At 30 nm thickness, in Figure 4a the BaTiO<sub>3</sub> capacitor  $C_2$  displays lower capacitance than in the bilayer. Incorporation of the 25 nm SrTiO<sub>3</sub> thickness has led to an increase in total capacitance due to the stabilized negative capacitance layer in the bilayer (further detail in Supporting Information, Figure S1a,b). The tunable capacitance trends are also shown to increase in Figure 4b as the thickness of BaTiO<sub>3</sub> increases. This is consistent with the insulator becoming dominated with BaTiO<sub>3</sub> due to its higher Curie temperature  $T_c$ . The quality of BaTiO<sub>3</sub> was verified using the single 30 nm layer deposited on SrRuO<sub>3</sub> and investigated using piezoforce microscopy (Supporting Information, Figure S6).

The relative permittivity for bulk SrTiO<sub>3</sub> is widely reported<sup>7</sup> to be around 300, while it is lower for nanometer scale thin films of SrTiO<sub>3</sub><sup>8</sup> (relative permittivity for 25 nm SrTiO<sub>3</sub> capacitor  $C_1$  is 200). Using this bulk value for SrTiO<sub>3</sub> permittivity, the capacitance of the 25 nm SrTiO<sub>3</sub> layer is included as a dashed line in Figure 4a. Even for this most conservative estimate of SrTiO<sub>3</sub> permittivity, the total capacitance for the bilayer stack having a BaTiO<sub>3</sub> layer 50 nm thick is larger than with SrTiO<sub>3</sub> alone, which indicates an effective negative capacitance for the BaTiO<sub>3</sub> layer. This comparison rules out the possibility of the capacitance enhancement resulting from a dead layer effect in the 25 nm SrTiO<sub>3</sub> capacitor, which may otherwise lead to incorrect assumptions about the capacitance enhancement.<sup>9</sup> It also discounts any leakage-mediated reductions in capacitance measured on the single layer SrTiO<sub>3</sub> capacitor and points to the increased total capacitance arising from the stabilization of BaTiO<sub>3</sub> negative capacitance.

The Maxwell–Wagner effect is known to cause dielectric permittivity enhancement in superlattices,<sup>10</sup> and evidence of this in BaTiO<sub>3</sub>/SrTiO<sub>3</sub> heterostructures has been reported previously.<sup>11</sup> But the Maxwell–Wagner effect is known to correlate with the number of heterojunction interfaces and reduces at low frequency. This explanation is therefore not relevant for the capacitance enhancement reported here, which only has a single interface. Moreover, electrical measurements carried out up to 1 MHz also showed capacitance enhancement in these bilayers (Supporting Information, Figure S5). This further rules out Maxwell–Wagner effects as well as defect mediated influences.

The greatest challenge facing nanoelectronics scaling is power dissipation in MOSFETs. Using existing CMOS technology, the subthreshold slope in the transfer characteristic is 60 mV/decade of current (or larger). Thus, for a given on-state current requirement this imposes a limit on either the on-state voltage or the off-state current. The incorporation of effective negative capacitance in the gate stack has been proposed<sup>1,6</sup> to overcome this barrier and experimental investigations have been reported. For example, MOSFETs incorporating polymer ferroelectrics in the gate stack demonstrate a subthreshold swing less than 60 mV/decade over limited current ranges below 10<sup>-10</sup> A/μm, compared with a typical MOSFET threshold current of 10<sup>-7</sup> A/μm.<sup>12,13</sup> These studies showed hysteretic electrical characteristics, which does not correspond to fully stabilized ferroelectric layers as shown in the present work. However, the results indicate the likelihood of negative capacitance as a technology for reducing the subthreshold swing. Similarly, a 2.5 nm layer of AlInN in the gate stack of a metal oxide semiconductor high electron mobility transistor (MOS-HEMT) shows a reduced subthreshold slope, but again only over a restricted current range below 10<sup>-11</sup> A and believed to be due to polarization effects.<sup>14</sup> The structure also required an ultrathin 2.5 nm layer of AlInN with lateral compositional gradients, and the reduced subthreshold slope was lost at a thickness of 7 nm.

A study using the perovskite ferroelectric Pb(Zr<sub>0.2</sub>Ti<sub>0.8</sub>)O<sub>3</sub> in previous bilayer capacitors has been shown.<sup>15</sup> Negative capacitance was stabilized across a temperature range exceeding 573 K, and therefore is unsuitable for integration into modern integrated circuits. Furthermore, stabilization was shown at temperatures up to 773 K and beyond the Curie temperature of the ferroelectric.<sup>16</sup> Explanations for this may be due to straining as the latticed matched structures impose strains that lead to increases in the Curie temperature;<sup>17</sup> however, this was not discussed in the study. The study highlighted that using low Curie temperature materials will enable negative capacitance stabilization at room temperature, such as BaTiO<sub>3</sub> used here.

The present work demonstrates the feasibility of negative capacitance at room temperature using a lead-free perovskite ferroelectric of varying thickness. The robust material can be integrated into CMOS or included as a performance booster within innovative devices such as tunnel field effect transistors<sup>3</sup> in order to realize a future low power technology.

## ■ ASSOCIATED CONTENT

### 📄 Supporting Information

Details on bilayer design and additional simulations. Further experimental evidence of negative capacitance and bilayer material quality. This material is available free of charge via the Internet at <http://pubs.acs.org>.

## AUTHOR INFORMATION

### Corresponding Author

\*E-mail: anthony.oneill@newcastle.ac.uk. Telephone: +44 (0) 191 208 7328. Fax: +44 (0) 191 208 8180.

### Author Contributions

The manuscript was written through contributions of all authors. All authors have given approval to the final version of the manuscript.

### Notes

The authors declare no competing financial interest.

## ACKNOWLEDGMENTS

We thank B. G. Mendis and E. Arac for their help with the transmission electron microscopy experiments. This work was supported by EPSRC and Intel Ireland.

## REFERENCES

- (1) Salahuddin, S.; Datta, S. Use of Negative Capacitance to Provide Voltage Amplification for Low Power Nanoscale Devices. *Nano Lett.* **2008**, *8*, 405–410.
- (2) Gopalakrishnan, K. I-MOS: a novel semiconductor device with a subthreshold slope lower than  $kT/q$ . *IEEE Int. Electron Devices Meet.* **2002**, DOI: 10.1109/IEDM.2002.1175835.
- (3) Ionescu, A. M.; Riel, H. Tunnel field-effect transistors as energy-efficient electronic switches. *Nature* **2011**, *479*, 329–337.
- (4) Salahuddin, S.; Datta, S. Can the subthreshold swing in a classical FET be lowered below 60 mV/decade? *IEEE Int. Electron Devices Meet.* **2008**, DOI: 10.1109/IEDM.2008.4796789.
- (5) Krowne, C. M.; Kirchoefer, S. W.; Chang, W.; Pond, J. M.; Alldredge, L. M. B. Examination of the Possibility of Negative Capacitance Using Ferroelectric Materials in Solid State Electronic Devices. *Nano Lett.* **2011**, *11*, 988–992.
- (6) Zhirnov, V. V. & Cavin, R. K. Negative Capacitance to the rescue? *Nat. Nanotechnol.* **2008**, *3*.
- (7) Jang, H. W.; et al. Ferroelectricity in Strain-Free SrTiO<sub>3</sub> Thin Films. *Phys. Rev. Lett.* **2010**, *104*, 197601.
- (8) Rabe, K. M. New life for the ‘dead layer’. *Nat. Nanotechnol.* **2006**, *1*.
- (9) Stengel, M.; Spaldin, N. A. Origin of the dielectric dead layer in nanoscale capacitors. *Nature* **2006**, *443*, 679–682.
- (10) Catalan, G.; O’Neill, D.; Bowman, R. M.; Gregg, J. M. Relaxor features in ferroelectric superlattices: A Maxwell-Wagner approach. *Appl. Phys. Lett.* **2000**, *77*, 3078.
- (11) Tabata, H.; Tanaka, H.; Kawai, T. Formation of artificial BaTiO<sub>3</sub>/SrTiO<sub>3</sub> superlattices using pulsed laser deposition and their dielectric properties. *Appl. Phys. Lett.* **1994**, *65*, 1970.
- (12) Salvatore, G. A.; Bouvet, D.; Ionescu, A. M. Demonstration of Subthreshold Swing Smaller Than 60mV/decade in Fe-FET with P(VDF-TrFE)/SiO<sub>2</sub> Gate Stack. *IEEE Int. Electron Devices Meet.* **2008**, DOI: 10.1109/IEDM.2008.4796642.
- (13) Rusu, A.; Salvatore, G. A.; Jiménez, D.; Ionescu, A. M. Metal-Ferroelectric-Metal-Oxide-Semiconductor Field Effect Transistor with Sub-60mV/decade Subthreshold Swing and Internal Voltage Amplification. *IEEE Int. Electron Devices Meet.* **2010**, DOI: 10.1109/IEDM.2010.5703374.
- (14) Then, H. W.; et al. Experimental Observation and Physics of “Negative” Capacitance and Steeper than 40mV/decade Subthreshold Swing in Al<sub>0.83</sub>In<sub>0.17</sub>N/AlN/GaN MOS-HEMT on SiC Substrate. *IEEE Int. Electron Devices Meet.* **2013**, 13–691.
- (15) Khan, A. I.; et al. Experimental evidence of ferroelectric negative capacitance in nanoscale heterostructures. *Appl. Phys. Lett.* **2011**, *99*, 113501.
- (16) Rabe, K.; Ahn, C. H.; Triscone, J.-M. Physics of Ferroelectrics: A Modern Perspective. *Top. Appl. Physics* **2007**, *105*, 31–68.
- (17) Pertsev, N. A., Zembilgotov, A. G., Tagantsev, A. K. Effect of Mechanical Boundary Conditions on Phase Diagrams of Epitaxial Ferroelectric Thin Films. *Phys. Rev. Lett.* **1998**, *80*.