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Experimental Verification of Robust PID Controller Under Feedforward Framework for a Nonminimum Phase DC–DC Boost Converter

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***Abstract*— This article addresses the disturbance rejection problem of a nonminimum phase dc–dc boost converter operating in the continuous conduction mode (CCM) using a novel robust proportional–integral–derivative (PID) controller design method. The proposed idea is to design the controller using the equivalent feedforward formulation of the modified direct synthesis (MDS) approach. The advantages of the proposed MDS design are: 1) systematic incorporation of disturbance dynamics and the converter dynamics explicitly in the controller design to reduce the complex tuning effort of the controller parameters; 2) allowing the converter to operate close to the performance limit set by the zero in the right half-plane (RHP); 3) the closed-loop performance specifications can be incorporated into the desired loop response using only single tuning parameter based on Bode's gain crossover frequency inequality; 4) attenuates the loop gain to improve the disturbance rejection; and 5) realization of controller requires only output voltage as a feedback signal. The strength of the proposed MDS method is compared with the internal model control (IMC) method in both simulations and experiments. Based on these responses, the proposed PID ensures robust performance to the model-plant mismatch and allows the output voltage to quickly recover back to the operating voltage in the presence of external disturbances with less inductor current.**

***Index Terms*— DC–DC converter, disturbance dynamics, modified direct synthesis (MDS), proportional–integral–derivative (PID), voltage regulation.**

I. Introduction

A UNIQUE feature of stepping up the low input source voltage makes the continuous conduction mode (CCM) operated boost-type dc–dc converter attractive in numerous industrial applications, such as renewable energy-based DC microgrids and battery-powered applications [1]–[3]. However, the transfer of energy from input to output in such converters leads to nonminimum phase (NMP) behavior, and it appears as a right half-plane (RHP) zero in the transfer function between the duty cycle control input and the controlled output voltage [4]. These systems exhibit an initial inverse response to a step input [5] and limit the achievable bandwidth. The current-mode control (CMC) is conventionally employed to maintain constant output voltage across the load terminals of a dc–dc converter [4]. However, the CMC mode of operation exhibits some serious problems, such as subharmonic instability for duty ratio > 0.5, regardless of the dc–dc converter topology and requires additional current sensors for practical implementation [4]. In addition, it suffers from poor load regulation and noise immunity issues [4]. These undesirable features make the CMC less-preferred mode of operation for industrial applications. On the other hand, the voltage-mode control (VMC) does not have such a limitation on the duty ratio as in CMC. Being a better solution, VMC exhibits sluggish dynamic response due to the presence of RHP zero when employed for dc–dc boost converter [4]. Thus, achieving a fast closed-loop dynamic response with a dc–dc boost converter is still a challenging control problem using the VMC framework.

Some prior work has been reported in the literature to remove the RHP zero in boost-type dc–dc converters [6]–[8]. A formal attempt has been made using leading-edge pulsewidth modulation (PWM) [6], where a higher effective series resistance (ESR) of the output capacitance is required. This leads to a noticeable increase of ripple in the output voltage, particularly at higher load currents. RHP zero may be eliminated using a tristate boost converter with an additional switch across the inductor [7] and also using integrated magnetics [8]. All these attempts lead to an increase in the conduction and switching losses due to the use of additional power components. Several VMC control schemes [9]–[19] have been employed to reduce the effect of RHP zero while improving the closed-loop response of the NMP boost-type dc–dc converter. In [9], the RHP zero is considered as dead time, and then, the Smith predictor technique is applied. This method provides no insight into the hardware implementation. PWM-based sliding mode control (SMC) law requires additional sensors for output capacitor current and input voltage to achieve desired voltage regulation [10] but does not deal with NMP dynamics. Also, the hardware implementation of SMC is nontrivial when both the current and voltage state variables are involved in control signal computation and also notably when sensing of the filtering capacitors' current might affect the efficiency [11]. For controlling the NMP boost

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converter, the SMC using the stable system center method was addressed with the NMP dynamics [12]. However, this article reported only simulation results. The complex hybrid VMC algorithm [13] for the NMP boost converter requires the sensing of the inductor current, output voltage, load current, and input voltage to achieve the satisfactory closed-loop operation. Feedforward compensation has been applied to reduce the effect of input voltage variation using an additional voltage sensor [14]. Furthermore, in [15], the additional current sensor for measuring the inductor current to implement the time delay control under VMC is discussed. The absence of modulator in the practical implementation of enumeration-based voltage-mode model predictive control causes the variable switching frequency [16]. This leads to oversized filters, which is a major drawback, apart from high computational complexity. From the practical implementation standpoint, the above-discussed works are highly complex in nature. Such solutions may not be attractive in the cost-sensitive and high-volume production applications due to the addition of many voltage and current sensors. Failure of any additional sensor not only degrades the closed-loop performance but will also lead to closed-loop instability.

The Type II compensator [28] cannot be used under VMC to control the output voltage of CCM-operated dc–dc converters that exhibit a large phase lag, such as boost-type dc–dc converters [17]. Type III compensator [28] has been applied to boost-type dc–dc converter under VMC [18]. However, such compensators lack a systematic approach of placing the zeros and poles to achieve the desired output voltage regulation. Furthermore, the design method does not include RHP zero in the design stage itself, which leads to poor voltage regulation and so not the preferable choice for the practitioners. Only the simulation studies for the set-point tracking are reported, and also the experiment is not validated for the input voltage variation [18]. The majority of the abovementioned works have shown satisfactory results for disturbance rejection or for set-point tracking, but not for both. Only a few works are reported that consider improving disturbance rejection and set-point tracking using a single output voltage sensor [16], [19]. The experimental validation of a model-based internal model control (IMC) for both disturbance rejection and set-point tracking with two degrees of freedom is carried out in [19]. Here, the dynamic disturbance models are used in the IMC design stage to achieve a significant improvement in the disturbance rejection response. However, the closed-loop operation always requires a large number of computations that make the practical implementation cumbersome, which is a major drawback. Apart from the abovementioned problems, issues such as systematic and computationally simplistic controller design that provides critical insight into the effects of tuning on the closed-loop responses and ability to handle the model-plant mismatch (MPM) have not been fully addressed yet. This motivates the authors to provide a systematic design with the output disturbance dynamic models of NMP boost-type dc–dc converter. Furthermore, there is a necessity to develop a computationally simple voltage-mode controller that works close to the bandwidth limit set by the NMP component, quick disturbance rejection to the input voltage, and load current variation and also obtain the fast set-point tracking using only sensed output voltage as feedback.

Despite the advancements in the controllers, the proportional–integral–derivative (PID) controller is still considered as the most widely used in many industries due to its easy computation in hardware realization, clear functionality, and vast applicability to industrial control loops [20]. A recent survey on the industrial impact and challenges [21] proclaims the PID controller as the most effective and highest impact making technology. However, the major hurdle with the PID controller is the tedious tuning, and nearly 75% of the PID controllers used in industries are poorly tuned and can lead to poor closed-loop response [22]. In convention, the PID controller is employed to control the output voltage of dc–dc converters [19], [23]. Tuning the PID parameters to achieve excellent closed-loop responses for the end applications of dc–dc converters becomes extremely difficult when dealing with the RHP zero. Based on the phase margin information obtained from an additional phase-sensitive multimeter device, the PID parameters were tuned for an NMP boost-type converter [23].

For second-order systems, such as conventional dc–dc converter topologies, the direct synthesis (DS) method leads to a PID control structure. The idea behind the DS approach is to incorporate the dynamic plant model explicitly and a desired closed-loop response based on a time constant in the design procedure. Then, a feedback controller is analytically obtained so that the closed-loop tracking response matches the desired response [24], [25]. The PID tuning parameters are then the function of the desired closed-loop response with a time constant, which is the only tuning parameter. The DS-based controllers perform satisfactorily for the set-point changes. However, these methods fail to exhibit good disturbance rejection, particularly for small time-delay/time-constant systems, such as power electronic converters [24], [25]. Thus, the controller design that underscores the disturbance rejection has motivated to employ the modified DS (MDS) to NMP dc–dc boost-type converters because it incorporates the dynamic disturbance model in the controller design stage. The compelling feature of MDS-based PID control formulation is that the closed-loop performance specifications can be incorporated into the desired loop response using a single tuning parameter and requires only one voltage sensor. The tuning is carried based on Bode's gain crossover frequency inequality [26]. Recently, the stability boundary locus-based PID controller design for NMP high-gain dc–dc boost converter is proposed in [29] and [30], and the comprehensive review on advanced control techniques for the bidirectional dc–dc converter is discussed in [31].

To the best of our knowledge, the achievable performance improvement of the proposed MDS-based PID design approach is possible using only one output voltage sensor. Such a cost-effective solution has not been reported in the literature. The strength of the proposed MDS-based PID controller is validated for linear and nonlinear simulations and on an experimental prototype. It was observed that the proposed robust PID controller provides excellent disturbance rejection and set-point tracking responses over the IMC-PID.

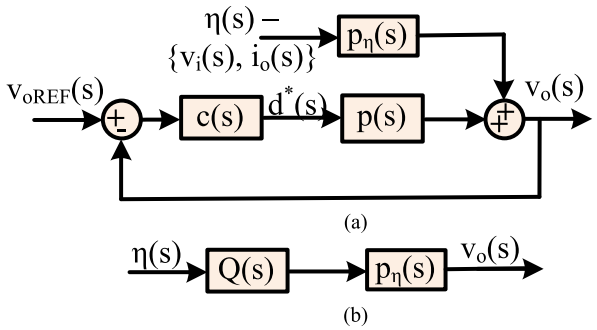

Fig. 1. (a) Feedback control structure with output disturbance dynamics. (b) Equivalent open-loop control structure in feedforward control framework.

The rest of this article is organized as follows. The details of MDS-based PID design are given in Section II. The application of the proposed MDS method to design the robust PID controller for the NMP dc–dc boost converter is discussed in Section III. Section IV presents the linear and nonlinear simulation results. The experimental results are presented in Section V. The key conclusions are provided in Section VI.

II. Modified Direct Synthesis Design for Disturbance Rejection

The controller designed using the DS method provides an interesting perspective as it can handle the NMP component of the boost-type dc–dc converter in an elegant way [24]. The highlight behind using the DS-based controller design is its computational simplicity. The conventional DS approach is a renowned approach that uses the dc–dc converter transfer function and the desired closed-loop transfer function. This method conveys the desired closed-loop response using a closed-loop transfer function for set-point changes. Though the DS approach achieves excellent set-point tracking, it fails to reject the external disturbances [24]. In the majority of power electronic dc–dc converter applications, rejecting the external disturbances, such as changes in input voltage and load current variations and recovering back, quickly, to a steady-state operating point, is vital. Thus, in this work, the control problem is formulated for achieving good disturbance rejection capability. Modification of the conventional DS approach is adopted, which exploits the dc–dc converter transfer function, disturbance dynamics (input voltage and load current), and the desired disturbance transfer function.

The standard feedback control structure with output disturbance dynamics is shown in Fig. 1. In this figure, $p(s)$ represents the control-to-output-transfer function of the dc–dc converter, $c(s)$ represents the feedback controller, and $V_{o\mathrm{REF}}(s)$ and $V_o(s)$ represent the set-point and the measured output voltages, respectively. The external disturbance transfer function models of input voltage and load current are represented by $p_\eta(s)$, and $d^*(s)$ represents plant input (duty ratio). The Laplace domain operator is denoted by "s". It is assumed that the dc–dc converter is open-loop stable. The relation between the external disturbances and the controlled output voltage can be expressed as follows:

$$\frac{v_0(s)}{\eta(\mathrm{s})} = \frac{p_\eta(s)}{1 + p(s)c(s)} \tag{1}$$

Assume that the converter model is perfect, i.e., $p(s) = p_m(s)$, and the disturbance model is also perfect, i.e., $p_\eta(s) = \tilde{p}_\eta(s)$. Under these assumptions, the classical feedback control structure with disturbance dynamics at the dc–dc converter output voltage, as shown in Fig. 1(a), is equivalent to the feedforward control structure, as shown in Fig. 1(b), where

$$\frac{v_0(s)}{\eta(\mathrm{s})} = Q(s)\tilde{p}_\eta(s) \tag{2}$$

The feedforward controller Q(s) can be chosen as follows:

$$Q(s) = \frac{1}{1 + p_m(s)c(s).} \tag{3}$$

In the literature studies [27], it is well known that the design of feedforward controller Q(s) is comparatively easier than the design of feedback controller c(s). The hurdle in the design of the feedback controller arises from the relationship between $[V_o(s)/\eta(s)]$, and $c(s)$ in (1) is nonlinear. Thus, a convenient option is to design a feedforward controller $Q(s)$ and obtain the feedback controller $c(s)$ using the following relation [24]:

$$c(s) = \left[\frac{1 - Q(s)}{Q(s)}\right]\frac{1}{p_m(s).} \tag{4}$$

For the converter systems that exhibit NMP dynamics due to the presence of time delays/RHP zeros, $c(s)$ leads to an unstable controller. To overcome this problem, the converter transfer function is decomposed into invertible and noninvertible parts [24], [27]. The dc–dc converter transfer function is expressed as

$$p_m = p_{m^+}(s)p_{m^-}(s) \tag{5}$$

where $p_m^+(s)$ denotes the minimum phase part that has all poles and zeros in the left half of s-plane, and $p_m^-(s)$ denotes the NMP part that includes RHP zeros and time delay. This decomposition into the minimum phase and NMP is carried such that $p_m^+(0) = 1$ [27].

Assuming that the perfect converter model and perfect disturbance models are available, the desired closed-loop transfer function between the external disturbance and the output voltage can be given by

$$\frac{v_0(s)}{\eta(\mathrm{s})} = G_d(s). \tag{6}$$

Using (2), the feedforward controller can be synthesized as

$$Q(s) = G_d(s)(p_\eta(s))^{-1}. \tag{7}$$

Equations (4) and (7) show that the MDS approach has pole–zero cancellation. Thus, with this formulation, the resultant feedback controller can be expressed as

$$c(s) = \left[\frac{\tilde{p}_\eta(s)}{G_d(s)} - 1\right]\frac{1}{p_{m^+}(s)}. \tag{8}$$

As mentioned in [24], $\tilde{p}_\eta(s)$ is taken as $p_m(s)$. Note that the desired closed-loop transfer function $G_d(s)$ should be chosen

with the NMP component of the converter model so as to cancel the NMP part of the control to the output transfer function.

Using (1) and (8), the closed-loop transfer function between the output voltage and disturbances can be expressed as

$$\left(\frac{v_0(s)}{\eta(s)}\right)^{\text{MDS}} = \frac{p_m(s)p_\eta(s)G_d(s)}{p(s)\tilde{p}_\eta(s) + G_d(s)[p_m(s) - p(s)]}. \quad (9)$$

With the assumption of perfect converter model and the disturbance model, (9) can be further written as

$$\left(\frac{v_0(s)}{\eta(s)}\right)^{\text{MDS}} = G_d(s). \quad (10)$$

Therefore, from (10), it is evident that the desired dynamics is obtained between the controlled output voltage and the disturbances. The feedback controller c(s) obtained from (8) leads to a PID structure if the desired closed-loop transfer function between the external disturbances and the controlled output is chosen appropriately [24].

III. Application to NMP Boost-Type DC–DC Converter

This section deals with the application of the MDS design procedure outlined in Section II to design a PID controller for a boost converter. The circuit diagram of a power stage boost converter is shown in Fig. 2.

The following dc–dc boost converter parameters are chosen for CCM operation: $L = 3.3$ mH, $R_L = 0.3\ \Omega$, $C = 2350\ \mu$F, and $R_c = 0.1\ \Omega$. The load resistance is $R_{\text{nominal}} = 90\ \Omega$. Switching frequency is 20 kHz. The input voltage $V_i = 100/3$ V, and the output voltage $V_o = 50$ V. Using the state-space averaging method and followed by the linearization [4], the small-signal models of the control-to-output transfer function $[\tilde{v}_o(s)/\tilde{d}(s)]$, line-to-output transfer function $[\tilde{v}_o(s)/\tilde{v}_i(s)]$, and the output impedance transfer function $[\tilde{v}_o(s)/\tilde{i}_o(s)]$ are given as follows [19]:

$$p_m(s) = \frac{\tilde{v}_o(s)}{\tilde{d}(s)} = \frac{V_o}{1-D}\frac{(1+CR_Cs)[R^2(1-D)^2 - (R+R_C)(R_{\text{eq}}+Ls)]}{\text{den}(s)} \quad (11)$$

where $\text{den}(s) = R(1-D)[R(1-D) + R_C(1+C(R+R_C)s] + (R+R_C)(R_{\text{eq}}+Ls)(1+C(R+R_C)s)$

$$\frac{\tilde{v}_o(s)}{\tilde{v}_i(s)} = \frac{(1+CR_Cs)(1-D)R(R+R_C)}{\text{den}(s)} \quad (12)$$

$$\frac{\tilde{v}_o(s)}{-\tilde{i}_o(s)} = \frac{(1+CR_Cs)R[R(1-D)R_C - R(1-D)^2R_C + (R+R_C)(R_{\text{eq}}+Ls)]}{\text{den}(s)} \quad (13)$$

Substituting the CCM-operated converter parameters into the abovementioned equations gives the following plant and disturbance models, and we get:

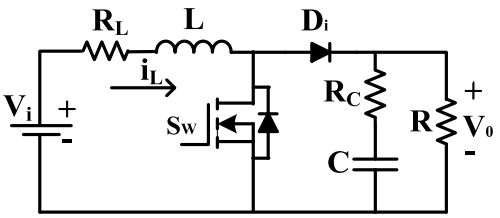

Fig. 2. Power stage of a dc–dc boost converter.

$$p_m(s) = \frac{70.4504(2.35\times10^{-4}s+1)(-3.069\times10^{-4}s+1)}{1.7004\times10^{-5}s^2 + 2.2484\times10^{-4}s+1}. \quad (14)$$

The nominal transfer function of the boost converter in (14) has the RHP zero at 3.2583×10^3 rad/s. The audio-susceptibility transfer function relating the variation in the output voltage to variation in the input voltage is given as

$$\frac{\tilde{v}_0(s)}{\tilde{v}_i(s)} = \frac{1.456(2.35\times10^{-4}s+1)}{1.7004\times10^{-5}s^2 + 2.2484\times10^{-4}s+1}. \quad (15)$$

The output impedance transfer function that relates the variation in the output voltage to the variation in the load current is

$$\frac{\tilde{v}_0(s)}{\tilde{i}_0(s)} = \frac{-0.73409(2.35\times10^{-4}s+1)(9.8175\times10^{-3}s+1)}{1.7004\times10^{-5}s^2 + 2.2484\times10^{-4}s+1}. \quad (16)$$

Equations (15) and (16) show that the variations in source voltage and load current affect the load voltage qualitatively in the same manner as the duty ratio control input [19].

A. Controller Design Requirements

The controller is designed to achieve the following objectives during the dynamic variations for the disturbance rejection and set-point change cases with steady-state error $< 1\%$ of the desired output voltage:

1) to regulate the nominal output voltage (V_o) to the nominal reference voltage ($V_{o\text{REF}}$);
2) fast recovery to the steady-state output voltage in the presence of external variations that occur in the form of input voltage and load current variations;
3) quick transition from the nominal reference voltage to the new desired output voltage.

A popularly used parallel form of PID can be written as

$$c(s) = K_c\left(1 + \frac{1}{\tau_I s} + \tau_D s\right). \quad (17)$$

The desired closed-loop transfer function between the controlled output and the external disturbances is chosen such that the controller results in the form of a PID controller [see (8)]. Hence, the desired closed-loop transfer function in [24] is given as follows:

$$G_d(s) = \frac{K_d s(-as+1)}{(\tau s+1)^3} \quad (18)$$

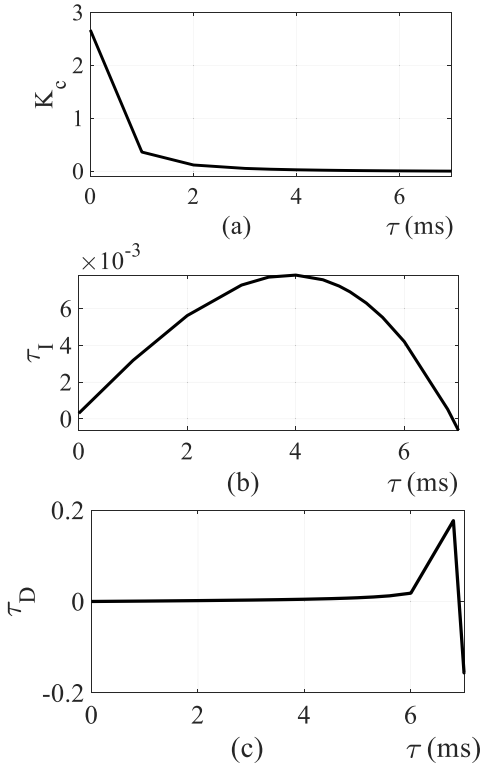

Fig. 3. MDS PID values for different τ Values. (a) K_c versus τ. (b) τ_I versus τ. (c) τ_D versus τ.

where $K_d = \tau_I/K_c$, and a represents the position of RHP zero of the boost converter. Moreover, the time constant that determines the speed of the closed-loop response is denoted as τ.

B. Effect of "τ" on the Choice of Control Parameters

It is essential to investigate the effect of "τ" in obtaining the appropriate PID control parameters that decide the performance and stability of the converter. A brief overview of selecting the upper bound on "τ" is discussed here.

Fig. 3 shows the MDS-PID controller values for different values of the closed-loop time constant (τ). From Fig. 3(a), it is observed that the proportional gain (K_c) of the PID controller is inversely related to τ. To achieve the fast dynamic response in the closed loop (small τ), a large proportional controller gain is required, and vice versa. From Fig. 3(b), as τ increases, the integral time (τ_I) increases up to $\tau \leq 4$ ms and then decreases and becomes negative for $\tau > 6.9$ ms. Similarly, from Fig. 3(c), the derivative time (τ_D) increases initially, then decreases, and becomes negative for $\tau > 6.9$ ms. Thus, for the boost-type dc–dc converter, $\tau < 6.9$ ms becomes the upper bound to obtain the positive PID gains that can be realized for the hardware implementation.

Using this upper bound, the frequency-domain analysis has been carried out to understand the effect of the single tuning PID controller parameter, i.e., τ in the MDS approach. The effect of the disturbance attenuation can be graphically visualized in the frequency domain using the bode plots. The NMP behavior of the boost converter restricts the upper bound on the achievable crossover frequency (ω_{gc}) of the loop transfer function $[L(s) = p_m(s)c(s)]$ in the closed-loop using the gain crossover frequency inequality based on the RHP zero [26]. It is given as

$$\omega_{gc} \leq \begin{cases} \frac{a}{2} \text{ for } S_p, \quad T_p < 2 \\ \frac{a}{5} \text{ for } S_p, \quad T_p < 1.4 \end{cases} \tag{19}$$

where S_p and T_p are the peak values of the sensitivity function $S = 1/(1 + L)$ and the complementary sensitivity function $T = L/(I + L)$ and are defined as

$$S_p = \overset{\text{Max}}{\omega}|\text{S}(j\omega)|, \quad T_p = \overset{\text{Max}}{\omega}|\text{T}(j\omega)|. \tag{20}$$

With the restrictions on ω_{gc} (19), due to the NMP boost-type dc–dc converter, the maximum attainable gain crossover frequencies are around 650 and 1630 rad/s, respectively. To compare the performance of PID design using the MDS approach, another approach using IMC-based PID design that also incorporates the RHP zero in the design stage itself has been considered. Both the controllers are tuned to have the same gain crossover frequencies, i.e., $\omega_{gc} = 650$ and 1630 rad/s, as shown in Fig. 4. This leads to four sets of PID values due to two sets corresponding to each ω_{gc}. At $\omega_{gc} = 650$ and 1630 rad/s, the corresponding controllers are denoted as PID-1_{MDS}, PID-1_{IMC} and PID-2_{MDS}, PID-2_{IMC}, respectively. The corresponding PID gains for both MDS and IMC designs are shown in Table I. The loop-shaping plots with different PID controllers designed using the different methods without and with derivative filter [see (17) and (21)] are shown in Fig. 4 along with the values listed in the Table I. In Figs. 5 and 6, the effect of input voltage disturbance attenuation and the output impedance attenuation is shown for the four different sets of PID controller's parameters.

All the PID controllers provide sufficient gain at low frequencies (see Fig. 4) for attenuating both the input voltage and output impedance disturbances, as shown in Figs. 5 and 6. Such a high gain makes the steady-state error to be very small. For the NMP dc–dc boost converter, the resonant poles of plant model (14) and disturbance models (15) and (16) are the same, and it appears around 36 Hz. Thus, the mid-range frequency shaping between 10 and 100 Hz is crucial. The MDS approach incorporates the dynamic disturbance models in the PID design, will provide more gain in magnitude than the IMC-PID

TABLE I
VARIATION OF K_c, τ_I, AND τ_D WITH τ IN MDS AND IMC-BASED PID

Controller	τ (ms)	K_C	τ_I	τ_D
PID-1_{IMC}	1	2.186776 e-2	2.0134 e-3	7.117273 e-3
PID-2_{IMC}	0.3121	4.616958 e-2	2.0134 e-3	7.117273 e-3
PID-1_{MDS}	3.78	2.888858 e-2	7.8093 9e-3	4.690974 e-3
PID-2_{MDS}	1.5	1.915423 e-1	4.4752 58e-3	1.648574 e-3

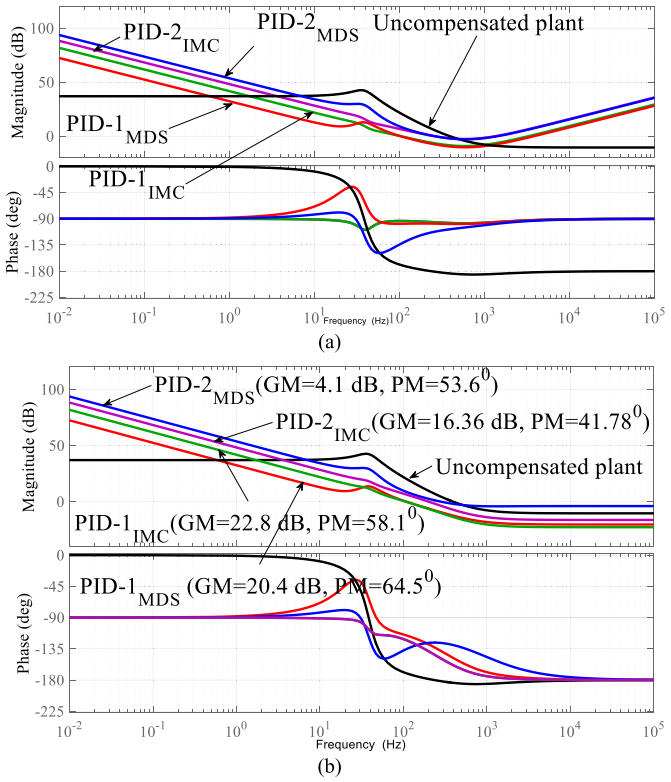

Fig. 4. Loop-shaping plot with different sets of PID parameters (a) without derivative filter [see (17)] and (b) with filter [see (21)].

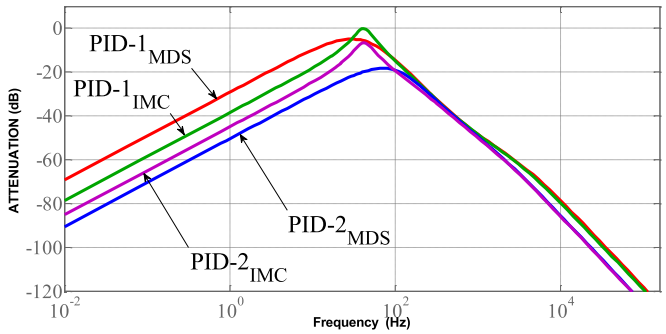

Fig. 5. Frequency response of the input voltage disturbance attenuation $([1/(1+L)](\tilde{v}_o(s)/\tilde{v}_i(s)))$.

design in attenuating the disturbances around the resonant pole frequency range, i.e., the occurrence of disturbance/plant poles (see Fig. 4), and amplifies the attenuation (see Figs. 5 and 6). As a result, the effect of external disturbances gets reduced and leads to a fast recovery of the output voltage to the steady state with MDS-based PID compared with the IMC-PID.

From the abovementioned analysis, it can be seen that the tuning of three parameters of PID controllers' has been reduced to one parameter with the chosen PID designs. This makes the tuning simpler, especially when tuning the PID to have the same gain crossover frequency.

IV. Simulation Studies

Before proceeding to the experimental evaluation, it is necessary to verify the strength of the proposed MDS method using the linear (transfer function) and nonlinear circuit

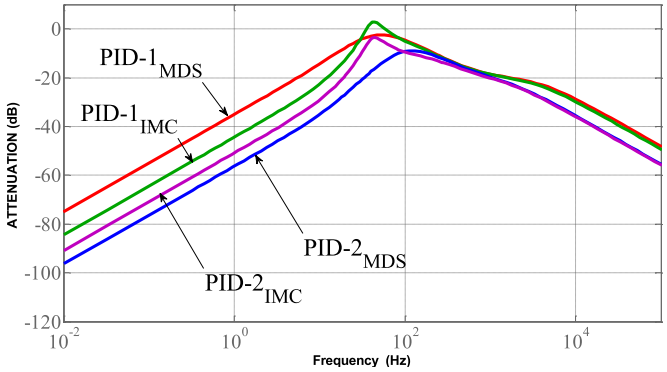

Fig. 6. Frequency response plot of the output impedance disturbance attenuation $([1/(1+L)](v_0(s)/i_0(s)))$.

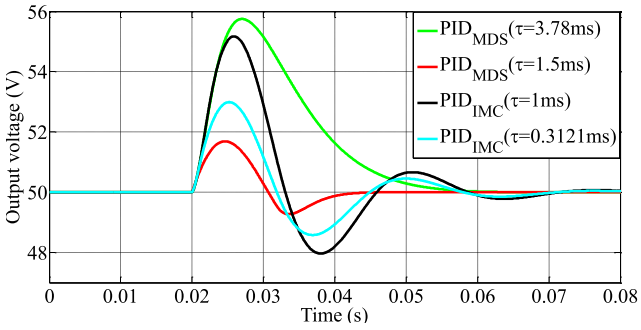

Fig. 7. Regulatory behavior comparison of load voltages with PID control schemes in linear simulations for a step change in the input voltage from 33.3 to 48.3 V at $V_{oREF} = 50$ V.

models through the simulations. The following two scenarios are considered for carrying the simulations.

1) *Linear Simulation Studies:* The dynamic transfer function model of the NMP dc–dc boost converter (14) is used.
2) *Nonlinear Simulation Studies:* The nonlinear model of dc–dc boost converter circuit is developed in SimPowerSystems Toolbox of MATLAB/SIMULINK with the values given in Section III. The simulations are carried to show the potential advantages of the proposed MDS-based PID controller for rejecting the disturbance capability and robustness (MPM). The designed PID controllers are implemented in the widely used "parallel form," given as follows:

$$c(s) = K_c\left(1 + \frac{1}{\tau_I s} + \frac{\tau_D s}{\alpha\tau_D s + 1}\right). \tag{21}$$

The derivative filter parameter $\alpha = 0.1$ is used in this work [24]. The closed-loop responses of the designed PID controllers for a step change in input source voltage from 33.3 to 48.3 V are shown in Figs. 7 and 8, respectively, for both linear and nonlinear simulations. The performance indices, such as output voltage deviation (Δv_o) and settling time (T_s), are compared in Table II.

Among the different PID controllers, the proposed MDS-based PID controller with $\tau = 1.5$ ms performs significantly better than the other PID's in terms of the performance

TABLE II
REGULATORY BEHAVIOR: CHANGE IN V_i (33.3 TO 48.3 V) AT $V_{oREF} = 50$ V

PID controller	Linear simulation		Non-linear simulation	
	Δv_o(%)	T_s (ms)	Δv_o(%)	T_s (ms)
MDS (τ=1.5ms)	3.37	20	2.8	10
IMC (τ=0.3121ms)	5.98	45	5.02	25
IMC (τ =1ms)	10.34	48	9	30
MDS (τ =3.78ms)	11.49	34.5	11.2	30

indices for both the linear and nonlinear simulations (see Table II). The MDS-based PID with $\tau = 1.5$ ms exhibits excellent transient behavior in terms of performance indices that underscored the robustness in the presence of MPM. Also, it can be seen from Fig. 8 that the MDS-based PID with $\tau = 1.5$ ms utilizes less inductor current in providing excellent improvement in the output voltage response [see Fig. 8(b)]. The output voltage responses in nonlinear simulations are qualitatively similar to the linear simulations. Thus, from the simulation results, it can be concluded that the PID is tuned by incorporating the dynamic disturbance models using the MDS approach with $\tau = 1.5$ ms. Then, the closed loop exhibits an excellent dynamic response in rejecting external disturbances and provides robustness in the presence of MPM.

V. EXPERIMENTAL VALIDATION

To verify the robustness of the designed PID controller using the proposed MDS method and to validate the observations reached from the simulation studies, an experimental prototype of the boost converter is synthesized using Semikron module (model no. SKM75GB12T4). The complete experimental test bed is shown in Fig. 9(a). Lower switch of the IGBT module is used as the main switching device of the boost converter for which the controlled pulses will be given. To expedite the experimental verification, the designed controllers were implemented on the hardware setup using OPAL-RT real-time simulator (Model no. OP5700) with a fixed time step of 3 μs. The controller is implemented in MATLAB/Simulink (R2012a), and the RT-LAB software (version 11.0.8.13) is used to interface with the real-time simulator, as shown in Fig 9(b). A 16-bit analog-to-digital converter (ADC) module having a sampling rate of 500 kSPS is used to measure the output voltage. The data acquisition system OP8660 scales down the measured output voltage by a factor of 1/60 before giving it as feedback to the analog input port of the real-time simulator. Here, the quantization error due to the A/D conversion is about 0.915 mV, which is negligible. A programmable DC electronic load of rating 500 V, 15 A, and 200 W (Keithley Model no. 2380-500-15) is used to perform the step load changes. In order to verify the robustness in the realistic MPM, the PID parameters used in simulations (see Section IV)

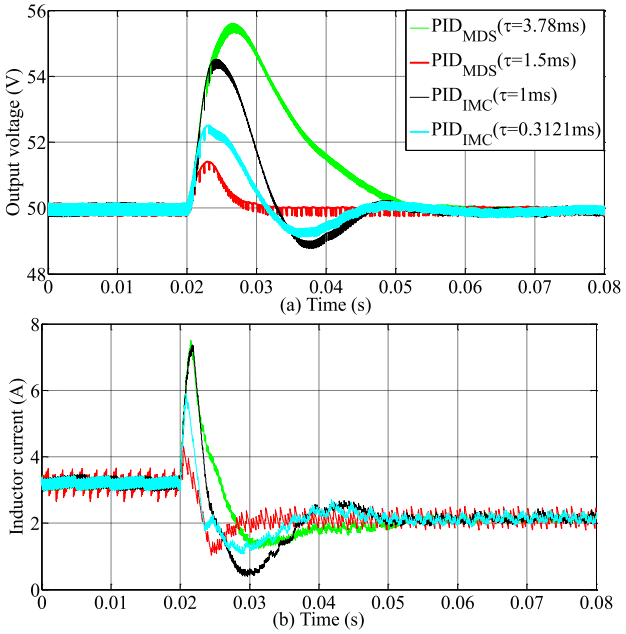

Fig. 8. Regulatory behavior comparison of PID control schemes in nonlinear simulations for a step change in input voltage from 33.3 to 48.3 V at $V_{oREF} = 50$ V. (a) Load voltage. (b) Inductor current.

are kept the same while conducting the experiments. The following regulatory and servo scenarios are considered to verify the robustness for the external variations and dynamic performances:

A. Regulatory Scenarios

1) *Step Changes in the Input Voltage:*
   (a) 33.3–48.3 V at I_o(nominal) = 2 A and $V_o = 50$ V.
   (b) 33.3–23.3 V at I_o(nominal) = 2 A and $V_o = 50$ V.
   (c) 33.3–48.3 V at I_o(nominal) = 2 A and $V_o = 60$ V.
2) *Step Changes in the Load Current:*
   (d) 2–0.2A at V_i(nominal) = 33.3 V and $V_o = 50$ V.
   (e) 2–0.2A at V_i(nominal) = 33.3 V and $V_o = 60$ V.

B. Servo Scenario (V_i(Nominal) = 33.3 V, I_o(Nominal) = 2 A)

(f) Step change in the output reference from 50 to 60 V.

For the aforementioned case studies, closed-loop responses at load terminals are shown in Figs. 10–15.

1) Scenarios (a)–(c): Step changes in the input voltage from 33.3 to 48.3 and 33.3 to 23.3 V are given with $V_{oREF} = 50$ V. The corresponding variations in the output voltage and the inductor current are shown in Figs. 10 and 11, respectively, along with the input voltage variation. In both the scenarios, the PID controller designed using the proposed MDS approach with $\tau = 1.5$ ms rejects, quickly, the external variation in the input voltage and reaches the operating output voltage with a smaller deviation quite faster compared with the IMC-based PID design approach, as shown in Figs. 10(a) and 11(a), respectively.

Among the two MDS-based designs, the MDS approach with $\tau = 1.5$ ms performs better than the MDS approach

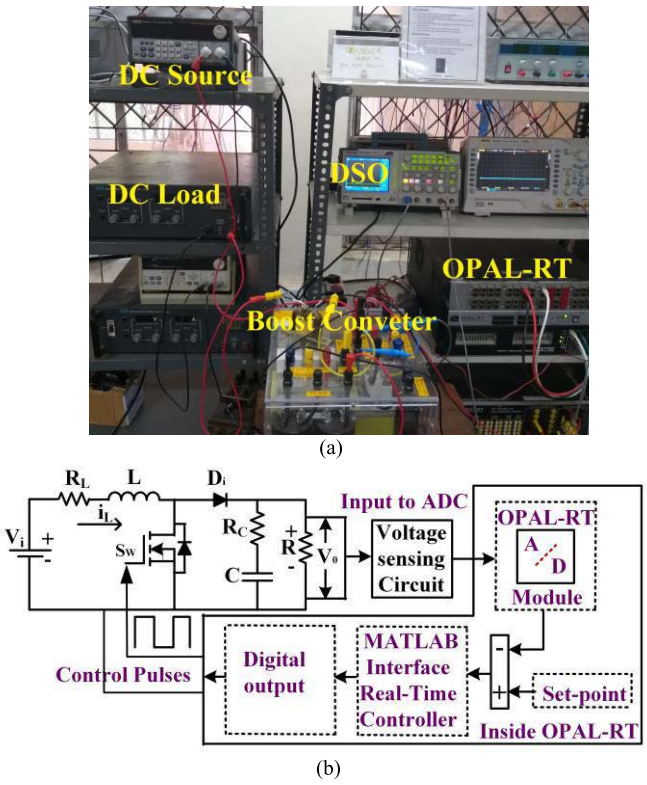

Fig. 9. (a) Laboratory prototype of the experimental setup. (b) Block diagram of the implementation of the controller using OPAL-RT.

with $\tau = 3.78$ ms due to the provision of high gain in the low- and mid-frequency regions (see Fig. 5). Also, as seen from Figs. 10(b) and 11(b), the MDS-based PID ($\tau = 1.5$ ms and $\tau = 3.78$ ms) exhibits less inductor current swing during the transients compared with the IMC-based PID ($\tau = 0.3121$ ms and $\tau = 1$ ms), respectively. Thus, it can be concluded that for both the step-up/step-down changes in the input voltage [see Fig. 10(c) and 11(c)], the MDS approach with $\tau = 1.5$ ms exhibits excellent dynamic response while drawing smaller inductor current during the dynamic cases.

Furthermore, to test the robustness of the PID controllers, the experiments were conducted at a different operating point with desired output voltage $V_{o\text{REF}} = 60$ V. The resultant closed-loop responses of load voltage and inductor current are shown in Fig. 12. The PID controllers were tuned for the same gain crossover frequency $\omega_{\text{gc}} = 650$ rad/s, and $\text{PID}_{\text{MDS}}(\tau = 3.78$ ms) reaches the steady state quickly but with minor deviation compared with $\text{PID}_{\text{IMC}}(\tau = 1$ ms). Also, it can be seen from Fig. 12(b) that the inductor current exhibits large swing with $\text{PID}_{\text{IMC}}(\tau = 1$ ms) than $\text{PID}_{\text{MDS}}(\tau = 3.78$ ms). On the other hand, when the PID controllers were tuned for the same higher gain crossover frequency $\omega_{\text{gc}} = 1630$ rad/s, the response due to $\text{PID}_{\text{IMC}}(\tau = 0.3121$ ms) controller exhibits voltage swing and takes time to settle, whereas $\text{PID}_{\text{MDS}}(\tau = 1.5$ ms) controller response shows small deviation. In this extreme scenario, the improvement in the output voltage is achieved with less inductor current during the transient [see Fig. 12(b)] using the proposed MDS approach-based PID controller.

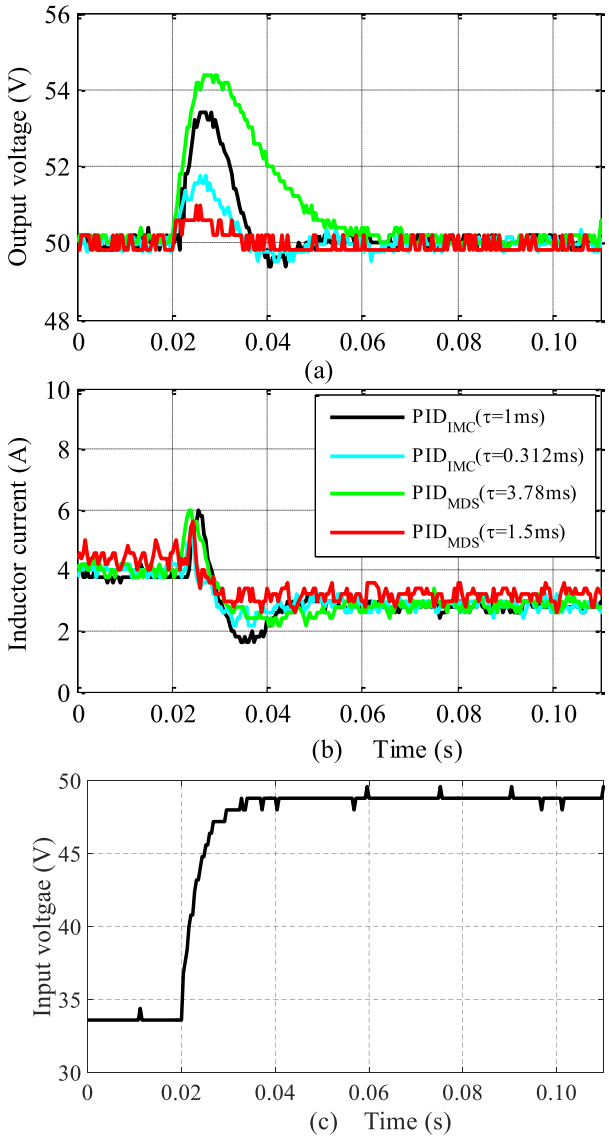

Fig. 10. Regulatory responses of PID controllers' in experiments for input voltage variation from 33.3 → 48.3 V at nominal load and $V_o = 50$ V. (a) Output voltage. (b) Inductor current. (c) Input voltage.

2) Scenarios (d)-(e): In this scenario, the designed PID controllers are validated near the DCM operation by changing the nominal load current from 2 to 0.2 A for $V_{o\text{REF}} = 50$ V. The corresponding closed-loop responses are shown in Fig. 13. Among the PID controllers that were tuned for the same gain crossover frequency $\omega_{\text{gc}} = 650$ rad/s, the $\text{PID}_{\text{MDS}}(\tau = 3.78$ ms) controller response exhibits the lesser voltage swing and reaches the steady state quickly compared with the $\text{PID}_{\text{IMC}}(\tau = 1$ ms) response. On the other hand, when the PID controllers were tuned for the higher gain crossover frequency $\omega_{\text{gc}} = 1630$ rad/s, the response due to $\text{PID}_{\text{IMC}}(\tau = 0.3121$ ms) exhibits voltage swing and takes time to settle, whereas $\text{PID}_{\text{MDS}}(\tau = 1.5$ ms) shows no hint of undesirable voltage swing. To investigate the robustness and the fast dynamic response of the MDS approach-based PID controller, further experiments were conducted to validate the near DCM operation by changing the nominal load current from 2 to 0.2 A for $V_{o\text{REF}} = 60$ V, and the corresponding

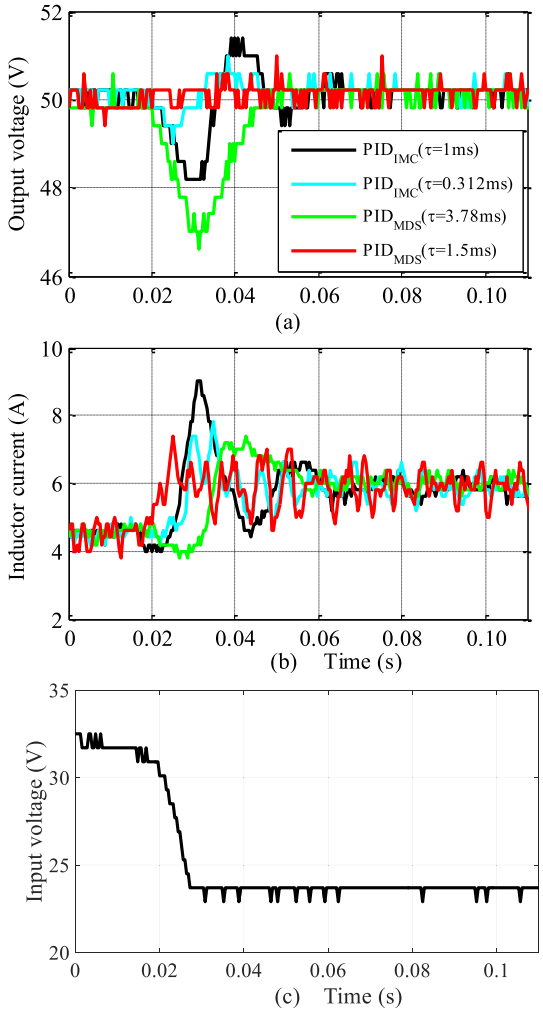

Fig. 11. Regulatory responses of PID controllers' in experiments for input voltage variation from 33.3 → 23.3 V at nominal load and V_o = 50 V. (a) Output voltage. (b) Inductor current. (c) Input voltage.

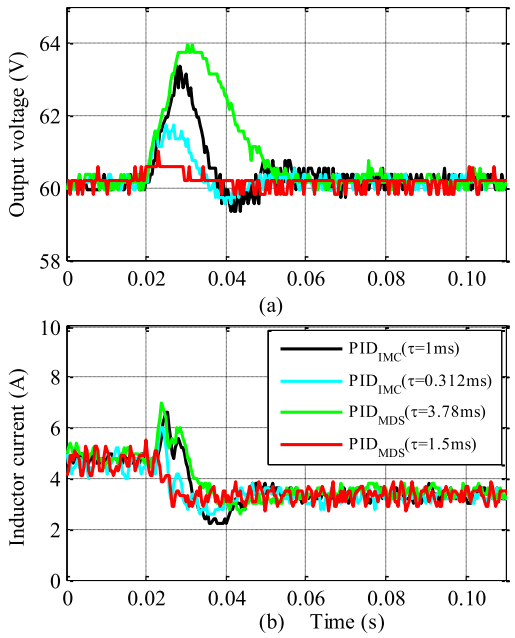

Fig. 12. Regulatory responses of PID controllers' in experiments for input voltage variation from 33.3 → 48.3 V at nominal load and V_o = 60 V. (a) Output voltage. (b) Inductor current.

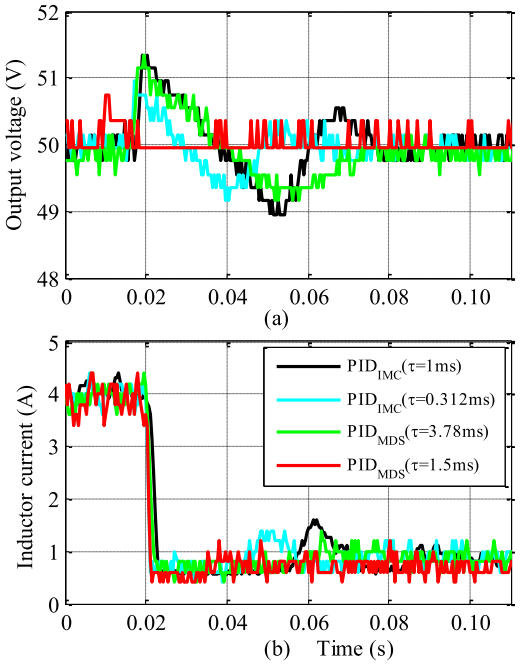

Fig. 13. Regulatory responses of PID in experiments for variation in load current from 2 → 0.2 A at V_i = 33.3 V and V_o = 50 V. (a) Output voltage. (b) Inductor current.

closed-loop responses are shown in Fig. 14. In this scenario as well, the PID design using the MDS for the two sets of gain crossover frequencies (ω_{gc} = 650 and 1630 rad/s) exhibits excellent dynamic behavior over its counterparts, i.e., IMC-PID (τ = 1 ms and τ = 0.3121 ms), respectively, in terms of both voltage swing and the settling time [see Fig. 14(a)]. Thus, it can be concluded that for the near DCM operation, the PID controller using the proposed MDS approach has the upper hand in terms of voltage swing and faster settling time for both the gain crossover frequency sets (ω_{gc} = 650 and 1630 rad/s) over the IMC-PID design.

3) Scenario (f): Finally, the designed PID controllers are analyzed for the set-point tracking response by changing the output reference voltage from 50 to 60 V. The corresponding closed-loop response is depicted in Fig. 15. Here, with the PID design using the MDS approach (denoted as PID-1_{MDS} and PID-2_{MDS}), the set point reaches the new desired output voltage level as fast as possible in comparison to the IMC-PID controllers (denoted as PID-1_{IMC} and PID-2_{IMC}), respectively [see Fig. 15(a)]. In particular, it is interesting to observe that PID-1_{MDS} (based on ω_{gc} = 650 rad/s), the output voltage response, reaches, quickly, the new desired voltage with very little deviation, whereas the corresponding IMC-PID exhibits oscillations and takes a longer time in reaching a new steady state.

Thus, from the various regulatory cases investigated in the experiments, it can be concluded that the proposed PID controller design using the MDS approach under the feedforward design framework provides excellent disturbance rejection for variations in both the input voltage and the load current.

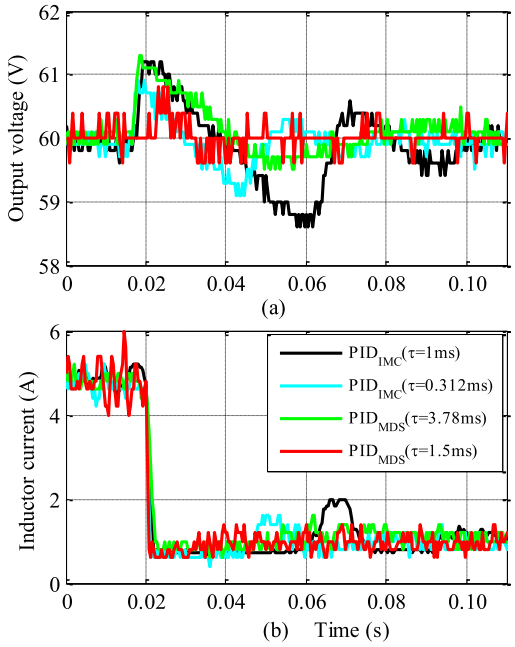

Fig. 14. Regulatory responses of PID in experiments for variation in load current from 2 → 0.2 A at $V_i = 33.3$ V and $V_o = 60$ V. (a) Output voltage. (b) Inductor current.

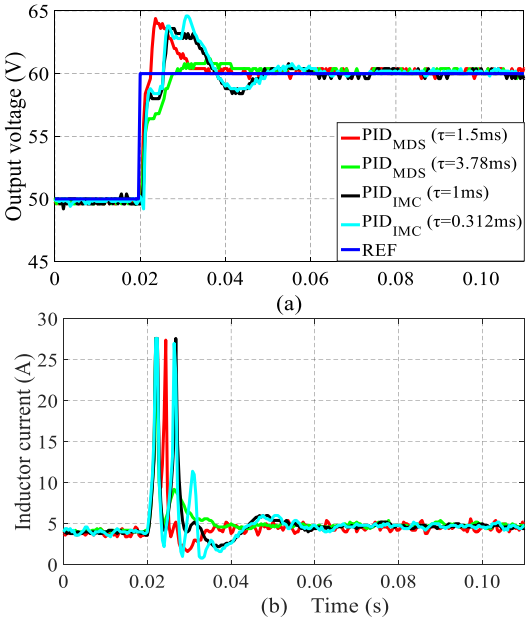

Fig. 15. Servo responses of PID controllers' in experiments for set-point voltage variation from $V_{oREF} = 50 \rightarrow 60$ V at nominal load and $V_i = 33.3$ V. (a) Output voltage. (b) Inductor current.

Also, for the set-point tracking, the response with MDS design reaches, quickly, the new desired operating output voltage with lesser deviation.

VI. Conclusion

In this article, the robust PID controller design based on the MDS approach for CCM-operated NMP dc–dc boost converter is proposed to regulate the output voltage using only sensed output voltage as feedback. The proposed MDS-based PID allowed the converter to operate close to the performance limits set by the RHP zero. The proposed MDS approach incorporates the converter transfer function model explicitly in the controller design procedure that reduces the laborious tuning of controller gains. Using the converter and the disturbance dynamic models, the desired response for the external variations can be effectively attenuated with the proposed MDS approach to achieve the desired closed-loop disturbance rejection response using only a single tuning parameter due to the usage of Bode's gain crossover frequency inequality. Both the simulation and experimental demonstrations illustrated that the proposed MDS-based PID design exhibits excellent disturbance rejection over the IMC-PID design. The significantly improved dynamic response with the proposed MDS-based PID design with less inductor current is the attractive feature of the presented work.

Appendix

The mathematical expressions are as follows:

$$K_c = \frac{(2\zeta\tau\theta + \tau^2)(3\tau_c + \theta) - \tau_c^3 - 3\tau_c^2\theta}{K(\tau_c + \theta)^3} \tag{A.1}$$

$$\tau_I = \frac{(2\zeta\tau\theta + \tau^2)(3\tau_c + \theta) - \tau_c^3 - 3\tau_c^2\theta}{\tau^2 + (2\zeta\tau + \theta)\theta} \tag{A.2}$$

$$\tau_D = \frac{3\tau_c^2\tau^2 + \tau^2\theta(3\tau_c + \theta) - (2\zeta\tau + \theta)\tau_c^3}{(2\zeta\tau\theta + \tau^2)(3\tau_c + \theta) - \tau_c^3 - 3\tau_c^2\theta}. \tag{A.3}$$

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