EXPLORATION OF LIQUID CRYSTAL POLYMER PACKAGING TECHNIQUES FOR RF WIRELESS SYSTEMS

A Dissertation
Presented to
The Academic Faculty

by

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In Partial Fulfillment
of the Requirements for the Degree
Doctor of Philosophy in the
School of Electrical and Computer Engineering

Georgia Institute of Technology
August 2012

EXPLORATION OF LIQUID CRYSTAL POLYMER PACKAGING TECHNIQUES FOR RF WIRELESS SYSTEMS

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“I find that the harder I work,

the more luck I seem to have.”

-Thomas Jefferson

“Insanity: doing the same thing over and over again

and expecting different results.”

-Albert Einstein

To my family and friends for their unwavering faith and support.

ACKNOWLEDGEMENTS

I would first like to thank Dr. John Papapolymerou and Dr. Gary May for their guidance and exemplary role as my Ph.D. advisors. John has taught me not only what it takes to become a research engineer but also the drive necessary to become successful in whatever endeavors I may encounter. Gary selflessly took me under his advisement so that I could pursue additional opportunities that invaluably expanded my breadth of research and business knowledge. I would like to thank them both for their faith and trust, which gave me freedom to pursue ideas in a creative manner.

I would also like to thank the additional members of my Ph.D. advisory committee, Dr. John Cressler, Dr. Andrew Peterson, Dr. Hua Wang and Dr. Christos Alexopoulos, who provided significant support and advisement during my graduate studies.

It has been a great honor and experience working with the entire MIRCTech team. I owe a debt of gratitude to the graduated members, Dr. Yuan Li, Dr. David Chung, Dr. Negar Tavassolian, Dr. Arnaud Amadjikpè, Dr. John Poh, and Dr. Eric Juntunen, for taking time to train me on cleanroom and laboratory equipment, and providing an invaluable depth of knowledge accessible in a moment's notice. I would also like to acknowledge the current team members, Dr. Benjamin Lacroix, Carlos Donado, Aida Vera, Wasif Khan, Spyridon Pavlidis, Fan Cai and Outmane Lemtiri, whose new ideas and problems have helped reinforce my current knowledge as well as inspired me to further explore innovative and interesting topics. Lastly of the MIRCTech team, I would

like to thank Dr. Swapan Bhattacharya for taking me under his wing at an early stage and instilling the hands-on fabrication knowledge required to propel my research activities.

I am also thankful to the members of Dr. Cressler's SiGe research group, with extra thanks to Dr. Tushar Thrivikraman. It was a wonderful experience working together and jointly developing projects into great successes. I must also add that the overly-generous access to their laboratory equipment was immensely helpful in expediting my work for a timely graduation.

I wish to acknowledge those individuals whom I closely collaborated with throughout the many projects I have been involved. I would like to especially thank Jack Ajoian from Lockheed Martin and Bill Wilson, Ted Heath, Sean Begley and Greg Hampton from the Georgia Tech Research Institute. I believe the milestones we achieved were a direct result of these highly talented individuals and an excellent synergy of technical backgrounds.

I want to recognize Lisa Gardner and Craig Cotton for finding time to assist me despite their busy schedules. I also wish to thank the cleanroom staff at Georgia Tech for fighting a never-ending battle to keep equipment functional and maintaining a pleasant work environment amid seeming chaos.

I would like to extend my most sincere thanks to the Beta Pi chapter of Tau Kappa Epsilon Fraternity at Georgia Tech for providing a positive personal and academic influence on my life. I would not be in the position I am today without the resources provided by my fraternity brothers and Board of Trustees.

I am grateful to my friends in Georgia and Maryland for providing a social outlet that seems all too vacant in the life of a graduate student. I would like to give a special

shout out to the *born ballas* and *steak night'ers* for their relentless complaints when I was too busy to hang out and for their 'positive' encouragement to shed my Peter Pan complex. I hope this dissertation serves as evidence to my excuse for sporadic absences and confirmation of my newly developed maturity.

Finally and most importantly, I would like to thank my family for believing in my determination to complete this seemingly endless feat. They have supported me emotionally and financially throughout my entire academic career. I am forever indebted to my mother, Gail Patterson, for literally giving me the clothes on my back. She has been an unwavering fan and personal confidante. I also owe my siblings, Sarah Patterson, Shannon Palik and Brian Patterson, a great deal for always taking an interest in my endeavors and offering their encouragement throughout the years. I would like to especially thank my father, Michael Patterson, and uncle, Col. Jerry Patterson, for inspiring me to excel in academia and encouraging me to follow it through to completion. I am also grateful to my beautiful girlfriend, Robyn, for her patience and support. Like a true chip off the old block, I needed someone to push me out of my comfort zone and to compel me into bringing my graduate studies to a conclusion, which she seemingly did all too easily.

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NOMENCLATURE

List of Symbols

Å	Angstrom (1×10^{-10} m)
°C	Degree Celsius
ε_r	Relative Permittivity
µm	Micrometer
µF	Microfarad
Ω	Ohm
σ_c	Conductivity
A	Amp
cm	Centimeter
dB	Decibel
dBm	Decibel referenced to 1 milliwatt
GHz	Gigahertz
Hz	Hertz
kHz	Kilohertz
K	Kelvin
m	Meter
mm	Millimeter
mW	Milliwatt
MHz	Megahertz
oz	Ounce
PSI	Pounds Per Inch^2

S	Siemens
tanδ	Loss tangent
V	Volt
W	Watt
Z_0	Characteristic Impedance

List of Abbreviations

2-D	Two Dimensional
3-D	Three Dimensional
3G	Third Generation
Ag	Silver
ADS	Advanced Design System
AoC	Antenna on Chip
Au	Gold
AUT	Antenna Under Test
AWG	American Wire Gauge
BAW	Bulk Acoustic Waveguide
BCB	Benzocyclobutene
BFN	Beam Forming Network
BiCMOS	Bipolar Complementary Metal Oxide Semiconductor
BP	Bondply
BT	Bismaleimide-Triazine
BW	Bandwidth
C4	Controlled Collapse Chip Connection
C band	4 GHz to 8 GHz
CMM	Coordinate Measuring Machine

CMOS	Complementary Metal Oxide Semiconductor
CPS	Coplanar Strip
CPW	Coplanar Waveguide
CPW-G	Grounded Coplanar Waveguide
CSLP	Chip Scale Level Package
CTE	Coefficient of Thermal Expansion
Cu	Copper
DC	Direct Current
DUT	Device Under Test
ESD	Electrostatic Discharge
FOM	Figure of Merit
FR-4	Flame Retardant 4
GaAs	Gallium Arsenide
GPS	Global Position System
GSG	Ground-Signal-Ground
GSGSG	Ground-Signal-Ground-Signal-Ground
HBT	Heterojunction Bipolar Transistor
HDI	High Density Interconnect
HFSS	High Frequency Structure Simulator
HTCC	High Temperature Co-Fired Ceramic
IC	Integrated Circuit
IEEE	Institute of Electrical and Electronics Engineers
I/O	Input/Output
IPA	Isopropyl Alcohol
K band	18 GHz to 26.5 GHz

K_a band	26.5 GHz to 40 GHz
K_u band	12 GHz to 18 GHz
KrF	Krypton Fluoride
LCP	Liquid Crystal Polymer
LNA	Low-Noise Amplifier
LTCC	Low Temperature Co-Fired Ceramic
MCM	Multi-Chip Module
Mo	Molybdenum
NF	Noise Figure
NHA	Next Higher Assembly
Ni	Nickel
P_{1dB}	1 dB Power Compression Point
PA	Power Amplifier
PAE	Power-Added Efficiency
PCB	Printed Circuit Board
P_{out}	Output Power
PS	Phase Shifter
P_{sat}	Saturated Output Power
PTFE	Polytetrafluoroethylene
Q	Quality
RIE	Reactive Ion Etching
RF	Radio Frequency
RMS	Root Mean Square
RRP	Risk-Reduction Panel
SiC	Silicon Carbide

SiGe	Silicon Germanium
SIP	Stacked Integrated Circuit and Package
SIW	Substrate Integrated Waveguide
SMR	Surface Mounted Resonator
Sn	Tin
SoC	System on Chip
SoP	System on Package
S-Parameters	Scattering Parameters
SPDT	Single Pole Double Throw
T/R	Transmit/Receive
Ti	Titanium
TRM	Transmit/Receive Module
TSV	Through-Silicon Via
UV	Ultra Violet
VCO	Voltage-Controlled Oscillator
V band	55 GHz to 75 GHz
VSWR	Voltage Standing Wave Ratio
W	Tungsten
W band	75 GHz to 110 GHz
X band	8 GHz to 12 GHz

SUMMARY

In the past decade, there has been an increased interest in low-cost, low-power, high data rate wireless systems for both commercial and defense applications. Some of these include air defense systems, remote sensing radars, and communication systems that are used for unmanned aerial vehicles, ground vehicles, and even the individual consumer. All of these applications require state-of-the-art technologies to push the limits on several design factors such as functionality, weight, size, conformity, and performance while remaining cost effective. There are several potential solutions to accomplish these objectives and a highly pursued path is through the utilization of advanced integrated system platforms with high frequency, versatile, multilayered materials.

Many new materials are being explored for advanced package design that are thinner, lighter, and have better high frequency characteristics that make a wider range of applications possible. Liquid Crystal Polymer (LCP) has been established as an excellent microwave organic dielectric due to its key performance and packaging advantages. It has been shown that LCP is a prime candidate for integration of active circuits in 2-D and 3-D packaging configurations. Additionally, its large processing format and compatibility with the build-up process in a printed circuit board foundry allows for a smooth transition to commercialization of products.

This work intends to explore advanced 3-D integration for state-of-the-art components in wireless systems using LCP multilayer organic platforms. Several packaging techniques are discussed that utilize the inherent benefits of this material. Wire bond, via interconnect, and flip-chip packages are implemented at RF and millimeter-wave (mm-wave) frequencies to explore the benefits of each in terms of convenience, reliability, cost, and performance. These techniques are then utilized for the

demonstration of bulk acoustic waveguide (BAW) filter applications and for the realization of highly integrated phased-array antenna systems.

A combination of flip-chip and via interconnects are applied to the integration of state-of-the-art BAW filter technology with LCP packaging. The hermetic nature of LCP is utilized to prevent moisture absorption from degrading RF performance by use of a solder ring die attachment. Additionally, via interconnects route the signal directly from the chip interface to matching networks implemented on package for a 50 Ω impedance matching. For the first time ever, this packaging approach is demonstrated at C-band and K_u-band frequencies.

This work also investigates the possible applications for LCP platforms where the benefits of this material can be exploited for highly integrated wireless antenna systems. Active and passive components are incorporated on LCP using a system-on-package approach to improve performance and enhance capability of the antenna. Wire bond interconnects are utilized as a convenient, low-cost packaging solution, ideal for prototype development. The demonstration of several prototype antennas at X-band and V-band frequencies provide substantial evidence as to the broad range of potential applications for LCP.

CHAPTER 1

INTRODUCTION

The current pace of RF technology development and innovation is in response to market pressures for miniaturization, with increased functionality at lower costs. This rapidly growing facet of the electronics industry is especially apparent in wireless systems. In the last decade, there has been substantial growth in communication devices, anti-collision radars, remote sensing, and satellite communication and navigation systems. Many of these technology advancements have now become fundamental components of day-to-day operation for the average consumer. These include global positioning system (GPS) devices (1 GHz to 2 GHz), smart phones (0.6 GHz to 2.7 GHz), automobile collision avoidance radars (24 GHz and 77 GHz), and satellite television (10 GHz to 13 GHz).

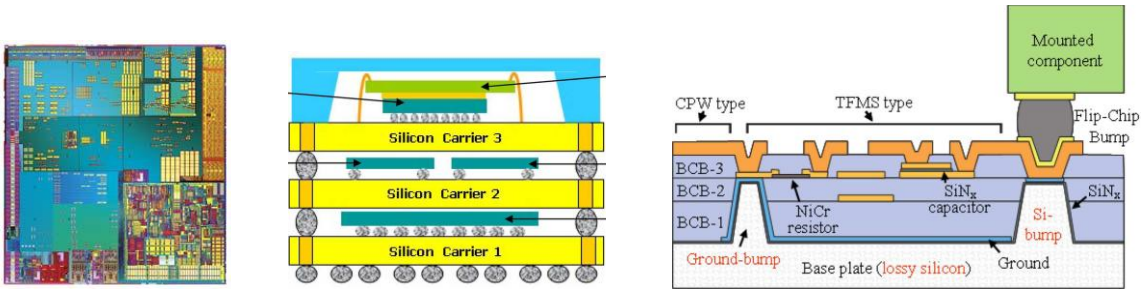
Portable wireless devices have experienced a boom in consumer popularity with an overwhelming necessity for instant data, voice, and video access. This spark in demand has been met by the electronics industry with new and innovative technologies that push the current state-of-the-art performance and functionality in a cost-effective manner. For example, in 2001, third-generation (3G) mobile telecommunication networks gave birth to wireless internet access, video calling and media streaming to cell phones, personal digital assistants, and laptop computers. Since then, smart phones, iPads, and tablet personal computers have been developed that are not only smaller than their predecessors in size and profile, but also packed with additional functionality, such as multitask software applications, GPS, high-definition photo/video cameras, and data storage. With the growth in smart phone sales up to over 303 million units in 2010 and a forecasted 49 % growth in sales for 2011, there is a clear financial interest driving the RF component in this market [1].

In addition to packed functionality, the electronics industry is coming up with innovative ways to replace current radar and communication systems with ones that are lighter, lower power, and more adaptable [2]. In the past, these have consisted of heavy, bulky, and expensive waveguide feed networks and antenna arrays [3]-[5]. This type of system is costly and impractical for applications where mobility is required. Added weight and bulk to airborne and ground vehicles reduces maneuverability, increases air drag, and raises gas consumption. An innovative way to eliminate a large portion of the weight, size, and cost is by utilizing microstrip technology on lightweight, flexible, high frequency substrates.

Products of this complexity require advanced RF designs and highly integrated system platforms that can be manufactured at low costs. Hundreds of electronic components must be seamlessly interconnected into a low form factor device, which presents an enormous challenge from an electrical and mechanical standpoint. In addition to dense complex interconnections, concerns of weight, reliability, and RF performance must be addressed. Response to these hurdles has fostered advanced packaging techniques utilizing low-cost, high frequency, versatile materials [6]-[8].

1.1 Background on Advanced Package Technologies

The primary focus of today's wireless systems are component integration, size miniaturization, cost reduction, reliability increase, and performance enhancement; all of which are largely handled in part by the system package design. In order to achieve these objectives, advanced packaging techniques have been developed that replace traditional bulky package configurations. These concepts include system-on-chip (SoC), stacked integrated circuits (ICs) and packages (SIP), and system-on-package (SoP) technologies, illustrated in Figure 1.1. The term "system" refers to everything required for device operation, including the digital and analog circuitry, embedded software, thermal coupling structures, and power sources.



(a) (b) (c)

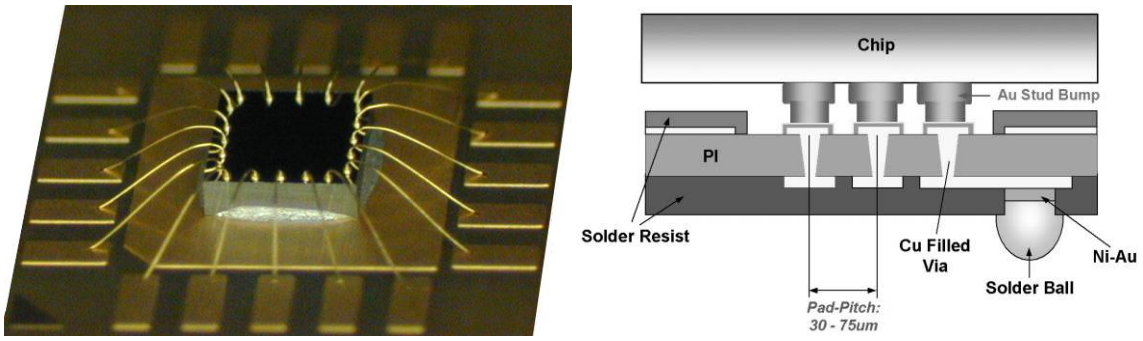
Figure 1.1: Advanced packaging techniques: a.) system-on-chip [9], b.) stacked ICs and packages [10], c.) system-on-package [11].

The simplest packaging approach is the integration of the system onto a single chip (SoC). This offers compact size and high performance functionality capable of mass production. However, this technology limits the system to a single substrate platform, which causes long design times due to complex function integration, noise coupling issues, and mixed-signal processing complexities [12]. Additionally, the inclusion of passive circuitry on chip significantly increases the die footprint; inflating fabrication costs.

SIP and SoP technologies address many of these disadvantages through multi-functional integration at the package level, rather than at the chip level. The degree of freedom realized at the package level allows for multi-chip integration at a higher performance/cost index than SoC technologies [13]. With SIP technology, multiple ICs or chip packages are integrated into a single package through chip stacking and are interconnected using wire bonds, flip-chip bonding, or through-silicon vias (TSV). This approach enables differing semiconductor platforms to be exploited in the system, greatly simplifying design complexity [14]. SIP uses the package solely for inter-chip connection; however, SoP technology takes system integration even further by incorporating functionality into the package itself. In this manner, the system platform is utilized as the IC packaging substrate. Many system components, traditionally integrated on chip, are embedded into the package, taking advantage of the substrate high frequency

electrical properties [15]. By utilizing low-loss packaging substrates, high quality-factor (Q-factor) passive components can be achieved, which is not easily realized on lossy chip substrates. The relocation of system components off chip greatly reduces the chip size, saving fabrication costs significantly. Furthermore, this packaging technology enables the inherent benefit of chip and package substrates to be better utilized and co-designed for their respective strengths. Traditionally, the advantages of IC design reside within transistor integration, while the advantages of package design are in analog and digital component integration [16], [17].

There are several technologies available for integration of passive and active ICs into the system platform. Conventional methods make use of wire bonds and flip chip, which are proven to be easy and effective, with relatively low loss [18]-[20]. Wire bonding remains the most commonly used and flexible type of interconnecting technology, shown in Figure 1.2(a). It is low cost and very easily re-worked; however, it incurs high parasitic losses due to large loop inductances caused by long wire lengths. It is also limited to a 2-D package topology, which restricts input/output (I/O) interconnect density, taking up valuable real estate. These limitations can be overcome through the use of flip-chip technology, shown in Figure 1.2(b). Parasitic losses and package footprint sizes are reduced by replacing long wire lengths with solder bumps. Additionally, high density interconnects (HDIs) are used on package to achieve very fine pitched traces and micro-vias down to 30 μm [21], [22]. This increase in number of chip interconnects has become critical in supporting higher power requirements, bandwidths, and data rates. However, the disadvantages of this technology are higher costs, limited re-workability, and its susceptibility to interconnect failure from thermal and mechanical stresses [23], [24].



(a) (b)

Figure 1.2: Package interconnects utilized in IC integration: a.) wire bonds, b.) flip chip with HDIs [22].

One possible option for further improvement in parasitic losses and miniaturization for these package technologies is embedding chips within the core of the package. Conceptually, embedding active components can be encompassed by three major categories: (i) cavity formation to the dimension of the chip, (ii) lamination of chips within multilayer laminated sheets, and (iii) over-molding upon placement of the chips on the surface of the package. Significant research has been published in the past 5 years toward embedding chips using ceramic substrates and other platforms [25]. Aside from the improvement in parasitic losses, a clear advantage in embedding actives is the reduced thickness of the package and slim form factor.

1.2 Radio-Frequency Substrates for System-on-Package Technology

For SoP design, the platform substrate must not only maintain excellent high frequency electrical properties, but also be suitable for versatile package integration and remain cost effective. There are two categories of materials fitting this profile that have become leaders in the packaging industry: ceramic substrates and organic substrates. Until recently, ceramic substrates have been widely established as the leading material in microelectronic packages, sensors, and passive components. Ceramic materials have long been favored because of their high reliability, multilayer thin-film processing (>50

layers), endurance to harsh environments, and low fabrication costs [26]-[28]. These substrates are typically comprised of multilayered aluminum oxide material, engineered to co-fire at temperatures around 1500 °C. Lamination occurs in one fluent step, which hardens and bonds the substrate and metal layers together into a planar rigid platform. Ceramics of this composition are known as high temperature co-fired ceramics (HTCC). Due to the high firing temperatures of HTCC, high temperature metals such as tungsten (W) and molybdenum (Mo) are used, which limits this material to low RF applications because of their low conductivity [27]. As the electronics market pushed for high frequency applications, low temperature co-fired ceramics (LTCC) were developed from a hybrid ceramic-organic composition, which lowered the firing temperature to 850 °C [29]-[30]. This allowed highly conductive metals like silver (Ag) and gold (Au) to be used, which in conjunction with low-loss LTCC, enabled high RF performance up to millimeter-wave (mm-wave) applications. LTCC has since become the favored ceramic substrate; however, this material is twice the cost of HTCC and has additional complexities of design and fabrication due to a 10 % to 20 % size shrinkage that occurs after firing [31].

In the last decade, organics have become a primary candidate, as they are a low-cost replacement of the standard high performance ceramic materials, exhibiting potential as the next generation technology for SoP wireless systems. Several disadvantages inherent in LTCC technology are resolved by the use of organic substrates. These include the high material costs, material shrinkage after lamination, and high processing temperatures that are incompatible with active chip embedding. For this reason, there have been studies on embedding active circuits with low-cost organic materials that have excellent performance up to mm-wave frequencies and do not have the manufacturing and cost limitations of ceramic substrates. Table 1.1 shows a comparison of material properties for LTCC with several alternative organic materials: Flame Resistant 4 (FR-4), Polytetrafluoroethylene (PTFE or Teflon), and Liquid Crystal Polymer (LCP).

Table 1.1

Comparison of material properties for RF substrates

Material Characteristics		**LTCC**	**FR-4**	**PTFE**	**LCP**
ε_r @ 10 GHz		4.3 to 9.1	3.8 to 4.5	2.08 to 2.3	2.9
tanδ ($1x10^{-3}$) @ 10 GHz		1 to 4.5	16	0.6 to 1.1	2.5
Min Layer Thickness (μm)		12.5	60	125	25
CTE (ppm/°C), [x,y,z]		3 to 7	14, 13, 175	25, 35, 260	17, 17, 150
Conductor Material	Internal	Ag	Ag, Au, Cu	Ag, Au, Cu	Ag, Au, Cu
	External	Ag, Au	Ag, Au, Cu	Ag, Au, Cu	Ag, Au, Cu
Processing Temperature (°C)		850	185	<285	<300
Thermal Conductivity (W/m·K)		2 to 4	0.27	0.62	0.5
Moisture Absorption (%)		<0.1	<0.25	0.02	0.04
Density (g/cm^3)		3.1	1.85	1.9	1.4

Sources: [29]-[32], [34], [36]

FR-4 is a commonly used printed circuit board (PCB) material. It is very low cost with high mechanical strength and good electrical insulation suitable for applications up to 10 GHz [32]-[33]. However, for applications above 10 GHz, this material exhibits very high losses, which can quickly outweigh its low-cost advantages. PTFE is a low-loss material also used in PCB manufacturing [34]. While this material has excellent RF performance, it is more expensive than the other organic materials and has difficulties in multilayer processing. Additionally, there are issues with circuit failure due to the high coefficient of thermal expansion (CTE) for this material, which causes de-lamination of metal layers during thermal cycling.

In recent years, LCP has been established as an exceptional microwave organic dielectric due to its key performance and packaging advantages [35]-[36]. It has many

favorable characteristics that make it easy to employ while maintaining excellent performance. There is an abundance of literature investigating the benefits of LCP including [37]-[44]; some key advantages are listed below:

- Superior cost/performance index
- Flexibility for application in conformal flex circuits
- Low permittivity and dielectric loss with minimum dispersion up to 110 GHz
- Low CTE compatible with Ag, Cu, and Au
- Near-hermetic
- Naturally flame retardant
- 3-D multilayer integration
- Compatible with sequential build up process in a PCB Foundry

LCP is now established as a low-cost material with excellent high frequency electrical properties extending well into the mm-wave band. Its low dielectric constant (ε_r = 2.9 @ 10 GHz), low loss tangent ($\tan\delta$ = 0.0025), and near-hermetic nature make it an outstanding material for high frequency applications. Its strong packaging properties also give it an edge over competing materials. It is a lightweight, conformal composition with density of 1.4 g/cm^3, which is less than half that of ceramics. It is also naturally flame retardant, which allows for convenient laser patterning of vias and cavities, and requires low temperature (less than 300 °C) processing for multilayer lamination, making IC embedding possible. The combination of these inherent properties allows a 3-D packaging capability on a conformal platform capable of being mounted to almost any surface (aircraft wing, boat hull, car roof, etc.).

1.3 Background on LCP Fabrication

In addition to evaluating the substrate electrical and mechanical properties optimal for a given application, fabrication limitations must also be considered. The product size, reliability, performance, and cost will all be greatly affected by the

capability of the fabrication vendor. This becomes especially apparent at mm-wave frequencies where the physical dimensions of the module tend to shrink in size to maintain acceptable performance. Optimally, very thin substrates with a low permittivity are desired to provide small feature sizes for reduced module size and, ultimately, reduced cost, while also providing the highest performance. Additionally, for high-quantity productions, fabrication can quickly become a dominant cost contributor, which makes the number of units produced per fabrication run a very important issue. Large-panel processing compatible with a PCB infrastructure enables a low cost solution with inexpensive fabrication and fewer production runs.

Table 1.2 shows state-of-the-art commercial fabrication capabilities for multilayer ceramic and organic stackups. LTCC and FR-4 materials have been developed over the last two decades into very mature technologies, while LCP is a relatively newer technology that has entered into commercial fabrication only in the last decade. LCP has a limited number of layers compared to other materials because it is an unfilled material with no reinforcement (fiberglass weave or ceramic particles); however, this also allows the creation of high-aspect ratio vias. The fabrication design rules for this material maintain very small line widths/spaces and via diameter/pitch, which allows highly condensed line routing and via interconnects. Additionally, LCP is processed in large-panels comparable to FR-4. This not only allows batch production of devices, but also the realization of large area, multi-element antenna arrays not feasibly fabricated on the limited panel size of LTCC.

Table 1.2

Design rules for commercial multilayer fabrication

Guidelines		**LTCC**	**FR-4**	**LCP**
Minimum Layer Thickness (µm)		12.5	60	25
Minimum Line Widths / Spaces (µm)	External	75 / 75	75 / 75	50 / 50
	Internal	75 / 75	50 / 75	40 / 50
Minimum Via Diameter / Pitch (µm)		100 / 300	150 / 250	25 / 200
Panel Size (mm^2)		200 x 200	570 x 570	450 x 600
Maximum Layer Count		25	70+	7
Technology Maturity		High	High	Medium

Sources: [36], [45], [46]

LCP has been proven as a viable substitute for competing substrates; however, fabrication limitations have not yet been fully analyzed with regard to RF performance yield. There is currently very little published on large-scale LCP manufacturability. The following sections outline the fundamental considerations of substrate fabrication and describe the added complexities when implementing LCP.

1.3.1 Material Thickness

LCP core material (ULTRALAM® 3850), double clad, is available in 25 µm, 50 µm, and 100 µm thicknesses with copper foil available down to 9 µm thick. LCP Bondply (ULTRALAM® 3908) is available in 25 µm and 50 µm thicknesses and is used to bond core layers together. The material manufacturer of LCP used in this thesis, Rogers Corporation, guarantees the product to be within ±12.5 % of the specified thickness. During the lamination process, the material stack-up is brought to a temperature of 285 °C under a pressure of 300 pounds per $inch^2$ (PSI), allowing the Bondply layers to flow and adhere to the adjacent core layers. Consequently, during this

process it has been observed that the LCP core layers will slightly compress, yielding a thickness less than what is expected. In addition, as the material stack-up increases in thickness, a larger temperature gradient across the layers will occur, causing the external layers to be exposed to higher temperatures than the internal layers. This temperature gradient can ultimately cause varying compression in the z-axis between layers. Considering all variations, it is expected that increasing the number of LCP layers during lamination will make the total thickness tolerance greater and more difficult to predict.

1.3.2 Registration Error

Layer-to-layer registration is a challenge using any substrate technology process and/or material. This obstacle is exacerbated when using LCP because of its inherent un-filled, un-reinforced state, which enables its excellent electrical properties (low loss, low dielectric constant, and high moisture resistance) but consequently allows the material to 'swim' during the lamination cycle. This results in a steep learning curve for process development; the amount of controllable registration error between layers directly impacts the sizing of via catch pads, which can have degrading effects on RF performance in layer-to-layer transitions. Catch pad sizing, and even more so, RF via transition designs can ultimately be the limiting factors in routing density; isolation also being of primary concern.

1.3.3 Minimum Feature Size

Utilizing thin LCP laminates of 25 µm, 50 µm, or 100 µm thicknesses for package substrates requires maintaining a 50 Ω system impedance. It has been shown in Table 1.2 that commercial fabrication is limited to lines and spaces down to 50 µm. These capabilities are heavily dependent on copper thickness and typically presume ¼ or ½ oz copper. For optimized performance and producibility, it is essential to design all transmission lines to be as wide as possible while maintaining 50 Ω system impedance.

Furthermore, as 50 µm or smaller lines and spaces are approached, the fixed etch tolerance becomes a significant percentage of the feature size and the RF performance must sustain fabrication tolerances. As the minimum feature size is pushed to its limit, the accuracy of line widths and gaps becomes harder to control. Small variations can have a large effect on line impedances and overall matching in the design. Finish plating will also play an important role in feature resolution and assembly compatibility at the package level and should be considered early in the design phase.

Another important feature for wide-band RF transitions and increased routing density is the use of micro-vias. Aspect ratio, the measure of via diameter with respect to drill depth, for micro-vias is 2:1 across the industry for laminate PCB substrates. Micro-vias are drilled using either a UV or CO_2 laser, or often combinations of both, yielding precision depth-controlled interconnect vias and cavities. Decreasing the aspect ratio enables two key parameters: 1) reduced via diameter, which favorably increases inductance and concurrently reduces via catch-pad diameters that are the dominant capacitive features allowing for a better RF match, and 2) ground stitching (fence of ground vias) between adjacent RF transmission lines for isolation, thus smaller via sizes can accommodate finer RF IC interconnect pitch.

CHAPTER 2

SYSTEM-ON-PACKAGE MODULES ON LCP

Comprehensive research and prototypes have been published leading to the realization of embedded RF components and devices in LCP packages [43], [47]-[49]. In an effort to better understand the extent of LCP packaging capabilities at microwave and mm-wave frequencies, several packaging methods have been explored. Special techniques are utilized to minimize RF parasitics incurred through the package interconnects. The aim is to offer high performance integration for low-cost and lightweight applications. The advantages of silicon-based chips, combined with the packaging versatility of LCP, provide a unique opportunity for organic based RF SoP solutions. These investigations are discussed in this chapter.

2.1 Embedded Wire Bond Package at K_a Band

For state-of-the-art proof-of-concept applications, the flexibility for last-second modifications to the circuit module can be crucial for success. Often, it is necessary to incorporate wire bond packaging to enable this flexibility even at mm-wave frequencies where RF parasitics run the potential of degrading performance. Such occurrences require die-embedding techniques to minimize packaging parasitics. LCP has many favorable characteristics that make it easy to utilize while maintaining excellent performance, which makes it a strong candidate as a wire bond packaging material for mm-wave applications. In this section, a silicon-germanium (SiGe) voltage-controlled oscillator (VCO) that has been embedded into an LCP organic material that acts both as substrate and package is described [50].

2.1.1 Circuit Description

The packaged circuit demonstrated is a voltage controlled oscillator operating at the upper end of K_a band. Shown in Figure 2.1, the oscillator uses a cross-coupled negative resistance topology implemented in IBM's third generation SiGe technology node. The differentially configured common emitter stage creates a negative resistance across the collectors of the two HBT's by steering current back and forth between them. The circuit is made unstable by cross-coupling the base contacts to the opposing collector, ensuring that as random noise steers the current toward one transistor, the bias point of the opposite transistor increases steering the current back in the other direction. This oscillation will increase until the non-linearities of the transistor decrease the current gain to an equilibrium condition with the resonator.

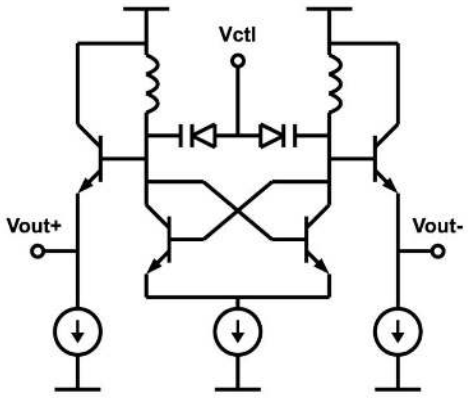


Figure 2.1: Schematic of the negative resistance oscillator.

The negative resistance generated by the transistor pair is used to offset the loss of the resonator tank. The resonator sets the oscillation frequency of the VCO. In this circuit, the resonator is formed monolithically using a combination of varactors and metal lines. Adjusting the control voltage varies the effective capacitance of the varactor and adjusts the resonant frequency of the tank. The high impedance lines on the thick analog metal layer act as inductors with a much higher self resonant frequency than traditional spiral inductors. These state-of-the-art passive elements allow the circuit to push the

frequency limits of this design topology. Emitter-follower buffers are used to extract the signal with minimal loading of the resonant tank. Since these buffers need to drive an inductive load in the form of package bond wires, care must be taken in the design to ensure that the amplifier is stable by adjusting the bias current and emitter scaling.

The VCO circuit was diced from its original wafer using a soft cutting blade with a 50 µm width. It was necessary to dice the chip as small as possible without damaging it in order to reduce wire bond lengths. After dicing, the chip dimensions measured 550 µm x 850 µm x 525 µm. For best packaging results, the dimensions of the cavity produced for mounting this chip will be approximately the same, but slightly larger, to allow for any errors. Before packaging, the VCO was measured on chip to ensure its integrity.

When measured at the wafer level without the package, the circuit achieves an output power of -13.6 dBm, with a phase noise of -94 dBc/Hz at a 1 MHz offset from the carrier frequency. The VCO has a tuning range of over 1 GHz, from 36.5 GHz to 37.8 GHz. The measured oscillation frequency represents a 5 % downward shift despite complete parasitic extraction during design. The VCO and buffer combined draw 13 mA on a 1.2 V supply. It is often convenient to combine several of these metrics into a common figure of merit that can be used to compare performance on an equal footing. A commonly used figure of merit to normalize phase noise is defined as

$$FOM = \Phi_n(f_m) - 20log\left(\frac{f_0}{f_m}\right) + 10log\left(\frac{P_{diss}}{1mW}\right) \quad (2.1)$$

where $\Phi_n(f_m)$ is the measured phase noise at a given offset frequency, f_m [51]. The oscillation frequency and DC power dissipation are represented by f_0 and P_{diss} respectively. Using this standard, the design shown here has a -173.7 dBc/Hz figure of merit.

2.1.2 LCP Package Development

A 200 µm thick sheet of LCP with double copper laminated (metal thickness of 18 µm) is used for the package substrate. This is the thickest form of LCP commercially

supplied. In order to minimize wire bond lengths of the package, the chip is embedded into a cavity drilled in the LCP. The effect of the bond wires were simulated in a full 3-D EM model using Ansoft High Frequency Structure Simulator (HFSS), as shown in Figure 2.2. This model uses an on-chip reference with wire bonds connecting from chip pads to 50 Ω coplanar waveguide (CPW) lines on LCP. The CPW line has 90 µm line widths and spaces. The resulting simulation data was then imported into the Cadence design environment for integration with the nonlinear active models provided by the foundry.

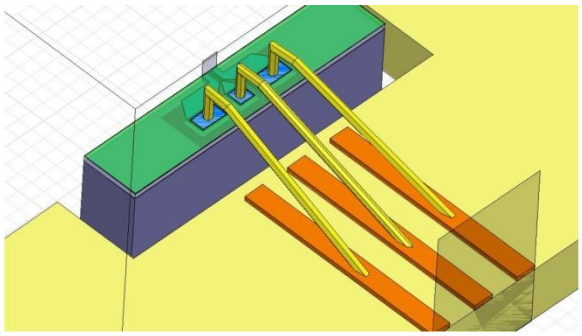
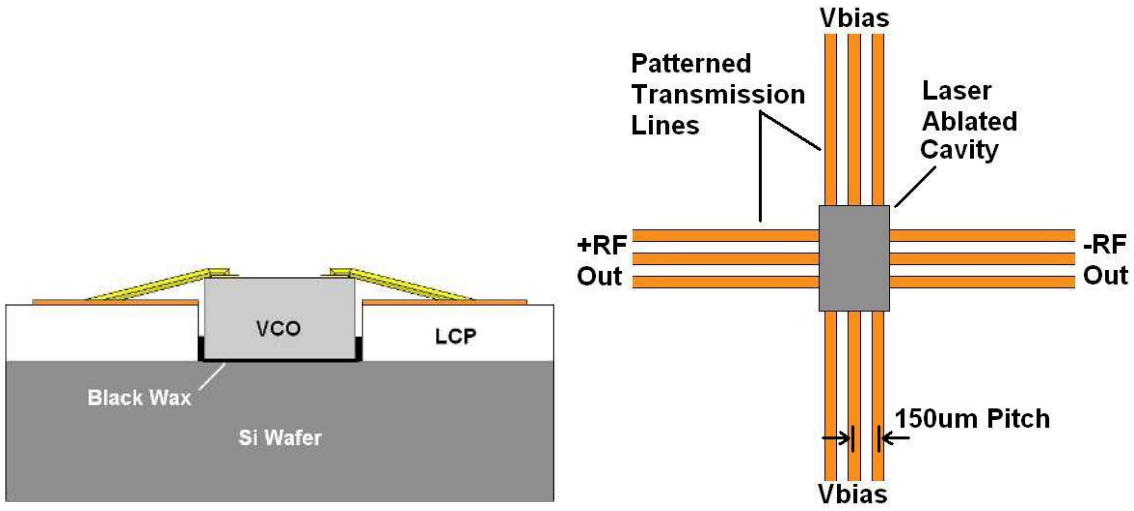


Figure 2.2: Simulation of the LCP package.

The final package design is shown in Figure 2.3. This uses a laser ablated cavity with dimensions of 600 µm x 880 µm. There were two possible ways to wire bond the VCO to the packaging: ball bonding and wedge bonding. Both types of bonding use a combination of pressure, heat and ultrasonic energy to make a weld. However, wedge bonding is capable of creating a nearly flat wire from bond to bond. This becomes very important when minimizing the length of bond wire.

The wire bonds were done using a wedge wire bonder utilizing a 38 µm diameter gold bond wire. By using the wedge wire bonder, lengths of the wire bonds are minimal. The longest bond wire length was about 700 µm and the average length was about 550 µm. This helped to reduce the parasitic effects that are produced by this type of packaging. An image of the packaged circuit can be seen in Figure 2.4.



(a) (b)

Figure 2.3: a.) Cross-section and b.) Overhead view of the wire bond VCO package.

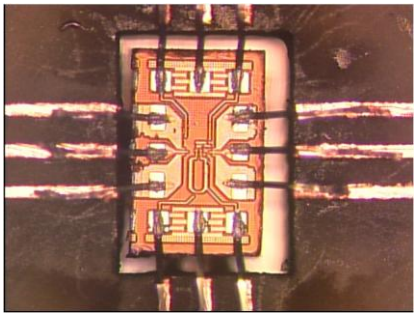
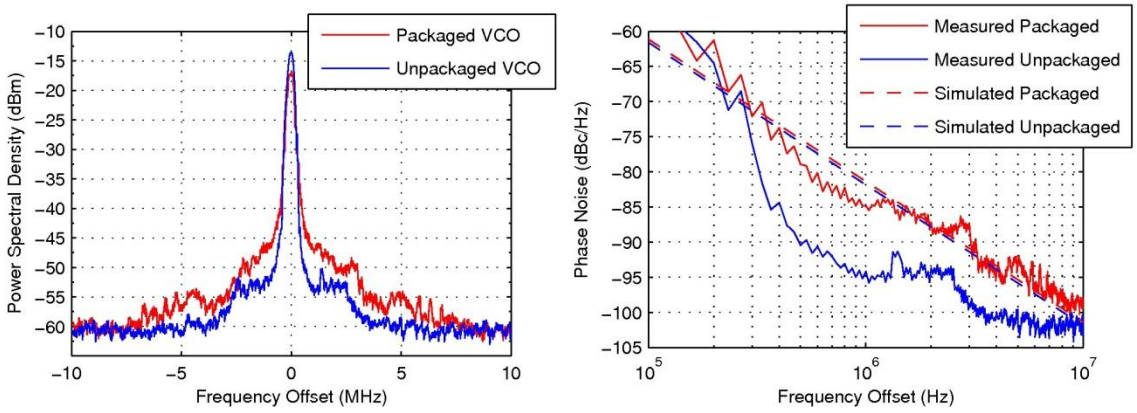


Figure 2.4: Die photograph of the packaged oscillator.

2.1.3 Measured Performance

Measurements of both the wafer level and package level oscillators were done on an Agilent E4446A spectrum analyzer. A K_a-band rat race coupler and phase tuners were used to combine the differential signal into single ended for measurement. A plot of the output spectrum of the packaged oscillator with respect to the unpackaged performance can be seen in Figure 2.5(a). Note that the x axis has been normalized to the oscillation frequency. The increased parasitics of the packaged part causes an additional 1.9 % shift in oscillation frequency. The output spectrums are overlaid to give a sense of the package

loss and increased noise. The results show that the output power of the packaged part is 3 dB down from that of the unpackaged part, while the sidebands of the signal are noticeably higher in the packaged part. The tuning range of the VCO also suffers when packaged, decreasing by an order of magnitude from over 1 GHz to around 100 MHz. This also is caused by the increased parasitics that are largely inductive because of the bond wires. The increased inductance adds with the existing inductance and decreases the influence of the varactors on the tank circuit. The effect is large because the element values are small at K_a band.



(a) (b)

Figure 2.5: a.) Output spectrum and b.) Phase noise of the packaged and unpackaged VCO.

Phase noise of the VCO was estimated from the spectrum. Without the proper equipment to lock the signal, attempts at using the built-in phase noise personality of the spectrum analyzer would be invalid. The phase noise was conducted under battery power rather than a wall powered DC source to eliminate as much low frequency noise as possible. Measurements were conducted in a shielded room with large decoupling capacitors on all of the supply lines. The signal was measured at a resolution bandwidth of 300 kHz and a video bandwidth of 3 kHz to average out the free running oscillator bounce as best as possible. The measured value of the packaged VCO came to -83.5

dBc/Hz at 1 MHz offset, which matches very closely with simulation, but is almost a 10 dB degradation from the unpackaged circuit. The measurement was targeted to give an accurate estimate of phase noise at a 1 MHz offset. Figure 2.5(b) shows the measured packaged and unpackaged VCOs compared to their simulation counterparts. The measured phase noise of the unpackaged VCO actually outperforms the simulated values at 1 MHz offset, which may be an anomaly.

The figure of merit for the packaged oscillator is calculated to be -160.16 dBc/Hz. This degradation from the unpackaged circuit is almost entirely caused by the change in phase noise measurement. Table 2.1 summarizes the difference between the packaged and unpackaged circuit.

Table 2.1

Performance summary of the packaged and unpackaged VCO

Performance	**Packaged VCO**	**Unpackaged VCO**
Output Power	-16.87 dBm	-13.64 dBm
Tuning Range	36.25 GHz to 36.55 GHz	36.5 GHz to 37.8 GHz
Phase Noise @ 1 MHz Offset	-83.5 dBc/Hz	-94.2 dBc/Hz
Current Draw on a 1.2 V supply	23 mA	13 mA
Figure of Merit	-173.7 dBc/Hz	-160.3 dBc/Hz

2.1.4 Discussion

A mm-wave SiGe oscillator was successfully packaged using an LCP organic material for the first time while maintaining a high performance profile. In order to reduce the parasitic effects introduced by the package, an embedding technique is utilized to minimize the wire bond interconnect length. Measurements after packaging showed a figure of merit 13 dB down from the on-chip measurements. Much of this degradation in

oscillator performance was expected due to the wire bond connections. However, this can be improved by using a thicker LCP laminated substrate, comparable to the chip height (525 µm), to further minimize wire bond length or by implementing an impedance matching network to compensate for the added parasitics.

It is apparent that the decision to use wire bond packaging at mm-wave frequencies must be weighed with the convenience and re-workability versus its inherent more lossy performance compared with other packaging processes. For applications requiring lower loss and condensed package interconnects, the inherent packaging characteristics of LCP can offer additional solutions.

2.2 Embedded Via Interconnect Package at X Band

A novel technique to minimize package parasitics is utilizing via technology for direct interconnect between the package and chip. Interconnect structures are fabricated by placing a dielectric layer directly over the chip and opening vias down to the necessary chip pads. This technique has been successfully demonstrated with various dielectric materials [47], [52]. LCP would be an excellent candidate for this type of SoP technology considering its distinctive 3-D packaging capabilities. In this section, an X-band SiGe low-noise amplifier (LNA) has been embedded in LCP with interconnecting vias for the first time [53]. This integration technique is a hybrid wafer-level packaging scheme that can lead to low-cost 3-D SoP RF front ends with excellent performance at microwave and, eventually, mm-wave bands.

2.2.1 Circuit Description

The packaged LNA die was fabricated in a 0.13 µm BiCMOS SiGe technology and designed using the inductively degenerated cascode architecture. The circuit was designed for ultra-low power operation, consuming less than 2 mW of DC power from a 1.5 V supply. The LNA has 10 dB of gain and 2 dB noise figure (NF) across X-band (9.5 GHz to 10.5 GHz). The circuit is matched to 50 Ω at the input/output and the die comes

with standard 95 µm x 95 µm chip pads. A picture of the die is depicted in Figure 2.6 and further details are discussed in further detail in [54].

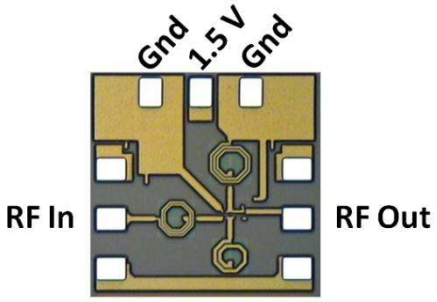


Figure 2.6: Photo of the X-band SiGe LNA.

2.2.2 LCP Package Development

For lamination of the LCP onto the LNA die, a core material and bond ply would be necessary. In order to maintain a small via diameter compatible with the chip pad size and pitch, the LCP total thickness was minimized to 50 µm. This uses a 25 µm layer for the core and bond ply layers. The design of the RF input/output transitions were simulated in Advanced Design System (ADS) using Momentum. For compatibility with the CPW input and output of the die, 50 Ω CPW lines were incorporated on package. The dimensions of this structure were calculated using ADS Linecalc and have a 433 µm line width and 20 µm gap. These dimensions do not match up well with the 150 µm pitch size of the chip pads. In order to maintain a 50 Ω CPW line at input/output, a transition was designed to accommodate for the large disparity. The resulting simulation took into account the input/output CPW lines, via interconnects and input/output lines of the LNA. This model is illustrated in Figure 2.7. The optimized design was simulated over the frequency range 8 GHz to 20 GHz and predicted reflections of less than -25 dB and insertion loss of less than 0.1 dB, as seen in Figure 2.8. The final topology of the packaged amplifier is shown in Figure 2.9. This illustrates the RF input/output CPW transitions along with the necessary DC bias lines.

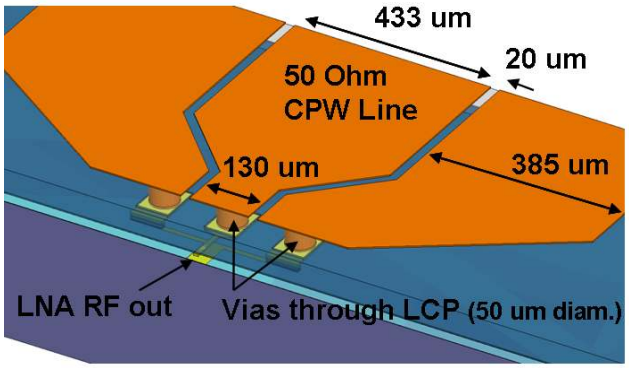


Figure 2.7: Simulation of the CPW transition lines with via interconnects.

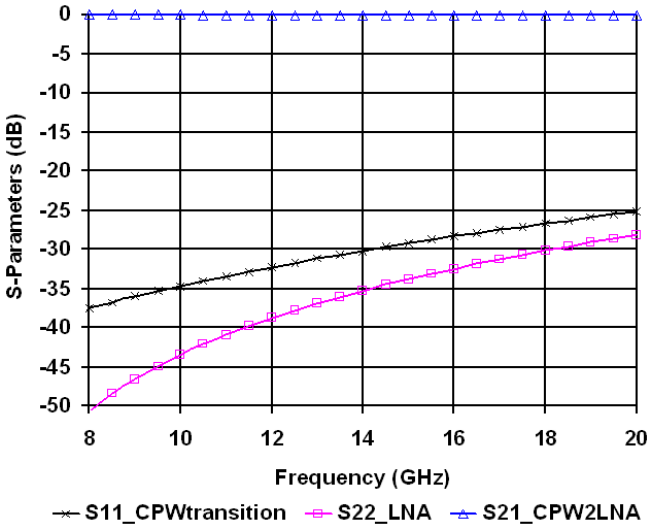
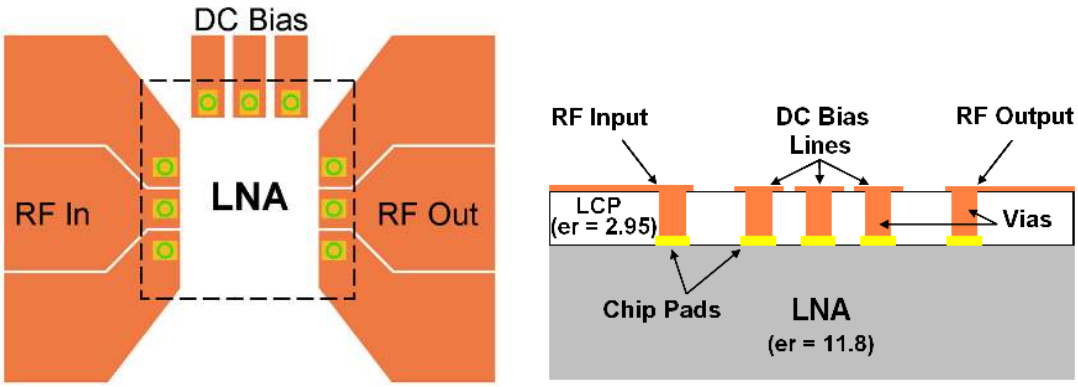


Figure 2.8: S-parameters of simulated CPW transition lines with via interconnects.



(a) (b)

Figure 2.9: a.) Over-head and b.) cross-section view of the package design with via interconnects and patterned CPW lines.

The fabrication of the optimized package design laminates a layer of 50 µm LCP onto the LNA, then exposes the chip pads by drilling 50 µm diameter via-holes through the LCP with an excimer laser. The sample is metalized and patterned accordingly. A picture of the finished package is depicted in Figure 2.10.

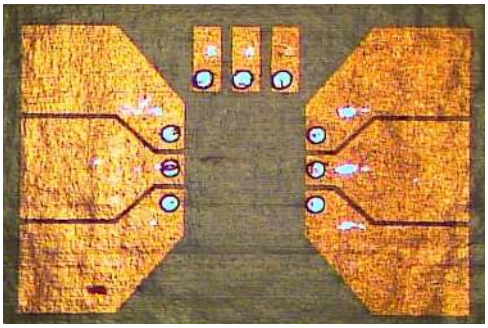


Figure 2.10: Photograph of the packaged LNA.

2.2.3 Measured Performance

The amplifier characterization was performed in a custom-built integrated S-parameter, noise figure, and load-pull on-wafer probing station. This station allows for single probing of the circuit with RF switching between the network analyzer, signal sources, and spectrum analyzer to conduct all RF and DC characterization without modifying the measurement setup. The tuners, switches, and RF components are mounted on a Suss Microtech PM-8 probe station with probe shield technology providing RF shielding to the device under test (DUT).

The S-parameters are measured with both tuners initialized and the input and output switches are configured to the "VNA" setting, connecting the DUT to the Agilent E8363B PNA. NF is measured with the switches configured for the noise receiver and is computed using the "cold-out" method (as discussed in [55]). The noise power is measured using the noise figure option of the Agilent E4446A spectrum analyzer.

Measurements were made using 250 µm ground-signal-ground (GSG) probes and a TRL calibration was performed prior ensuring the acquired measured data was referenced up to the probe tips. S-parameter and NF measurements were made with an

unpackaged and packaged LNA for comparison of performance. The S-parameters were measured over a frequency band of 8 GHz -20 GHz. A plot of the input and output return loss of the unpackaged amplifier with respect to the packaged amplifier is shown in Figure 2.11(a). A comparison of the output gains are shown in Figure 2.11(b). In both figures, there is an evident shift in frequency between the unpackaged and packaged LNA performance. Despite this shift, both LNAs retained a return loss greater than 10 dB. The S_{11} and S_{22} of the packaged amplifier showed only a slight degradation compared to the unpackaged LNA. At X-band, the unpackaged die produced a peak gain of 10.3 dB while the packaged die produced 10.2 dB. This 0.1 dB difference in gain output is accounted for by the simulated 0.1 dB insertion loss from the CPW transition lines.

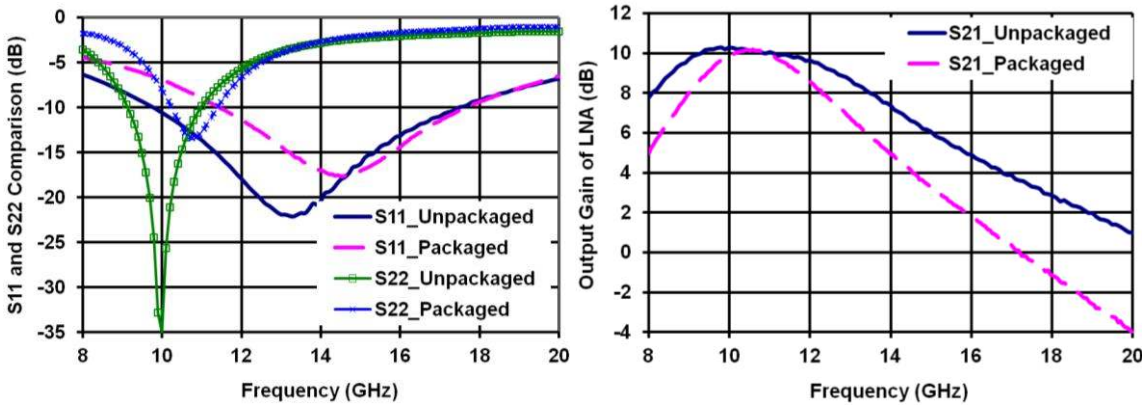


Figure 2.11: Comparison of S-parameters before and after packaging.

The NF of the unpackaged and packaged amplifier was measured at 9.5 GHz. The minimum NF for the unpackaged LNA was 1.8 dB while the packaged LNA was 1.9 dB, which is a negligible change. However, the 50 Ω NF increased from 1.9 dB to 2.5 dB. This 0.6 dB increase in NF of the packaged LNA is attributed to the impedance mismatch from the CPW transitions. This mismatch can be readily seen by observing the noise circles of the unpackaged and packaged LNA, displayed on a smith chart in Figure 2.12. It is seen that the middle noise circle of the packaged LNA is shifted away from the

center of the smith chart and has become inductive. Since the minimum noise figure showed only a small change, the CPW transition can be optimized to preserve noise matching indicating only a minor effect due to the LCP packaging.

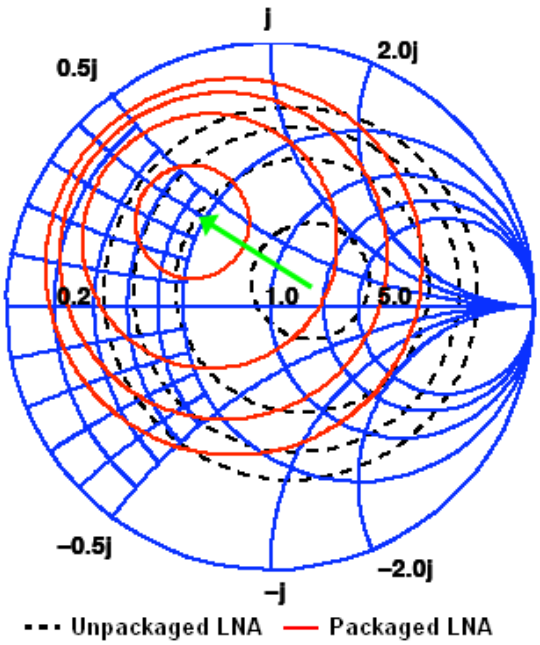


Figure 2.12: Smith chart showing noise circles of the unpackaged and packaged LNA.

2.2.4 Discussion

An X-band SiGe LNA was packaged for the first time into an embedded SOP module using a via interconnect packaging technique. Measurements after packaging showed only a 0.1 dB of loss in the peak output gain and a 0.1 dB increase in noise figure. However, there is an evident shift in frequency for the return loss and a degradation of 0.6 dB in 50 Ω NF. Further investigation is required to optimize this packaging technique and improve the performance.

In theory, this method of wafer-scale packaging provides seamless chip integration with minimized interconnect length and package size. The realization of this technique with LCP in a large-panel fabrication process is a different story. There are several pending issues that need to be addressed before implementation. These matters include: die cracking during LCP lamination, LCP de-lamination from the die during

thermal cycling, and misalignment when packaging multiple die together. At present, a packaging method with increased reliability, yet still excellent performance, would be preferable to this technique.

2.3 Encapsulated Flip-Chip Package at X Band

An encapsulated die concept is implemented to achieve a reduced form factor, planar profile, and near-hermetic packaging. The benefits of flip-chip technology enables minimized interconnect lengths, comparable to those achieved with via technology, along with high alignment accuracy for multiple chips in a large-panel processing environment. The low temperature processing of LCP allows a fully encapsulated die package that would otherwise not be possible with ceramic substrates. This section discusses a transmit/receive module flip-chipped and encapsulated into an all LCP package [56].

2.3.1 Circuit Description

The transmit/receive module (TRM) was fabricated in a 0.13 µm SiGe BiCMOS technology and designed to be used in conjunction with an external PA chip for phased array antenna systems. The topology and photo of the die is shown in Figure 2.13. The module contains an LNA, bi-directional phase-shifter, and SPDT duplexer switch. In addition, a digital interface using 2.5 V logic levels allows control of the phase-shifter as well as the on/off states of the receive amplifier. The receive side was designed for ultra-low noise performance while simultaneously achieving a power match. It consumes only 35 mW of DC power and has a reported 7 dB of gain and 2.5 dB noise figure across the X band (9.5 GHz to 10.5 GHz). The LNA has a self-bias circuitry to simplify total design and requires only a 3.5 V DC supply. The module is matched to 50 Ω at all RF ports on chip, thus no matching network is necessary on package. The total area of the TR chip is 1.4 mm x 2.8 mm. Further details of the LNA and PS design are discussed in [54] and [58], respectively. Since only the receive component of this module is active, the results presented are focused chiefly on this RF path.

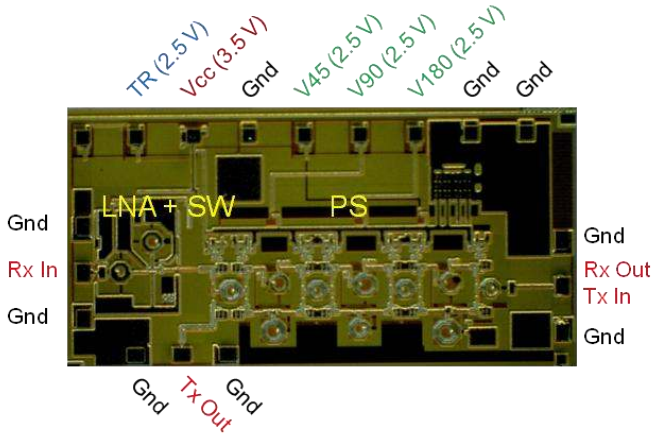


Figure 2.13: Photo of SiGe TRM.

2.3.2 LCP Package Development

The package development was completed in two steps to verify performance of first the standard flip-chip bonding process and second the fully embedded die. The package designs were simulated and optimized using HFSS to maintain performance while accommodating the flip-chip assembly process.

The TRMs to be flip-chipped came standard with wire bondable 95 µm x 95 µm aluminum pads that had to be bumped before further processing was possible. Gold stud bumps were formed on each I/O pad using a 25 µm Au wire ball bonder by thermo-sonic compression. The bumped chips were then flipped onto a heated flat surface where pressure was applied to compress the bumps into a uniform height of approximately 75 µm. Figure 2.14 shows the stud bumps formed on die. A silver epoxy (σ_c = 2.5 x 10^6 Siemens/m) was used to adhere the Au bumps to the pads on package.

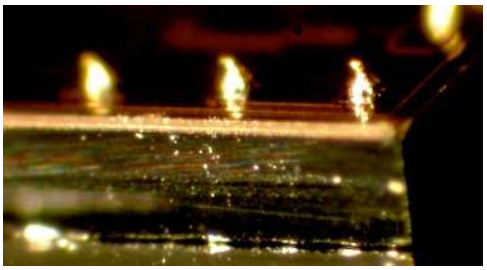
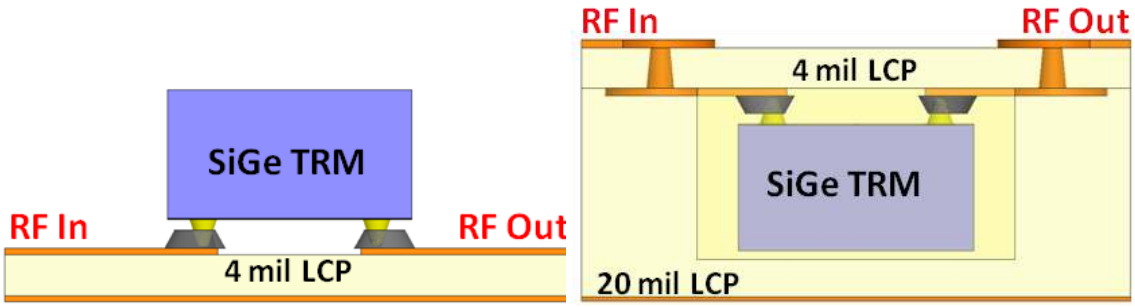


Figure 2.14: Picture of Au bumps bonded on SiGe die.

The design of the flip-chip LCP package was determined based on the 250 µm GSG RF pad pitch of the TRM. In order to maintain 50 Ω CPW input/output lines on package, an LCP thickness of 100 µm was chosen. This gave a CPW line width and gap of 210 µm and 80 µm, respectively, which matched the pitch of the chip pads as well as allowed room for potential misalignment of the bonding. An illustration of the stackup for both packages is shown in Figure 2.15.



(a) (b)

Figure 2.15: LCP package stackup for T/R module using the a.) conventional exposed flip-chip and b.) fully embedded flip-chip approaches.

The flip-chip transition, including the Au bumps and silver epoxy, was modeled in HFSS from a microstrip line reference on chip to the 50 Ω line on package. The results were de-embedded from the chip transmission line to the chip pads to focus on the effect of the flip-chip bond. These models are shown in Figure 2.16. The simulation showed a return loss greater than 25 dB and an insertion loss less than 0.15 dB at X band. From

this, it is predicted that the flip-chip bonding will account for 0.3 dB of insertion loss through the package.

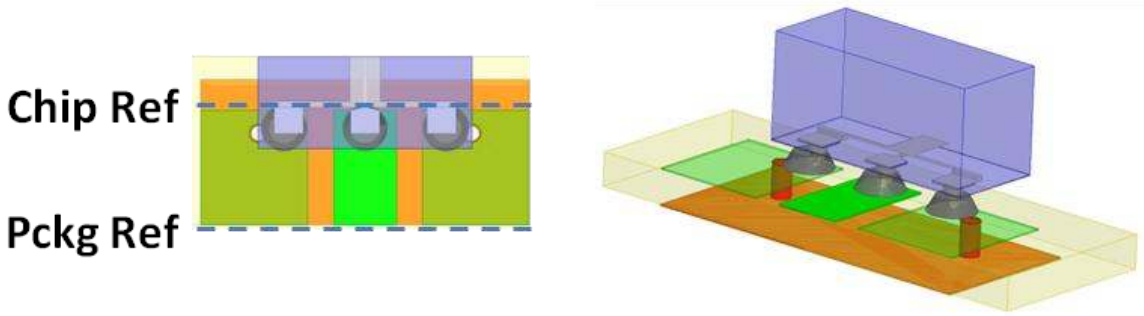


Figure 2.16: HFSS model of the standard flip-chip transition.

An extension of the standard flip-chip package is to fully embed the die in LCP. Via interconnects are utilized to transition through the 100 µm LCP so the package can be DC biased and probed for measurement. Additionally, the exposed chip is embedded in an air cavity in 500 µm thick LCP. This package was simulated in HFSS; modeling the transition from the CPW line on package, through the via and flip-chip interconnects, and on to the chip. This final package model is illustrated in Figure 2.17. The optimized design has simulated reflections of less than -27 dB and insertion loss of less than 0.2 dB over X-band. The simulations predict that the total loss of the embedded chip package through the input and output will be 0.4 dB. The performance for the two packaging approaches is compared in Figure 2.18.

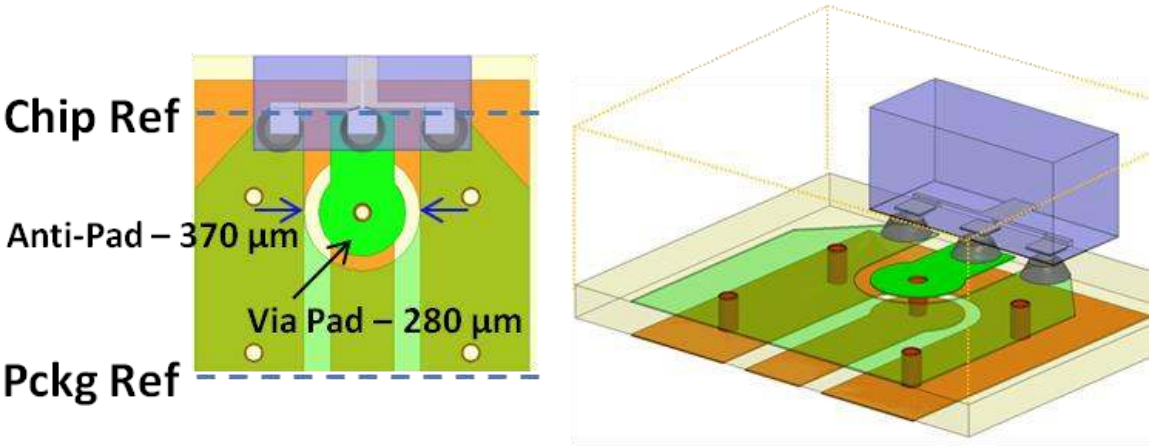


Figure 2.17: HFSS model of embedded flip-chip transition.

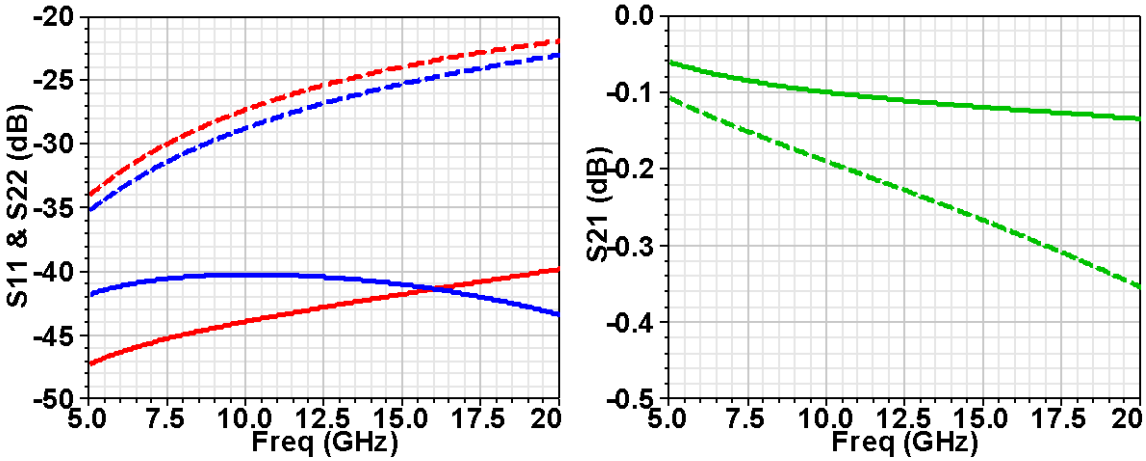
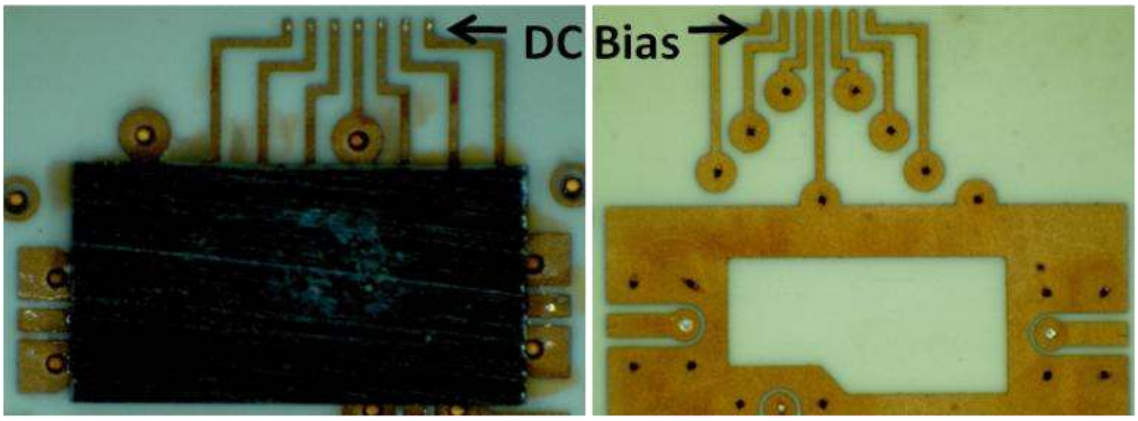


Figure 2.18: Simulated S-parameters of the standard flip-chip package (solid) and fully embedded flip-chip package (dashed).

Both the flip-chip and embedded test packages were fabricated and assembled in the same manner. Holes were drilled for signal and ground via interconnects using an excimer laser. The samples were then metalized and patterned accordingly. The TRMs were flip-chip bonded onto each package. Additionally, the 500 µm LCP layer was drilled with a CO_2 laser to create a cavity of dimensions 1.7 mm x 3.1 mm. The 100 µm LCP with flip-chip bonded TRM was then bonded to this layer completely embedding the die. The standard flip-chip package and embedded flip-chip package are shown in Figure 2.19.

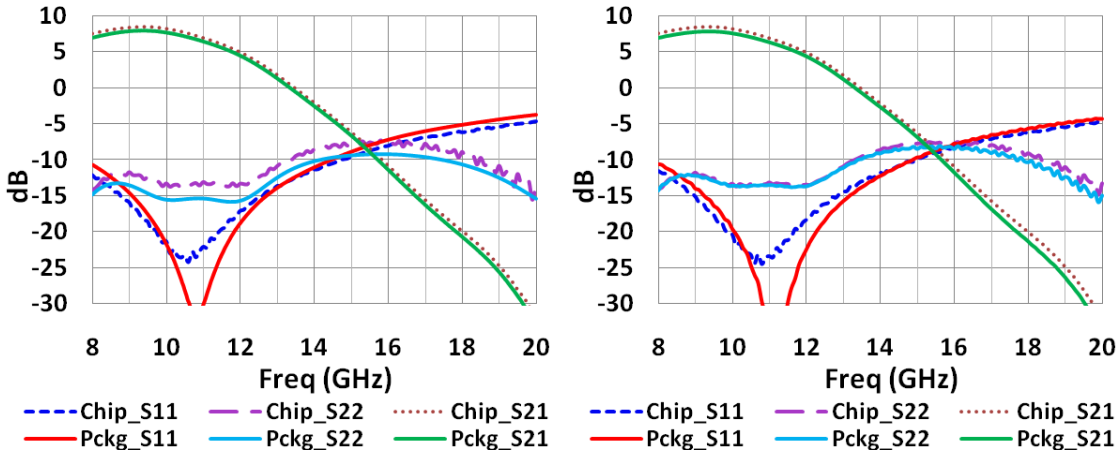


(a) (b)

Figure 2.19: Fabricated and assembled a.) standard flip-chip package and b.) embedded flip-chip package.

2.3.3 Measured Performance

S-parameter and NF measurements were made with unpackaged and packaged TRMs for comparison of performance. The S-parameters were measured over a frequency band of 8 GHz to 20 GHz. A plot of the S-parameters for the unpackaged TRM with respect to the standard flip-chip packaged TRM is shown in Figure 2.20(a). The measurements show no degradation in return loss and there is 0.4 dB of added loss from the flip-chip interconnects. This is only 0.1 dB more loss than simulated. Figure 2.20(b), shows the S-parameters for an unpackaged TRM versus the embedded flip-chip package. This package also shows no sign of mismatch in the return loss and there is 0.6 dB of added loss through the flip-chip and via interconnects. The phase shift for each state of the module was also analyzed over X band, and the largest disparity between the unpackaged and packaged die was measured to be less than 1 degree.



(a) (b)

Figure 2.20: Comparison of S-parameters before and after a.) standard flip-chip packaging, and b.) fully embedded flip-chip packaging.

The noise figure measurement of the fully embedded flip-chip TRM is shown in Figure 2.21. The minimum and 50 Ω NF are very close, meaning the package is well matched. There is a 0.3 dB increase in 50 Ω NF, which correlates directly to the added loss from the flip-chip package at the input of the die.

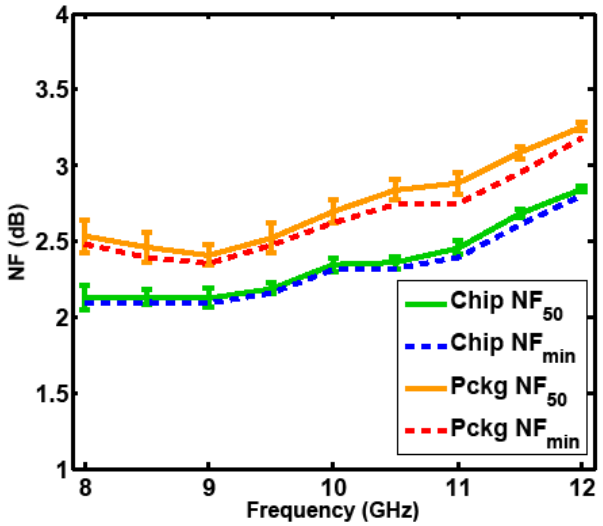


Figure 2.21: Noise figure measurement of fully embedded flip-chip package.

2.3.4 Discussion

An X-band SiGe TRM was packaged into an SoP module using a combination of flip-chip technology and LCP embedding techniques. Measurements of the package showed a 0.6 dB decrease in output gain and a 0.3 dB increase in noise figure. While the flip-chip interconnect was shown to have 0.4 dB of loss, the embedding of the die added only 0.2 dB of loss.

This technique exploits the benefits of flip-chip technology for embedding active and passive IC devices into an all-LCP platform. In this approach, the embedded chip package utilizes gold bumps for better chip placement and flip-chip bonding for minimal stress to the chip. This eliminates die cracking and provides significantly higher process yield compared to the technique in *Section 2.2*. Additionally, this process allows pre-fabrication of two multilayer laminates with higher interconnect densities that are then fused together by a single lamination step. Fewer lamination steps, combined with minimal stress on the chips, allows commercial viability of the embedded chip package with literally hundreds of embedded chips within a large area multilayer package that has not been achieved as of today. This technique can be adopted for embedding various active and passive components, such as filters, VCOs, power amplifiers (PAs), etc. While an embedded flip-chip concept has been proven, the next step for improvement is to utilize commercially available controlled collapse chip connection (C4) bumps and add an epoxy underfill. This will create a stronger, more reliable bond to the package and enhance the technique to further accommodate industry standards.

2.4 Encapsulated Flip-Chip Package at W Band

The packaging technique outlined in *Section 2.3* has been extended to mm-wave frequencies to demonstrate the applicable broad frequency range for LCP embedded flip-chip modules. Comprehensive research and prototypes have been published, leading to the realization of mm-wave standard flip-chip packaging on ceramic and lossy-silicon

substrates [59]-[60]. A 90 nm CMOS PA flip-chipped on a ceramic substrate with compensation networks has been reported for W-band applications [60]. However, never before has the die been fully embedded into the substrate at these frequencies. This section discusses the integration of mm-wave CMOS amplifiers with flip-chip packaging fully encapsulated into an all-LCP platform at W band [61].

2.4.1 Circuit Description

The three-stage PA was designed in 45 nm SOI CMOS technology using a common-source transistor architecture. The first two stages, with inter-stage matching circuitry, are designed to work as a driving gain-stage while the final power-stage output loading is designed as a class-E switching amplifier. The combination of these stages maintains overall good power added efficiency (PAE) and low required supply voltage. The die photo of this 3-stage PA is shown in Figure 2.23(a) with dimensions of 886 µm x 540 µm, including bond pads.

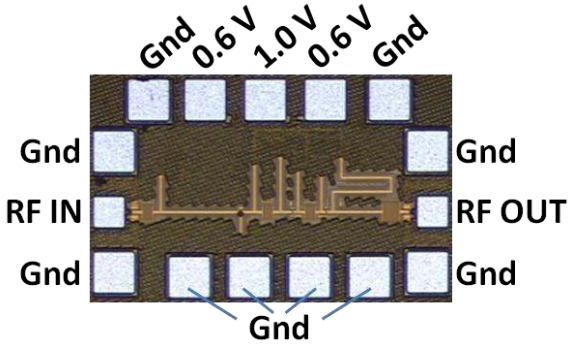


Figure 2.22: Die photo of the W-band 45 nm SOI CMOS 3-stage power amplifier.

2.4.2 LCP Package Development

The LCP package was developed in a two step process. The encapsulated flip-chip package was first designed for a broadband transition from chip to substrate utilizing gold stud bumps on chip and via interconnects on package. Then utilizing the measured S-parameters of the die, a matching network was also designed at the input and output of the package to improve the broadband performance.

The CMOS die came standard with wire bondable 95 µm x 95 µm aluminum pads and were stud bumped using the technique outlined in *Section 2.3*. During the coining process, the gold bumps were compressed to a uniform height of approximately 40 µm. This reduced height would help to minimize the interconnect parasitics. Figure 2.23(b) shows the stud bumps formed on die.

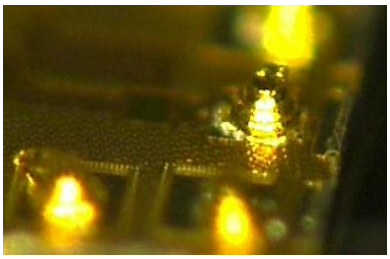
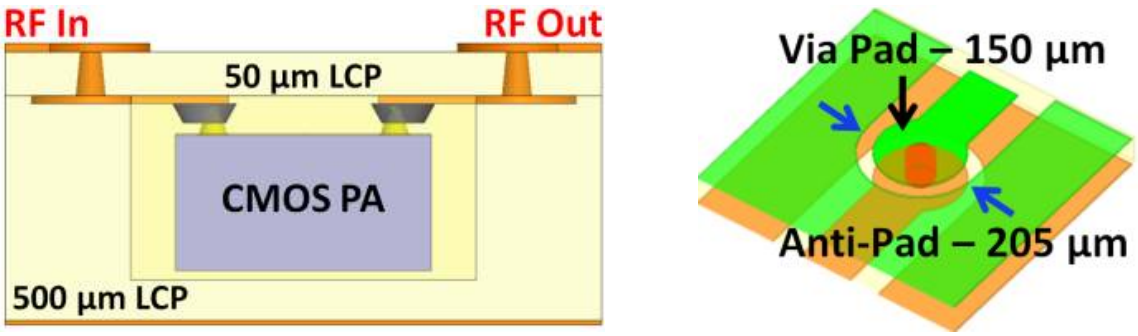


Figure 2.23: Picture of a gold stub bump with height of 40µm.

The design of the encapsulated flip-chip LCP package was determined based on the 150 µm ground-signal-ground RF pad pitch of the PA die. In order to maintain 50 Ω CPW input/output lines on package, an LCP thickness of 50 µm was chosen. This gave a CPW line width and gap of 95 µm and 55 µm, respectively, which matched the pitch of the chip pads as well as allowed room for potential misalignment of the bonding. The stack up of this design is shown in Figure 2.24(a). It is seen that via interconnects are utilized to transition through the 50 µm LCP so the package can be DC biased and probed for measurement. A via diameter of 50 µm was used to accommodate a 1:1 aspect ratio for laser drilling and metallization. Additionally, the exposed chip is embedded in an air cavity in 500 µm thick LCP.



(a) (b)

Figure 2.24: a) LCP package stack-up for PA using a fully encapsulated flip-chip approach, b) Model of the via interconnect transition.

The package transition, including the Au bumps, silver epoxy and via interconnect, was modeled in HFSS from a microstrip line reference on chip to the 50 Ω line on package. Simulation results were de-embedded from the chip transmission line to the chip pads to focus on the effect of the flip-chip bond. While using a via catch pad diameter of 150 µm, the anti-pad was tuned to a diameter of 205 µm for the best performance, shown in Figure 2.24(b). The optimized transition S-parameters are shown in Figure 2.25. It has simulated reflections less than -13 dB and insertion loss less than 0.7 dB across W band. It is predicted that the total loss of the embedded chip package through the input and output will be 1.4 dB.

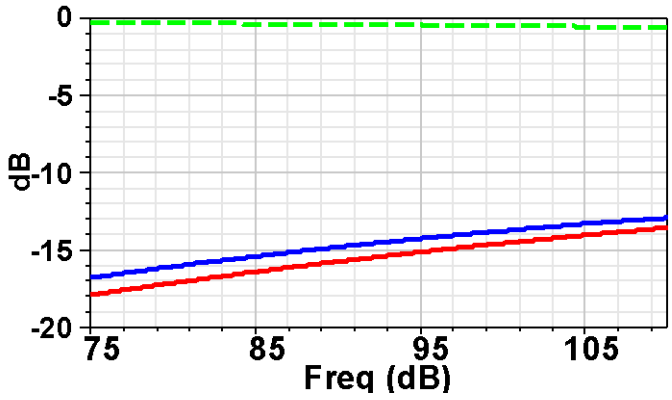


Figure 2.25: Plot of the S_{11} & S_{22} (solid) and S_{21} (dashed) for the encapsulated flip-chip transition.

Utilizing the measured die S-parameters, single stub input/output matching networks were designed and optimized for broadband performance centered at 90 GHz. For this PA, the on-die input and output impedances were measured to be 22-*j*22 Ω and 30-*j*9 Ω, respectively. For both the package input and output, a single open radial butterfly stub was used to achieve the desired 50 Ω impedance match. Using the reference plane of the measured die, the encapsulated flip-chip package with matching stub was modeled in HFSS, shown in Figure 2.26. By extracting the S-parameters of this model, a block simulation was performed in ADS to predict the matched package performance of the die. The respective input and output matching stub parameters were optimized to: d_{in} = 150 µm, l_{in} = 485 µm, d_{out} =180 µm, l_{out} = 365 µm, $\theta_{L,in} = \theta_{L,out} = 60°$, where $d_{in,out}$ is the distance from via interconnect to stub, $l_{in,out}$ is the stub length, and $\theta_{l,in/out}$ is the subtended angle of the stub.

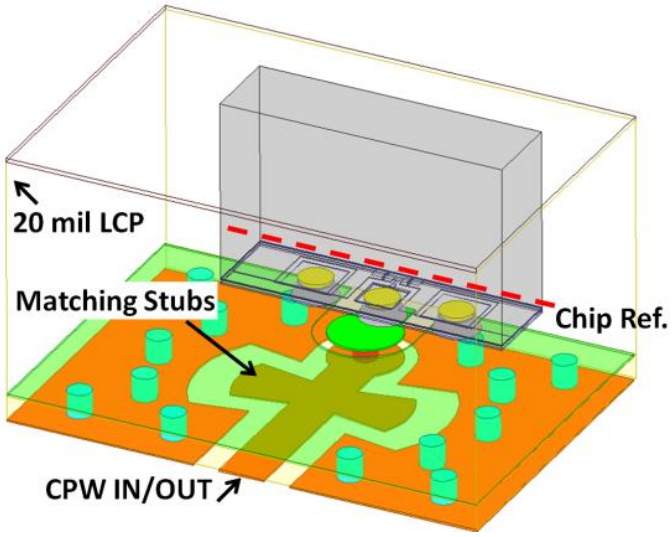
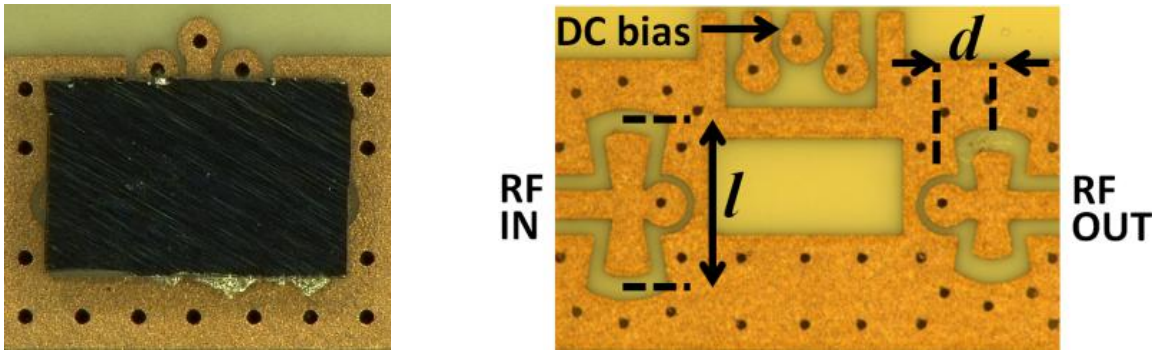


Figure 2.26: Model of the encapsulated flip-chip transition with a single open radial butterfly stub.

Both embedded packages with and without matching networks were fabricated and assembled in the same manner. Fabrication of the 50 µm thick LCP layer was performed in a cleanroom environment. The chips were bonded to this layer using a

silver epoxy to adhere the Au stud bumps to the pads on package. The 500 µm thick LCP layer was drilled using a CO_2 laser to create a cavity of dimensions 1.2 mm x 0.85 mm that hosted the chip. The 50 µm LCP layer with flip-chip bonded PA, seen in Figure 2.27(a), was then bonded to this layer completely encapsulating the die. The embedded flip-chip package with matching networks is shown in Figure 2.27(b). The overall package size is 1.8 mm x 0.9 mm.



(a) (b)

Figure 2.27: Photos of a) the flip-chipped die on package b) the encapsulated flip-chipped die in LCP with input and output matching networks.

2.4.3 Measured Performance

S-parameter and large signal measurements were made with the unpackaged and packaged PAs for comparison of performances. A plot of the S-parameters for the unpackaged PA and the encapsulated flip-chip packaged PA is shown in Figure 2.28. The results show the package yields only a slight degradation in return loss and a 1.5 dB decrease in peak gain. Figure 2.29 shows the S-parameters for an unpackaged PA versus the simulated and measured performance of the matched package. There is a significant improvement in return loss and a 1.1 dB increase in peak gain from an unmatched package.

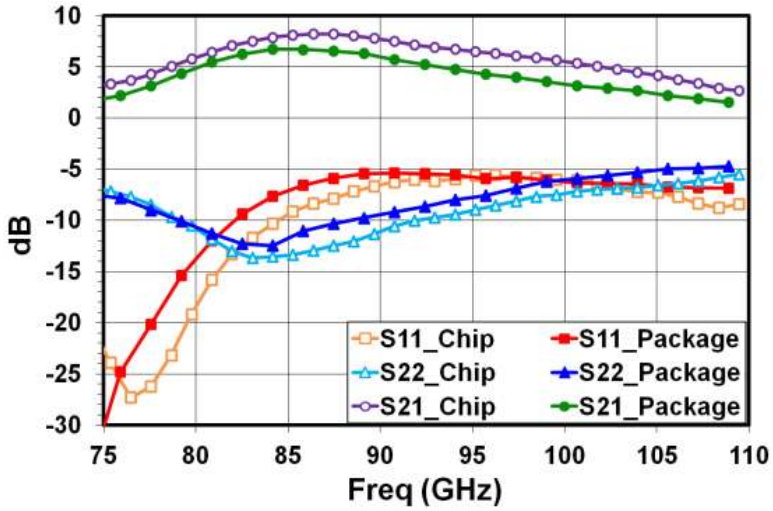


Figure 2.28: Comparison of measured S-parameters before and after encapsulated flip-chip package without matching networks.

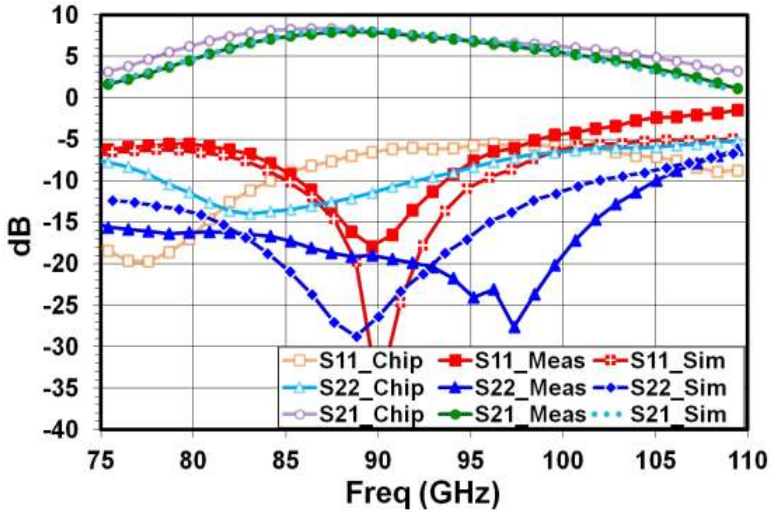


Figure 2.29: Comparison of S-parameters before and after encapsulated flip-chip package with matching network.

The large signal performances of the bare die and the encapsulated flip-chip packaged die with matching circuitry are shown in Figure 2.30. The results show this PA bare die achieves 10.0 dB small-signal gain, 6.0 dBm output power at 7.0 dB of power gain and 6.6 % PAE at 90 GHz with a single 1.0 V DC supply. This low PAE is due to the two linear driving stages. The packaged die achieves 5.0 dBm of output power (P_{out}) at 6.0 dB power gain and 5.2 % PAE at 90 GHz. Unfortunately, the proper equipment to drive

this device into saturation was not available. However, by following the data trend in this figure, it is expected that this packaged PA could achieve a saturated output power (Psat) of over 6.0 dBm with PAE of 5.8 %.

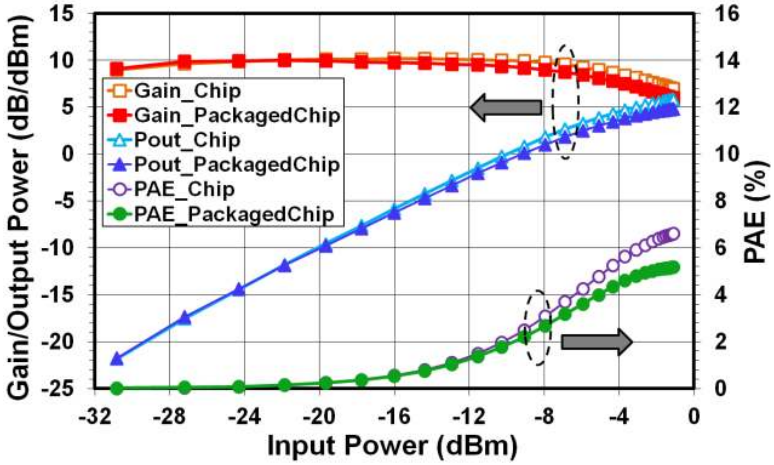


Figure 2.30: Comparison of PA output power before and after fully encapsulated flip-chip package with matching network.

2.4.4 Discussion

A W-band PA has been successfully packaged using a fully embedded flip-chip technique, completely encapsulating the die in LCP. Measurement shows only 0.75 dB of loss per flip-chip interconnect, which directly correlates to the degradation of power at the output. Additionally, a matching network was successfully implemented on-package to improve broadband performance and increase the gain by 1.1 dB. This fully encapsulated packaged W-band CMOS PA achieves 5.0 dBm output power at 6.0 dB power gain and 5.2 % PAE at 90 GHz with a 1.0 V DC supply. At present, this is the highest performance demonstrated for a fully encapsulated flip-chip W-band CMOS PA.

This work verifies that the encapsulated flip-chip packaging technique demonstrated at X band can also be applied at mm-wave frequencies with excellent performance. The inclusion of on-package matching networks to improve package

performance provides even further evidence as to the wide capability of SoP modules utilizing LCP.

2.5 Summary

This chapter has discussed several packaging techniques using LCP substrates for microwave and mm-wave applications. The benefits of LCP as a high frequency packaging platform has been demonstrated by exploiting its inherent characteristics for wire bond, via, and flip-chip interconnect technologies. The advantages for each of these packaging techniques have been discussed, along with possible improvements for reliability and performance in a large-panel processing environment.

CHAPTER 3

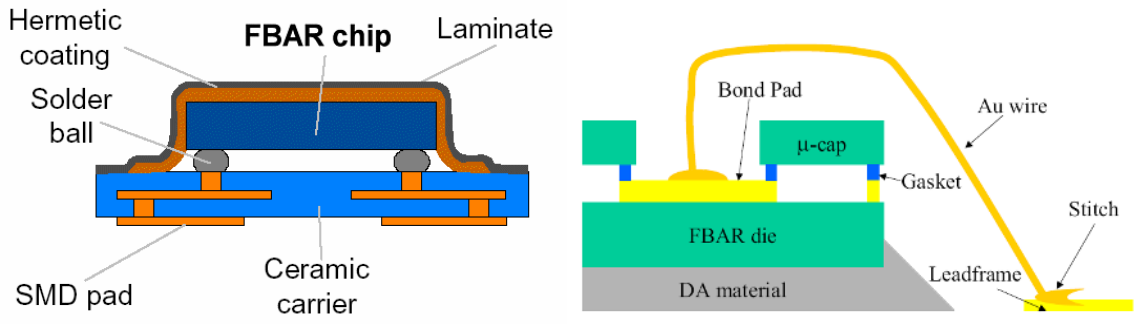
INTEGRATION OF BAW FILTERS ON LCP

3.1 Background on BAW Filter Devices

Bulk acoustic wave (BAW) devices are a maturing technology that has emerged primarily from the ever increasing demands of the mobile communications industry. For years, the market has driven the technology to lower costs, smaller sizes, and higher performance, but largely in the 2 GHz to 5 GHz range [62]-[64]. Recently there has been an increased interest at higher frequencies for other applications such as RF instrumentation, sensors, and radar systems.

The work published on BAW devices shows promising performance reaching up to K-band; however, these measurements are performed at the wafer level and not on package [65]. As this technology extends to higher frequencies, the packaging component of these devices will play a key role in maintaining cost and performance. Conventional package configurations are illustrated in Figure 3.1. Most commonly, BAW devices are sensitive to moisture, which requires hermetic packaging. Also, in order to maintain small die size and high performance, impedance matching networks are excluded and must be integrated on the package. While ceramic packaging incorporates on-package matching, it also adds cost, weight, and size [66]. A wafer-level package would maintain lower costs, but it does not incorporate necessary impedance matching and requires wire bond interconnects to the on-package matching networks. These packaging schemes are counter intuitive when striving for low cost, small sized components for highly integrated systems. With the cost benefits and near-hermetic nature of LCP, it is an attractive candidate for the moisture-sensitive nature of these filters. This work utilizes state-of-the-

art BAW technologies and LCP packaging techniques, and shows great potential for extension up to mm-wave applications.



(a) (b)

Figure 3.1: Conventional package configurations for BAW filters using a.) ceramic packaging [66] and b.) wafer-level packaging [67].

The BAW filters used in this chapter utilizes a solidly mounted resonator (SMR) with a Bragg reflector stack built on a silicon carrier substrate. The Bragg reflector consists of stacked high and low impedance, quarter wavelength films which act as an acoustic reflector to generate the desired resonance. The sensitive nature of these filters requires a hermetic seal around the die to prevent moisture from condensing on the resonator surfaces. Any residual moisture will drastically shift the resonant frequency and severely degrade performance. Consequently, these filters have been fabricated specifically for flip-chip packaging with a seal ring encapsulating the circuitry. They have been outfitted with a Sn solder finish on the bond pads and seal ring which provides a strong bond and hermetic seal for the die attachment. Due to the high operating frequency of these resonators, on package impedance matching at the input and output is required to reach the desired performance while minimizing the chip dimensions. Additionally, these die have been fabricated in a two-channel configuration with each filter independently operated and having separated RF I/O. This chapter discusses the steps for integration of BAW filters on LCP at C band and K_u band frequencies [68]-[70].

At present, these are the highest reported operating frequencies for packaged BAW filters on a 3-D multilayer organic platform.

3.2 C-Band Filter Package

The C-band circuit is a 4-pole resonator with two SMR sections to be connected electrically in series on package. The layout of the entire 1.3 mm x 1.77 mm x 0.51 mm die with two-channel filter is shown in Figure 3.2. The device requires an on-package impedance matching network at the input and output, as well as at the interstage between SMR sections. Each SMR section of the die was measured on a network analyzer to be used in conjunction with the design of the matching networks.

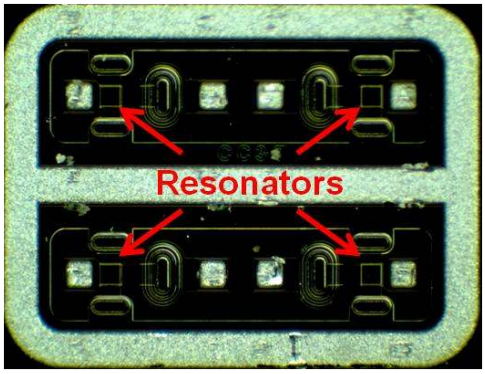


Figure 3.2: Picture of the C-band BAW die.

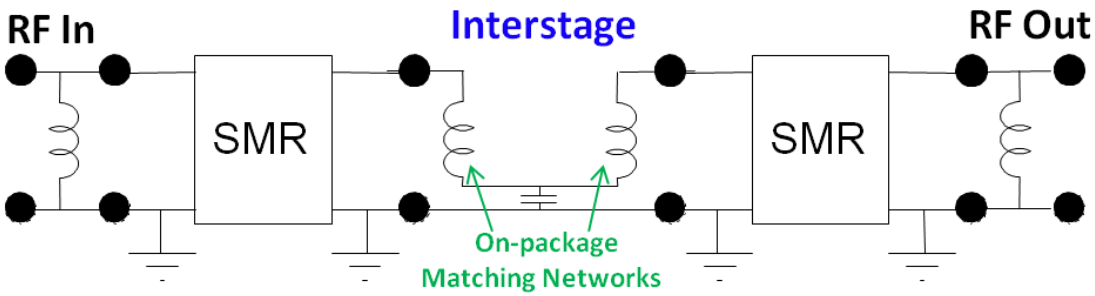


Figure 3.3: Schematic of single channel filter showing necessary matching for each SMR.

A block level simulation of the measured on-die S-parameters in the ideal case of lossless impedance matching shows operation at a center frequency of 7.45 GHz with a 3 dB bandwidth of 525 MHz (7 % BW). It has an ideal insertion loss of 4.5 dB and a shape factor of 2.1:1 at 30/3 dB. The die is expected to maintain at least 40 dB of isolation between channels.

3.2.1 LCP Package Design

A wide-band transition was designed to accommodate the flip-chip BAW filter bonded onto LCP. Because this device requires a hermetic seal, the RF inputs and outputs are accessible only through via interconnects. These transitions are simulated from a reference plane on chip to ensure accurate modeling of the chip transmission lines down to via interconnects and out to 50 Ω lines on LCP. Additionally, the small size of the chip does not allow for impedance matching to take place within the solder ring. Therefore, once the RF signal is transitioned out onto LCP, a matching circuitry is required to attain 50 Ω impedances. This work utilizes single stub tuning to minimize the package size while achieving an accurate match.

Design of 3-D Transitions

The package for the filter uses the same design scheme, seen in Figure 3.4, with modifications made to the matching networks necessary to tune to the specific filter impedances. This design utilizes two laminated LCP layers consisting of 25 µm and 50 µm (25 µm core plus 25 µm bond-ply) thicknesses. One bond ply layer (25 µm thick) was needed for the multi-layer lamination, leading to a total thickness of 76 µm. A thin LCP layer was used for the via transitions to minimize via diameters and the necessary catch pad dimensions. On top of the stack are CPW lines for input and output of the package as well as bond pads for the attachment of the BAW die. These CPW lines consist of a 50 µm wide signal line and 75 µm gap to ground. The top and bottom ground layers have connecting vias to prevent unwanted propagating modes and to maintain high isolation between channels. The embedded RF layer has striplines that are 45 µm wide

and minimized in length to conserve space. There are two via transitions on each input and output of the package. The CPW-to-stripline via transition uses 75 µm diameter vias and 150 µm diameter catch pads. The stripline-to-bond pad via transitions were limited by space constraints inside the solder ring cavity and thus use 50 µm diameter vias and 125 µm / 100 µm diameter catch pads.

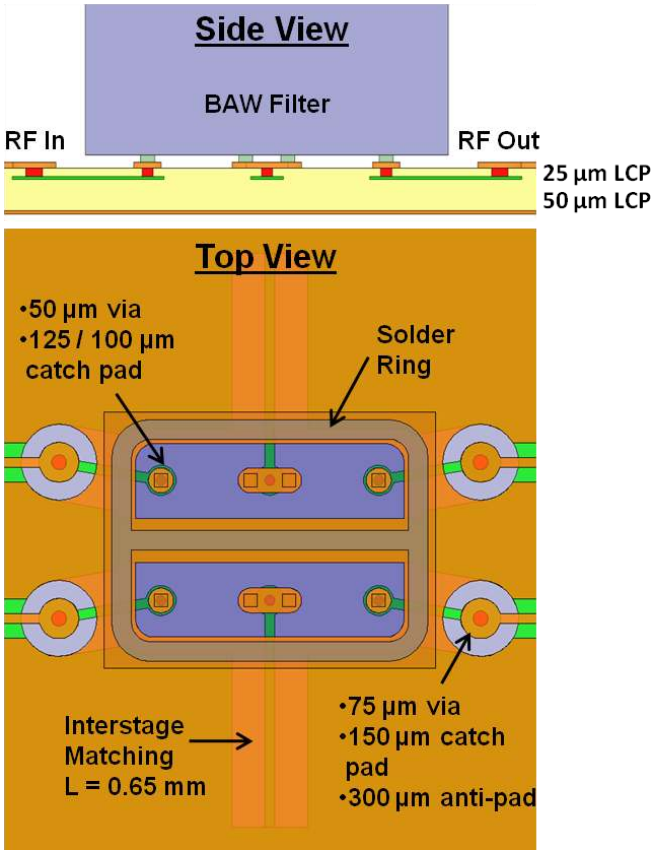


Figure 3.4: Layout of via interconnects for dual-channel filter package.

This package design was optimized using HFSS and showed a return loss better than 22 dB at all ports, and an isolation better than 45 dB at frequencies up to 30 GHz. This was verified by packaging a die with thru microstrip lines fabricated in place of the SMR sections. On-chip measurements showed a maximum insertion loss of 1.05 dB per section. The die was attached onto the package for measurement and compared to simulation results in Figure 3.5. The measured return loss was better than 10 dB with an

insertion loss less than 2.25 dB up to 30 GHz. Less than 0.2 dB of the overall loss is attributed to the package. The length of the package is 3.14 mm, yielding an insertion loss less than 0.7 dB/mm up to 30 GHz. The return loss was slightly worse than expected but this is likely due to the misalignment of the stripline layer within the package.

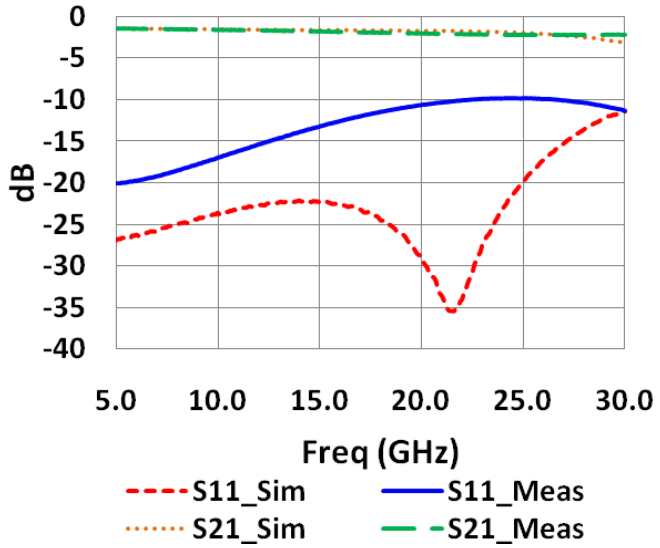


Figure 3.5: Measured and simulated results for microstrip thru fabricated on the BAW substrate and packaged on LCP with the 3-D transition.

Matching Network Design

A two step process was used to design the matching networks on package. First the interstage matching between SMR sections was designed and simulated in HFSS, shown in Figure 3.4, using ideal input/output matching. A single shorted, stripline stub of 0.65 mm was used to achieve the desired impedance match. The BAW die was then packaged with only the designed via interconnects and interstage matching, seen in Figure 3.6. This allowed measured data to be used in conjunction with the simulated model to develop the input and output matching networks accordingly and achieve 50 Ω impedances. This method guaranteed the best performance out of the filter. Measured on-chip and on-package results are compared to simulation without input/output matching in Figure 3.7.

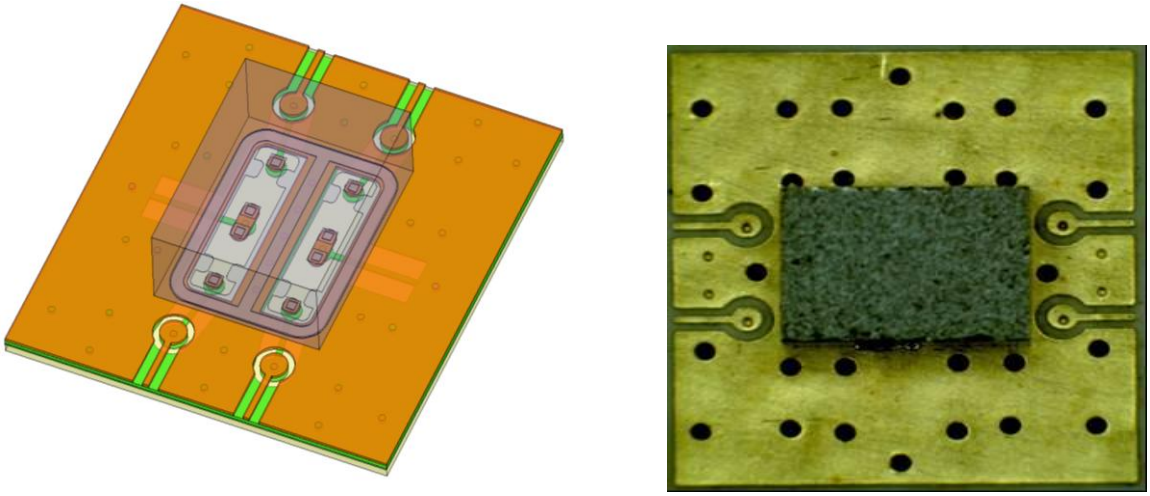


Figure 3.6: Model and photo of the C-band BAW filter with interstage matching but without input/output matching networks.

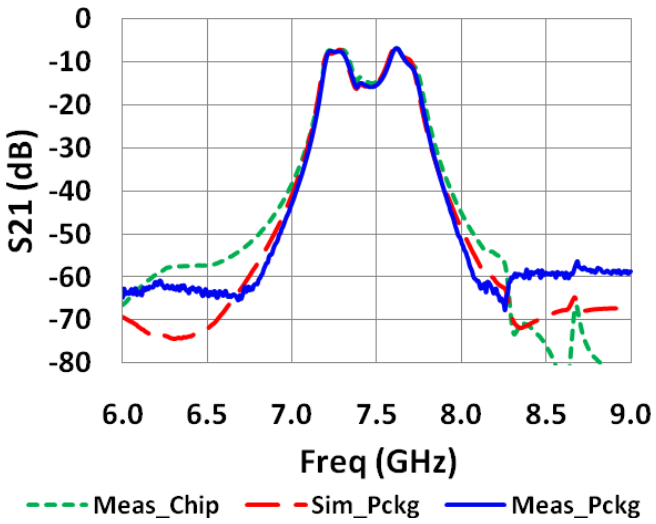


Figure 3.7: Simulated and measured results (on-chip and on-package) for the C-band BAW filter without input/output matching networks.

Utilizing this data, single stub input/output matching networks were designed and optimized. For this filter, the on-die input and output impedances were designed to be the same. Therefore, the same matching network was used for both the input and output of the package. Figure 3.8 illustrates the initial capacitive input impedance on-die and its progression through the designed matching network on-package. A single open radial

stub was used to achieve the desired impedance match. Using the reference plane of the measured die packaged without I/O matching networks, the open stub was adjusted to a distance of 2.56 mm with an angle of 70° and a length of 1.17 mm. It is expected that the filter will show 5.6 dB of insertion loss with minimal change in bandwidth and shape factor.

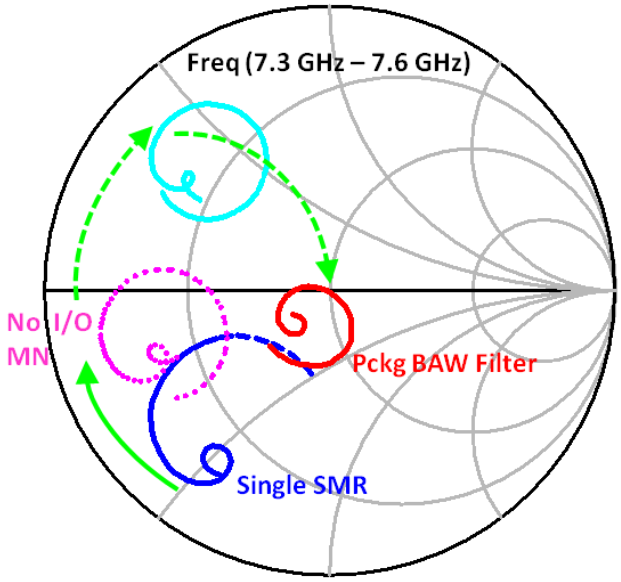


Figure 3.8: Smith chart illustrating the progression of the unmatched impedance on die to the matched filter response on package.

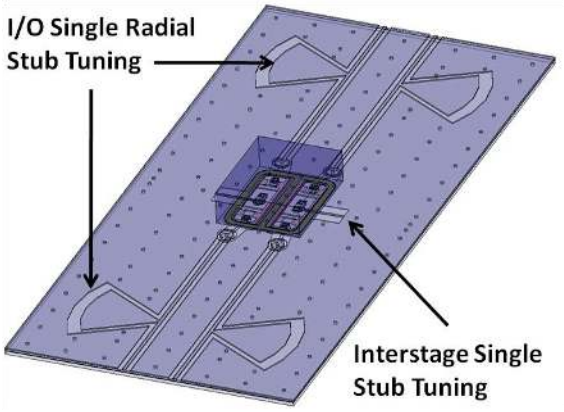


Figure 3.9: Model of the C-band filter package with integrated matching networks.

3.2.2 Measured Performance

The LCP package was fabricated with electrolytic nickel gold finish for compatibility with the filter attach process. The die was bonded using a Finetech Sub-micron Flip-chip Bonder. This machine comes equipped with dual temperature control of the die and substrate. While in contact, the die temperature was raised to 360ºC and the substrate temperature was brought up to 260ºC for 45 seconds. The final packaged filter with matching networks is shown in Figure 3.10.

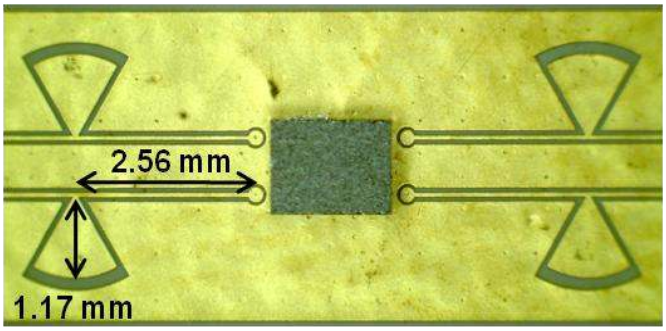
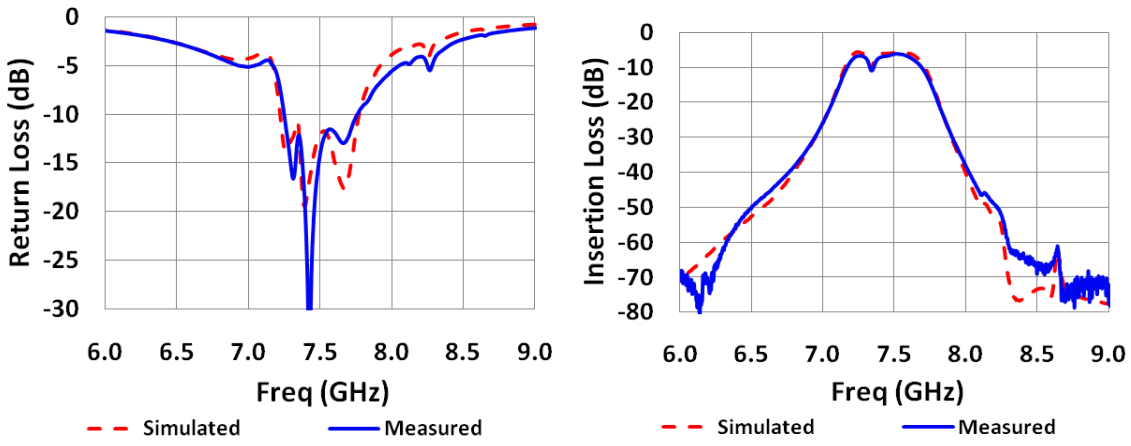


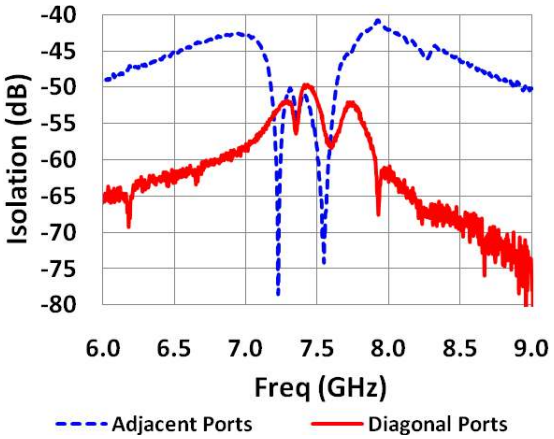
Figure 3.10: Photo of the C-band BAW filter packaged on the multilayer LCP substrate.

The assembled package was measured with an Agilent E8361C PNA. The measured and simulated S-parameters are shown in Figure 3.11. It is seen that the packaged filter matches very closely with the modeled results. The C-band filter shows operation at a center frequency of 7.45 GHz with a 3 dB bandwidth of 495 MHz (6.65 % BW). It has a measured insertion loss of 6 dB and a shape factor of 2.3:1 at 30/3 dB. The isolation between channels was measured to be better than 40.5 dB, the worst case being at adjacent ports.



(a)

(b)



(c)

Figure 3.11: Simulated and measured on-package a.) return loss and b.) insertion loss of the matched filter; c.) Isolation measurement between channels of the packaged filter.

A notch can be seen in the pass band of the filter however this is not due to the package but rather a perturbation in the on-die response. The reason for this perturbation is an over sized top electrode on the resonator stack causing a second or third order acoustic effect. The manufacturer of the BAW device is currently working on notch mitigation techniques.

3.2.3 Discussion

This work has demonstrated for the first time a BAW filter operating at 7.45 GHz packaged in a three-dimensional multilayer organic platform. The packaging effects on

the die performance for this concept show minimal degradation. The packaged BAW filter has an insertion loss of 6 dB and a channel-to-channel isolation better than 40 dB.

3.3 K_u-Band Filter Package

The K_u-band circuit, shown in Figure 3.12, is a 2-pole resonator with a die size of 1.03 mm x 1.53 mm x 0.51 mm. The device requires an on-package impedance matching network at the input and output of each channel. Each SMR was measured on a network analyzer to be used in conjunction with the design of the on-package matching networks.

A block level simulation of the measured on-die S-parameters, in the ideal case of lossless impedance matching, shows operation at a center frequency of 12 GHz with a 3 dB bandwidth of 2.15 GHz (17.9 % BW). It has an ideal insertion loss of 3.3 dB and a shape factor of 1.8:1 at 15/3 dB.

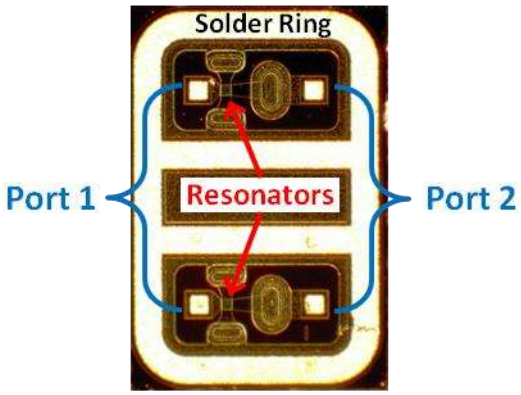


Figure 3.12: Picture of the dual-channel K_u-band BAW die.

3.3.1 LCP Package Development

The requirements driving this work specified that an LCP interposer be used to house the packaged BAW filter which would then be mounted on a motherboard of the exact same material stack-up. The BAW die would be mounted on top of the interposer and the RF in/out would be accessed from the bottom metal layer. For mechanical stability, an overmold (G770) with a height of 700 µm was used on top of the interposer to encapsulate the die. The interposer was equipped with a GGSGSGG pad layout at the

input/output to interface with a CPW fed motherboard. The full package stack-up is illustrated in Figure 3.13. Thin LCP layers were used to minimize via diameters and catch pad dimensions for the layer-to-layer transitions. Both the motherboard and interposer stack-ups utilize three laminated LCP layers consisting of 50 µm thick core and bond ply materials. One bond ply layer (50 µm thick) was needed for the multilayer lamination, leading to a nominal thickness of 150 µm. The filter package uses the design scheme seen in Figure 3.14. This comprises of direct via transitions from the BAW die to $M2_{Int}$, and from $M2_{Int}$ to $M1_{MB}$. Additionally on $M2_{Int}$, is a shorted stub used for impedance matching on port 1 and a shorted stub in series with an open stub for impedance matching on port 2. For this work, only $M1_{MB}$ is utilized on the motherboard for RF signal routing. This layer contains four 50 Ω CPW lines with a 75 µm wide signal line and 60 µm wide gap to ground. The ground layers for both boards have connecting vias to prevent unwanted propagating modes and to maintain high isolation between channels.

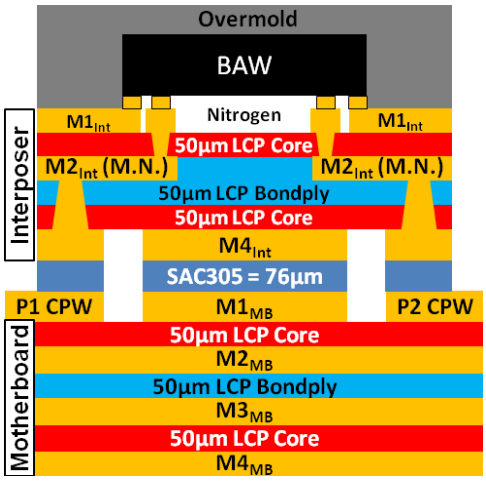


Figure 3.13: Material stack-up of the packaged and mounted BAW filter interposer on motherboard.

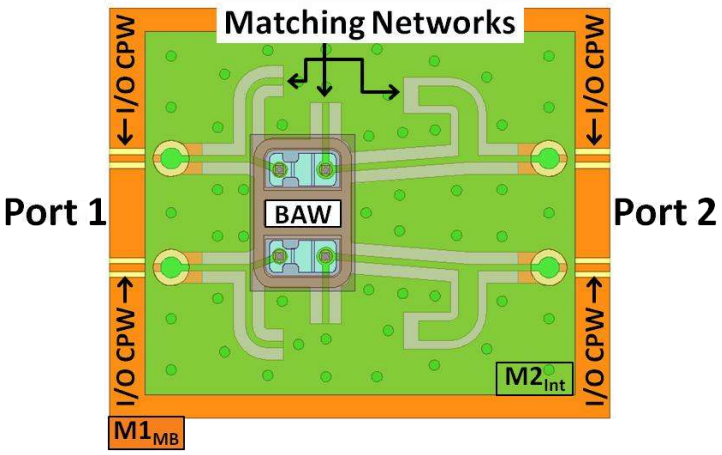


Figure 3.14: Top view showing the embedded matching networks on layer M2 of the interposer, and the I/O CPW lines on the motherboard.

Design of 3-D Transitions on Interposer

On top of the interposer stack ($M1_{Int}$) are bond pads for the attachment of the BAW die. These are 100 µm in diameter and also act as a catch pad for 50 µm vias that transition down to 125 µm catch pads on $M2_{Int}$. The dimensions of these features were determined by a compromise between restricted space within the die solder ring cavity and limitations of the fabrication process. Because the impedances of the die are not yet matched to 50 Ω, the effects of these transitions are accounted for in the matching networks.

The $M2_{Int}$ layer contains 50 Ω quasi-CPW (GSG 120 µm / 65 µm / 120 µm) striplines for the on-package matching networks that feed the input and output of each channel into vias that transition down to the motherboard. A 75µm via connects through the interposer from 200 µm catch pads on $M2_{Int}$ down to $M4_{Int}$, where a solder paste (SAC305) is later used to attach on $M1_{MB}$. This transition also uses 356 µm anti-pads located in the grounds of $M1_{Int}$, $M2_{Int}$, $M1_{MB}$ and $M2_{MB}$. These anti-pads are used to tune the transition and maintain a 50 Ω structure. This via transition was optimized using HFSS and showed a return loss better than 30 dB at all ports and an insertion loss less than 0.1 dB.

Matching Network Design

Although the BAW die is bi-directional, the on-die measurements show different input impedances for port 1 and 2. As such, each port required a custom matching network. Figure 3.15 illustrates the initial capacitive input impedance on-die and its progression through the designed matching network on package. For Port 1, a single shorted stub of length L_{P1} = 975 µm was spaced a distance D_{P1} = 320 µm from the BAW die pad. Port 2 was designed with a shorted stub of length $L1_{P2}$ = 625 µm placed immediately at the via transition on $M2_{Int}$ and another open stub of length $L2_{P2}$ = 990 µm spaced a distance D_{P2} = 1.4 mm further. Additionally, the open stub on Port 2 has a wider line width of 190 µm in order to achieve a shorter stub length with the same impedance effect.

A 3-D model, shown in Figure 3.16(a), was designed and simulated in HFSS which included all the via transitions and matching networks. These S-parameters were then extracted and imported into a block simulation with the measured on-die S-parameters. By coherently modifying both port matching networks, the design was optimized for the outlined die specifications. It is expected that the filter will show 3.9 dB of insertion loss with minimal change in bandwidth and shape factor. The package module size is 4.20 mm x 3.55 mm.

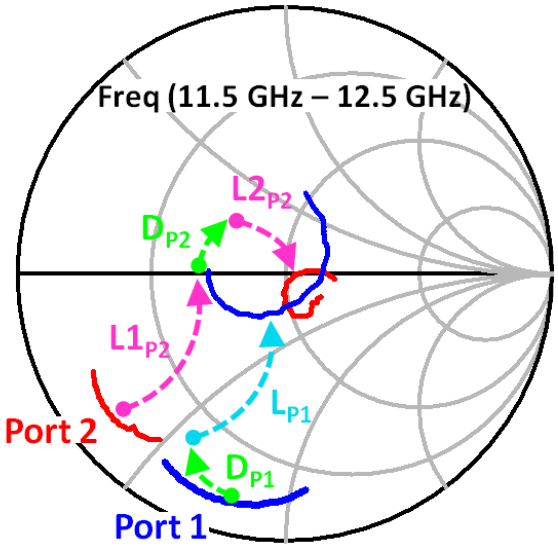
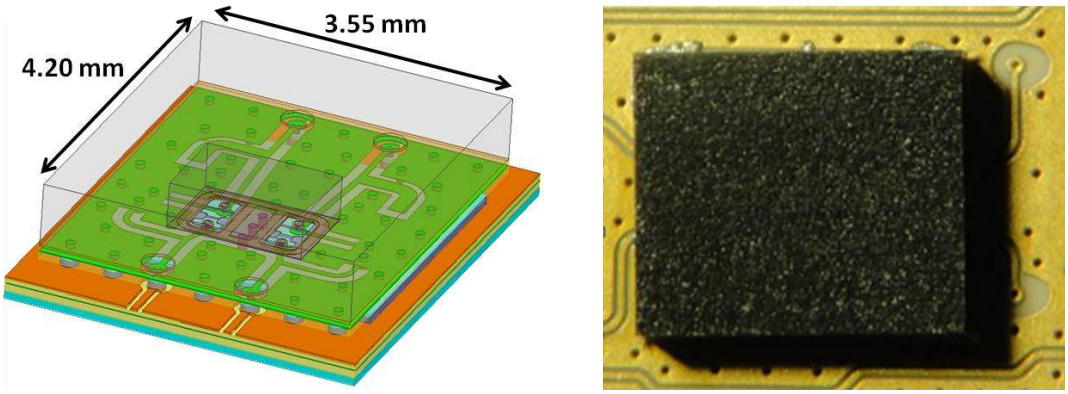


Figure 3.15: Smith chart illustrating the progression of the unmatched impedance on die to the matched filter response on package.



(a) (b)

Figure 3.16: a) Full simulated package with matching networks, b) Picture of the packaged BAW filter interposer mounted on motherboard.

3.3.3 Measured Performance

The LCP package was fabricated with electrolytic nickel gold finish for compatibility with the die attach process. The die was bonded using the technique outlined in *Section 3.2.2*. A picture of the final packaged filter is shown in Figure 3.16(b).

The assembled package was measured with an Agilent E8361C PNA. Figure 3.17 shows a comparison of the measured and simulated S-parameters. The packaged filter matches very closely with the modeled results. The measured K_u-band filter shows operation at a center frequency of 12 GHz with a 3 dB bandwidth of 2.1 GHz (17.5 % BW). It has a measured insertion loss of 2.8 dB and a shape factor of 1.7:1 at 15/3 dB.

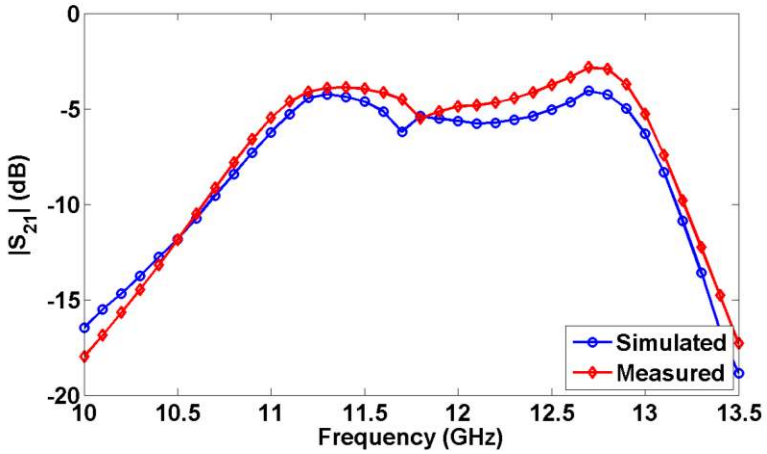


Figure 3.17: Comparison of the simulated and measured on-package performance of the K_u-band BAW filter.

A notch is present in the pass band of the filter, however this is not due to the LCP package or matching networks but rather a perturbation in the on-die response. This effect is from an over sized top electrode on the resonator stack causing a second or third order acoustic effect. Techniques for mitigating this notch are being investigated by the BAW die manufacturer.

3.3.3 Discussion

This work has demonstrated for the first time a BAW filter operating at 12 GHz packaged on a highly integrated multilayer LCP interposer board. The packaged BAW filter has an insertion loss of 2.8 dB and a half-power bandwidth of 17.5 %. The embedded matching networks were designed in a manner to condense the package size while achieving an accurate 50 Ω impedance match. Additionally, a protective

overmolding was applied to the packaged die for mechanical strength of the hermetic attachment.

3.4 Summary

BAW devices have been packaged on multilayer LCP using a hermetic die attachment and incorporated matching networks. Several via interconnects were required for a direct transition from the chip interface to an embedded stripline layer. The package was first demonstrated with a flip-chip attached die with microstrip thru-lines fabricated in place of the BAW resonators. This confirmed a reliable package process with low insertion loss. A C-band BAW filter was then packaged using this process with the addition of incorporated matching networks for a 50 Ω impedance match. Using an incremental design method, the interstage and I/O matching networks were tuned for optimized performance. A comparison of the simulated and measured performance for the final packaged 7.45 GHz filter verified excellent results. The concept of this packaging technique was also implemented in the K_u band for a 12 GHz BAW filter. A package module for this filter was intended for integration with a system motherboard. The package was designed with embedded matching networks for condensed size and precise impedance matching. The overall size of this module was 4.20 mm x 3.55 mm. The resulting performance of the packaged 12 GHz BAW filter showed excellent correlation with the simulation data. The inherent performance and packaging benefits of LCP creates a compelling advantage over other competing solutions. As BAW devices extend to mm-wave frequencies, this packaging approach exhibits potential for a viable low cost solution.

CHAPTER 4

X-BAND ACTIVE RECEIVING PHASED-ANTENNA ARRAY

The packaging techniques discussed in *Chapter 2* shows the integration of active devices onto LCP for a variety of low-cost, high performance applications. A struggle to lower costs and reduce weight while maintaining high performance is a primary motivation for this work. The multilayered LCP integration scheme discussed in this chapter takes the next step in which the opportunity for low-cost, lightweight compact radars becomes achievable.

The incorporation of highly functional, low-power 0.13 µm BiCMOS SiGe circuits on LCP makes this technology [71] niche uniquely positioned compared to other technologies available in the literature [72], [73]. It has been successfully shown that the integration of SiGe with radar systems is a viable low-cost solution [73]. The potential for several integrated functions, on a single chip that offers high performance at lower costs, keeps this technology in high demand [74], [75]. In [76] and [77], this technology is applied to a SoC approach where the active antenna is fully integrated onto silicon. However, this limits antenna performance due to the restriction of real estate, as well as added losses from the substrate. The work discussed in this chapter utilizes an SoP concept by integrating SiGe technology for the first time with the benefits of high gain microstrip antennas on low-loss organic substrates. A progressive approach is taken in the demonstration of several prototype antennas for the development of an 8x2 active receiving phased-antenna array in the X band.

4.1 Antenna Array Overview

A series of microstrip antennas have been sequentially designed with increasing array elements and component integration. Small array sizes of 4x1 and 8x1 antennas

were utilized for preliminary testing of the antenna design and incorporated ICs. A controlled comparison of passive and active antennas is used for verification of performance development for the final 8x2 phased-array antenna.

Each antenna array was designed for operation at 9.5 GHz with a bandwidth of 500 MHz. The array element spacing was optimized for beam scanning of ±20° in the *x*-dimension. The expression for the required *x* and *y* element spacing of the array is given as

$$\Delta d = \frac{c}{f_{max}(1+|\sin\theta_S|)} \tag{4.1}$$

and was determined using the scan angle (θ_S = 20° for x and θ_S = 0° for y) and maximum frequency (9.75 GHz). The spacing for the *x* (beam scan direction) and *y* dimension were calculated to be a maximum of 22.9 mm and 30.7 mm, respectively. These numbers reflect only the maximum spacing required to meet the necessary scan angle. The actual element spacing chosen is less than the calculated in order to increase the maximum scan angle and thus effectively reduce the appearance of grating lobes at the optimized scan angle of 20°.

The selected organic substrate in this study is a combination of low-loss LCP and low-loss RT/duroid 5880LZ. A lightweight composition is an essential attribute for all applications where portability is of importance, including both airborne and ground devices. For the initial array designs (4x1 and 8x1 arrays), an all LCP platform was implemented. However, with the discontinuation of thicker LCP substrates during the development of this study, RT/duroid 5880LZ was selected as a replacement substrate for the radiating antenna elements. This material is a PTFE composite with a low dielectric constant (ε_r = 1.96) and low loss tangent (tanδ = 0.002). It was chosen primarily for its lower density and process compatibility with LCP (8x2 array). Additionally, it is accessible in thicker form (>1 mm in substrate thickness), no longer commercially available for LCP, which allows higher achievable bandwidths.

The final 8x2 antenna design utilizes two columns, spaced $0.644\lambda_o$ apart, that are uniformly fed in parallel and are comprised of several aperture coupled microstrip patches spaced $0.855\lambda_o$ apart. The stack up of the antenna is shown in Figure 4.1. This design utilizes two LCP layers consisting of 75 µm (50 µm core plus 25 µm bond ply) and 100 µm thicknesses laminated to a 1.27 mm thick antenna core layer using a 25 µm LCP bond ply. Two bond ply layers (25 µm each) are needed for the multi-layer lamination, leading to a total thickness of 1.47 mm. Thin LCP layers are used to limit radiation losses through the large feed network and a thicker antenna core layer is used to achieve the necessary bandwidth. On top of the stack, there is an array of microstrip antenna elements where each element in a column is spaced 27 mm apart (y-dimension) and the columns are spaced 20 mm apart (x-dimension). The aperture layer contains sixteen slots centered directly below each patch element. The dimensions of a single aperture coupled patch for each prototype antenna are illustrated in Figure 4.2. The embedded feed layer uses 50 Ω line stubs to excite the aperture coupled patches. Part of the antenna feed network is embedded in the LCP and fed through a signal via from the bottom layer. This is to allow additional room for packaging components on the bottom metallization feed layer. For both the embedded and bottom feed layers, reactive 3 dB power dividers are used to parallel feed the antenna array. There are several 50 Ω microstrip-to- CPW transitions on the bottom layer to accommodate the integrated circuit packaging. These CPW lines consist of a 375 µm wide signal line, 100 µm gap and 2680 µm wide ground lines. The ground lines have vias connecting to the embedded ground layer to prevent unwanted propagating modes. The microstrip lines on this layer are 446 µm wide.

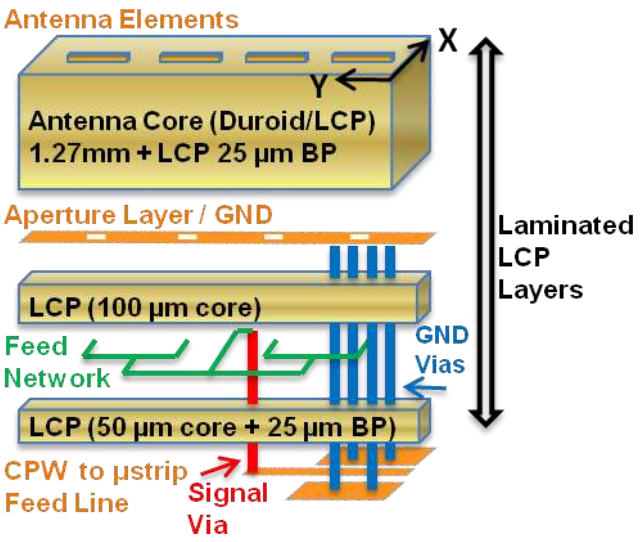
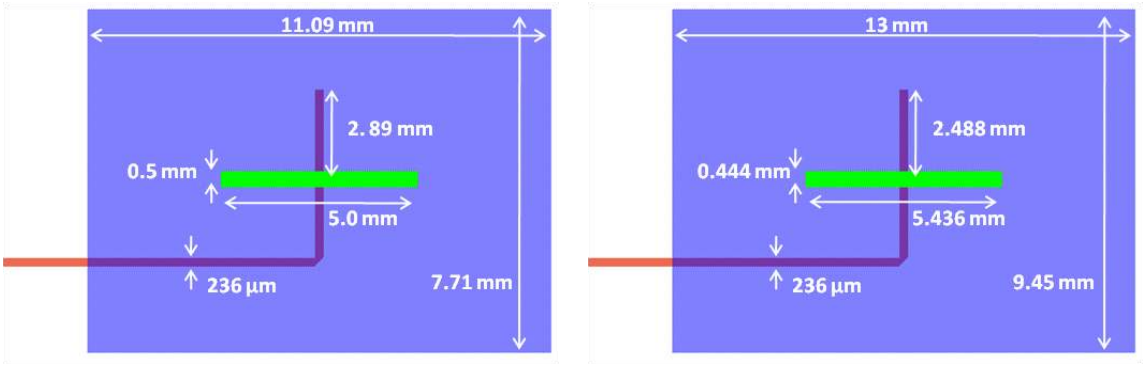


Figure 4.1: Stack up of multilayer antenna array showing only one column with four elements.



(a) (b)

Figure 4.2: Dimensions of each aperture coupled patch for the a.) 4x1 and 8x1 antenna array using an LCP antenna layer and b.) 8x2 antenna array using a Duroid antenna layer.

Each antenna is designed and modeled using HFSS simulation software. The return loss and far-field patterns are simulated and optimized for the design frequency and required bandwidth. The designs aim to make a return loss better than 10 dB across the 500 MHz bandwidth.

An anechoic chamber is used to measure the radiation patterns from 8.5 GHz to 10.5 GHz. Each antenna is mounted vertically on a stand and placed in the near-field of an X-band rectangular waveguide antenna. A cylindrical scan is necessary to

accommodate the broad beamwidth in the azimuth direction. After completion of the radiation patterns, the broadside gain of the antennas are measured over the frequency band. This data is then compiled with the near-field data and transformed to the far-field. Plots of the measured Electric (E) and Magnetic (H) planes taken at 9.5 GHz are compared with results simulated in HFSS. These are discussed further in the following sections.

The measured gain for passive and active antenna arrays is presented with a distinction between the associated units. Traditionally, the unit *dBi* is used to indicate a measure of gain for an antenna. However, this infers that the gain is referenced to an isotropic radiator with 100 % efficiency. Theoretically, the highest achievable antenna gain is equal to its directivity. It would not be appropriate to use *dBi* for active antennas because the measured gain is a product of an IC plus the antenna gain, which often leads to a value higher than the directivity. Doing so would infer that the antenna has efficiency greater than 100 %, which is theoretically impossible. In this chapter, the terms 'system gain' or 'active gain' are used to imply that the measurement incorporates gain from additional components integrated on the antenna. These values are associated with the unit *dB*. Additionally, the directivity will be presented to offer the reader insight to the radiation pattern beamwidths. For a passive antenna, the gain can sometimes provide insight as to the maximum theoretical beamwidth. This correlation is lost in providing only the measured gain of an active antenna since the beamwidth is often much wider than the theory would dictate.

4.2 4 x 1 Antenna Array

The first building block of this work integrates an X-band SiGe LNA onto a functioning 4x1 array [78]. A single column of four microstrip patch antenna elements are spaced 27 mm apart, consistent with the design requirements set for the final 8x2 phased array. This is excited by a BFN and CPW line structure that were designed and routed

within the LCP feed layers. The CPW feed line was designed intentionally for compatibility with the LNA packaging.

The antenna array was initially designed and optimized without the inclusion of the LNA. By designing and measuring a passive (also referred to as *baseline*) version of the antenna, a direct correlation could be attained for the added performance of the incorporated IC. The passive antenna design was modeled in HFSS using a thru-line in place of the LNA, shown in Figure 4.3. The return loss and far-field patterns were simulated and optimized for the design frequency and required bandwidth. The return loss is shown in Figure 4.4. The design clearly makes a return loss better than 10 dB across the 500 MHz bandwidth. The directivity and gain were both simulated at 9.5 GHz and determined to be 13 dBi and 9.2 dBi, respectively. The low efficiency of this antenna is due to the large corporate feed network necessary to uniformly excite the patch antennas and to package the active component.

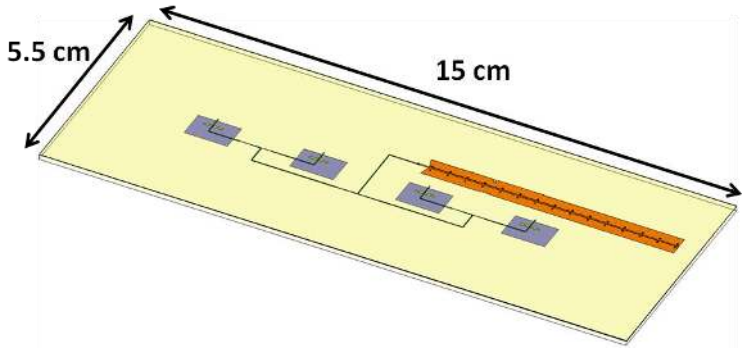


Figure 4.3: HFSS model of passive 4x1 antenna array.

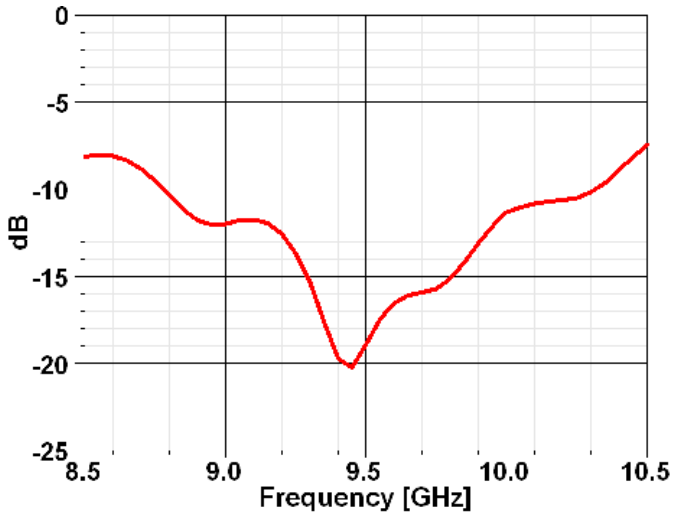


Figure 4.4: Simulated S_{11} plot of passive 4x1 antenna array.

The LNA packaged on this array was fabricated in a 0.13 µm BiCMOS SiGe technology and designed using the inductively degenerated cascode architecture. The circuit was designed for ultra-low noise performance while simultaneously achieving a power match. It has a self-bias circuitry to simplify total design and requires only a 2.5 V DC supply. The amplifier consumes only 22 mW of DC power and has a reported 17 dB of gain (G_{LNA}) and 1.37 dB noise figure (NF_{LNA}) across X-band (9.5 GHz to 10.5 GHz). The die is matched to 50 Ω at all RF ports on chip, thus no matching network was needed on package. It comes with standard 150 µm pitch aluminum pads for wire bond packaging. Further details of the LNA design are discussed in [79].

The LNA chip was diced from its original wafer using a soft 50 µm wide cutting blade. The die size was kept to a minimum to reduce wire bond length. After dicing, the chip dimensions were measured to be 820 µm x 940 µm. Prior to packaging, the LNA was measured on chip to ensure performance integrity.

To ensure the LNA performed properly on the array, it was first packaged separately on LCP using the same CPW feed line structure for the antenna design. The packaging layout is shown in Figure 4.5. The LNA was mounted using silver epoxy and allowed to cure for 20 minutes at 120 °C. The chip pads were then wire bonded onto the

copper traces on LCP. The wire bonds were done using a ball-wedge wire bonder utilizing a 38 µm diameter gold bond wire. This type of wire bonder uses heat applied to the sample and ultra-sonic energy to make a weld between contact points.

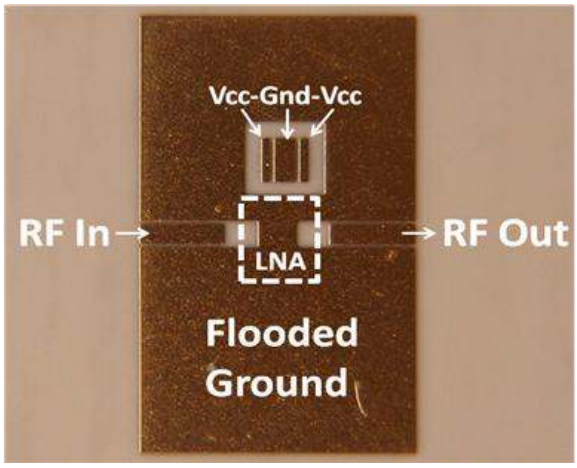


Figure 4.5: Layout for the packaged LNA.

Measurements of both the wafer level and package level LNA were done using GSG CPW probes. The LNA was biased at a Vcc = 2.5 V drawing a current of 6 mA. The S-parameters were recorded using an Agilent E8361C PNA. Measurement comparisons of the bare LNA versus the packaged LNA are seen in Figure 4.6. This plot shows a slight degradation of performance in the packaged LNA which is expected due to added parisitics from the wire bonds. Over the frequency of interest, there is a 0.5 dB of loss in output gain for the packaged LNA. This implies there will be about 16.2 dB of added gain to the antenna. This number was expected to vary slightly for each LNA.

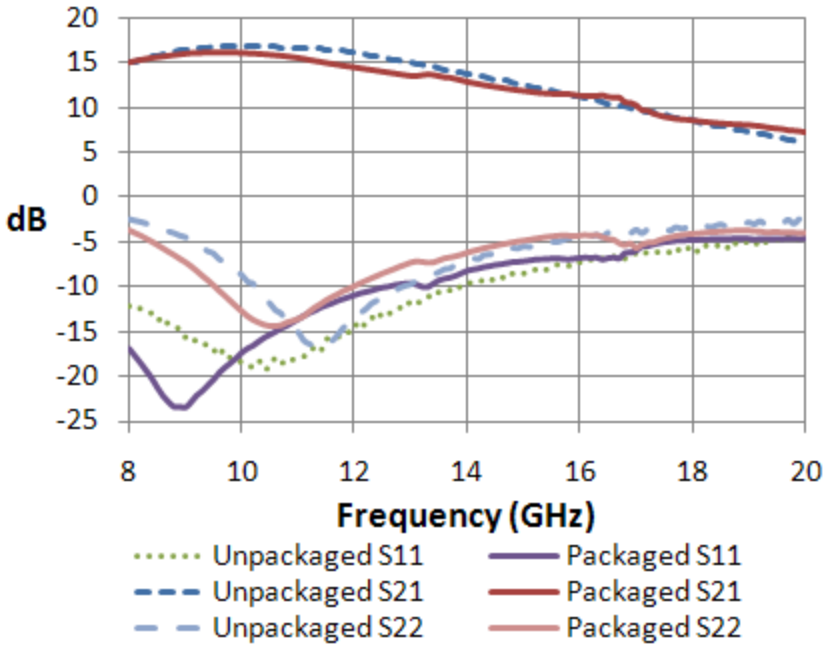


Figure 4.6: Comparison plot of the unpackaged and packaged LNA.

The baseline 4x1 antenna array was modified to integrate the LNA using the same packaging layout seen in Figure 4.5. This layout was integrated into the already existing CPW feed line and the bias lines were extended out to 2 mm x 2 mm pads where a wire could be attached for easier operation. Figure 4.7 shows a photograph of the packaged LNA. The assembled antenna with integrated LNA is shown in Figure 4.8.

Figure 4.7: Picture of the packaged LNA on antenna array.

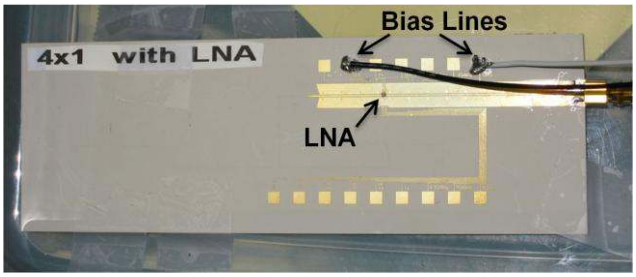


Figure 4.8: Picture of the antenna array with integrated LNA.

After fabrication of both the baseline antenna and the LNA integrated antenna, SMA connectors were soldered to the inputs. The return loss was measured on the network analyzer and an anechoic chamber was used to obtain the radiation patterns. As shown in Figure 4.9, the baseline antenna has a return loss greater than 8 dB over the design bandwidth and the LNA integrated antenna is greater than 10 dB. This deviation from simulated results is attributed to misalignment during fabrication and the large corporate feeding network.

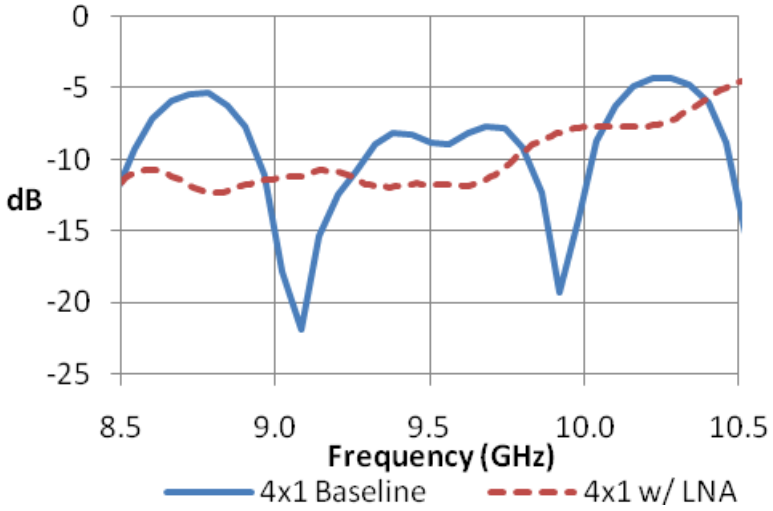
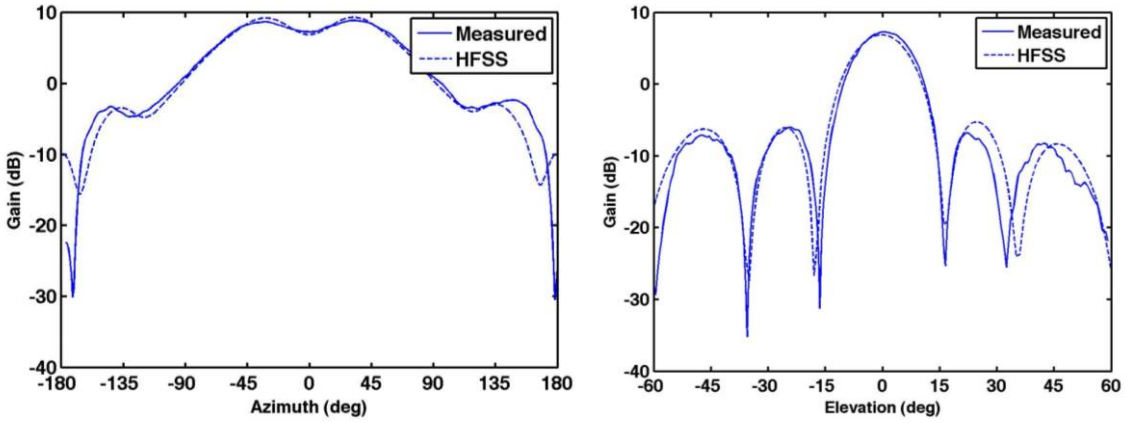


Figure 4.9: S_{11} plot for the baseline and packaged LNA 4x1 antenna array.

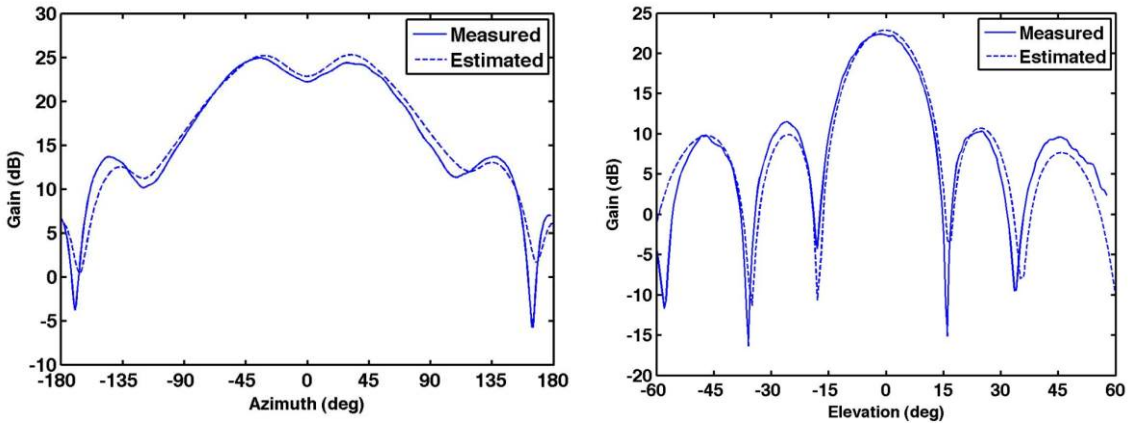
Plots of the measured E & H planes taken at 9.5 GHz are compared with results simulated in HFSS. As shown in Figure 4.10, the 4x1 baseline antenna results are very closely matched to those in simulation. The broadside gain of this antenna was measured at 9 dBi. Likewise, Figure 4.11 shows the 4x1 antenna with packaged LNA having

similarly good correlation with the expected results. The broadside system gain of this antenna was measured at 25 dB. The estimated radiation patterns for the antenna with packaged LNA uses the simulated results for the baseline antenna adjusted by the predicted additional gain (16.2 dB) for the packaged LNA. For both antennas, the location of peaks and nulls correspond very well and the maximum gain is within 1.0 dB of the simulated results. The 3 dB beamwidths at 9.5 GHz are seen in Table 4.1. There appears to be only a slight difference between both antennas and that in simulation. A comparison of gain over the frequency band is plotted in Figure 4.12. The 3 dB bandwidth for the gain is well beyond the 500 MHz design requirement for both antennas.



(a) (b)

Figure 4.10: Measured a.) E-Plane and b.) H-Plane at 9.5 GHz of the baseline 4x1 array.



(a) (b)

Figure 4.11: Measured a.) E-Plane and b.) H-Plane at 9.5 GHz of the 4x1 array with integrated LNA.

Table 4.1

4x1 antenna array comparison of half-power beamwidths @ 9.5 GHz

Antenna	**Elevation**	**Azimuth**
Simulated 4x1 baseline	16°	129°
Measured 4x1 baseline	17.5°	130°
Measured 4x1 with integrated LNA	15.5°	123°

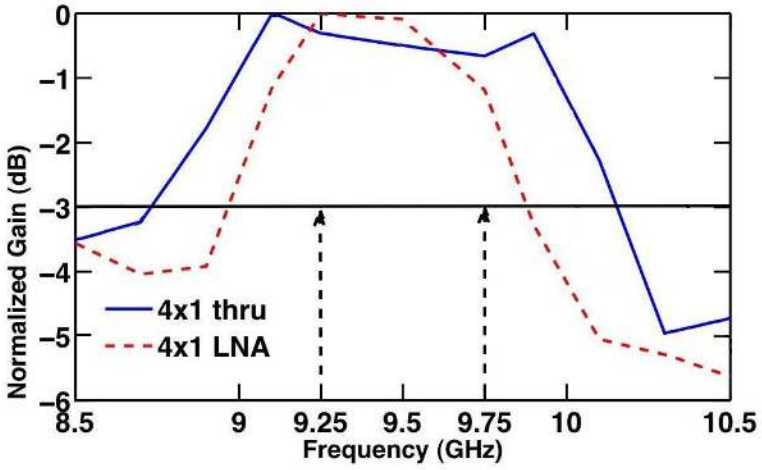


Figure 4.12: Normalized gain plot comparison.

4.3 8 x 1 Antenna Array

The next step for developing the 8x2 phased array is incorporating a phase shifting capability. This section demonstrates a SiGe 3-bit PS, in addition to the LNA, packaged onto an 8x1 array [80]. The previously discussed passive 4x1 array design has been expanded into an 8x1 antenna array using the same element spacing with a modified BFN. This was modeled using HFSS, shown in Figure 4.13. The return loss and far-field patterns were simulated and optimized for the design frequency and required bandwidth. The design clearly makes a return loss better than 10 dB across the 500 MHz bandwidth. The directivity and gain were simulated at 9.5 GHz and found to be 16 dBi and 9 dBi, respectively.

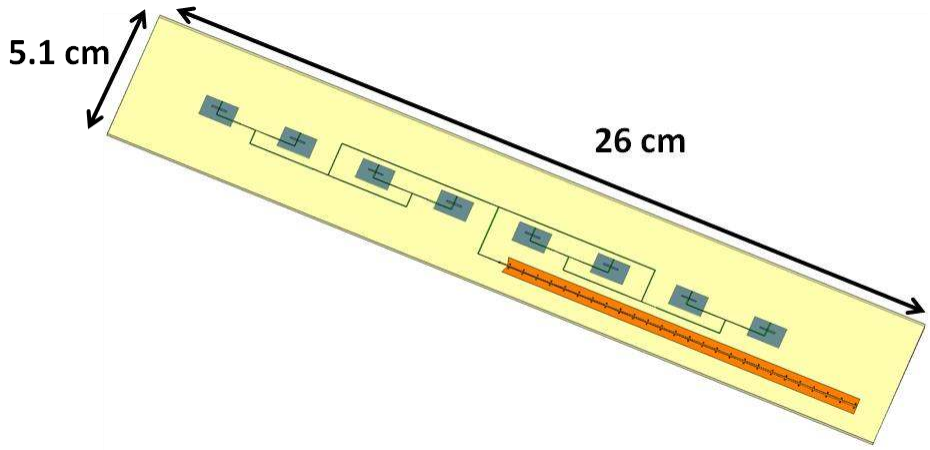


Figure 4.13: Model of the 8x1 antenna array.

The phase shifter incorporated into this antenna is a dual channel device with each channel consisting of two LNAs and a 3-bit CMOS phase shifter, illustrated in Figure 4.14. Each channel consumes only 4 mW of DC power while achieving a gain (G_{PS}) of over 10 dB, a noise figure (NF_{PS}) less than 5 dB, and an OTOI of over 10 dBm. In addition, the RMS gain and phase errors were reported less than 0.5 dB and 2º, respectively. The internal LNAs were designed using the power-constrained inductive degeneration design technique outlined in [54]. The Hi/Lo pass phase shifter was

designed using CMOS single-pole-double-throw (SPDT) switches to toggle between hi- and low-pass filter sections. In this work, only one channel will be used from each die.

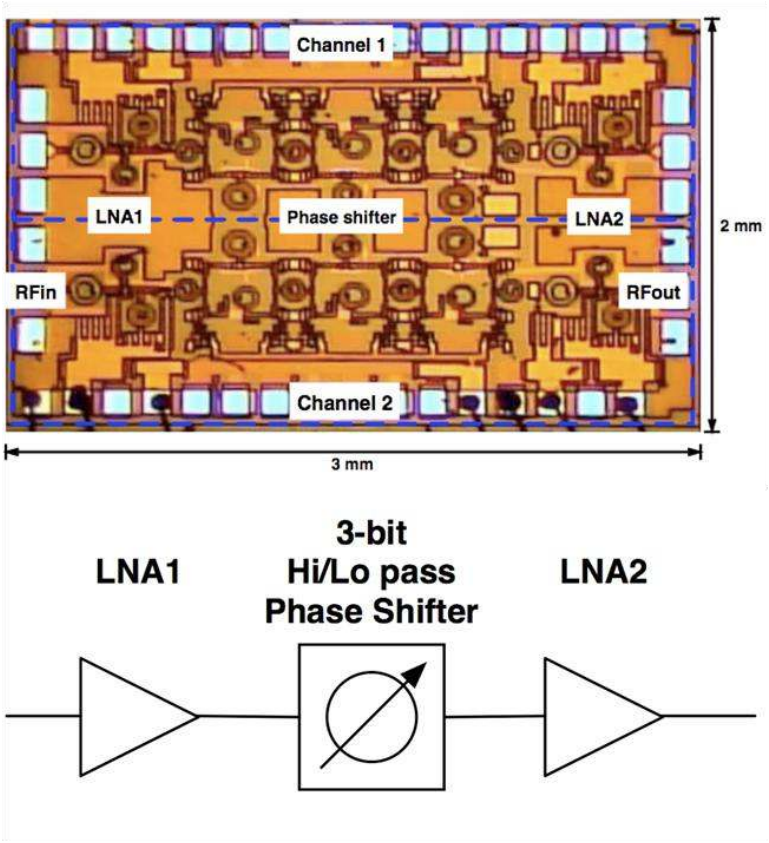


Figure 4.14: Picture and schematic of the SiGe phase shifter.

This device requires several DC supplies. This includes a 0.85 V and 1.5 V bias for each LNA and a 1.2 V and 2.4 V bias for each bit on the phase shifter. It is matched to 50 Ω at all RF ports on chip, thus no matching network is needed on package. It comes with standard 250 µm pitch aluminum pads for wire bond packaging. A more comprehensive description of the full phase shifter can be found in [58].

The SiGe PS was first packaged individually on LCP and characterized. The final package layout for this device is shown in Figure 4.18. The 4.7 kΩ resistor is used as an RF block for a wire bond that will connect the RF input of the PS to a DC bias line.

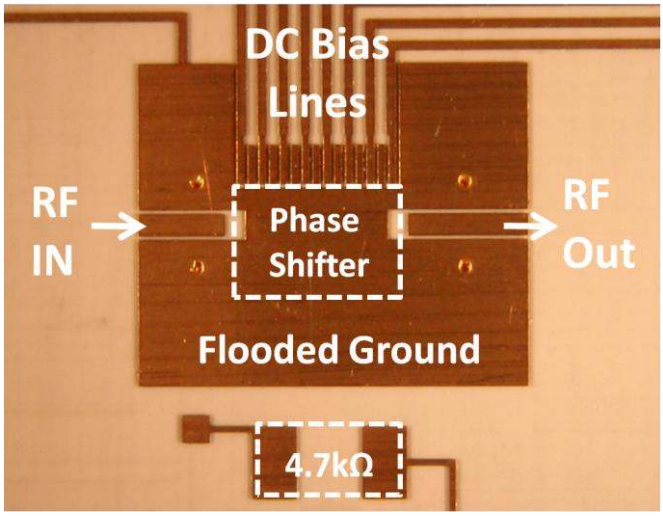


Figure 4.15: Layout for the packaged phase shifter.

S-parameters of the packaged PS were taken using the same measurement setup as the LNA and biased according to the specifications in [58]. Measurement comparisons of the bare PS versus the packaged PS are shown in Figure 4.16. This plot shows only slight degradation of performance for the packaged PS. At 9.5 GHz, the plot shows about 11 dB of added gain to the antenna from this packaged component. Obviously, this number will vary slightly for each PS and for each phase state. Also, as shown in Figure 4.17, there is a slight error in phase shift for each state. This will be accounted for in S*ection 4.4* when predicting the steering angle of radiation patterns. The largest disparity in phase shift between 9.25 GHz and 9.75 GHz for the unpackaged and packaged die was measured to be 5.8º.

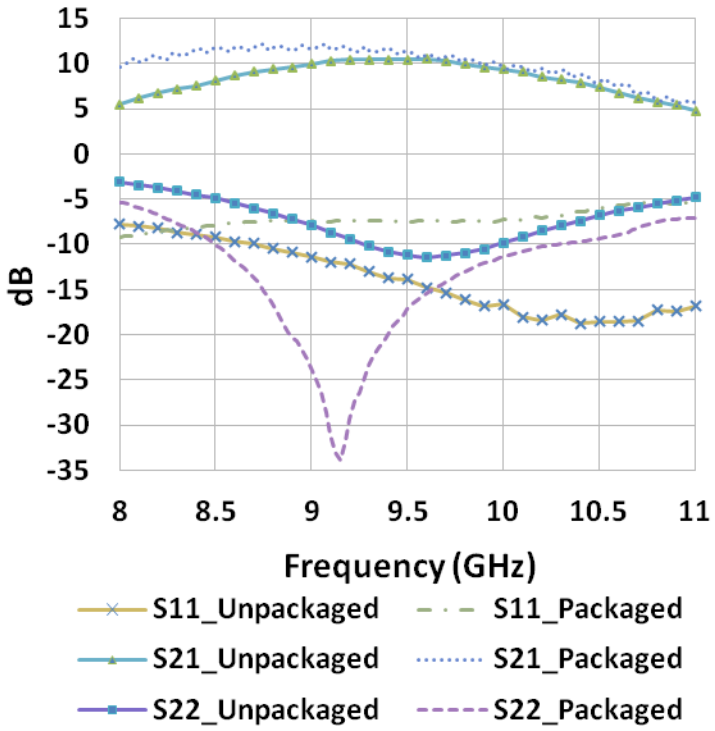


Figure 4.16: Comparison of S-parameters for the unpackaged and packaged phase shifter.

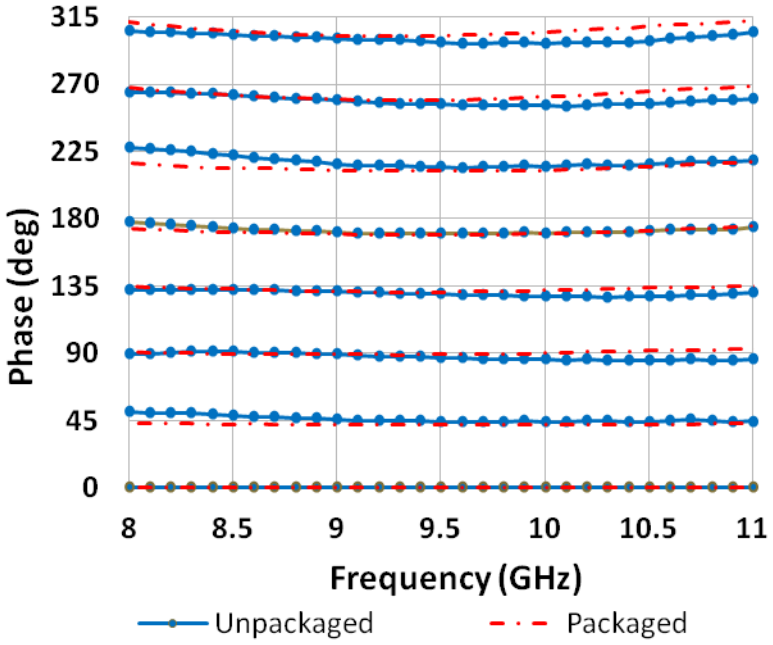


Figure 4.17: Comparison of unpackaged and packaged phase shifter for each phase state.

After verifying the LNA and PS could be successfully packaged on LCP, the next step was to package both in series on LCP. The packaged LNA and PS are shown in Figure 4.18. The effective S-parameters were estimated by using those acquired from the individually packaged LNA and PS and using ADS to simulate them in series. The measured and simulated S-parameters are shown in Figure 4.19. The measurements match very closely with the simulations. From these results, it is shown that the packaged LNA and PS will add about 26.6 dB of gain to the antenna array. Since the simulated gain of the 8x1 baseline antenna is 9 dBi, it was predicted that the 8x1 with packaged LNA and PS would have a front-end system gain of around 35.6 dB. This gain could be improved by increasing the bias voltage to compensate for the added loss from packaging; however, this is not recommended as it would stress the bias circuitry and potentially damage the chips.

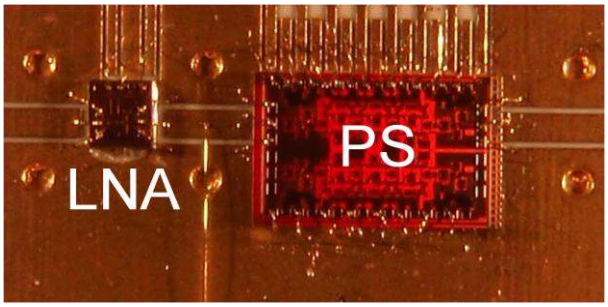


Figure 4.18: Picture of the packaged SiGe LNA and PS.

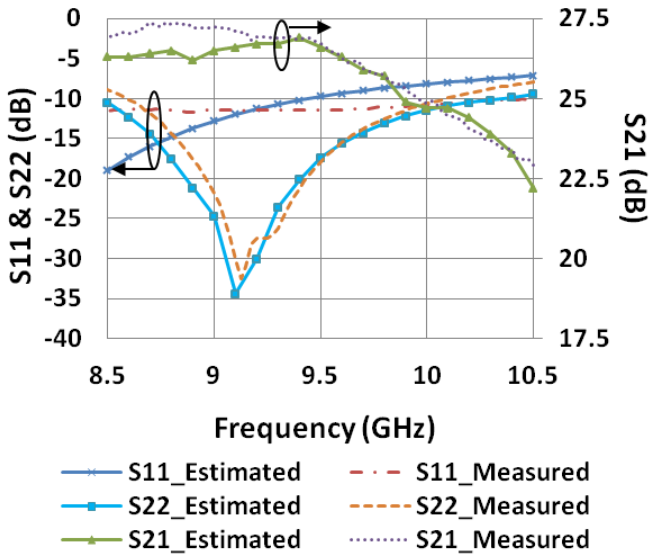


Figure 4.19: Comparison of measured and simulated S-parameters for LNA and phase shifter packaged in series on LCP.

Two antenna boards were fabricated to verify the added performance of the integrated PS. An 8x1 array with packaged LNA was assembled and tested to provide a baseline for the 8x1 array with packaged LNA and PS. A picture of the assembled LNA/PS integrated antenna is shown in Figure 4.20. The S-parameters of both antennas were measured on a network analyzer and showed a return loss around 10 dB across the desired frequency band (Figure 4.21).

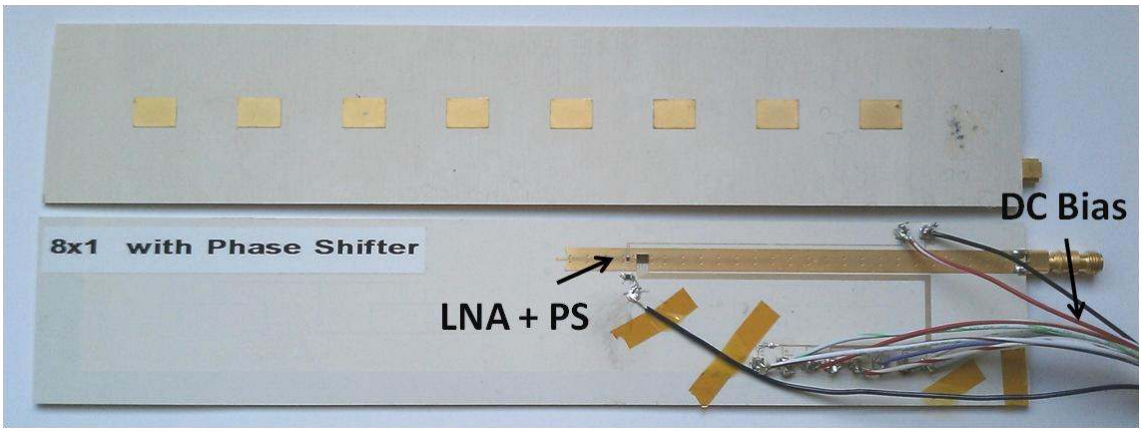


Figure 4.20: Front and back picture of the assembled 8x1 antenna array with integrated LNA and PS.

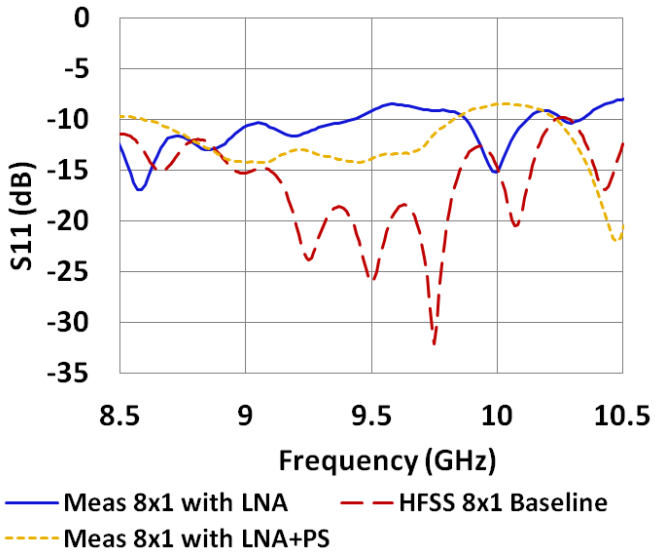


Figure 4.21: Return loss of the simulated baseline array and measured active arrays.

The assembled array being measured in the anechoic chamber is depicted in Figure 4.22. Plots of the measured E and H planes taken at 9.5 GHz are compared with results simulated in HFSS. The data from the pattern measurements are plotted in Figure 4.23 and Figure 4.24. The estimated radiation patterns for the antennas use the results for the simulated baseline antenna adjusted by the predicted additional gain (16 dB and 26 dB) for the packaged LNA and packaged LNA and PS. The measured active gain of the 8x1 with LNA and the 8x1 with LNA and PS was approximately 25 dB and 34 dB, respectively. In addition, the side lobes were within -10 dB to -13 dB with respect to the peaks. For both antennas, the location of peaks and nulls correspond very well and the maximum gain is within 1.0 dB of the estimated results. Surface roughness of LCP, misalignment tolerance during fabrication, and loss contributed by the vias and connectors are attributed to any deviation from simulation.

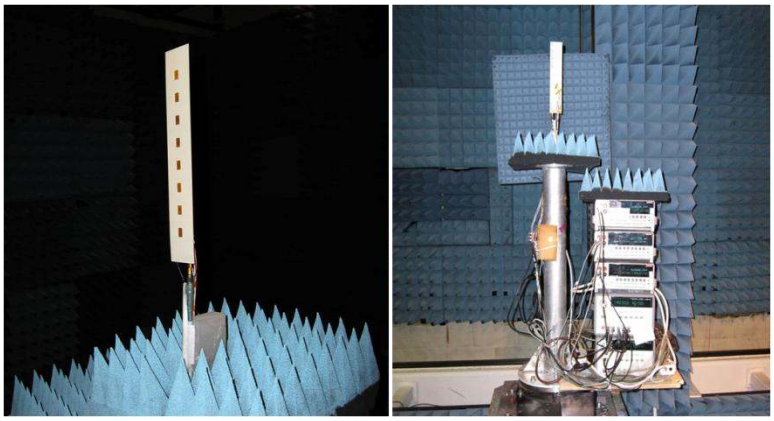
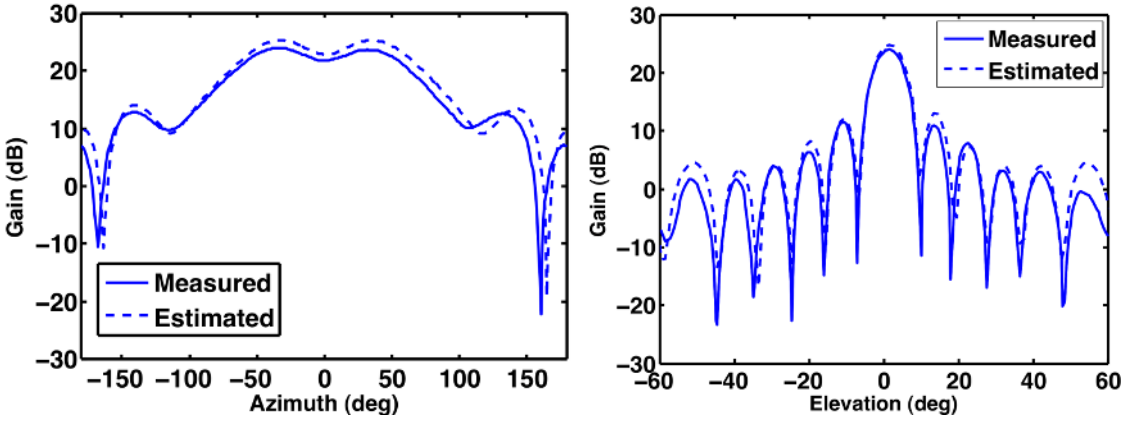
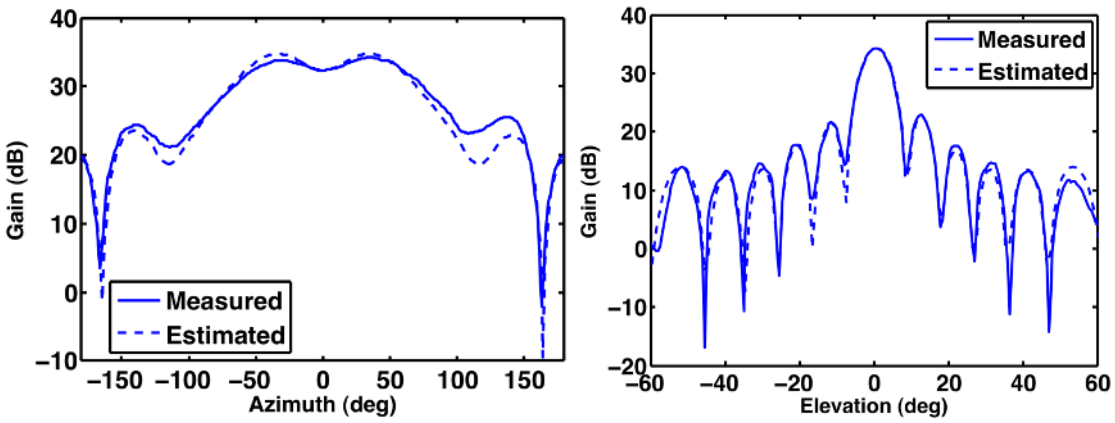


Figure 4.22: Antenna chamber setup of 8x1 array with SiGe LNA and PS.



(a) (b)

Figure 4.23: Measured a.) E-Plane and b.) H-Plane at 9.5 GHz of the 8x1 array with integrated LNA only.



(a) (b)

Figure 4.24: Measured a.) E-Plane and b.) H-Plane at 9.5 GHz of the 8x1 array with integrated LNA and PS.

Measured and simulated beamwidths at the central 9.5 GHz are shown in Table 4.2. Simulated results of the passive antenna are, as expected, very similar to the results of the measured active antennas.

Table 4.2

8x1 antenna array comparison of half-power beamwidths @ 9.5 GHz

Antenna	**Elevation**	**Azimuth**
Simulated 8x1 baseline	7°	114°
Measured 8x1 with integrated LNA	8°	121°
Measured 8x1 with integrated LNA & PS	7.5°	128°

The gain of the 8x1 with LNA and PS plotted over frequency is shown in Figure 4.25. The gain did not deviate more than 1 dB within the 500 MHz bandwidth of the center frequency (9.5 GHz). Only the first seven states of the phase shifter were measured due to the eventual failure of the on-chip digital control of the phase shifter caused by ESD. Future designs include ESD protection on the I/O pins, and should not affect performance, allowing robust operation of these antennas. The gain of the 270 degree

phase state is several dB down from the rest which is attributed to partial failure of the circuit and the last state (315 degree phase shift) was unable to be measured due to complete failure.

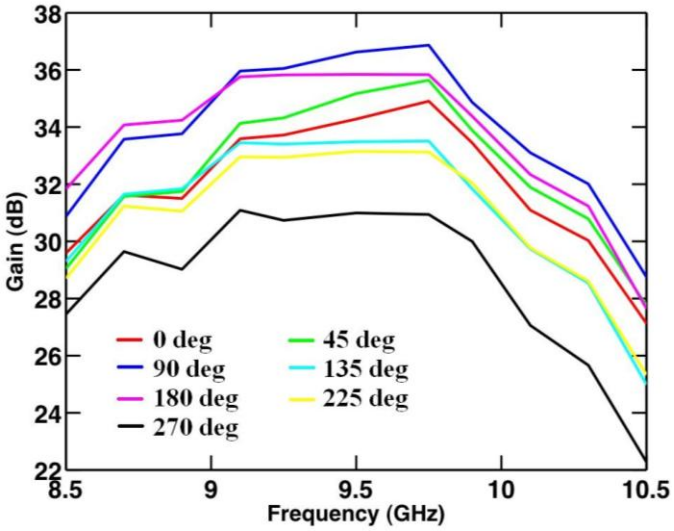


Figure 4.25: Gain versus frequency for each phase state of the 8x1 array with integrated LNA and PS.

4.4 8 x 2 Antenna Array

Thus far, substrate level integration of a SiGe LNA and PS has been demonstrated with good correlation of simulated and measured radiation patterns; however, no beam steering could be achieved. This section makes further progress by expanding the antenna to an 8x2 array design and incorporating an LNA and PS into each column of elements for beam steering capability [81]. The previously designed 8x1 array has been tiled with a spacing of 20 mm to include a second column of microstrip elements. Additionally, a 3 dB reactive power divider has been implemented on the bottom LCP layer to feed the embedded BFN for each column of elements. The passive array design was modeled in HFSS, shown in Figure 4.26. The return loss and far-field patterns were simulated and optimized for the design frequency and required bandwidth. The design clearly makes a

return loss better than 10 dB across the 500 MHz bandwidth. The directivity and gain was also simulated at 9.5 GHz and predicted to be 19.7 dBi and 15.2 dBi, respectively.

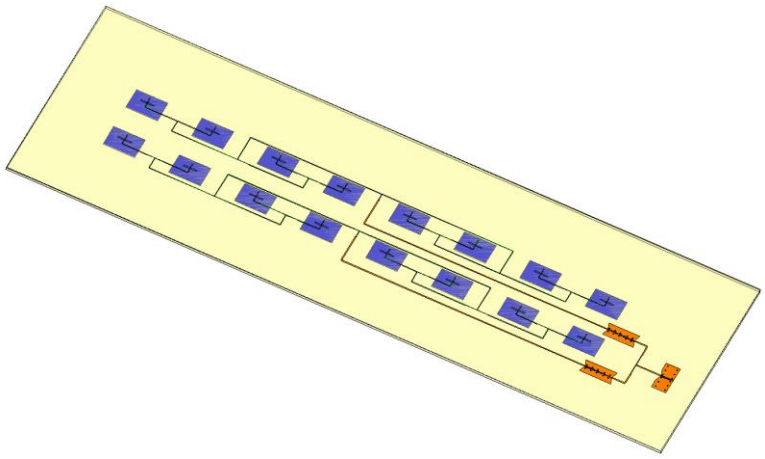


Figure 4.26: HFSS model of the 8x2 antenna array.

In order to steer the beam of the 8x2 array and maintain a large antenna gain, the SiGe LNA and PS used previously were incorporated into each column of the design. The baseline 8x2 antenna array was modified to integrate the LNA and PS using the same package scheme used for the 8x1 antenna. This layout was integrated into the already existing CPW feed lines. Also, the DC bias lines were extended out to 2 mm x 2 mm pads where a wire could be attached for easier control. A picture of the antenna with the integrated LNA and PS is shown in Figure 4.27. As shown in Figure 4.17, there is a slight error in phase shift for each state of the device. This will be accounted for while predicting the steering angle of the radiation patterns.

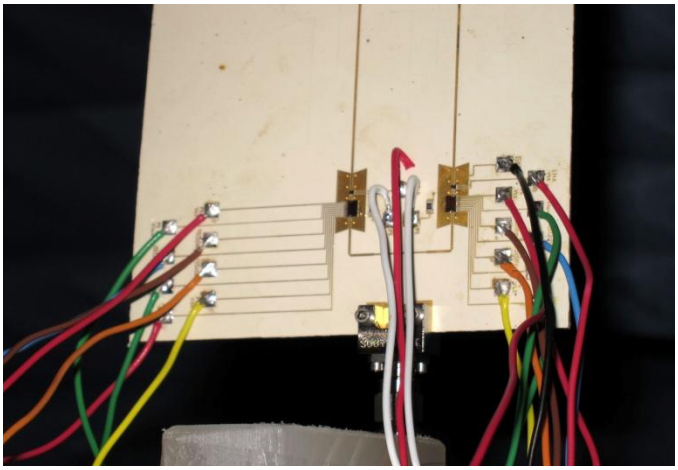


Figure 4.27: Picture of the packaged LNA and phase shifter on the 8x2 antenna array.

After fabrication of both the baseline antenna and the LNA/PS integrated antenna, SMA connectors were attached to the outputs. Because the active antenna required several DC supplies to power it, a low power supply board was built to accommodate all the necessary voltages. This board requires only a 5 V DC supply drawing 0.455 A and is capable of providing all the necessary DC biases for the LNA and PS. Also, since the phase shifter bits are controlled by a supply of 1.2 V or 2.4 V, a switch board was assembled for toggling through all the phase states. The entire setup is seen in Figure 4.28 and weighs only 12.6 ounces. The antenna array alone, with only a short wiring harness, weighs 3.5 ounces and consumes a total of 53 mW of DC power.

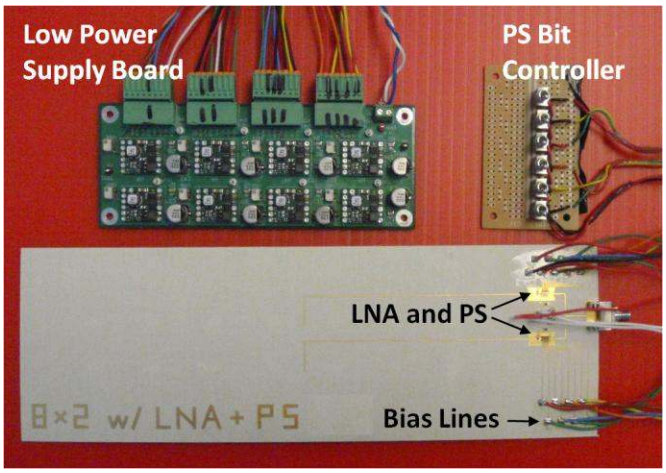


Figure 4.28: Picture of the assembled antenna array with low power supply board and phase shifter bit controller.

Both antennas were measured on a network analyzer and maintained a return loss better than 10 dB across the desired frequency band, shown in Figure 4.29. The simulation results compared to the measured baseline antenna are very close and show only a 100 MHz shift in frequency.

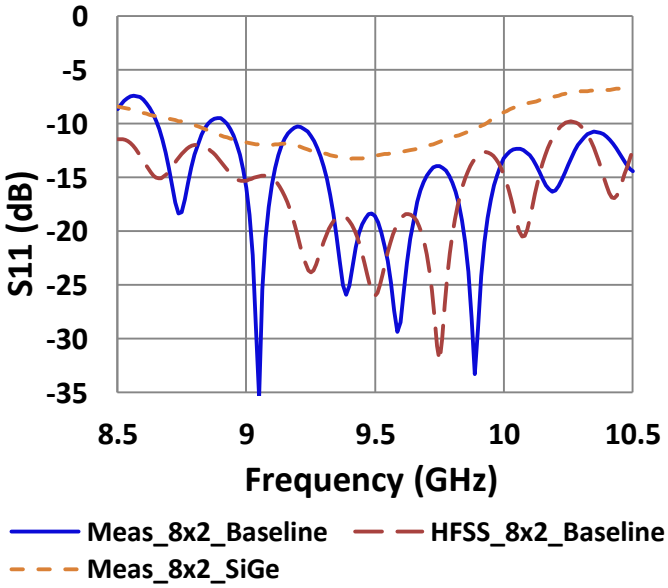


Figure 4.29: S_{11} plot of the simulated and measured 8x2 antenna arrays.

A picture of the antenna under test (AUT) in the anechoic chamber is shown in Figure 4.30. Plots of the measured E & H planes taken at 9.5 GHz are compared with results simulated in HFSS. As shown in Figure 4.31, the 8x2 baseline antenna results are very closely matched to those in simulation. The broadside gain of the baseline antenna was measured to be 15.1 dBi. The location of peaks and nulls correspond very well and the max gain is within 0.1 dB of the simulated results. A plot of the measured gain over frequency compared with simulations is shown in Figure 4.32. Over the frequency band of interest (9.25 GHz to 9.75 GHz), there is a 1.2 dB variation in gain.

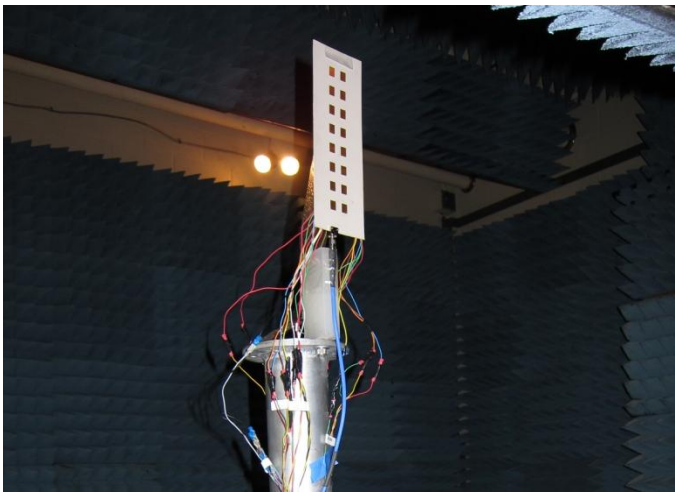
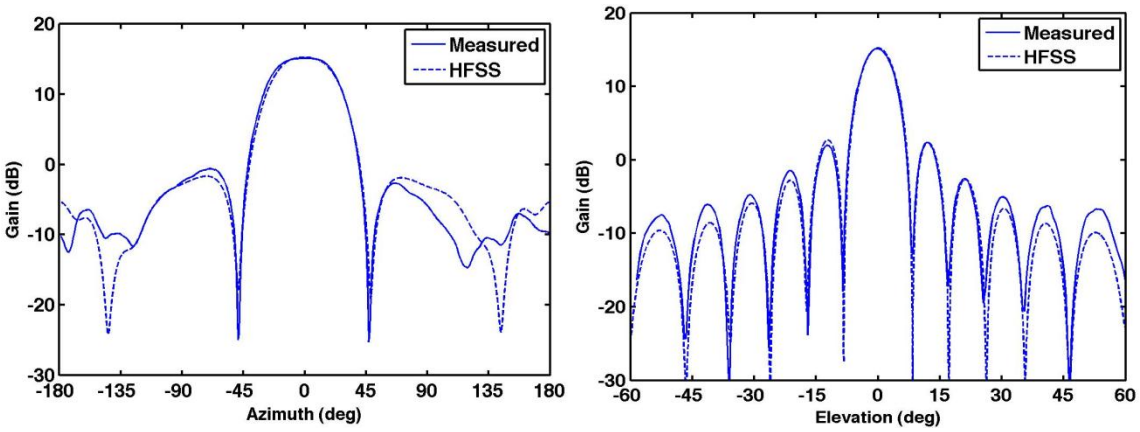


Figure 4.30: Picture of the 8x2 antenna array being measured in the anechoic chamber.



(a) (b)

Figure 4.31: Measured a.) E-Plane and b.) H-Plane at 9.5 GHz of the 8x2 baseline antenna array.

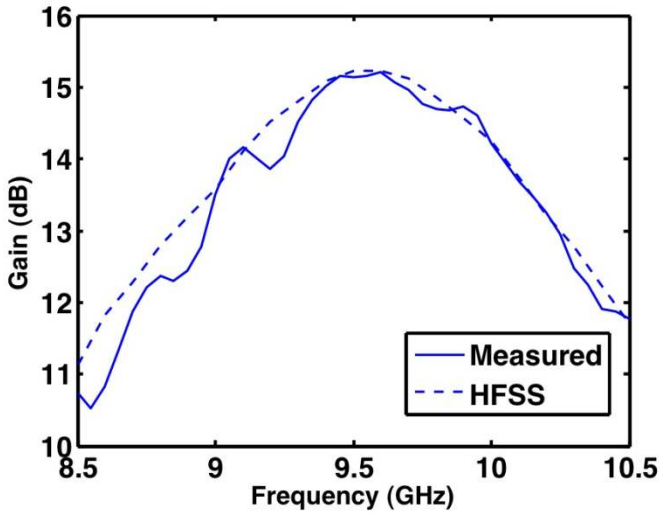
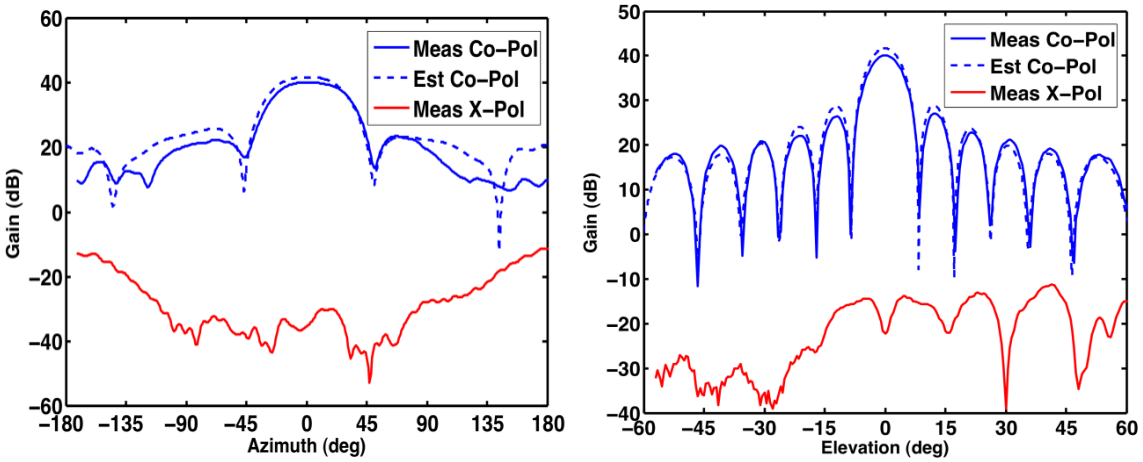


Figure 4.32: Gain versus frequency of the 8x2 baseline antenna array.

Measurements for the 8x2 antenna with packaged LNA and PS are shown in Figure 4.33 and Figure 4.34. It is seen that these measurements are very close to the predicted radiation patterns. The estimated radiation patterns in Figure 4.33 use the simulated results for the baseline antenna adjusted by the predicted additional gain of 26.6 dB provided by the packaged LNA and PS. The measured front-end system gain at broadside seen in these figures is 40.1 dB. Using the gain of the baseline antenna as a control, the additional gain supplied from the LNA and PS is calculated to be 25 dB. The

low cross-polarization gain shown in these figures confirm the linear polarization of the antenna. The beam steering capability is shown in Figure 4.34. The radiation patterns are normalized to compare the measured beam steering with the simulated beam steering predicted in HFSS. The beam steering angles are more clearly seen in Table 4.3. The measured beam steering angle compared to simulation has a maximum error of 5.5° and an RMS error of 3.2°.



(a) (b)

Figure 4.33: Measured a.) E-Plane and b.) H-Plane at 9.5 GHz for the 8x2 antenna array with packaged SiGe LNA and phase shifter.

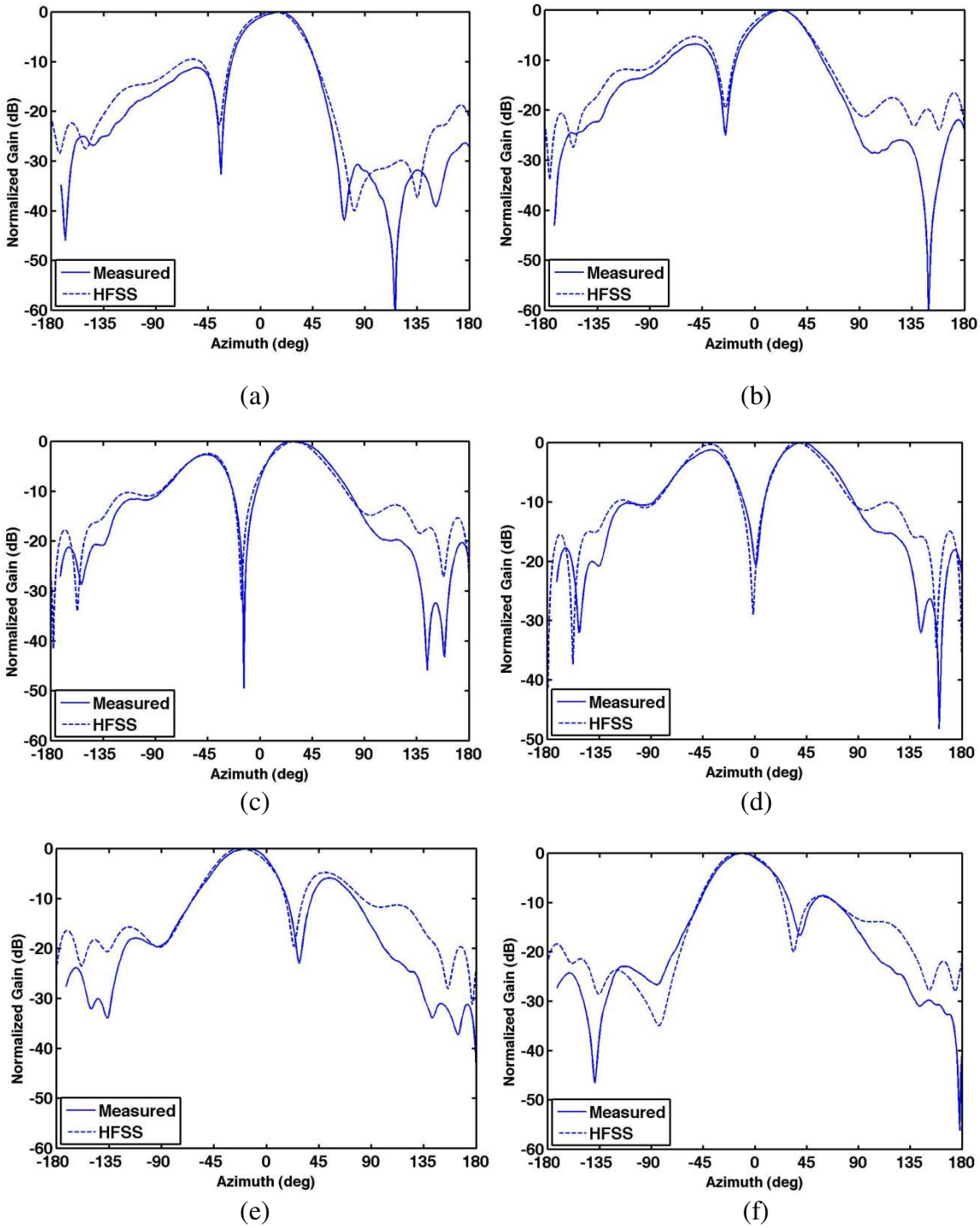


Figure 4.34: Normalized E-plane at 9.5 GHz of the 8x2 antenna array with a.) 44 degrees, b.) 87 degrees, c.) 129 degrees, d.) 170 degrees, e.) 257 degrees, and f.) 299 degrees phase change.

Table 4.3

Comparison of pattern beam steering @ 9.5 GHz

Phase Shift	Simulated	Measured
0 deg	0º	0º
44 deg	12º	16º
87 deg	20.5º	22º
129 deg	30º	27º
170 deg	36.5º	41º
215 deg	-31.5º	-31º
257 deg	-22.5º	-17º
299 deg	-13º	-11º

A comparison of antenna gain over the frequency band is plotted in Figure 4.35. The 3 dB bandwidth for the gain is over 10 % for all beam steering states, which is well beyond the 500 MHz design requirement.

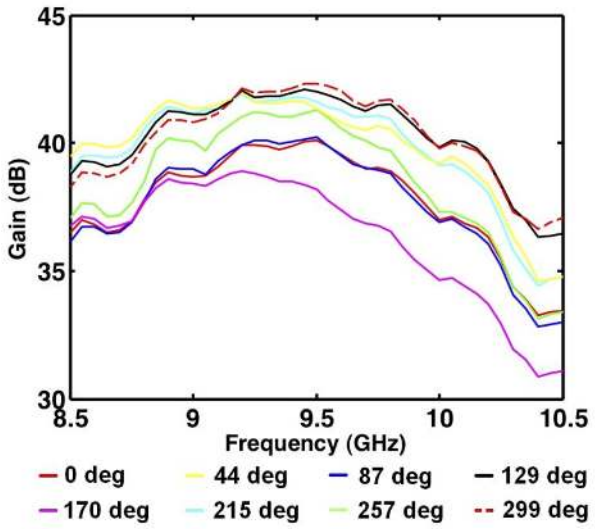


Figure 4.35: Gain versus frequency of the 8x2 antenna array for all phase changes.

The 3 dB beamwidths at 9.5 GHz are seen in Table 4.4. The simulated results of the passive antenna match very closely with the measured results of the baseline antenna and, as expected, are very similar to the results of the active antenna.

Table 4.4

8x2 antenna array comparison of half-power beamwidths @ 9.5 GHz

Antenna	Elevation	Azimuth
Simulated 8x2 baseline	7.5º	47º
8x2 baseline	8º	50º
8x2 with LNA & PS 0 deg	8.5º	50º
8x2 with LNA & PS 44 deg	8.5º	46º
8x2 with LNA & PS 87 deg	8º	41º
8x2 with LNA & PS 129 deg	7.5º	43º
8x2 with LNA & PS 170 deg	8º	45º
8x2 with LNA & PS 215 deg	7.5º	49º
8x2 with LNA & PS 257 deg	7.5º	44º
8x2 with LNA & PS 299 deg	7.5º	44º

Using the measured and simulated data of the antenna and active components, the resulting added noise performance of the system was determined. As discussed in [82] and [83], this is conventionally done by calculating the noise figure, NF_T, and FOM ratio, *G/T,* referenced at the output of the antenna. In this work, these parameters were calculated using

$$\mathrm{NF_T} = L_{A1} + (NF_{LNA} - 1)L_{A1}L_R + \frac{(NF_{PS}-1)L_{A1}L_{R1}}{G_{LNA}} \tag{4.2}$$

and

$$\frac{G}{T} = \frac{D}{T_0(NF_T - 1)} \tag{4.3}$$

where T_0 is the standard reference temperature 290 K, D is the directivity of the antenna, and L_{A1} and L_{R1} are the Ohmic loss and mismatch loss, respectively, in the feed line between the antenna element and LNA. From these equations, it is clear that when the LNA gain, G_{LNA}, is sufficiently large, the feed line loss and LNA noise figure will have the most effect on performance, and the components following it will have a negligible effect. Since this is true of this case, only the PS term is included in this calculation and the loss of the antenna feed line after the PS is ignored.

The measured and simulated results for this antenna were used to calculate the system noise performance. The directivity of the antenna was calculated to be 19.7 dBi using the measured radiation patterns at 9.5 GHz. The loss in the feed line, and the noise figure of the packaged LNA and PS were simulated in HFSS and ADS, respectively. These simulations showed a L_{A1} of 3.9 dB, a L_{R1} of 0.1 dB, a NF_{LNA} of 1.4 dB, and a NF_{PS} of 5.7 dB. The already measured gain of the packaged LNA at 9.5 GHz is 16.2 dB. Using these results, the NF of the system is 5.6 dB and the *G/T* is -9.4 dB/K. For this antenna, the ohmic feed line loss, L_{A1}, has the largest impact on these parameters and can be directly improved by moving the LNA and PS closer to the antenna elements. This would significantly lower the noise figure, thus increasing the G/T ratio.

4.5 Summary

This chapter has discussed the design of several passive and active antennas for the development of a lightweight, organic active receiving phased-array antenna. SiGe LNAs and PSs were successfully integrated onto an 8x2 antenna array fabricated using LCP and Duroid material. The measured return loss and radiation patterns were very comparable to those simulated. Using a passive version of the active array, a comparison showed excellent results from the packaged LNA and PS. The packaged components

supplied an additional 25 dB of increased gain to the antenna for a total of 40.1 dB in front-end system gain. The combined antenna and receiver performance yielded a *G/T* of -9.4 dB/K and a NF of 5.6 dB. Additionally, the antenna exhibited ±41° of beam steering capability. This is the first demonstration of such a lightweight, active receive antenna array in X-band built with low cost PCB fabrication technologies and Si-based RF electronics.

CHAPTER 5

60 GHZ SWITCHED-BEAM RECEIVER FRONT END

The demand for high-speed, high-capacity wireless communications has driven Gigabit-per-second (Gbps) applications into mm-wave frequencies where higher bandwidths can be achieved. In this regime, 60 GHz communications have received much attention because of the availability of unlicensed ISM bands and inherent propagation path loss in this spectrum [84]. These unique properties have spawned a path forward for short-range secure data transfer at ultra-high speeds, which requires a new generation of low-cost, compact, high-performance adaptive antennas [85].

The problems associated with this task reside not only in the system architecture but also in the selected platform material for system integration. LCP is an established low-cost alternative to ceramic technology for antenna applications due to its large panel processing. The low dielectric constant and loss tangent (ε_r = 3.16, tanδ = 0.004 @ 60 GHz) exhibited up to 110 GHz makes it a leader among competing materials [86]-[87]. Additionally, the thin-form availability of this material makes it a primary candidate for mm-wave applications where reduced feature sizes become critical for radio-frequency (RF) performance; conversely, LCP multilayer lamination capability also allows thicker layers for high antenna radiation efficiencies.

There are several techniques being investigated to improve antenna adaptability at V band. Phased array antennas utilize phase shifters integrated on substrate for controlled beam steering. In [88], a CMOS Hi-Lo pass switching phase shifter is used to control a 2x2 phased array on ceramic substrate. This device was integrated with several amplifiers to offset the high losses incurred. At mm-wave frequencies, there are limited types of low-loss phase shifters available for small size antenna applications. Switched line phase shifters have been used in conjunction with low-loss GaAs and MEMs switches [89].

This approach enables highly-directional arrays to scan a wide field-of-view with broadband performance. However, the inclusion of several integrated circuits (ICs) or multilayered structures necessary to achieve a wide beam scan drives up cost and consumes real estate. A low-cost solution is the use of switched-beam elements. By using a configuration of broad-side and end-fire antennas integrated together on a substrate, it is possible to achieve multiple beams controlled through a switch network. With this technique, antenna elements are oriented to radiate in various directions for multiple field-of-views that would otherwise be difficult to accomplish through phased-array beam steering [90]-[91]. While this technique avoids some inherent problems with phased arrays, it introduces blind spots between field-of-views that phased arrays can inherently solve.

A combined solution to these techniques is the integration of a switched beamforming network (BFN) that implements a phased array scanning capability [92]. One such structure is the Butler matrix, which consists of *N* number of RF inputs that independently feed *N* number of RF outputs with varying phase delays. This creates *N* number of fixed radiating beams accessed by the separate inputs. Utilizing this type of BFN reduces the number of ICs needed for conventional phase shifting techniques while retaining beam scanning capability. The structure is implemented in a variety of forms including substrate-integrated-waveguide (SIW) or microstrip lines. It has been successfully investigated as a viable solution for antenna beam switching capability at mm-wave frequencies where the size of the structure becomes inherently reduced [93]-[94]. In [95], a 4x4 Butler matrix was integrated with a 4x1 patch antenna array on Duroid substrate. This passive antenna structure demonstrated proof-of-concept beam steering capability but does not implement a switch network or integrate amplifiers for improved system performance.

Previously, a 4x1 quasi-Yagi array was developed on LCP for mobile platform integration at 60 GHz [96]. Using this design, a GaAs low-noise amplifier (LNA), power

amplifier (PA), and single-pole-double-throw (SPDT) switch were integrated for transmit and receive functionality [97]. Although substrate level integration was demonstrated, no beam steering could be achieved. The work discussed in this chapter makes further progress by redesigning the quasi-Yagi array to incorporate a Butler matrix for switched-beam functionality. Additionally, a switch network of GaAs SPDT switches are integrated to toggle between the beam states, and GaAs LNAs are integrated per antenna element to minimize the receive noise figure. These die are packaged and biased with a substrate level distribution network. This is the first fully integrated, lightweight V-band receive switched-beam antenna with GaAs LNAs and SPDT switches [98]. This work aims to serve as a building block for future low-cost Gbps antenna solutions.

5.1 System Layout

The 4x1 receive switched-beam array was designed for operation at 60 GHz and consists of several components, illustrated in Figure 5.1, that were co-designed and optimized for seamless integration. The antenna array was designed for maximum gain over a wide frequency band while maintaining 4 dB overlap points of the beams. The antenna element is a quasi-Yagi dipole array chosen due to its inherent small size and highly directional radiation patterns. A GaAs LNA was integrated onto each antenna element to both increase gain performance and minimize antenna noise figure (NF). The BFN utilizes a 4x4 Butler matrix to phase the antenna elements for beam steering capability. A switch network was implemented using three SPDT switches configured to feed from the four outputs of the Butler matrix to a single G3PO RF connector.

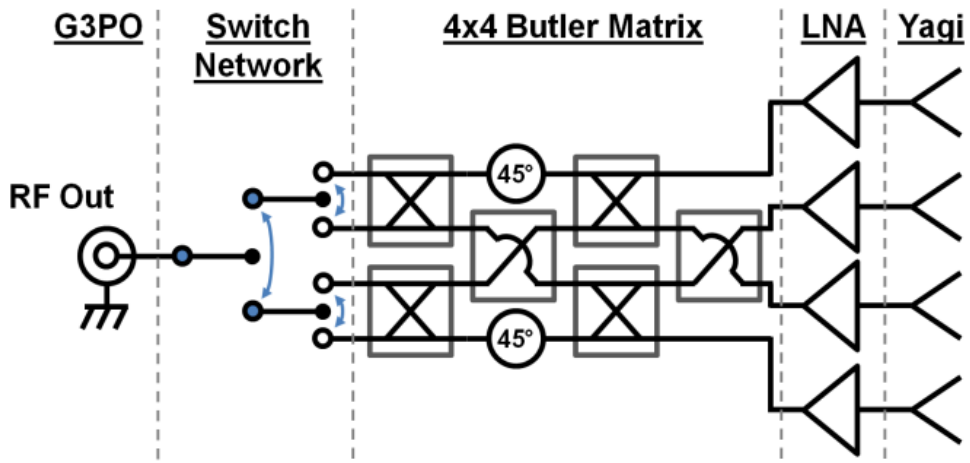


Figure 5.1: Schematic layout of the switched-beam array.

In designing each system component, trade-offs were assessed for deciding the LCP material and metal thicknesses. The thicknesses commercially available for LCP are 25 µm, 50 µm and 100 µm with 9 µm, 18 µm, or 35 µm copper metal cladding. For simplicity and cost-efficiency, a two metal stackup was chosen. The driving factors for choosing the material thickness were the Butler matrix performance, chip-to-package wire bond length, and minimum allowable feature size of the microstrip balun used for the dipole antenna element. Through several iterations of simulating each structure, it was found that a 50 µm thickness provided the best RF performance for the Butler matrix and chip packages while also maintaining feasibly achieved feature sizes for fabricating the microstrip balun. The chosen metal thickness was determined based on requirements for the bottom (ground) layer. This should be thick enough to withstand via and cavity lasering, and provide adequate thermal dissipation for the integrated amplifier. It was determined that at least 18 µm thick copper would be necessary for the lasering to avoid puncturing this layer and would also be adequate for thermal dissipation since the LNA is relatively low power.

5.2 Integrated Components Design

5.2.1 Butler Matrix

The Butler matrix consists of four RF inputs that independently feed four RF outputs with varying phase delays. The structure is host to a configuration of several microstrip quadrature hybrid couplers and phase delay lines. The purpose of this network is to uniformly feed the four antenna elements with progressive phase delays of -45°, +135°, -135°, and +45°, which is determined by the respective input port selected. The use of hybrid couplers provides high isolation between each input port, which allows a switch network to toggle between these ports without affecting the antenna performance. This creates four fixed radiating beams accessed by four independent inputs. Using the principle of reciprocity, this structure can be utilized in the same manner for transmitting or receiving antenna applications.

The individual components, as well as the entire Butler matrix structure, were designed using HFSS. It was found that using lines with characteristic impedances less than 50 Ω would be too wide to effectively design the hybrid couplers. Thus, the Butler matrix was designed for a system impedance of Z_0 = 70 Ω. The optimized hybrid coupler uses 70 Ω and 50 Ω lines having lengths of 930 µm and 780 µm, respectively. The simulated performance of this design has a return loss greater than 20 dB, an insertion loss less than 0.5 dB, and an isolation higher than 17 dB at 60 GHz over a bandwidth of 8 GHz. This served as a building block for the Butler matrix. The crossover structure uses two quadrature hybrid couplers in series spaced 925 µm apart with 70 Ω lines. This has a simulated performance of a return loss greater than 14 dB, an insertion loss less than 0.7 dB, and an isolation higher than 25 dB. The final layout of the 4x4 Butler matrix is shown in Figure 5.2.

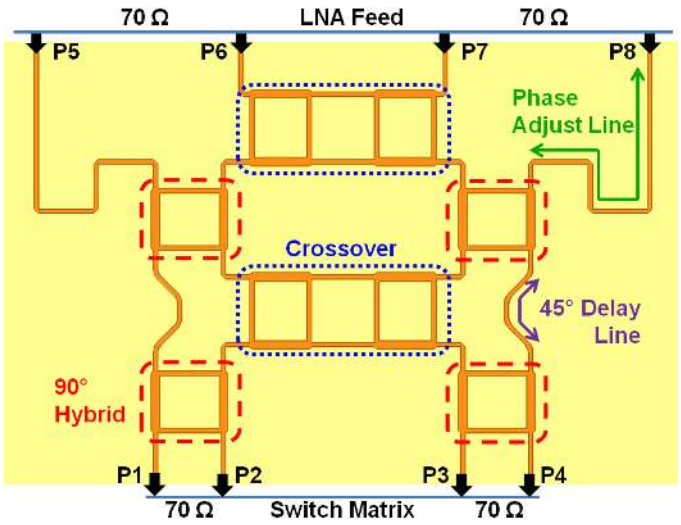


Figure 5.2: Model of the 4x4 Butler matrix.

For design purposes, the Butler matrix was optimized with matched ports; however, the implemented structure was to be incorporated with reflective switches on Ports 1-4. Because the Butler matrix maintains inherent isolation between these respective ports, the effect of reflective switches is minimal. The simulated performance of the Butler matrix is shown in Figure 5.3 - Figure 5.5. These results correspond to the assigned ports illustrated in Figure 5.2. Figure 5.3 shows the reflection coefficients when looking into each port. It maintains a return loss greater than 10 dB across the frequency band of 56 GHz to 67 GHz. Figure 5.4 shows the transmission coefficients associated with the toggled outputs of port 1 through 4. The variation of insertion loss for all ports is less than 1 dB from 56.5 GHz to 65.5 GHz. Figure 5.5 shows the simulated phase shift at adjacent antenna elements for excitations at P1 and P2. The design was optimized for minimal phase error at 60 GHz. These plots illustrate the relative variation of phase shift across the frequency band, which will have a direct effect on the antenna radiation patterns.

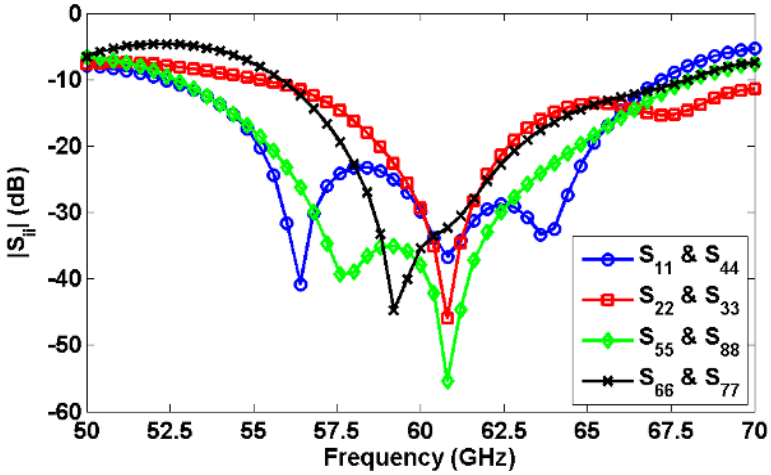
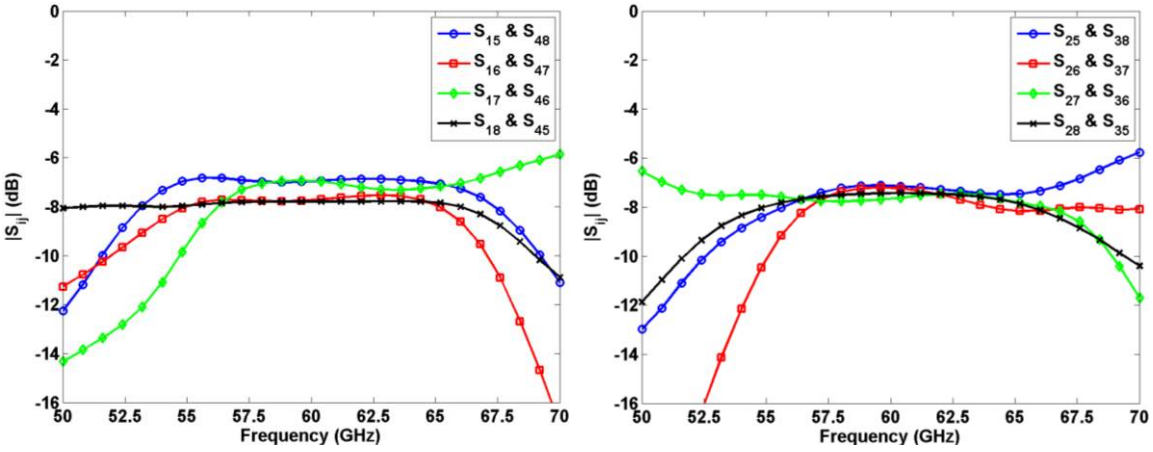
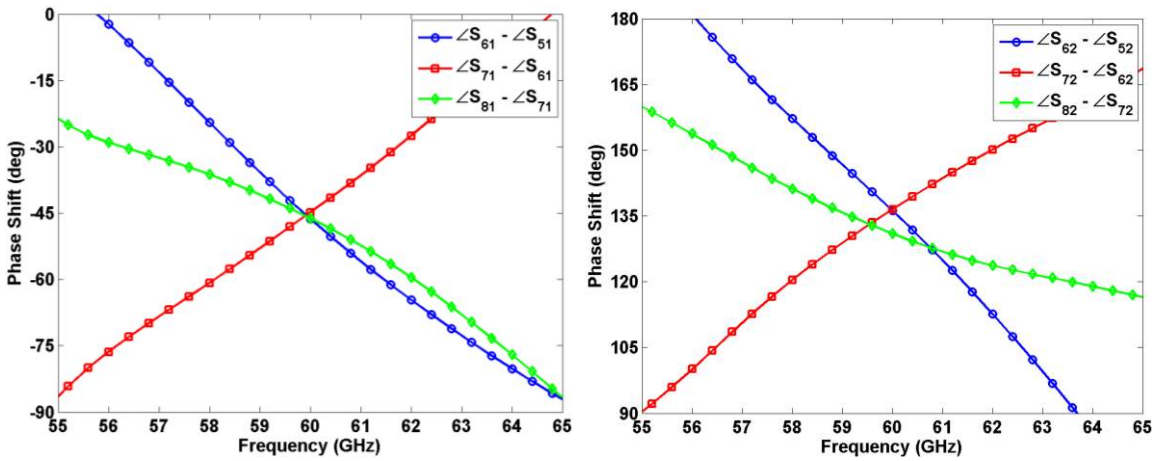


Figure 5.3: Simulated reflection coefficient for each port of the Butler matrix.



(a) (b)

Figure 5.4: Simulated transmission coefficients of the Butler matrix for a.) P1& P4 and b.) P2 & P3.

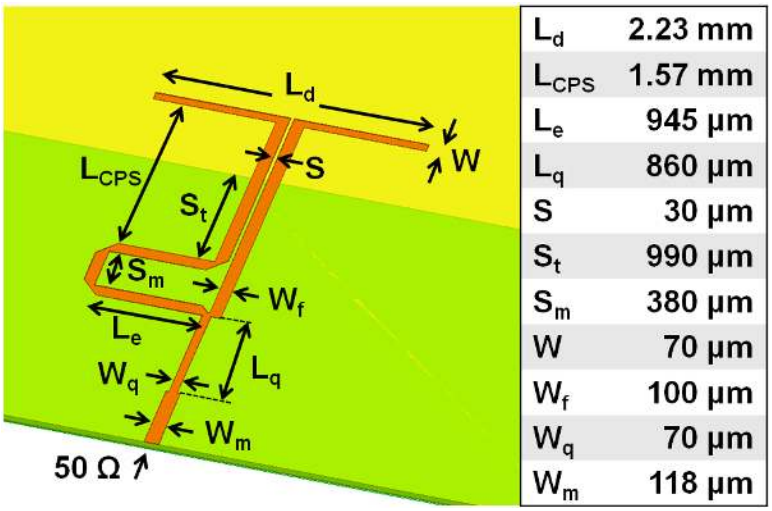


(a) (b)

Figure 5.5: Simulated phase shift between adjacent antenna elements for a.) P1 and b.) P2.

5.2.2 Quasi-Yagi Planar Antenna

The quasi-Yagi dipole array was optimized in conjunction with the Butler matrix. A single antenna element was first designed for 60 GHz operation using the technique outlined in [99]. The final layout of this element is illustrated in Figure 5.6. The design uses a driven dipole excited by a coplanar strip (CPS) line. A balun was used to couple the odd mode of a microstrip feed into the CPS line. This also incorporated a quarter-wave transformer at the unbalanced port of the balun to convert the input impedance to 50 Ω. The truncated microstrip ground acted as a pseudo-reflector to the driven dipole, increasing the antenna directivity by 3 dB. This design was simulated in HFSS and showed a resonance at 60 GHz with a 10 dB bandwidth of 3.5 GHz (5.8 % BW) and peak directivity of 5.2 dBi. Directors were not used in this design in order to maintain a wide beamwidth. This was done to minimize the drop in gain when the array is phased for wide beam scans.



L_d	2.23 mm
L_{CPS}	1.57 mm
L_e	945 µm
L_q	860 µm
S	30 µm
S_t	990 µm
S_m	380 µm
W	70 µm
W_f	100 µm
W_q	70 µm
W_m	118 µm

Figure 5.6: Model of the single antenna element illustrating feature dimensions.

The 4x1 array spacing was optimized using the dipole antenna modeled with the Butler matrix. A quarter-wave transformer was used to match the 50 Ω impedance of the antenna element with the 70 Ω impedance of the Butler matrix. Although this configuration was not consistent with the final active array design, it was necessary to investigate the effects of the Butler matrix on the antenna radiation patterns. Due to the fixed phase shifts of the Butler matrix, array factor (AF) theory dictates a 4x1 dipole array, with element spacing λ/2 and uniform amplitude distribution, will have a maximum overlap point of -3.7 dB. Since the designed antenna element is more directive than a conventional dipole, it was expected that the beam overlap points would fall slightly below this value. It was found that an array spacing of 2.8 mm ($0.56\lambda_0$) gave optimum gain levels for the four beam scans while also maintaining -4 dB overlap points.

Both single antenna element and 4x1 array with Butler matrix were fabricated and tested for S_{11} measurements. A 50 Ω CPW-to-microstrip transition was incorporated on to these structures for GSG probing. A photo of the fabricated antennas is displayed in Figure 5.7. The simulated and measured S_{11} for both structures are plotted in Figure 5.8. These plots verify good correlation between the successful fabrication of these samples and the accuracy of the HFSS modeling.

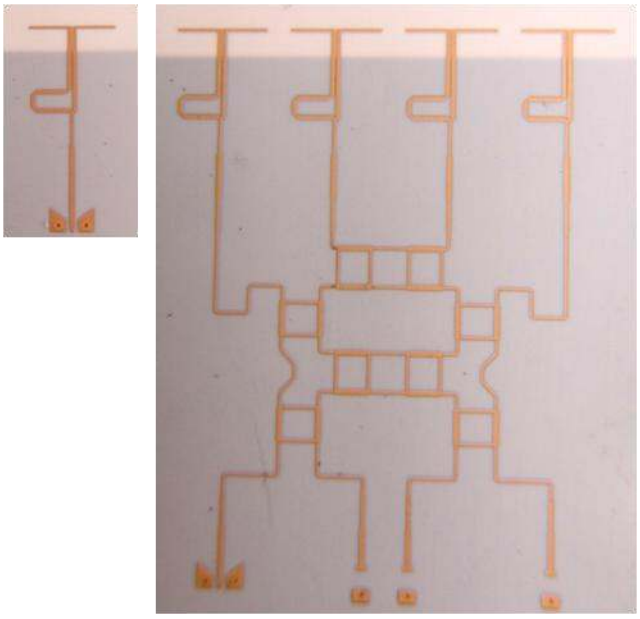


Figure 5.7: Fabricated a.) single Yagi element and b.) 4x1 array with Butler matrix.

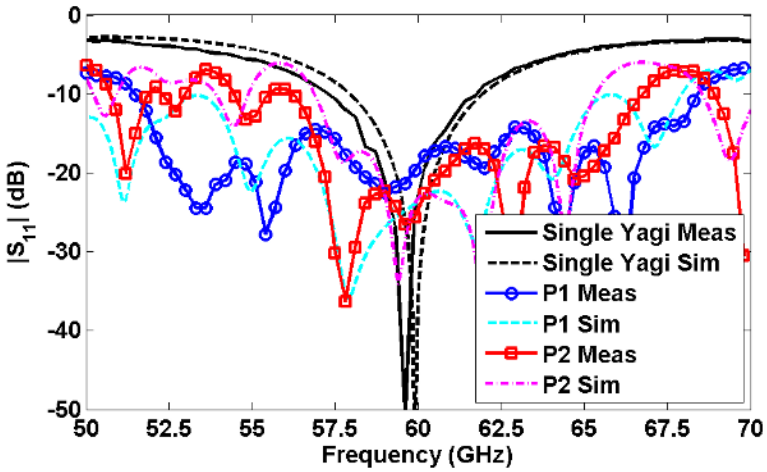


Figure 5.8: Simulated and measured S_{11} of the single dipole antenna and the 4x1 phased array with incorporated Butler matrix.

5.2.3 GaAs Chip Package Design

The LNA and SPDT switch were initially packaged using 50 Ω transitions to verify the on-die performance. Using accurate model representation of the chip-to-package interconnect, the measured S-parameters were de-embedded to capture the on-die performance. Using the de-embedded parameters, each die package could be more accurately optimized for performance over the desired frequency band.

Low Noise Amplifier Circuit Description

The GaAs LNA (Hittite HMC-ALH382) operates between 57 GHz to 65 GHz with a reported typical gain of 24 dB, noise figure of 4.5 dB, and 1 dB power compression point (P_{1dB}) of 12 dBm. The circuit requires a drain voltage of +2.5 V drawing 64 mA of current and is controlled by varying the gate voltage from -1 V to +0.3 V. The biasing network requires 100pF by-pass capacitors next to the drain and gate chip pads as well as 0.1 μF capacitors, which are not as critically placed. A 10 Ω resistor is also placed in series between the by-pass capacitors on the gate DC line. The die is fabricated for wire bond packaging on the RF and DC pads. The LNA die size is 1.55 mm x 0.73 mm x 0.1 mm. A more in-depth description of this device can be found in [100].

Single-Pole-Double-Throw Switch Circuit Description

The GaAs SPDT switch (Hittite HMC-SDD112) operates between 55 GHz to 86 GHz with a reported ON-state insertion loss of 2 dB and an OFF-state isolation of 30 dB. Each output of the circuit is controlled by an independent DC input line. The ON state requires a -5 V DC supply drawing -63 nA of current while the OFF state requires a +5 V DC supply drawing 22 mA of current. The biasing network requires 100 pF by-pass capacitors placed next to the chip to mitigate unwanted resonances. The die is fabricated for wire bond packaging on the RF and DC pads. The switch die size is 2.01 mm x 0.975 mm x 0.1 mm. A more in-depth description of this device can be found in [100].

De-Embedded Chip Performance

The LNA and SPDT switch packages were initially designed and optimized assuming an on-die 50 Ω match. A model was built for each die simulating a 76 µm x 12.5 µm Au ribbon wire interconnecting the on-die pads to a 50 Ω microstrip line on package. The width of the ribbon (76 µm) was chosen not only to minimize the wire inductance, but also closely mimic a 50 Ω line when bonded on top of the 100 µm thick GaAs chip substrates. This effectively minimized the length of the parasitic interconnect to the distance between chip edge and the on-package microstrip line. Both die were embedded into the 50 µm LCP substrate to also minimize wire bond lengths. Shunt capacitive stubs were incorporated on package to compensate for the wire bonds and tune out the parasitic inductance. Additionally, a 50 Ω CPW-to-microstrip transition was used to allow probe measurement. The final stub dimensions were 420 µm x 60 µm, and the simulated interconnect showed better than 20 dB return loss and less than 0.25 dB insertion loss up to 70 GHz. These simulated models are depicted in Figure 5.9.

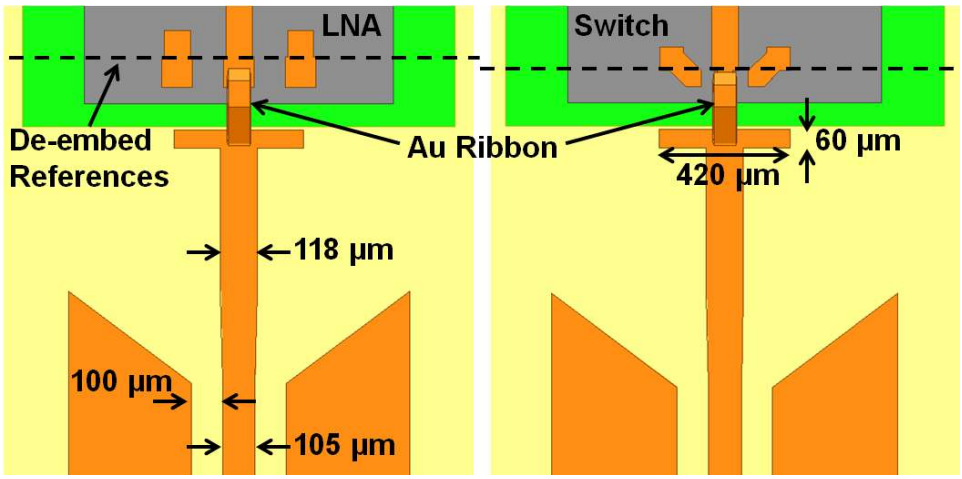


Figure 5.9: Simulated package of the LNA and SPDT switch assuming 50 Ω on-die matching.

Both chip packages were fabricated, assembled, and measured. Using Advanced Design System (ADS), this measured data was then used in conjunction with the simulated HFSS models to de-embed the S-parameters for the on-die response. The de-embedded parameters were referenced to 50 Ω lines on die, illustrated in Figure 5.9. Using this reference for the package design, the modeled wire bond transition included not only 200 µm length ribbon but also ribbon running on top of the chip to pad. Looking out from the reference plane on chip, this looks like a length of transmission line, very close to 50 Ω, in series with a wire inductance. The effect of this wire bond transition was considered in the design for both chip packages.

LNA Package Design

Using the de-embedded LNA S-parameters, the package was optimized for integration into each Yagi element of the antenna array. The RF input was designed for a 50 Ω impedance feed from the Yagi array and the RF output was designed for a 70 Ω impedance feed to the Butler matrix. This minimized the number of impedance transitions needed, reducing the incurred insertion loss and saving real estate. The final LNA package design is shown in Figure 5.10. At the input of the package, a 50 Ω microstrip line feeds into a compensation stub with dimensions 425 µm x 100 µm. The output of the package uses a compensation stub with dimensions 400 µm x 100 µm, followed by a 76 Ω quarter-wave impedance transformer feeding into a 70 Ω microstrip line. A comparison plot of the LNA S-parameters is shown in Figure 5.11. It is expected that the LNA will add 24 dB of active gain to the antenna array.

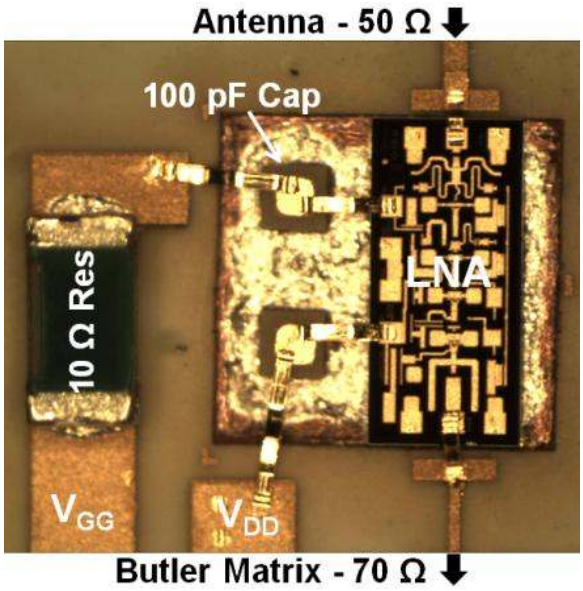


Figure 5.10: Picture of the packaged LNA integrated on the antenna.

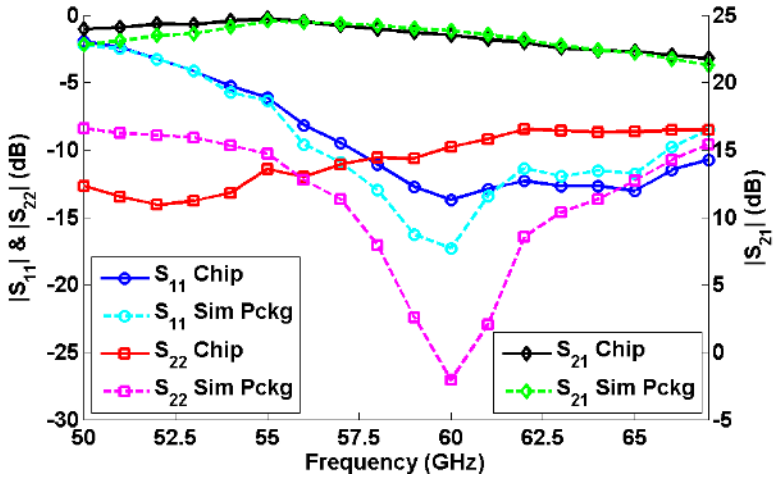


Figure 5.11: Comparison plot of the measured and simulated LNA package.

Switch Network Package Design

Using the de-embedded S-parameters of the SPDT switch, the switch network was optimized for integration with the Butler matrix and G3PO RF output. It was configured to selectively route four separate RF inputs to a single RF output using three SPDT switches. This required three different package interconnects to be optimized:

Butler matrix to switch, switch to switch, and switch to G3PO connector. The final SPDT switch network package design is shown in Figure 5.12. The common RF line for each switch did not require compensation stubs and was well matched when modeled in conjunction with the wire bond transition to a 50 Ω microstrip line. The four switched RF lines fed from the Butler matrix also did not require compensation stubs. These were well matched when wire bonded directly to a 70 Ω microstrip line. The two interconnecting microstrip lines from the common to split-port RF lines used a 50 Ω microstrip line feeding a 55 Ω quarter-wave impedance transformer. A plot of the measured and simulated switch package S-parameters is shown in Figure 5.13. The entire switch network is expected to account for less than 4 dB of insertion loss across the frequency band of interest.

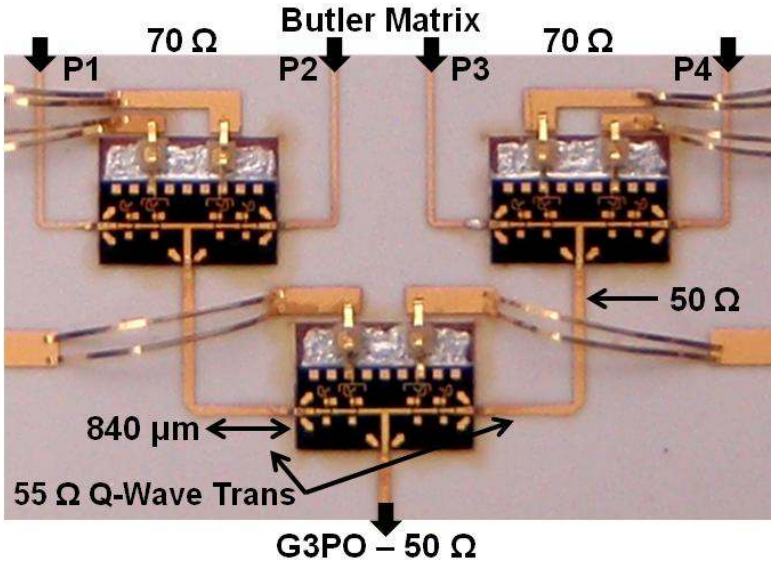


Figure 5.12: Picture of the packaged switch network integrated on the antenna.

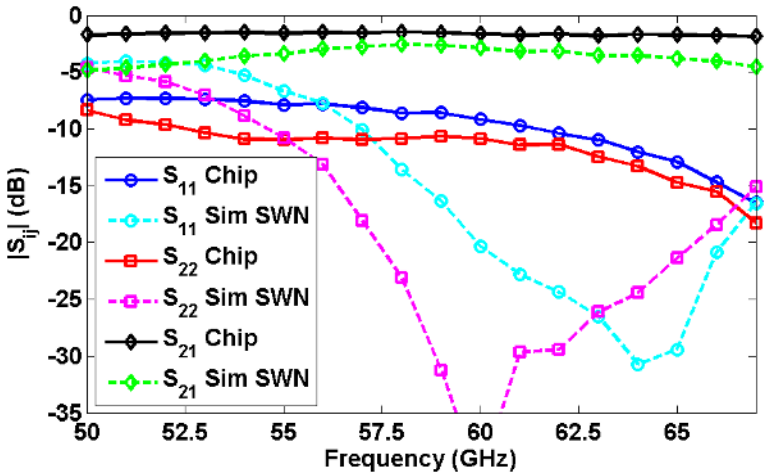


Figure 5.13: Comparison plot of the measured and simulated switch package.

5.2.4 G3PO Transition Design

A G3PO connector was used to interconnect the 50 Ω microstrip output of the antenna to a 1.85 mm coaxial connector. This component is specified to maintain a voltage standing wave ratio (VSWR) of 1.25 up to 65 GHz with an insertion loss less than 1 dB. Further details of the connector can be found in [101].

The G3PO-to-microstrip transition was modeled in HFSS using a tuning stub to improve impedance matching. The final layout of this transition is shown in Figure 5.14. An open butterfly stub of length 420 µm was placed 1.25 mm from the edge-mount interface. This improved the return loss to be greater than 10 dB from 53 GHz to 73 GHz with an insertion loss less than 0.9 dB.

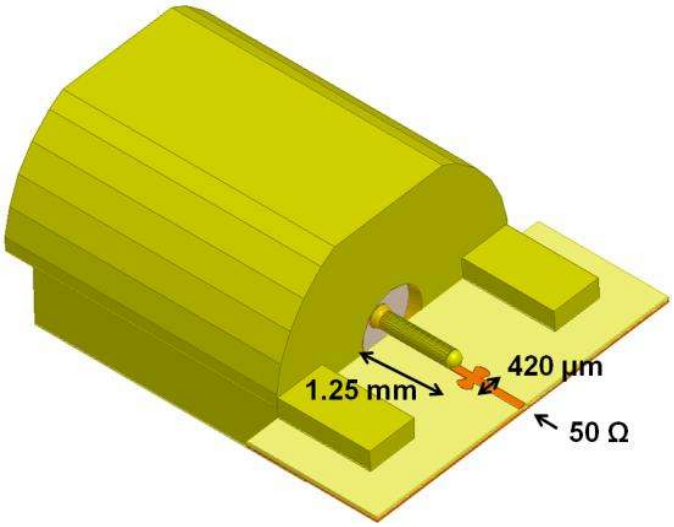


Figure 5.14: Simulated G3PO connector modeled with impedance tuning stub.

5.2.5 Antenna Fabrication & Assembly

The active array was fabricated on 50 µm LCP with 18 µm copper cladding. The top metal layer was first etched completely off to allow via drilling. A KrF 248 nm UV excimer was used to drill 100 µm diameter vias for interconnecting the top and bottom ground planes. The substrate was then metalized with a 200 Å Ti / 5 µm Cu layer using a DC sputterer. This allowed for a uniform deposition on the via walls ensuring a connection between top and bottom metallization layers. Both sides of the substrate were patterned using standard photolithography techniques. Additionally, a thin layer of gold was evaporated onto the top layer and selectively plated up to a 5 µm thickness. This layer was again patterned using photolithography. Cavities for embedding the chips were drilled through the LCP down to the bottom copper layer using the UV excimer. The LNA and SPDT cavities were made 1.65 mm x 1.65 mm and 2.1 mm x 1.5 mm, respectively. These were sized to accommodate the chips as well as the 100 pF by-pass capacitors. A hole was also laser drilled through the substrate for housing the G3PO connector.

The ICs, capacitors, and resistors were mounted on the fabricated sample using silver epoxy and were allowed to cure for 30 minutes at 120 °C. The RF and DC chip

pads were then wire bonded on to the gold traces on LCP. The wire bonds were made using a wedge-wedge wire bonder utilizing 75 µm x 12.5 µm Au ribbon. This type of bonder uses ultra-sonic energy to make a weld between contact points, therefore, avoiding the use of excessive heat and pressure which could damage the components. The last step in the assembly was mounting the G3PO connector. A no-clean R276 solder paste was applied to the ground and signal lines, and the connector was dropped in place. The entire sample was placed into an oven set at 265 °C for 3 minutes until the solder reflowed for a secure connection. A picture of the final active array is shown in Figure 5.15. Excluding the added DC line lengths and the G3PO connector, the entire active array is 1.4 cm x 1.75 cm.

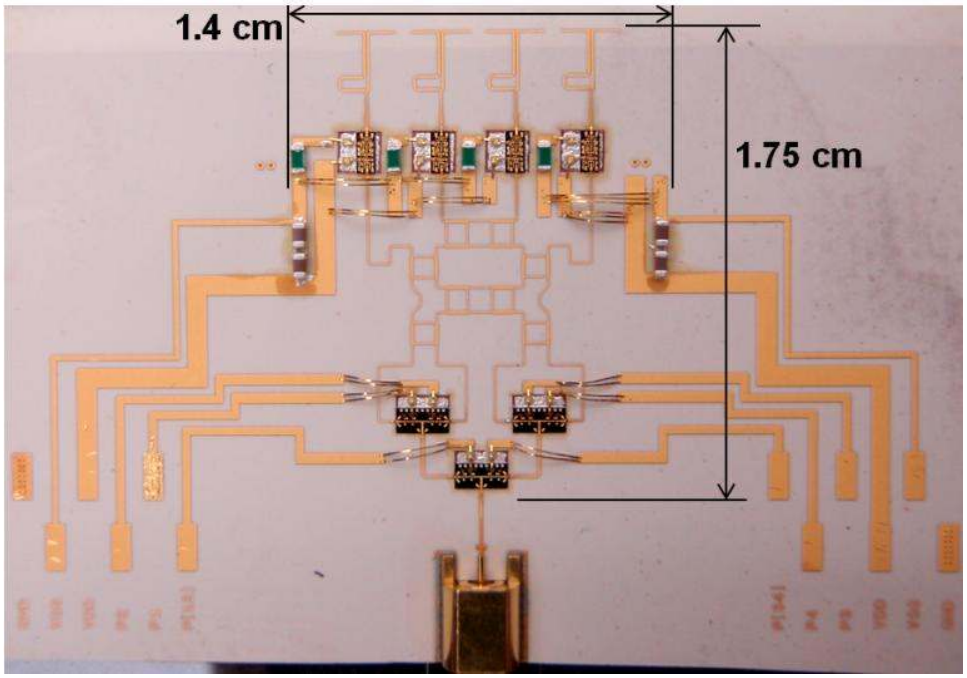


Figure 5.15: Fabricated and assembled 4x1 active receiving switched-beam array.

5.3 System Results

The antenna was biased using 38 AWG insulated wire soldered to the DC pads, and in any given beam state, it consumes 1.2 W of DC power and has an estimated iP_{1dB} of -17 dBm per element. A G3PO-to-1.85 mm adapter was used for S_{11} and radiation pattern measurements. Additionally, the antenna was analyzed to calculate the added noise performance.

The S_{11} and radiation pattern measurements for each beam state were measured using an Agilent PNA. Figure 5.16 shows that the active array maintains a return loss better than 10 dB centered at 60.2 GHz with a bandwidth of 7 GHz (11.6 % BW). The far-field radiation patterns were measured in an anechoic chamber. The minimum distance required for far-field measurements was calculated using the approximated formula from [102],

$$R_{ff} \geq \frac{2D^2}{\lambda_0}, \tag{5.1}$$

where D is the largest dimension of the AUT. Two Quinstar V-band standard gain horns were used to calculate the 4x1 switched-beam antenna gain using the Gain-Comparison method explained in [103]. While one gain horn was used as the transmitting probe during measurements, the other was used as a reference for gain calculation of the AUT. Using the largest dimension of the horn, D = 4 cm, the minimum distance for the far-field setup was calculated to be 64 cm. For measurement, the final setup placed the probe horn 75 cm from the AUT. The PNA was used to measure the relative received power of the AUT as the probe rotated 360 degrees about the fixed radial axis.

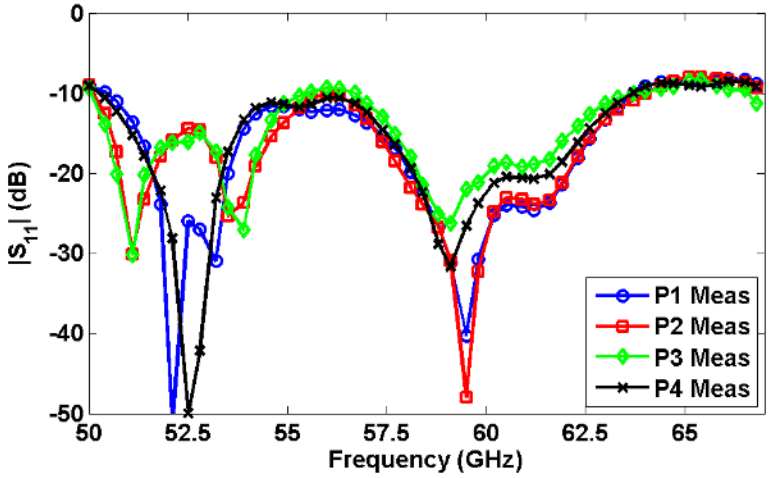


Figure 5.16: Measured S_{11} for each beam state of the 4x1 active switched-beam array.

Plots of the measured E and H planes were compared with results simulated in HFSS. Figure 5.17 - Figure 5.18 show the normalized radiation patterns at 60 GHz for each beam state. The locations of peaks and nulls correspond very well and the low cross-polarization levels confirm the linear polarization of the antenna. In the E-plane, the scanned beams for P1 & P4 steer ±12° with a half-power beamwidth of 20°, while P2 & P3 steer ±40° with a half-power beamwidth of 27°. In the H-plane, P1 & P4 have a half-power beamwidth of about 110°, and P2 & P3 have a half-power beamwidth of about 70°. A plot of beam steering angle versus frequency is shown in Figure 5.19. Each port exhibits a consistent beam steering angle across the band and is supported by excellent correlation with simulation data.

A plot of the measured gain versus frequency is shown in Figure 5.20. The estimated gain used for comparison in this plot is the simulated antenna gain for each beam scan adjusted by the predicted additional gain and losses of the LNA, Butler matrix, switch network, and G3PO connector. The antenna has a measured peak active gain of 27.5 dB and maintains better than 20 dB from 52.5 GHz to 62 GHz.

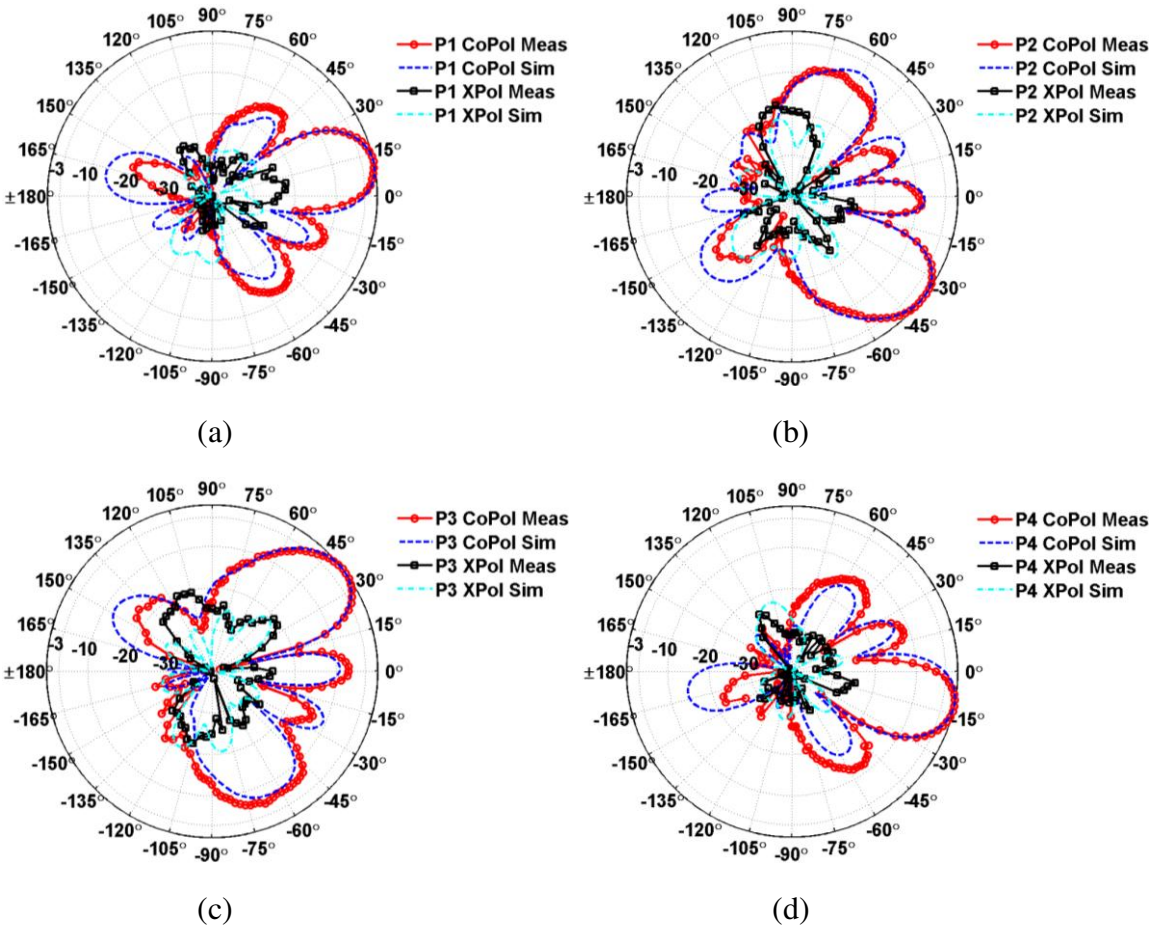


Figure 5.17: Normalized E-Plane of co-polarization and cross-polarization at 60 GHz for each beam scan in dB.

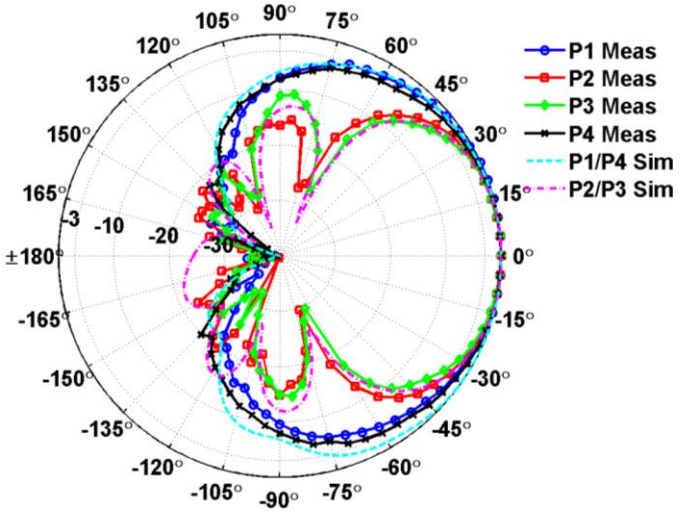


Figure 5.18: Normalized H-Plane at 60 GHz for each beam scan in dB.

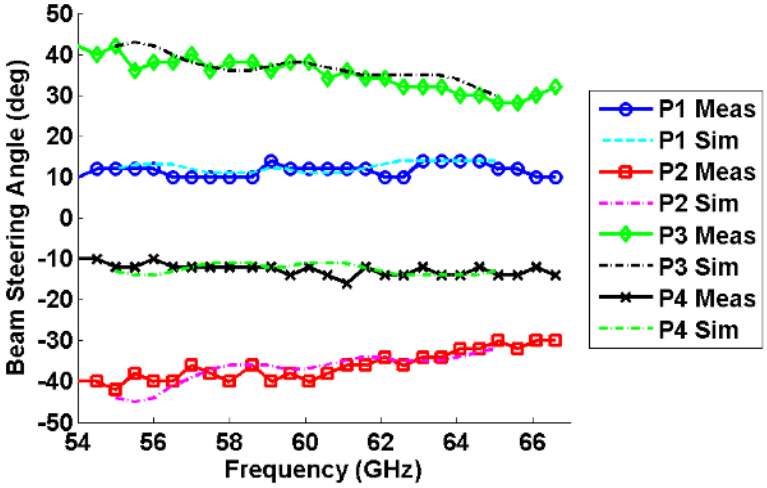


Figure 5.19: E-plane beam steering versus frequency of the 4x1 active switched-beam array.

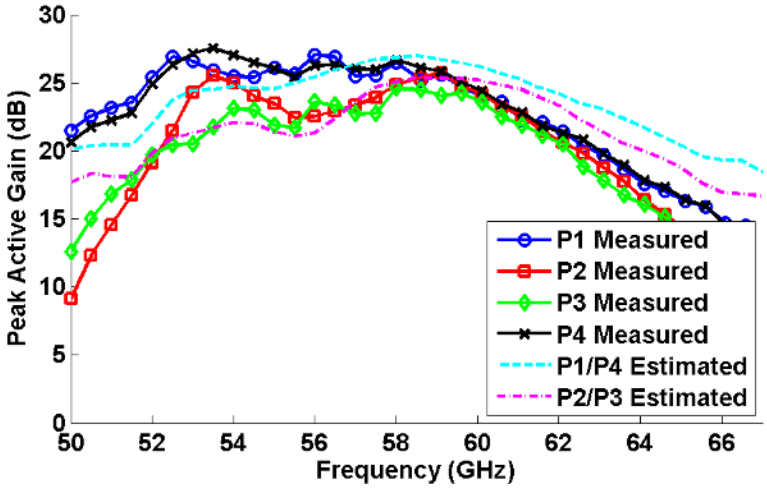


Figure 5.20: Gain versus frequency of the 4x1 active switched-beam array.

Using (4.2) and (4.3), the added noise performance for the antenna was calculated at the system output. Since the LNA gain is sufficiently large, the feed line loss and NF_{LNA} are the dominating factors in these equations. Therefore, the components after the LNA are ignored in the analysis. The feed line losses and antenna directivity could not be directly measured so these were simulated in HFSS. This showed an estimated L_{A1} of 0.8 dB, L_R of 0.1 dB, and a directivity of 9.2 dBi. This analysis resulted in an estimated system noise figure of 5.4 dB and G/T of -18.6 dB/K at 60 GHz. While the system noise

figure is minimized with the LNA placed directly after each antenna element, the *G/T* FOM can be improved by increasing the array size for higher directivity. However, this would require a more extensive Butler matrix to feed the array elements, making the system design more complex.

Resulting performances of the measured phased array can be evaluated with those works shown in the comparison table presented in [88]. Measuring the front-end block of these works, our antenna exhibits the highest front-end gain for 4-element arrays due to the low-loss beam forming network (Butler matrix & switch network), which accounts for only 6.5 dB of insertion loss. In addition, the use of GaAs LNAs placed directly behind the antenna elements has allowed the lowest NF, compared to all works in [88], but at the expense of slightly higher DC power consumption. Also, use of a thin LCP package layer allowed reduced feature sizes and condensed signal routing to minimize the array dimensions.

5.4 Summary

A V-band active receiving switched-beam array has been presented for the first time on a LCP substrate. Active and passive components were co-designed for seamless integration and demonstrate high performance correlating to the simulated results. The measured far-field patterns show a peak active gain of 27.5 dB with ±40° beam steering. By placing LNAs next to each Yagi element, the antenna noise figure was minimized to 5.4 dB with a *G/T* of -18.6 dB/K. This work could be tiled into a larger array for increased antenna performance or configured with additional arrays for a higher order switched element antenna.

CHAPTER 6

CONCLUSION

This thesis has explored advanced 3-D integration for state-of the art components in RF wireless systems using multilayer LCP platforms. In this chapter, a summary of the contributions presented in this dissertation are listed along with new directions for further research.

6.1 Contributions

The following technical contributions have been presented in this thesis:

1. A K_a-band SiGe VCO was embedded into an LCP package with wire bond interconnects. A cavity was drilled into LCP for chip placement, which minimized the parasitics incurred through the wire bonds and enabled improved performance. This paves the way for low cost mm-wave front ends combining Si devices with low temperature organic substrates.
2. For the first time, an X-band SiGe LNA was laminated with LCP for via interconnect packaging. It was demonstrated that LCP can be successfully utilized in a wafer-level packaging scheme for hybrid integration of SiGe RF electronics and organic packaging layers.
3. An X-band SiGe T/R module was flip-chip packaged and fully embedded into an all-LCP platform. An assembly process was developed for the die attachment and encapsulation in LCP. This provided a highly repeatable packaging scheme with excellent RF performance.
4. A W-band CMOS PA was packaged onto LCP using the previously developed all-LCP encapsulated flip-chip process. Additionally, an on-package matching network

was incorporated to improve the on-die performance. At present, this is the highest performance demonstrated for a W-band CMOS PA on SoP module.

5. For the first time, a 7.45 GHz BAW filter was packaged on LCP. State-of-the-art BAW technologies and 3-D packaging techniques were utilized to create significant benefits in terms of cost, size and performance. As BAW devices extend to higher frequencies, this work serves as the foundation for a viable low-cost packaging solution. This is the first ever reported BAW filter package above 7 GHz.
6. For the first time, a 12 GHz BAW filter was packaged on LCP. The previously developed BAW filter packaging scheme was extended to K_u-band frequencies and incorporated with embedded matching networks to enhance performance and size of the package. This is the first ever reported BAW filter package above 7.5 GHz and shows potential for extension up to mm-wave applications.
7. For the first time, a fully integrated, lightweight, high gain X-band receiving phased array with SiGe LNAs and PSs has been achieved. Advanced MMIC technologies and packaging techniques were utilized to integrate LNAs and PSs onto a lightweight antenna array with a multilayer LCP BFN substrate. This work utilized an SoP concept by integrating SiGe technology for the first time with the benefits of high gain microstrip antennas on low-loss organic substrates.
8. For the first time, a 60 GHz active receiving switched-beam antenna array was demonstrated on an organic platform. A switch network of GaAs SPDT switches was integrated to toggle between beam states, and GaAs LNAs were integrated per antenna element to minimize receive noise figure. The active and passive system components were co-designed for seamless integration and a de-embedding technique was implemented to ensure accurate correlation between simulated and measured performance. This work serves as a building block for future low-cost Gbps antenna solutions.

6.2 Future Work

The material discussed in this thesis has spawned an intrigue for future research, and the following provides insight into potential new directions on this topic:

1. **Flip-chip packaging with III-V semiconductor ICs:** The flip-chip packaging technique outlined in this thesis relies on the CPW I/O structure inherent of Si devices. These ICs do not require proper grounding on the back side of the chip and are thus left floating in a standard flip-chip process. Additionally, these ICs are considered low power and do not require a thermal sinking. If the same process was applied to packaging III-V semiconductor ICs, the problems initially avoided by using Si devices would undoubtedly appear. III-V devices are inherently microstrip on-die and require proper grounding from the backside of the chip. These die also consume much more DC power than Si devices, which translates into more heat generated on chip that must be dissipated through the package. For these reasons, it is imperative that sufficient grounding be applied to the backside of III-V devices. This is not a straight forward problem and should be investigated thoroughly.
2. **Techniques for thermal dissipation in LCP:** Thermal dissipation was not discussed in this thesis because the issue does not normally arise with low-power applications. However, when high power ICs are required in order to meet certain power specifications, thermal dissipation can no longer be ignored. LCP has a very low thermal conductivity (0.5 W/m·K), which makes it unattractive for high-power applications unless special dissipation techniques are utilized. There are techniques already published using a combination of thick copper heat spreaders, thermal vias, and micro-fluidic channels [49], [104]. However, these require a hybrid substrate stackup of LCP with Si, Silicon Carbide (SiC) or PCB, which adds complexity and cost to the fabrication and packaging processes. An all-LCP approach could provide a low-cost solution with possibly superior results. The design guidelines for LCP allow

higher aspect-ratio vias with a denser interconnect pitch. Using this advantage could yield a better effective thermal conductivity through dense thermal vias.

3. **60 GHz Transmit/Receive phased arrays:** While the work presented in this thesis shows beam steering, it does not incorporate a transmit functionality. A 60 GHz transmit/receive antenna array has been previously demonstrated but without beam steering capability [97]. At present, a 60 GHz T/R phased array has yet to be demonstrated on LCP. While it may be difficult enough to take the design presented in this thesis, move the LNA to the G3PO connector and incorporate an additional SPDT switch and PA, the antenna performance would suffer greatly. Preferably, a 60 GHz T/R module should be integrated per antenna element to minimize the receive system noise and maximize effective radiated power. However, this approach presents numerous issues with chip integration, limited packaging real estate, complex DC line routing, DC power consumption, and thermal dissipation.
4. **LCP fabrication analysis:** As new RF substrates are introduced into the market, there is an apparent lag between the development of applications and its embrace by industry. It often takes extensive evaluation of performance, reliability, and cost-effectiveness before successful entry into production. There is currently very little published on large-scale LCP manufacturability. Evaluating the current fabrication limitations of this material would provide an understanding of commercially achievable present-day capabilities, as well as insight for future development. Several parameters have been identified that most affect performance outcome, including substrate thickness after lamination, registration error, and metal etching tolerance. Each of these parameters has a considerable effect on transmission line characteristic impedances and 3-D interconnect circuitry matching.

CHAPTER 7

PUBLICATIONS TO DATE

The following is a chronological list of papers that have been submitted to and/or accepted by a peer-reviewed conference or journal for publication:

7.1 Journal Publications

1. **C. E. Patterson**, J. Ajoian, J. Papapolymerou, G. S. May, "LCP Characterization of broadband RF performance with consideration of fabrication tolerances for CSLP substrate suitability," *to be submitted to IEEE Transactions on Components, Packaging, and Manufacturing Technology*, June 2012.

2. **C. E. Patterson**, J. Ajoian, S. K. Bhattacharya, J. Zepess, S. Leiphart, W. G. Trueheart, Z. Coffman, J. Papapolymerou, "A 12 GHz BAW filter on a 3D organic package," *submitted to IEEE Microwave and Wireless Components Letters*, May 2012.

3. E. Juntunen, **C. E. Patterson**, W. Khan, S. K. Bhattacharya, D. Dawn, J. Laskar, J. Papapolymerou, "A Q-band low-power 2-channel vector modulator in 45-nm CMOS for LINC transmitters," *submitted to IEEE Transactions on Microwave Theory and Techniques*, May 2012.

4. **C. E. Patterson**, W. T. Khan, G. E. Ponchak, G. S. May, J. Papapolymerou, "An organic, 60 GHz active receiving switched-beam antenna array with integrated butler matrix and GaAs amplifiers," *Accepted to IEEE Transactions on Microwave Theory and Techniques*, May 2012.

5. C. A. D. Morcillo, **C. E. Patterson**, B. Lacroix, C. Coen, J. D. Cressler, J. Papapolymerou, "An ultra-thin, high-power and multilayer organic antenna array with T/R functionality in the X band," *submitted to IEEE Transactions on Microwave Theory and Techniques*, March 2012.

6. C. H. J. Poh, **C. E. Patterson**, S. K. Bhattacharya, S. D. Philips, N. E. Lourenco, J. D. Cressler, J. Papapolymerou, "Packaging effects of multiple X-band SiGe LNAs embedded in an organic LCP substrate," *in IEEE Transactions on Components, Packaging and Manufacturing Technology*, early access, 2012.

7. **C. E. Patterson**, T. K. Thrivikraman, A. M. Yepes, S. M. Begley, S. K. Bhattacharya, J. D. Cressler, J. Papapolymerou, "A lightweight organic X-band phased array with integrated SiGe amplifiers and phase shifters," *in IEEE Transactions on Antennas and Propagation*, vol. 59, issue 1, pp. 100-109, 2011. **[2012 H. A. Wheeler Prize Paper Award]**

7.2 Conference Publications

1. **C. E. Patterson**, D. Dawn, J. Papapolymerou, "A W-band CMOS PA encapsulated in an organic flip-chip package," *accepted to IEEE International Microwave Symposium*, 2012.

2. C. A. D. Morcillo, **C. E. Patterson**, J. Papapolymerou, "Design of stripline beam-former network components for low-profile, organic phased arrays in the X band," *in IEEE Radio & Wireless Symposium*, pp. 179-182, 2012. **[1st Place Student Paper Competition]**

3. **C. E. Patterson**, T. K. Thrivikraman, S. K. Bhattacharya, C. T. Coen, J. D. Cressler, J. Papapolymerou, "Development of a multilayer organic packaging technique for a fully embedded T/R module," *in European Microwave Conference*, pp. 261-264, 2011. **[Student Paper Competition Finalist]**

4. **C. E. Patterson**, S. K. Bhattacharya, J. Zepess, S. Leiphart, W. G. Trueheart, J. Ajoian, Z. Coffman, J. Papapolymerou, "A 7.45 GHz BAW filter on a low cost 3D organic package," *in IEEE International Microwave Symposium*, 2011. **[Student Paper Competition Finalist]**

5. C. A. D. Morcillo, **C. E. Patterson**, B. Lacroix, T. Thrivikraman, C. H. Poh, C. T. Coen, J. D. Cressler, J. Papapolymerou, "A lightweight, 64-element, organic phased array with integrated transmit-receive SiGe circuitry in the X band," *in IEEE International Microwave Symposium*, 2011.

6. W. T. Khan, S. K. Bhattacharya, **C. E. Patterson**, G. E. Ponchak, J. Papapolymerou, "Low cost 60 GHz RF front end receiver on organic substrate," *in IEEE International Microwave Symposium*, 2011.

7. E. A. Juntunen, W. T. Khan, **C. E. Patterson**, S. K. Bhattacharya, D. Dawn, J. Laskar, J. Papapolymerou, "An LCP packaged high-power, high-efficiency CMOS millimeter-wave oscillator," *in IEEE International Microwave Symposium*, 2011.

8. **C. E. Patterson**, T. K. Thrivikraman, A. M. Yepes, S. K. Bhattacharya, J. D. Cressler, J. Papapolymerou, "Implementation of a low cost, lightweight X-band antenna with integrated SiGe RF electronics," *in IEEE International Geoscience and Remote Sensing Symposium*, pp. 681-684, 2010.

9. **C. E. Patterson**, A. M. Yepes, T. K. Thrivikraman, S. K. Bhattacharya, J. D. Cressler, J. Papapolymerou, "A lightweight X-band organic antenna array with integrated SiGe amplifier," *in IEEE Radio & Wireless Symposium*, pp. 84-87, 2010.

10. C. H. J. Poh, T. K. Thrivikraman, S. K. Bhattacharya, **C. E. Patterson**, J.D. Cressler, J. Papapolymerou, "An LCP package model for use in chip/package co-design of an X-band SiGe low noise amplifier," *in IEEE EPEPS*, pp. 203-206, 2009.

11. **C. E. Patterson**, T. K. Thrivikraman, S. K. Bhattacharya, C. Poh, J. D. Cressler, J. Papapapolymerou, "Organic wafer-scale packaging for X-band SiGe low noise amplifier," *in European Microwave Conference*, pp. 141-144, 2009.

12. **C. Patterson**, S. Horst, S. Bhattacharya, J. D. Cressler, J. Papapolymerou, "Low cost organic packaging for silicon based mm-wave wireless systems," *in European Microwave Conference*, pp. 1242-1245, 2008.

APPENDIX A

CONSIDERATION OF FABRICATION TOLERANCES FOR LCP PLATFORMS

There are several challenges in implementing LCP for chip scale level packaging (CSLP), especially when broadband RF performance is required. As RF ICs incorporate an increasing level of system functionality and interconnection pitch approaches 150 μm, a substrate technology is required to satisfy 50 Ω RF transmission lines at said pitch while maintaining required trace-to-trace isolation. Furthermore, layer-to-layer RF transitions are also an integral piece of design versatility and pose significant challenges when required over 3:1 broadband mm-wave performance.

Several parameters have been identified that most affect performance outcome, including substrate thickness after lamination, registration error, and metal etching tolerance. Each of these parameters has a considerable effect on transmission line characteristic impedances and 3-D interconnect circuitry matching. To understand the producibility of LCP as a CSLP substrate, these parameters should be thoroughly considered in the preliminary stages of a design.

A preliminary analysis has been performed focusing on selected transmission line structure performance and varying fabrication tolerances. Additionally, via transitions were considered. There are several parameters that should be investigated and traded to balance between fabrication limitations and RF performance while achieving package requirements. A benchmark VSWR $\leq$ 1.2 (Return Loss > 20 dB) was used to drive the fabrication tolerances for acceptable RF performance.

A.1. Transmission Line Structures

To determine the optimum material thicknesses, an analysis was performed using theoretical calculations for characteristic impedance of different transmission lines. Microstrip, CPW-G and stripline structures were analyzed for varying LCP core material thicknesses of 25 µm, 50 µm, and 100 µm.

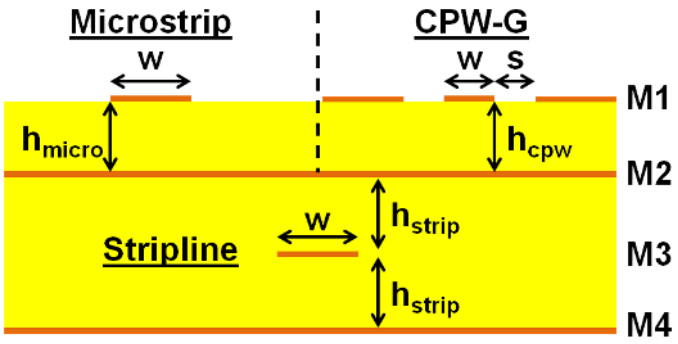


Figure A.1: Cross-section of transmission line structures on CSLP stack-up using LCP.

Design parameters are calculated for each transmission line structure using approximations from [102], [105]-[106]. Assuming a 50 Ω system impedance using LCP, the line widths and gaps for each transmission line structure are calculated for varying core material thicknesses. A comparison of the required line widths is shown in Figure A.2. To observe the sensitivity of the characteristic impedance for each structure, parameters were varied consistent with fabrication tolerances specified in *Section 1.3*. Figure A.3(a) - Figure A.5(a) illustrate the effects of the material thickness tolerances specified by Rogers Corporation. The characteristic impedance is calculated by varying the LCP core thickness ±12.5 % and maintaining nominal line widths and gaps. This appears to have a relatively minor effect on impedance for all transmission line structures. The characteristic impedance does not vary by more than ±10 %. Figure A.3(b) - Figure A.5(b) show the effect of metal etch tolerances, controlled by the fabrication process, for worst case variation of dielectric thicknesses. The characteristic impedance is calculated by varying the etch tolerance ±8 µm and maintaining worst-case

core material thicknesses. The degree of sensitivity for characteristic impedance varies for each type of transmission line structure. Etch tolerance has a relatively small effect on microstrip lines for all three core thicknesses, showing a variance in the impedance of ±5 %. The CPW-G structure also shows low sensitivity for the thicker core material. However, this increases with decreasing material thickness. The stripline structure shows the highest sensitivity for thin core layers. However, with material of 50 µm or thicker, there is less than ±10 % variation in characteristic impedance. Although microstrip has less sensitivity to process tolerances, it does not support the isolation requirements necessary in this application.

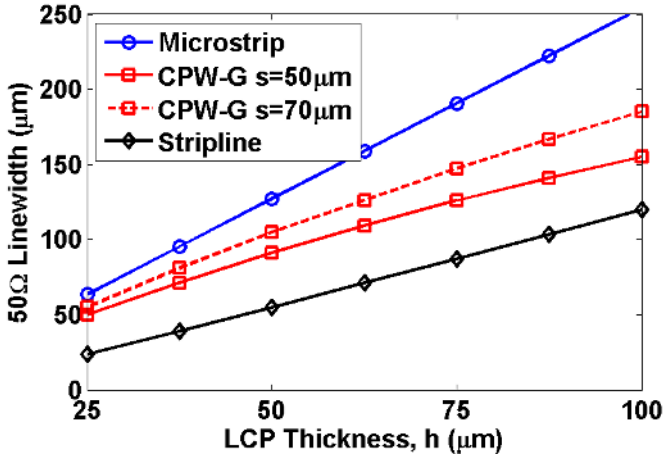
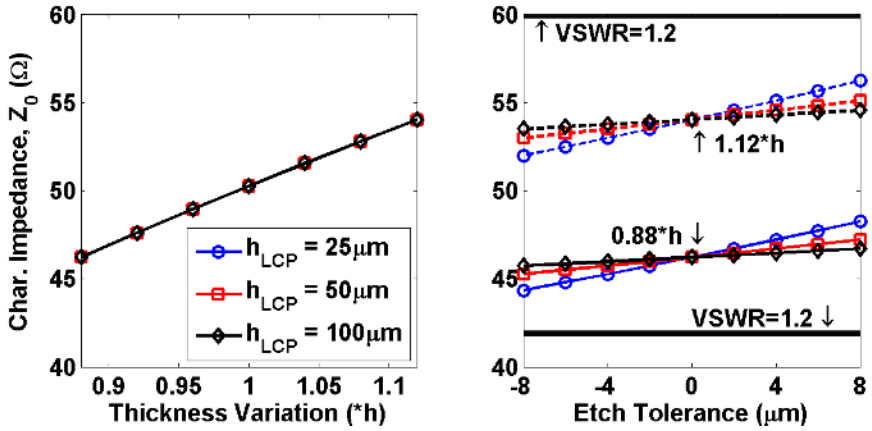
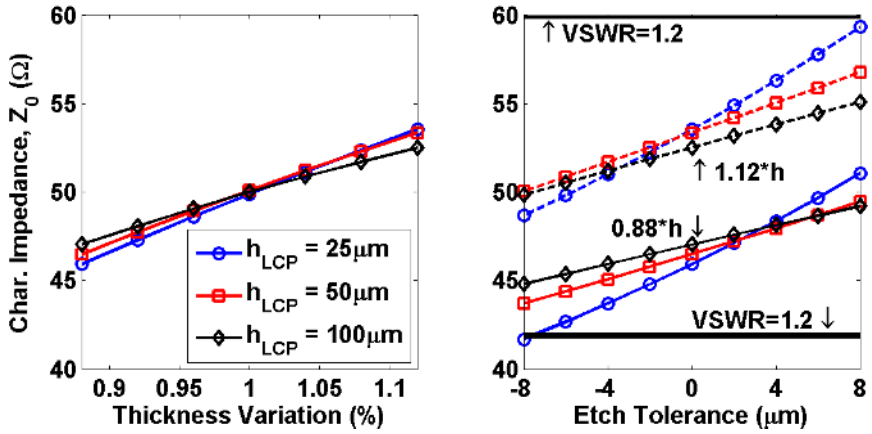


Figure A.2: Calculated 50 Ω line width for each transmission line structure.



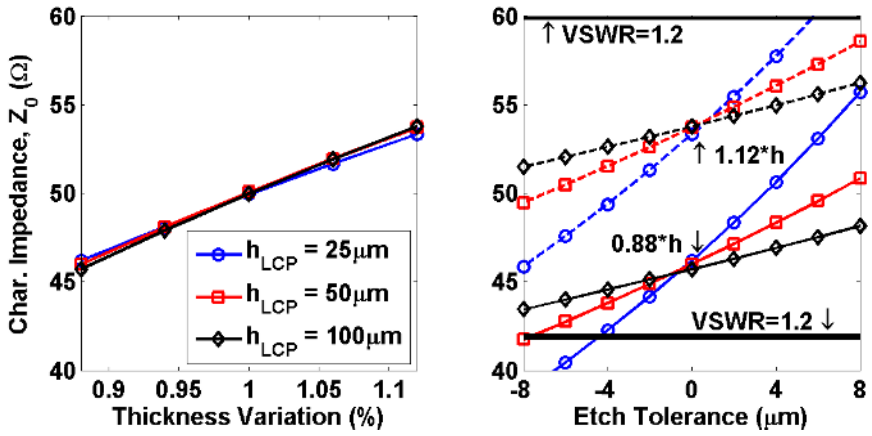
(a) (b)

Figure A.3: Microstrip transmission line characteristic impedance for a) substrate thickness variations, b) and worst-case etch tolerance variations.



(a) (b)

Figure A.4: CPW-G transmission line characteristic impedance with fixed line gap, s = 50 μm, for a) substrate thickness variations, b) and worst-case etch tolerance variations.



(a) (b)

Figure A.5: Stripline characteristic impedance for a) substrate thickness variations, b) and worst-case etch tolerance variations.

A.2. Via Interconnect Structures

A via transition is comprised of a top and bottom via catch pad, one or more ground plane anti-pads, and the via interconnect. For fabrication purposes, the minimum via diameter is determined according to an aspect ratio specified to enable proper metallization of the via. This minimum diameter then determines the minimum catch pad and anti-pad dimensions allowed. By over-sizing the catch pad and anti-pad, a higher yield of layer-to-layer interconnect can be achieved. This, however, can cause a large impedance mismatch and degrade RF performance.

Via interconnects are conventionally modeled through a distributed resistor-inductor-capacitor (RLC) network. For multilayer stack-ups, these become complex and application specific. Figure A.6 illustrates the various RLC components for a M1-M3 via transition in a four metal layer stack-up. While via inductance, L_V, and resistance, R_V, become essentially fixed, the capacitive components can be tuned to maintain 50 Ω impedance matching. However, for short via interconnects used in thin laminates, the parasitics incurred by the via can be potentially dominated by the large capacitance, C_b, seen from an oversized via catch pad on M3. This effect can be mitigated by reducing the

catch pad diameter, thus reducing the parasitic capacitance. In doing so, the via diameter must also be reduced to accommodate the registration tolerance, which may not be possible due to the limitations in the fabrication process. Thus it becomes imperative, for thin laminate interconnects, that the maximum via aspect ratio be extended further to maintain high RF performance. Evidence of how this capacitance affects impedance matching and a technique to reduce it when fabrication capabilities are pushed to the limits is demonstrated in [107]-[108]. However, the simplest solution, in terms of RF design, is to push the fabrication limitations of via diameter to smaller size.

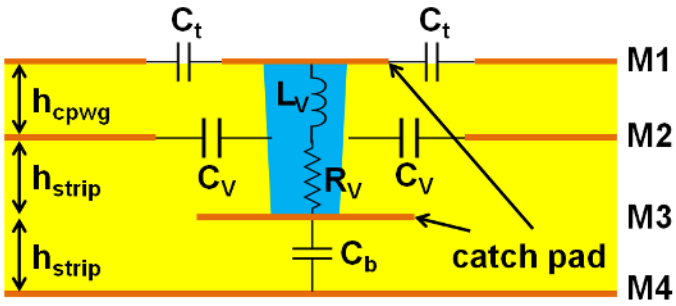


Figure A.6: Cross-section of M1-M3 via transition and model parasitics.

APPENDIX B

ITERATIVE N-PORT MATCHING NETWORK DESIGN

This appendix explains the steps to successfully design a matching network (MN) for an N-port design by using HFSS and ADS simulations tools in a coherent manner. HFSS is utilized for 2-D and 3-D model simulations while ADS is used for block simulations. The example illustrated here is a design method used for developing chip packages and is an extensive approach to ensure accuracy of the MNs. All or part of the steps outlined in this section may be applicable to a given application. *Chapters 2 to 5* all use a customized variation of this design technique.

Disclaimer: Throughout my experience, I have found HFSS to be the most accurate for RF modeling of 2-D and 3-D structures. This is only my opinion and should only be considered as such. I have also found ADS Momentum to be very useful for simulations that may be too large to model in 3-D, e.g. large antenna arrays. However, this is dependent upon available computer resources.

B.1. Development of Preliminary Designs

1. **Determine the best packaging technique for the device**, e.g. wire bond, flip-chip bond, via interconnect, etc (Refer to *Chapter 1*). It may take several design iterations over the course of development to find the optimal solution.

2. **Draw a basic model of the package in ADS Schematic using ideal transmission lines and components.** Incorporate the measured/acquired S-parameters of the bare device and the ideal model of the package interconnects. This is a crude way of getting an idea for the best-case packaged performance of the device. By looking at the smith chart, the type of matching network necessary for a 50 Ω match can be determined.

3. **Incorporate ideal MN components into the ADS Schematic model (Figure B.1).** The models of these components do not need to be very accurate. This is only a preliminary simulation to gauge the best configuration of the matching network. Try various configurations to optimize performance and real estate. Hint: The more condensed the matching network is, the less lossy it will be (Longer transmission lines correlate to more loss).

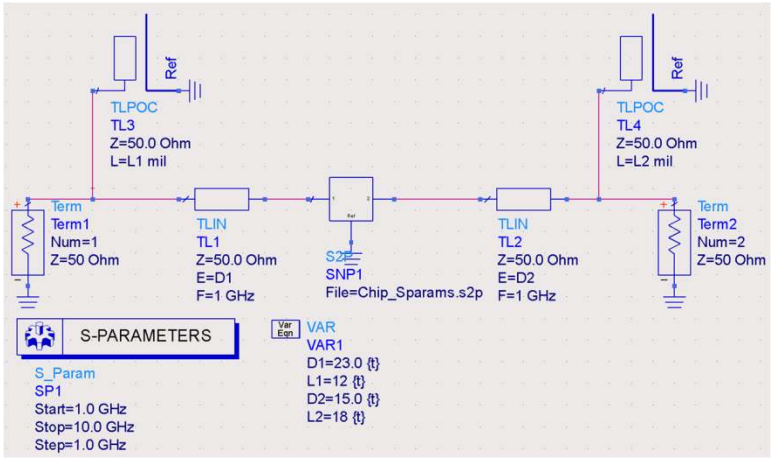


Figure B.1: ADS schematic of ideal MN components with device S-parameter block.

4. **Duplicate the model to include realistic (lossy) package and MN components (Figure B.2).** Now that the components have incorporated parasitics, the MN components may need to be adjusted to maintain a 50 Ω match. Comparing the performance of the ideal and lossy models will provide insight to how much loss is attributed to the package and how much loss is inherent in the device. Obviously, the packaged performance cannot be better than the ideal performance.

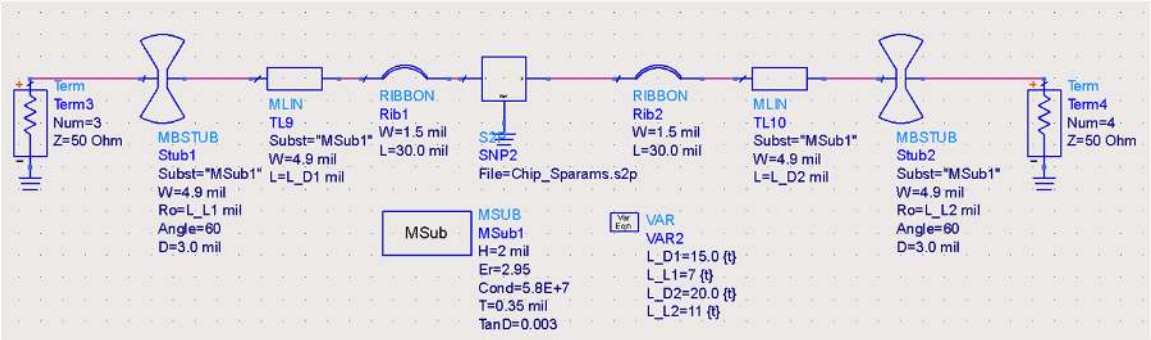


Figure B.2: ADS schematic of lossy package with butterfly stub MN components.

5. **Model the package interconnects in HFSS using 50 Ω references on the device and package (Figure B.3).** This model should be drawn as accurately as possible. It is important to model the package substrate height with respect to the mounted chip height. The accuracy of this step will directly affect the accuracy of the MN. (Note: I have always found it necessary to simulate with metal thickness. Using 2-D traces will not accurately simulate transmission lines.)

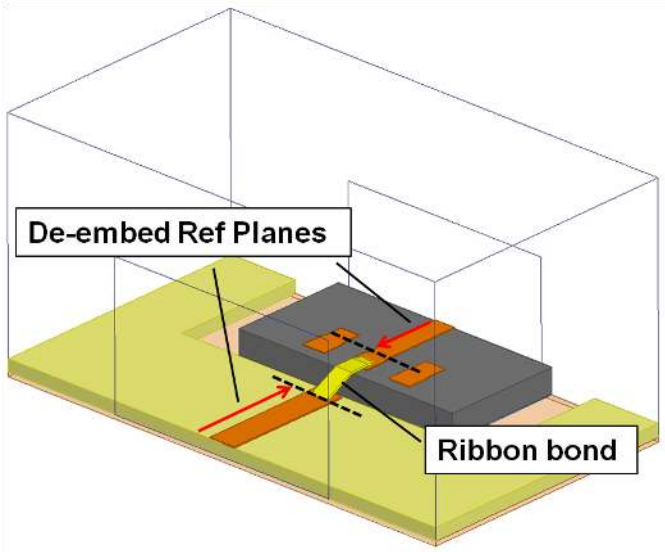


Figure B.3: HFSS model of the packaged device without MN components.

6. **De-embed the HFSS model to the device measurement reference plane and the package interconnect reference plane (Figure B.3).** HFSS has a de-embed feature for Wave Ports that allows the simulated S-parameters to be de-embedded a specified line

length referenced from that port. The modeled S-parameters can be referenced along any unchanging transmission structure. The plotted S-parameters are now representative of only the package interconnect. Keep in mind that this feature will not de-embed anything but line length. It will not magically de-embed wire bonds, 3 dB splitters or any other structure!

7. **Extract the HFSS model S-parameters and replace the equivalent package models in the ADS schematic (Figure B.4).** Re-simulate the ADS schematic model with the S-parameter block acquire through the HFSS model. Be sure to position the S-parameter block so the ports correlate to the chip and package references. Re-adjust the MN components to maintain a 50 Ω match. At this point, it is also advisable to look over the MN configuration to see if it can be further optimized.

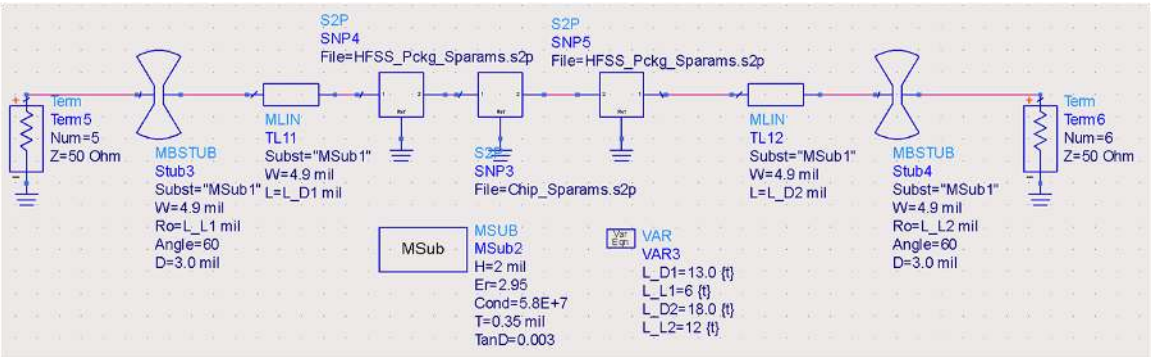


Figure B.4: ADS schematic of lossy package with HFSS extracted S-parameters for package interconnects.

8. **Duplicate the HFSS package model to include the MN (Figure B.5).** Add the MN components to the HFSS package model using the configuration determined from the ADS Schematic model. It is extremely important to incorporate variables into this drawing (I use variables for nearly every aspect of every component in my models to maintain versatility throughout the design stage.). This will allow for quick adjustments to line/stub lengths, widths, heights, positions, etc. The simulated S-parameters of this

model should also be de-embedded to the device measurement reference plane and the MN reference plane.

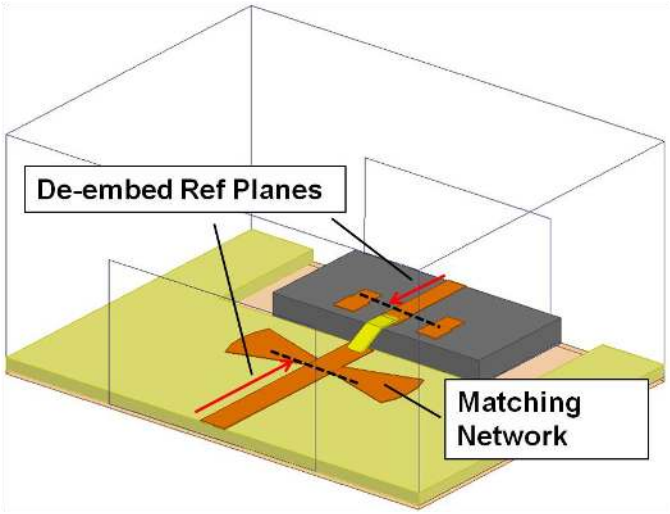


Figure B.5: HFSS model of the packaged device with MN components.

9. **Perform an S-parameter block simulation in ADS schematic with the chip and HFSS-modeled MN (Figure B.6).** Simulate the three developed ADS models (Ideal, Lossy, S-parameter Block models) together in one schematic window. A comparison of the newly developed HFSS block simulation with the already optimized performance of the ADS designed MNs will undoubtedly show the HFSS model needs to be adjusted. For simple MN structures, observing the input and output impedances on the Smith chart will provide direction on how to adjust the MNs in HFSS. Repeat this step for each adjustment of the MN until the S-parameters match closely with the ADS lossy model. For more complicated MN designs and further optimization of performance, it may not be as intuitive to look at impedances on the Smith chart for guidance. A less eloquent but effective method is discussed in Step 10.

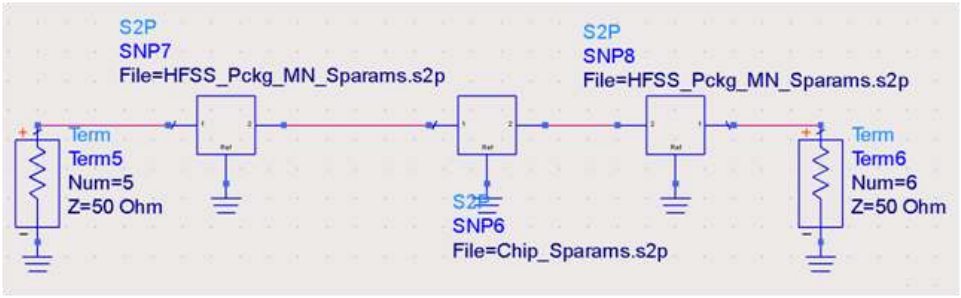


Figure B.6: ADS Schematic block simulation of extracted S-parameters from HFSS modeled MNs.

10. **Perform a parametric sweep to adjust the lossy model to overlap with the S-parameters of the block simulation.** This is a quick, backtracking method of determining which MN component should be adjusted in the HFSS model to attain a better impedance match. By adjusting the ADS lossy MN components to correlate with the poorly matched S-parameters observed in the block simulation, it is possible to figure out which component line lengths should be adjusted back in the HFSS model. This step is then repeated until the block simulation S-parameters match closely with the expected performance.

B.2. Design Verification & Feedback

11. **Fabricate, assemble and measure packaged device.** The simulated performance of the package is only accurate if the user is accurate in the modeling. The best way to verify accurate modeling is through fabrication and measurement of the package.

12. **Compare simulated and measured performance.** If the measured data matches well with the simulated response then the model can be confidently incorporated into the rest of the project. If this is not the case, a series of steps can be followed to deduce possible sources of error. The following list is a guide to help find these errors:

- Re-calibrate the measurement setup and re-measure the packaged device.
- Check HFSS simulations for proper setup. Ask someone to look over your models.

- Check the de-embedding performed in the HFSS models. Ensure the reference planes have been properly set.
- Inspect the assembled package to ensure the HFSS model accurately represents all of its aspects. Check metal thickness, line widths/lengths, wire bond loop, flip-chip bump height, etc.
- Verify the device S-parameters used in the simulations are valid.

13. **Update the HFSS model to match all physical aspects of the package.** There are certain aspects of the packaged device that may not have been accounted for in the models. It is important to use this feedback for further development of the package and optimization of the MNs.

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"If duct tape is what holds the world together,
Silver epoxy is what keeps my world from collapsing"