Extended Dynamic Range from a Combined Linear-Logarithmic CMOS Image Sensor

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Abstract

Dynamic Range determines the ability to see detail in scenes with varying illumination intensities, whether the viewing element is an eye, conventional film, or a digital image sensor. There are two distinct measures of dynamic range: interscene and intrascene. The first is the absolute range viewable, where the viewing mechanism has time to adapt to the full range of sensitivity to incident illumination and the second is the range achievable in just a single setting and time.

Digital image sensors are not renowned for their intrascene dynamic range capabilities and simply pointing a video camera at a scene that includes both indoor and outdoor ambient lighting levels will usually render the indoor or outdoor part of the scene useless. There are numerous situations where a wide intrascene range needs to be imaged.

CMOS imaging solutions are dominated by linear response sensors, as these devices offer the best signal to noise ratio. However, their dynamic range is usually limited. By contrast, logarithmic sensors compress the received signal to allow a greater range of illumination intensities to be captured. The compression unfortunately makes the noise more prominent.

The research reported in this Thesis investigates how to combine linear and logarithmic modes of circuit operation to improve CMOS imager intrascene dynamic range. A single chip, 360x288 pixel image sensor has been designed, fabricated and characterized to demonstrate the ideas developed during the research. The pixel circuits are switchable between linear and logarithmic modes: after the set exposure period the linear result is readout then the logarithmic mode is switched in and read-out. Single or two parameter calibration can be performed to reduce the relatively high level of FPN (Fixed Pattern Noise) in the raw logarithmic data. The settling time of the logarithmic mode of operation is identified as an important constraint on this approach and is optimized by the inclusion of an amplifier. To permit a pixel pitch of 5.6μm in a 0.18μm technology and achieve a 33% fill-factor, circuit and layout architectures have been devised to place the majority of the amplifier in the column in a way that allows it to be switchable between rows.

The combining of linear and logarithmic data in a single image provides an intrascene dynamic range in excess of 120dB. The sensor can operate at 26 frames per second when employing single parameter calibration of the logarithmic mode. Comprehensive characterization of both modes and the overall performance of the sensor is also outlined. Critical discussion and suggestions on further research conclude the Thesis.

Declaration of originality

I hereby declare that the research recorded in this thesis and the thesis itself was composed and originated entirely by myself in the Department of Electronics and Electrical Engineering at The University of Edinburgh, and at STMicroelectronics Imaging Division, Edinburgh.

Other people who have contributed significantly to this work are acknowledged at the appropriate places in the thesis text.

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Acronyms and abbreviations

3T	3-Transistor pixel
ADC	Analogue to Digital Converter
APS	Active Pixel Sensor
ASIC	Application Specific Integrated Circuit
BW	Bandwidth
CCD	Charge-Coupled Device
CDS	Correlated Double Sampling
CIF	Common Intermediate Format
CMOS	Complementary Metal Oxide Silicon
DAC	Digital to Analogue Converter
DDS	Double Data Sampling
FPGA	Field Programmable Gate Array
FPN	Fixed Pattern Noise
I^2C	Inter IC (two-wire serial bus connection)
IC	Integrated Circuit
LSB	Least Significant Bit
MOSFET	Metal Oxide Silicon Field Effect Transistor
MSB	Most Significant Bit
NMOS	N-type Metal Oxide Silicon
PCB	Printed Circuit Board
PMOS	P-type Metal Oxide Silicon
PSRR	Power Supply Rejection Ratio
RMS	Root Mean Square
SNR	Signal to Noise Ratio
SRAM	Static Random Access Memory
TFA	Thin Film on ASIC
VGA	Video Graphics Array

Chapter 1
Introduction

1.1 Introduction

The market for image sensors is increasing every year with new applications becoming apparent. Over the course of this project the most obvious uptake of image sensors has occurred in portable technology with the mobile phone being a prime example. Such applications generally incorporate lower resolution imagers that are optimised for low power and not image quality. Higher resolution sensors are mandatory in the digital stills market where image quality is of prime importance. In addition to the consumer driven markets imaging systems find use in areas such as machine vision and more recently automotive[1]. Image processing techniques are used to provide some form of automatic feedback control. Such systems may operate in harsh environments or may have to deal with extreme lighting levels. Such conditions often require more specialised imagers. An imager from any of the markets mentioned is likely to belong to one of two main technologies: CCDs or CMOS. The former is a 'Charge Coupled Device' and is a mature technology first reported by Boyle and Smith in [2]. It is used in systems ranging from camcorders to scientific space cameras and offers a low noise solution. As their name suggests, CCDs primarily operate on packets of charge. The light generated charge for each photo-site is transferred to an output stage by controlling the electric field applied to a set of serially connected registers. A high transfer efficiency has been achieved with the mature technology now available.

CMOS stands for Complementary Metal Oxide Silicon and although it is a long established semiconductor technology it has only recently been used for imaging. In 1967 Weckler [3] reported the sensing capability of MOS and predicted its use in imaging arrays. Due to a large feature size it was not until the early 1990s that the CMOS technology was realistically applied to image sensors [4]. CMOS imagers convert the photo-generated charge to a voltage at an earlier stage of the readout. The voltage signal is then read out using conventional circuitry easily implementable in a CMOS process. This is in contrast to CCDs in which conventional circuitry is not easily implemented in the highly optimised process. Other potential advantages

such as increased integration, lower power consumption and reduced cost have driven research and only recently CMOS imagers have approached the image quality offered by CCDs. Further information on the historical background of CMOS image sensors can be found in [5].

1.2 Dynamic Range

In any imaging system Dynamic Range is the ability to see or capture detail at varying illumination levels. There are two distinct measures of dynamic range: interscene and intrascene. The first is the absolute range viewable, where the viewing mechanism has time to adapt to the incident illumination. For example, consider the large difference in illumination intensity between a bright sunny day and a poorly lit indoor room. Humans can generally see in both these conditions if their eyes are given sufficient time to become accustomed to the illumination level. However, consider viewing both these scenes at the same time, i.e. being inside the poorly lit room and looking out into the bright sunshine (or outside in the bright sunshine looking into the poorly lit room). In such a situation the viewer is unlikely to be able to see the same detail in each scene as they did when looking at them individually. The range viewable at a single setting and time is referred to as the intrascene dynamic range and will be less than the interscene range.

An example scene with a wide dynamic range is shown in Figure 1.1.

The scene was captured with a linear integrating sensor and at the set exposure the indoor office environment is clearly visible. However, the majority of the oudoor part of the scene is saturated due to the increased brightness. Reducing the exposure period could capture more detail in the outdoor scene but would sacrifice detail from inside.

Dynamic range is often quoted in decibels where

$$Dynamic\_Range(\text{dB}) = 20 \log \left(\frac{Max\_illumination\_level}{Min\_illumination\_level} \right) \tag{1.1}$$

For a linear CMOS image sensor the maximum and minimum distinguishable illumination levels are given by the maximum and minimum detectable photo-currents. The first is given by the largest photo-current that doesn't cause a pixel to saturate whilst the minimum detectable photo-current is set by the noise floor.

Figure 1.1: *Wide dynamic range scene.*

Radiometry is a system of mathematical relationships and terminology used to describe and measure radiation [6]. The electromagnetic spectrum contains radiation of wavelengths from 0 to infinity however the human eye is only sensitive to a small part of this. The 'visible spectrum' refers to radiation with a wavelength between about 400nm and 760nm. Long wavelength radiation in the visible spectrum appears red and decreasing wavelengths will render green, blue then violet colour. The human eye is most responsive to radiation at about 555nm in wavelength. One lux is given by 1.46mW of radiant electromagnetic power impinging at a right angle on an area of one square meter. Because lux is dependent on the spectral content of the radiation (defined over visible spectrum) this work uses irradiance[7]. The irradiance from a halogen light source was measured in W/m^2. A protective blanket was used to block UV and IR radiation outwith the visible spectrum.

Some typical light levels are listed in Table 1.1.

It can be seen from Table 1.1 that the illumination level can vary widely in typical everyday situations. Conventional CCD or CMOS image sensors do not have a wide dynamic range and typically manage 55dB to 70dB. Specialised sensors have been developed and will be discussed

Scene	Illumination level (lux)
Starlight	0.001
Full moon	0.1
Twilight	10
Overcast day	1000
Sunny day (indirect light)	10000

Table 1.1: *Typical luminosity levels (Range shown is 7 decades=140dB).*

in Chapter 2 but such systems usually result in increased overhead.

There are specific applications where extreme illumination levels require an image sensor with a wide dynamic range, the automotive industry [1] being one of these. It has been suggested that some form of automatic navigation could be used to track the lines on the road. Obviously such a system would have to be able to cope with a variety of extreme conditions one of which would be extreme illumination levels. An example situation could be a vehicle exiting a dimly lit tunnel into bright sunshine. The lines on the road would need to be visible in both scenes at the same time.

1.3 Human vision

Humans can adapt to a luminance range in excess of ten log units as shown in Figure 1.2 [8]. At low illumination human eyes are most sensitive but acuity and ability to detect colours are both poor. This is known as the scotopic region. Conversely, with illuminance of daylight, good quality colour vision results but the absolute sensitivity is poor. This is known as the photopic region.

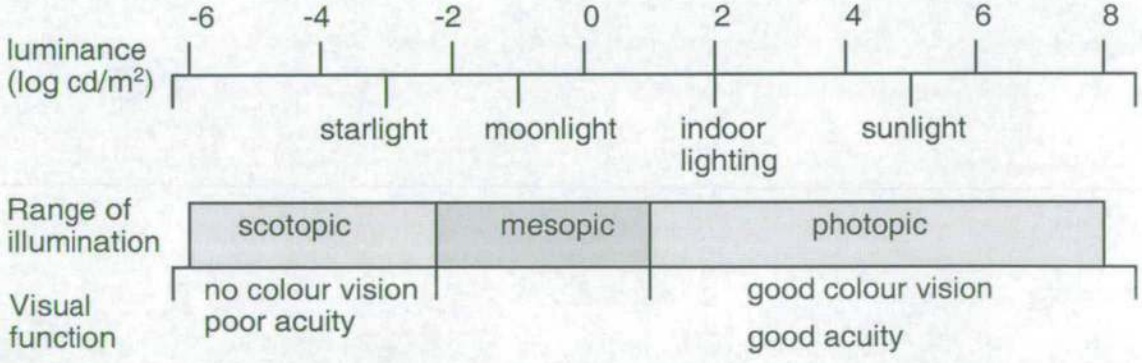


Figure 1.2: *Natural illuminaces and human visual parameters.*

In the eye, rods and cones sense the illumination and send signals to the brain. There are approximately 75-150 million rods which are used at scotopic levels, and only 6 to 7 million cones which sense at photopic levels. Adaption to the incident illumination is achieved by various mechanisms all of which have limitations. Variation of the pupil diameter increases or reduces the amount of light entering the eye whereas at a biological level a chemical process attempts to restore photosensitive pigments faster than the light can deplete them.

1.4 Project Aims

This thesis investigates a method to extend dynamic range in a CMOS image sensor. The majority of CMOS sensors obtain a linear response by integrating the photo-generated charge over a given exposure period. Although this method provides a good signal swing compared to the noise level the dynamic range is limited. Methods to extend the range of linear sensors are presented in Chapter 2 but usually increase the system overhead. In contrast, a sensor operating in logarithmic mode compresses the input illumination level into a greatly reduced voltage range. It is thus able to image scenes of a wide dynamic range. Unfortunately the compression also makes the noise more significant thus reduces the perceived image quality especially at low illumination levels.

This thesis looks at acquiring the two sets of data independently and asks the questions:

'can a wide dynamic range scene be imaged by combining linear and logarithmic data?'

and if so

'can the two sets of data be acquired and combined in a system operating in real-time?'

The inherent properties from logarithmic mode may realise a sensor with a wide dynamic range whilst the linear data maintains performance at reduced illumination. Such a sensor requires design and evaluation in two main areas:

New pixel architecture: each photo-site should produce both linear and logarithmic data. This requires the creation of a pixel that can be switched between the two operating modes. It is also desirable to maintain a small pixel pitch.

Overcoming Logarithmic shortcomings: Fixed Pattern Noise (FPN) and response time are

major drawbacks of conventional logarithmic operation and need to be addressed

The project required the use of many different tools but began and ended in a similar fashion. The initial feasibility study used actual data from a CMOS image sensor. The device was manually configured in the two modes to allow the formation of combined linear-logarithmic images. This work utilised test hardware, image capture software and then used purposely written software in C++ to combine and calibrate the image data. The second phase of the work focused on circuit design and consisted of circuit schematic creation then simulation to verify/optimise operation and performance. Circuit schematics were then translated into a set of 2D mask patterns that could be used to fabricate the device in silicon. Extraction of layout parameters and re-simulation was also required to confirm circuit operation. The fabricated devices were then tested and characterised on the bench.

1.5 Thesis Structure

- Chapter 2 provides background information on CMOS image sensors and introduces published work that is aimed at extending the dynamic range of CMOS sensors.
- Chapter 3 configures a standard sensor in logarithmic mode and investigates FPN reduction techniques. The combination of logarithmic data with linear data within a single frame is also performed.
- Chapter 4 compares two logarithmic architectures in terms of sensitivity and transient performance.
- Chapter 5 discusses the design of a Common Intermediate Format (CIF) array CMOS image sensor which can operate in linear and logarithmic mode and combine data whilst realising real-time operation
- Chapter 6 presents the characterisation results and evaluation of the individual and combined modes of operation.
- Chapter 7 concludes with a summary of the project and a critical discussion of the work.

The only other known work that combines linear and logarithmic operation in an image sensor was presented by Fox *et al* in [9]. The technique, which is discussed in Chapter 2, does not allow the two sets of data to be processed individually.

Chapter 2
Background

CMOS image sensors exist in different variants with several operating modes. This Chapter provides an overview of CMOS image sensors including the processes that take place from incident illumination through to the formation of the electronic image.

The work of this thesis is targeted at imaging high dynamic range scenes thus existing techniques are discussed. Such information can be compared to the author's work and provides justification for embarking on the research presented.

2.1 Digital Imaging System

Many blocks are required in an imaging system, each playing its own important role.

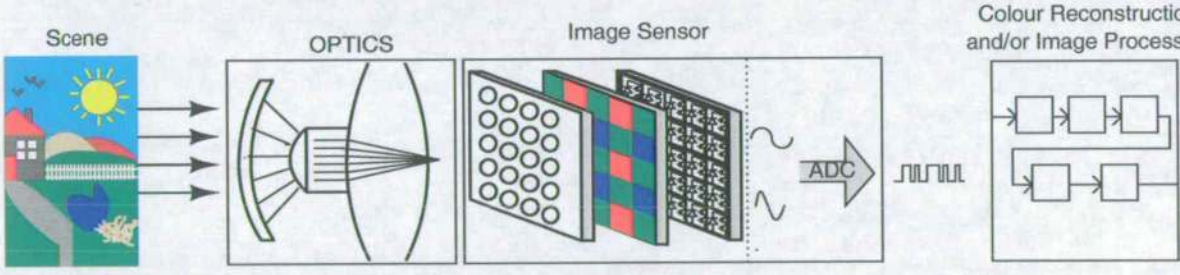


Figure 2.1: *Digital imaging system.*

Figure 2.1 shows the main blocks in a colour imaging system: optics, image sensor and post processing. The scene has to be correctly focused onto the CMOS or CCD sensor which contains thousands or millions of light sensitive sites. A lens mounted above the sensor provides the first layer of optics but it is common for each photo-site to have a microlens directly above. The microlens array further focus light to each photo-site. For conventional colour imaging different colour filters are patterned directly above each light sensing site.

Each photo-site converts the incident light into a collection of charges which are then collected to generate a photocurrent. The magnitude of photocurrent that flows is proportional to the

illumination intensity at that photo-site. A pixel contains at least one photo-site alongside additional circuitry required for either amplification, buffering, addressing or resetting. Each pixel is addressed and the information therein transferred to the output. This data is usually then converted to a digital value for any processing required.

2.2 Light conversion

Optical energy is absorbed and converted into charge carriers if photon energy is greater than the material bandgap voltage. Photo-detection, unlike solar cell applications, normally requires fast response and high sensitivity for narrow-band energy however the response is not normally so important in image sensors. The photon energy, E_{ph} is given by Equation 2.1 where h is Planck's constant and v is the frequency of the light.

$$E_{ph} = hv \tag{2.1}$$

If the energy of a photon is less than the band gap energy, E_g, of the semiconductor the material will appear transparent. Alternatively, if $E_{ph} \geq E_g$ then the photon will be absorbed and an electron-hole pair created. The fraction of photons absorbed is proportional to the photon flux $F(x)$.

$$F(x) = F_{ph} \exp^{-\alpha x} \tag{2.2}$$

where F_{ph} is the photon flux at distance x=0 into the silicon and α is the absorption coefficient. Since α is itself dependent on the wavelength of the incoming light Equation 2.2 can be written in terms of distance and wavelength.

$$F(\lambda, x) = F_{ph}(\lambda) \exp^{-\alpha(\lambda)x} \tag{2.3}$$

The absorption dependency on wavelength sees blue light being absorbed very close to the surface then green light slighter deeper and red light deeper still.

As mentioned, conventional imaging systems use a set of colour filters positioned above the sensor causing each photo-site to be sensitive to only a single colour. A common set of filters is the Bayer pattern [10] consisting of green, blue and red filters. The downside to this approach is a reduction in spatial resolution since 2 colour responses for each pixel need to be

estimated from its neighbours. Other colour reproduction techniques exist which aim to reduce the number of colour filters required [11] or completely remove the need for any filters [12]. Since radiation of different wavelengths is absorbed at different depths into the silicon, the techniques use photo-receptors stacked vertically to collect the charge. The challenge in such work is ensuring that radiation of a certain wavelength is collected by the correct sensing region. Colour theory is outside the scope of this thesis and will not be covered in any detail. In the remainder of this work each pixel or photo-site will be assumed to only have a single sensing element.

A common expression is the quantum efficiency, η, which expresses how well the photo-site converts the incident photons into a usable photocurrent.

$$\eta(v) = \frac{Number\_of\_collected\_electron\_hole\_pairs}{Number\_of\_incident\_photons\_of\_wavelength\_v} \tag{2.4}$$

η will generally be less than one due to effects such as recombination. The generated electron hole pairs can be collected using different structures. Moini's text on vision chips [13] contains a short but useful overview of different CMOS photo-detectors.

2.2.1 Photo-transistor

The photo-transistor is attractive as a sensing element as it provides a higher sensitivity compared to other structures due to the transistor gain. The base region of a conventional bipolar transistor can be used as the light sensitive element. The generated base current will be amplified by the β of the device, producing a collector current. Unfortunately, the advantages of sensitivity are out-weighed by poor matching of transistor gains and increased dark current [14][15]. An array of sensing elements should be well matched to reduce the FPN in an image. FPN may exist as offset errors, gain errors, both or even as a non-linear function. It is possible to correct for FPN but because the β of the photo-transistor is liable to change for low light levels the correction would be difficult and costly. The increased dark current (see Chapter 2.3.4) degrades a sensor's performance in low light conditions where the noise is comparable to the signal.

2.2.2 Photogate

By adjusting the voltage of a polysilicon gate, a potential well can be created in the silicon below. Photo-generated electrons will collect in this well and after a set exposure they can be transferred by pulsing the gate voltage. If a silicided process is used a poor response results due to the low transmittance of the gate [16].

2.2.3 Photodiode

A reverse biased p-n junction can be used to collect the light generated electron-hole pairs and produce a photocurrent. Collection is achieved by drift in the depletion region where the electric field collects electron hole pairs and recombination is zero. It is beneficial to have a large depletion region, thus an Nwell to Psubstrate diode is preferable to a more highly doped N+ to Psubstrate structure [17]. Also lower n-type doping means less chance of recombination. Diffusion from the lightly doped substrate can occur but the collection efficiency is much reduced from that of the depletion region.

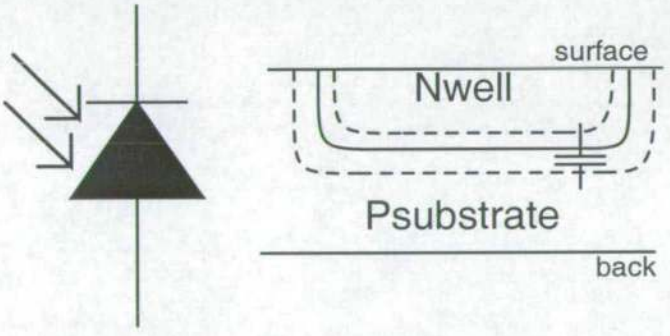


Figure 2.2: *Nwell/Psubstrate photodiode symbol and cross-section.*

Conventional operation of the sensing elements follow a reset, integration then read sequence of events. For the case of the photodiode, reset is achieved by reverse biasing the junction. It should be noted that the diode has an associated capacitance caused by the junction and this is charged during the reset phase. After the reset voltage is sampled this capacitance maintains the reverse bias field. A larger reverse bias will increase the depletion region of the junction thus collecting more photons. Incident radiation creates charges, causing the potential across the junction to reduce. After a period of integration the detector potential is sampled to give a measure of the incident illumination If the photo-current fully discharges the detector it is said to be saturated.

In a similar fashion, the detector can be thought of as a potential well. The photo-generated charge will gradually fill the well and when full the detector is said to be saturated. This is known as the full well capacity.

For wide dynamic range applications where extreme illumination levels are encountered the full well imposes a limit on the number of charges that can be collected. Assuming a single integration period, a large well would be preferred under high illumination to prevent saturation. However, an increased well capacity usually reduces the sensitivity at lower illumination. Since the sampled voltage is normally converted into a finite number of digital codes, linear systems are not well suited to wide dynamic range imaging when using a global integration period across the array.

2.2.4 Sensor overview

In addition to the light sensing element, a pixel contains circuitry that isolates the photo-site and allows multiplexing of data from other sites to the output of the device. Unfortunately, such additiona circuitry reduces the sensitivity of a device, as less area is used for light conversion. The use of microlenses as mentioned previously, can reduce this problem by concentrating the light at each photo-site.

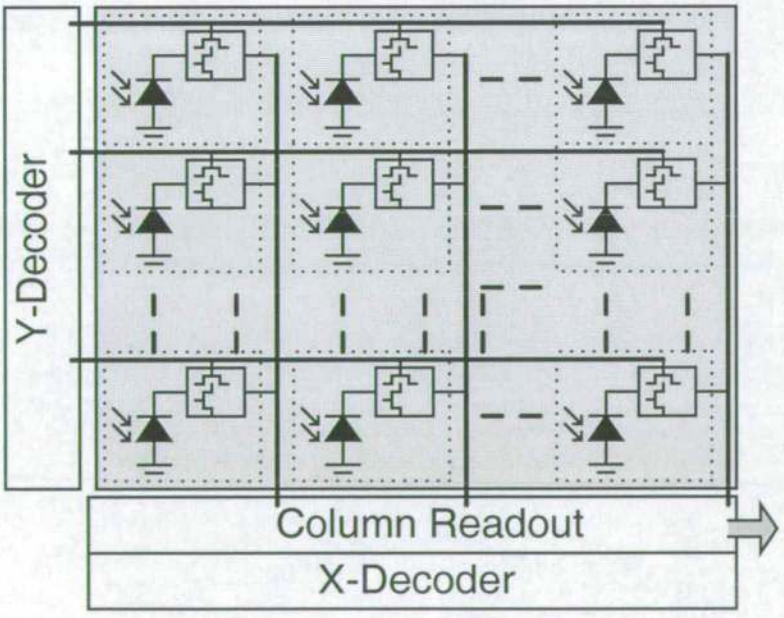


Figure 2.3: *Typical sensor architecture.*

Figure 2.3 shows a typical array of pixels with the surrounding control circuitry. Within each

pixel is a photo-detector and any additional circuitry (which can vary as will be shown in Chapter 2.4). All pixels of the same horizontal row are accessed concurrently thus transferring pixel information onto the corresponding column bus which is then multiplexed to a serial output. As such sensors are the front end to digital cameras it is common to ask at which point the transition from analogue to digital should take place? There are three places where an Analogue to Digital Converter (ADC) can be situated with corresponding pros and cons for each. A single ADC can be positioned in the analogue readout chain and could even be located off-chip. Such an ADC would have to perform the conversion relatively fast to achieve an acceptable frame rate and as array sizes increase, ADC conversion times would have to decrease as the square of the linear dimensions. However, the existence of a single output path subjects the data from all pixels to the same gain and offset errors thus not introducing any FPN.

Currently, the most common site for Analogue to Digital conversion is in the column. A single ADC per column converts the selected pixel data which can then be readout faster in the digital domain with less loss of sensitivity or introduction of additional noise. Column parallel ADCs need to be well matched to prevent column FPN becoming an issue. However, the ADC bandwidth is proportionately less and this improves its noise performance.

The final option is to place an ADC in every pixel within the array. Such ADCs can operate at very low conversion rates as well as maintaining very high frame rates. The major disadvantage of an in-pixel architecture is the adverse effect on fill factor and pixel size[18]. However, the continual advancement of process technology to smaller geometries is permitting more in-pixel circuitry without a dramatic increase in size [19]. Kleinfelder et al [20] report an 8bit ADC per pixel in a 'digital pixel sensor' with a pixel pitch of 9.4μm.

2.3 Noise

Before more detail is given on different pixel structures the main sources of noise are reviewed. A major concern in improving CMOS image sensor performance is noise reduction in the pixel and near pixel circuits.

2.3.1 kTC noise

Any resistance R generates thermal noise which is white and dependant on temperature. The noise voltage can be written as

$$v_R^2 = \int_{f_0}^{f_1} 4kTRdf \tag{2.5}$$

and when sampled onto a capacitor it produces what is known as kTC noise. k is Boltzmann's constant and T is the absolute temperature.

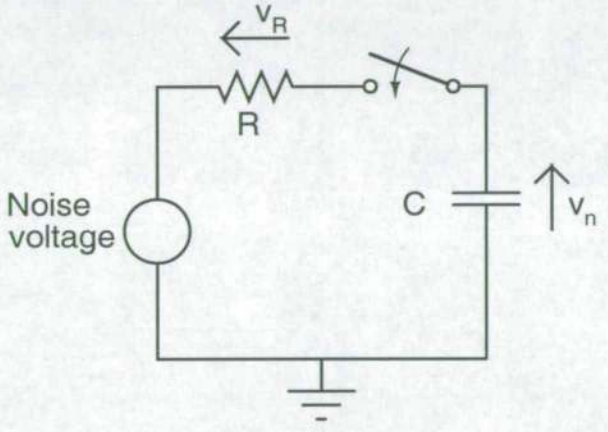


Figure 2.4: *Thermal noise sampled onto a capacitor.*

Consider the transfer function of the circuit in Figure 2.4 which is given by

$$H(\omega) = \frac{1}{1 + j\omega RC} \tag{2.6}$$

where $\omega = 2\pi f$. The output noise of the resistor is governed by the transfer function of the RC network and can be written as

$$v_n^2 = \int_0^{\infty} 4kTR|H(\omega)|^2 d\omega \tag{2.7}$$

$$v_n^2 = 4kTR \int_0^{\infty} \frac{1}{(2\pi fRC)^2 + 1} df \tag{2.8}$$

Now, using the inverse trigonometric relation

$$\frac{d(arctan(x))}{dx} = \frac{d(tan^{-1}(x))}{dx} = \frac{1}{x^2 + 1} \tag{2.9}$$

Equation 2.8 becomes

$$v_n^2 = 4kTR\frac{\pi}{2}\frac{1}{2\pi RC} = \frac{kT}{C} \tag{2.10}$$

Equation 2.10 can be expressed in terms of charge by multiplying by the capacitance

$$Q = CV = C\sqrt{\frac{kT}{C}} = \sqrt{kTC} \tag{2.11}$$

Equation 2.10 shows that the noise voltage can be reduced by increasing the capacitance, however, when considered in terms of a pixel's performance this would also reduce the signal swing. Alternately, Equation 2.11 shows that a reduction in the size of capacitor will reduce the noise associated charge.

2.3.2 Flicker or $\frac{1}{f}$ noise

Flicker noise is a measure of the conductive medium and needs to be added to thermal noise. It becomes dominant at low frequencies as shown in Figure 2.5 [21].

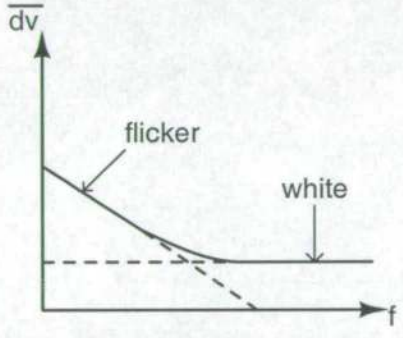


Figure 2.5: *Graph showing prominence of flicker noise at low frequencies.*

Flicker Noise is not dependent on temperature but is proportional to current. A high number of defect states and/or a small conductive volume increases $\frac{1}{f}$ noise. The $\frac{1}{f}$ component of noise is given by

$$v_{RF}^2 = \int_{f_0}^{f_1} KF_R\frac{R_s^2}{A_R}V_R^2\frac{df}{f} \tag{2.12}$$

from [21] where A_R is the area of the resistor, V_R is the DC voltage across the resistor, KF_R is a technology dependent constant and R_s is the sheet resistance.

Whilst large area devices display the $\frac{1}{f}$ spectrum, smaller area MOSFETS exhibit a **Random**

Telegraph Signal(RTS). Uren *et al* measured devices from $350\mu m^2$ to $0.4\mu m^2$ and found that individual devices with smaller areas deviated from the $\frac{1}{f}$ response although the average across devices remained $\frac{1}{f}$ [22]. Both a high and low state were clearly visible in a trace of the drain current. The work by Uren *et al* suggests that carrier trapping into states in the oxide drives the $\frac{1}{f}$ process.

2.3.3 Photon shot noise

Incident illumination itself introduces noise due to the statistical nature of photon emission. The distribution is known to follow a Poisson distribution where the number of noise electrons is given by the square root of the number of photon generated electrons [23]:

$$n_{shot} = \sqrt{\frac{Q_{ph}}{q}} \tag{2.13}$$

If shot noise is the limiting factor its effect can be reduced by collecting more light.

2.3.4 Dark current noise

Under zero incident illumination a reverse bias current will still flow in the photodiode. This is known as dark current and limits the low light performance of a sensor. Variation of the dark current across the array creates a fixed spatial error. The dark current generation mechanism is also random as a function of time thus dark current shot noise results and is described in the same way as photon shot noise. Thus the dark current at each photo-site in the array will vary in time but have a constant mean value. The dark current mean also shows an exponential increase with temperature, doubling every 7 to 9 ^oC [24].

2.3.5 Photo-Response Non-Uniformity (PRNU)

Due to process variations the sensitivity of each pixel in the array may not be the same. If PRNU is significant, uniformly illuminated areas of a scene will appear to differ.

2.3.6 Fixed Pattern Noise (FPN)

Process variations can also cause the offset or gain of the readout electronics to change. If a column parallel architecture is implemented a vertical strip pattern can result if the matching between columns is not maintained.

2.3.7 Quantization noise

Quantization noise results when any analogue signal is represented by a finite number of digital codes. It cannot be improved by design thus an ideal ADC with a finite number of bits still suffers from quantization noise. Consider an analogue input signal in the range 0V to V_{ref} which is digitised to an N bit word. The voltage change of the least significant bit (LSB) is given by

$$V_{LSB} = \frac{V_{ref}}{2^N} \tag{2.14}$$

The error introduced by representing the analogue signal with a finite number of states is given by V_x and lies in the range $-\frac{1}{2}V_{LSB} \leq V_x \leq \frac{1}{2}V_{LSB}$

The rms value of the noise signal is found to be

$$V_{Q(rms)} = \frac{V_{LSB}}{\sqrt{12}} \tag{2.15}$$

when the quantization error is assumed to be uniformly distributed between $\pm\frac{V_{LSB}}{2}$. This leads to a formula for the best SNR in an analogue to digital converter. If the input is a sinusoidal waveform between 0 and V_{ref} (AC power = $\frac{Vref}{2\sqrt{2}}$) then the SNR is given by

$$SNR = 20\log\left(\frac{V_{in(rms)}}{V_{Q(rms)}}\right) \tag{2.16}$$

$$SNR = 6.02N + 1.76 \tag{2.17}$$

of which the units are dB.

2.3.8 Power supply noise

Noise spikes can be generated by fast switching circuitry and regularly occur in high speed digital blocks. In modern designs analogue and digital blocks are commonly integrated within a single device thus interaction between the two is possible from shared supply lines, ground connections or the substrate. It is thus important that sensitive analogue circuits can reject the noise from its supplies. A measure of a circuits tolerance to noise on a supply is given by the Power Supply Rejection Ratio (PSRR). For a given circuit, if A_v is the gain from the input node to the output node and A_{sup} is the gain from one of the supplies to the output, then the PSRR is given by:

$$PSRR = \frac{A_v}{A_{sup}} \tag{2.18}$$

2.3.9 Conclusions

Developments in technology and continual design improvements will reduce the effect of some noise sources which in turn causes other noise sources to become the limiting factor. Historically the move from Passive pixels to 3T pixels reduced FPN and saw kTC noise become dominant. More recently the pinned photodiode has overcome kTC noise. This causes other noise sources to become dominant [25][26]. Pixel structures are discussed in the next section.

2.4 Pixels

As mentioned earlier, an imaging array is made up of an array of photo-detectors each of which are situated inside a pixel structure so that information can be appropriately stored and read out. This section briefly reviews some of the different pixel structures that have been used.

2.4.1 Passive pixel

The simplest pixel type is known as the passive pixel and consists of a single MOSFET connected to a photodiode as shown in Figure 2.6. The original idea was published in 1967 by Weckler [3] but it was many years before the surrounding circuitry caught up to enable fabrication of a sensor array like the ones available today.

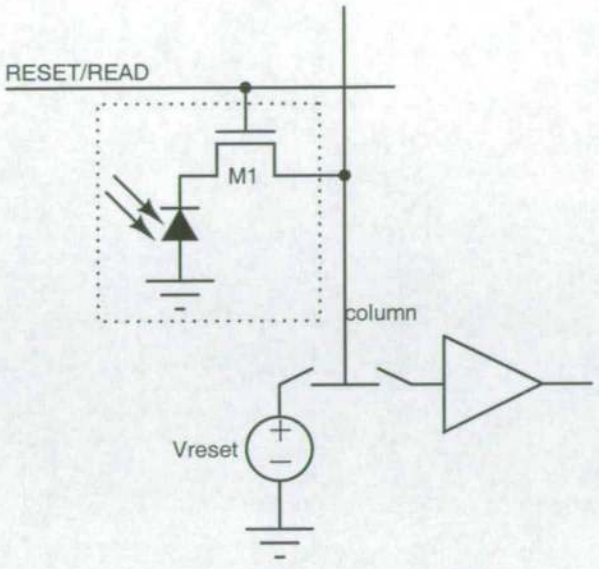


Figure 2.6: *Passive pixel.*

A single access transistor is used to reset and read the pixel. During the reset phase the column line is set to the reset voltage and *M1* turned ON. The photodiode voltage will thus be raised to the reset voltage. When *M1* is turned OFF the photodiode is isolated and light generated charge can discharge the associated capacitance of the diode. After a predetermined exposure time, *M1* is turned ON to read the pixel. A charge sense amplifier now connected in the column converts the collected charge to a voltage that is read out [4]. Transferring collected charge from a passive pixel to the column bus is a crucial design stage of the sensor. Small packets of charge are transferred to column lines with large capacitance thus the design of the charge sense amplifier is non-trivial to minimise noise.

This transfer of charge onto the large capacitance of the column line can be avoided if an amplifier or buffer is placed between the photo-detector and the column line. The active element is only activated during readout thus doesn't drastically increase the power consumption of the sensor. A sensor with an active amplifier in each pixel is known as an Active Pixel Sensor (APS).

2.4.2 Photodiode Active Pixel Sensor (APS) pixel

The arrangement shown in Figure 2.7 is often referred to as a 3T pixel due to the three active devices required. The photodiode is formed by extending the source implant of the reset transistor(*M2*). Reset is achieved by pulsing the gate of *M2* and integration begins. After a

set exposure time the read line is raised which connects the source of *M1* to a column current source thus creating a source-follower structure. The photodiode voltage minus the gate-source voltage of *M1* appears on the column line and can be processed as required. It has been shown by Yadid-Pecht *et al* that an extra device can be added to permit pixels of the same row to be reset at different times [27].

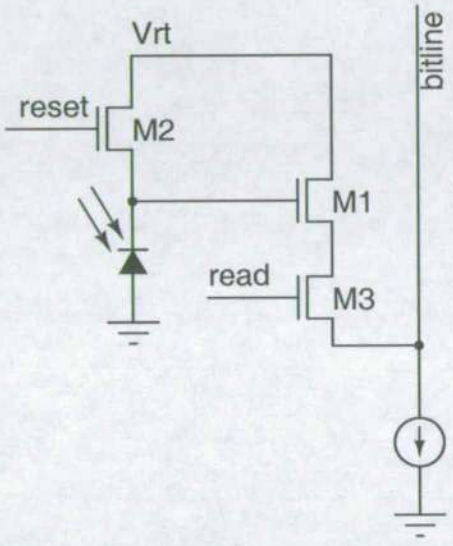


Figure 2.7: *3T active pixel and timing.*

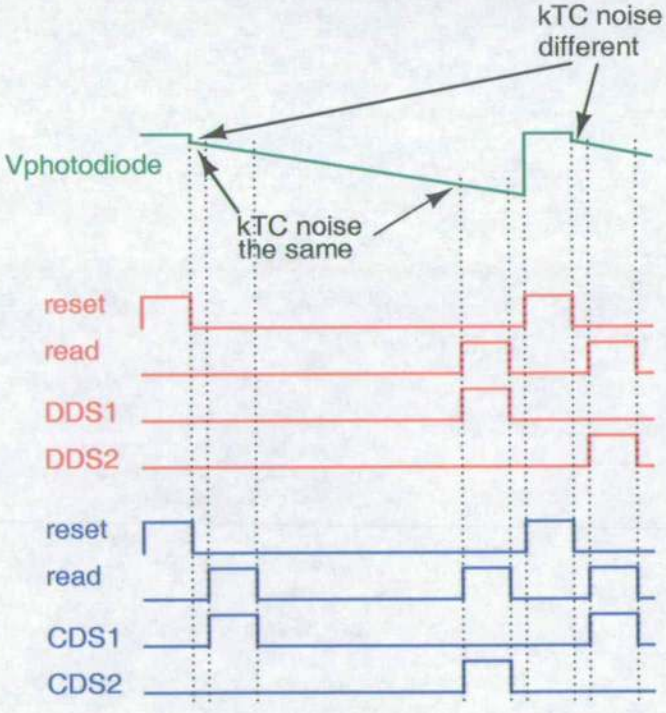


Figure 2.8: *3T active pixel and timing.*

Process variation across the array gives rise to FPN caused mainly by differences in the threshold voltage of device *M1*. Double Data Sampling (DDS) can remove this FPN by sampling the pixel voltage at the end of the integration period then again as the pixel is reset (represented by DDS1 and DDS2 in Figure 2.8. Unfortunately the kTC noise in the two samples is not correlated and cannot be cancelled. In fact, the kTC noise is increased by this double sampling technique. Correlated Double Sampling (CDS) reads the pixel twice from the same original reset level thus can cancel the kTC noise. Although it is often stated that a 3T architecture does not permit CDS, the use of a frame memory does in fact allow it to operate in this way.

2.4.3 Photogate APS pixel

The photogate APS [28][29] permits true CDS without the need for a frame memory. The pixel contains 5 transistors and is depicted in Figure 2.9 along with a charge potential diagram. Its operation uses a charge transfer technique similar to that used in CCDs.

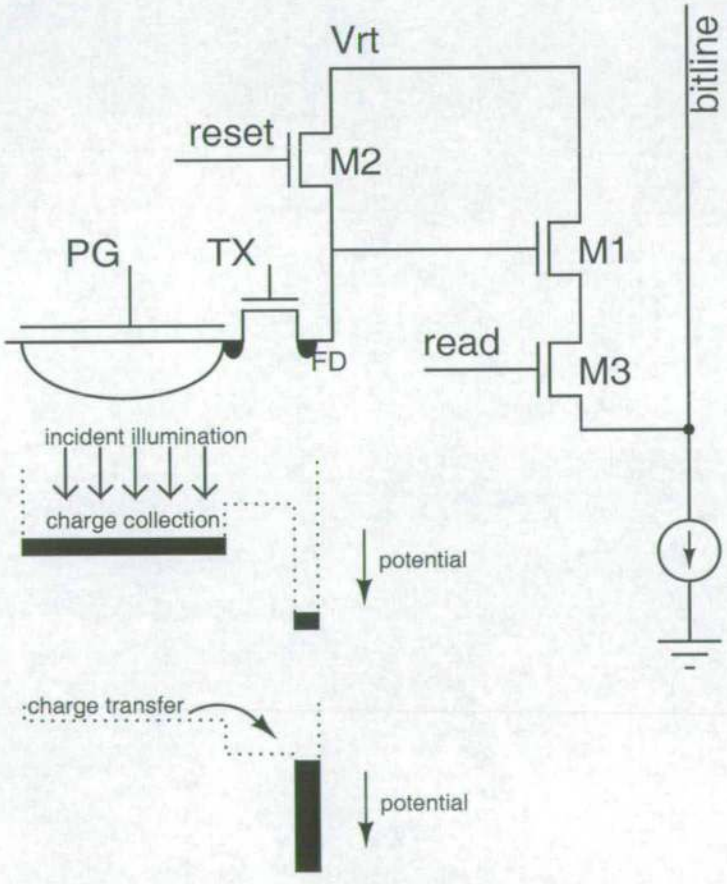


Figure 2.9: *Photogate APS schematic.*

The TX line is held at a constant voltage and does not change with time. When the PG line is raised high above TX, photo generated charge accumulates under the PG gate. After the set exposure the charge is transferred to the floating diffusion (FD) by lowering the voltage on PG below TX. The floating diffusion is reset prior to transferring the charge permitting CDS with consecutive reads of the same pixel. An additional advantage over a photodiode APS is the higher achievable conversion gain. This is the result of transferring the photo generated charge to a floating diffusion with a much smaller capacitance than that of a photodiode. A drawback as mentioned earlier is the response reduction caused by absorption in the overlying gate.

2.4.4 Pinned Photodiode (PPD) APS pixel

This arrangement can be seen as an extension/improvement to the photogate pixel.

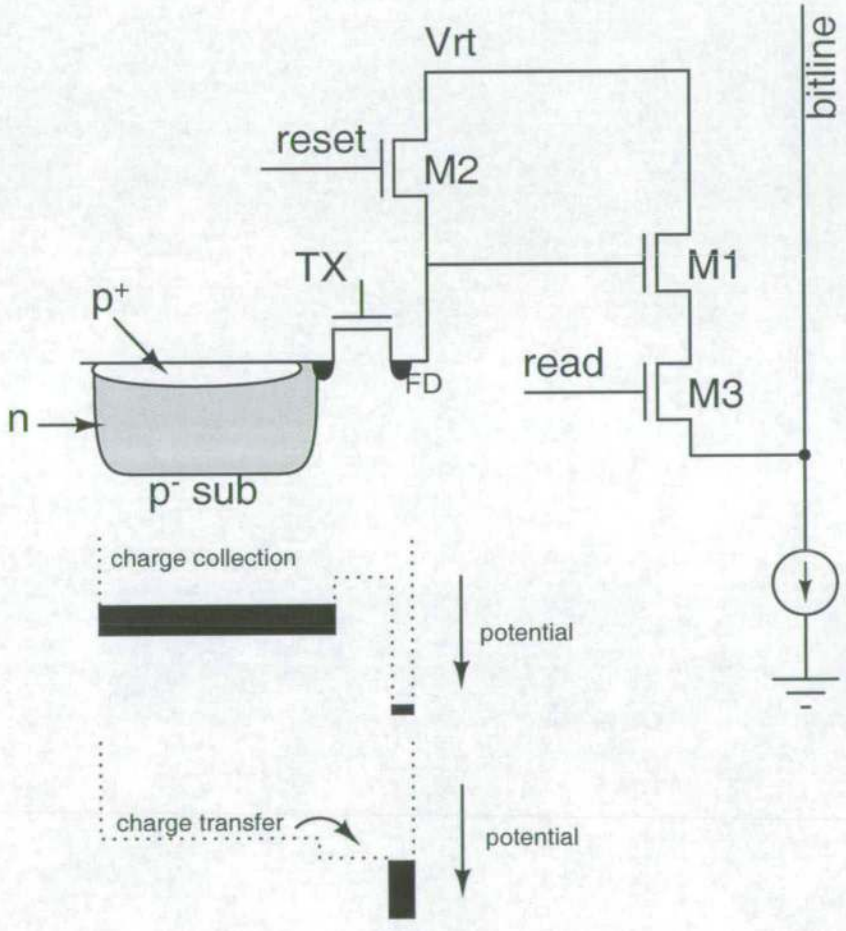


Figure 2.10: *Pinned photodiode APS.*

The structure consists of a p+np- structure where both the p-type layers are held at ground

potential. By increasing the voltage applied to the n-type layer the depletion regions at both junctions will extend until they meet. At this point the photo-sensing area is fully depleted (no kTC noise) and the potential is said to be pinned. The charge transfer is accomplished by pulsing the voltage applied to TX in Figure 2.10. CDS is achieved in the same manner as the photogate by first resetting and reading the floating diffusion. Compared to the photogate pixel the PPD has a reduced full well capacity. However, the PPD has good transparency above the photodiode and achieves a reduced dark current due to the surface layer pinning [30]. Recently, work has been done to reduce the effective pixel pitch. This is achieved by sharing the reset device and the readout source follower between a number of photodiodes. Mori *et al*[31] have four transfer devices connected to a single floating diffusion. They achieve a pixel pitch of 2.25μmx2.25μm with an effective 1.75 transistors per pixel. Their fill factor is 25% in a 0.25μm process. A disadvantage of the increased integration is a reduction in sensitivity since the capacitance of the floating diffusion node is likely to have increased.

2.4.5 Logarithmic pixel

The pixel architectures already described operate in a sampled manner such that after a given exposure period a photo-dependant signal is sensed. The relationship between the incident light intensity and the voltage output is linear. A logarithmic sensor differs by providing logarithmic conversion and operating continuously in time. Figure 2.11 shows the conventional 3-transistor logarithmic arrangement (although early work used a slightly different configuration [32]).

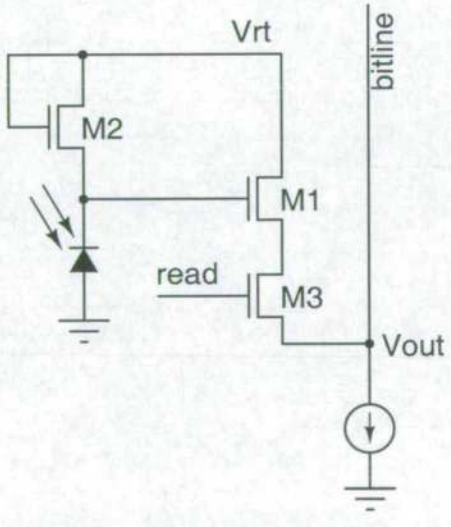


Figure 2.11: *Logarithmic APS.*

The photodiode generates a current which is supplied by diode connected device *M2*. This photocurrent is very small and will cause *M2* to operate in the sub-threshold region. In the sub-threshold (or weak inversion) region of operation the gate-source voltage varies as the logarithm of the current flowing thus providing non-linear compression on the photo-signal.

The current voltage relation can be written as in [33] neglecting the body effect.

$$I_{DS} = \frac{W}{L} I_{D0} e^{\frac{V_{GS}}{nV_t}} \left(1 - e^{-\frac{V_{DS}}{V_t}}\right) \tag{2.19}$$

and approximated as

$$I_{DS} = \frac{W}{L} I_{D0} e^{\frac{V_{GS}}{nV_t}} \tag{2.20}$$

where

- V_{GS} - gate source voltage
- V_{DS} - drain source voltage
- W - Width
- L - Length
- V_t - Thermal voltage ($\frac{kT}{q}$)
- n - sub-threshold slope factor
- I_{D0} - process dependent constant(known as the characteristic current)

The threshold voltage, V_{th}, is included in the term I_{D0} which takes the form

$$I_{D0} = I_{D1} e^{-\frac{V_{th}}{nV_t}} \tag{2.21}$$

Equation 2.20 can be rearranged to express the gate-source voltage in terms of the drain-source current.

$$V_{GS} = nV_t \ln\left(\frac{L}{W}\frac{I_{DS}}{I_{D0}}\right) \tag{2.22}$$

Such compression means a much wider range of illumination levels can be sensed, making it ideal for extended dynamic range applications. However, the pixel suffers from considerable disadvantages including lower SNR , increased lag and increased FPN. In addition, the

absence of a reference level prevents simple FPN correction as is done in linear integrating mode systems. Published work on overcoming the logarithmic pixel's drawbacks is discussed in Chapter 2.5.5.

Although the most common mode of logarithmic operation uses a photodiode under reverse bias, imaging is possible by using a photodiode operating in the photovoltaic mode. In [34] the photodiode is reset to zero volts then generates a negative voltage under illumination. Although the mismatch created by variations in device *M2* is removed the response of the detector is reduced. The absence of reverse bias means a smaller depletion region thus higher capacitance and reduced sensitivity.

2.4.6 TFA, amorphous pixel

The lateral integration of the photoreceptor with the additional pixel circuitry is non-ideal. Optimisation of the two independently is not possible due to their interaction. Image sensors which use a Thin Film on ASIC (TFA) approach do not suffer this trade-off and can optimise the light sensing area separately from the pixel circuitry. TFA technology deposits a thin film of amorphous silicon above the IC. It is actually hydrogenated amorphous silicon (a-Si:H) that is used due to its superior carrier mobility for electrical circuits. The basic layers of a TFA sensor are shown in Figure 2.12 [35]. The a-Si:H layer will further consist of a *pin* structure with a light absorbent intrinsic layer between two heavily doped regions that provide the electric field for collection of carriers.

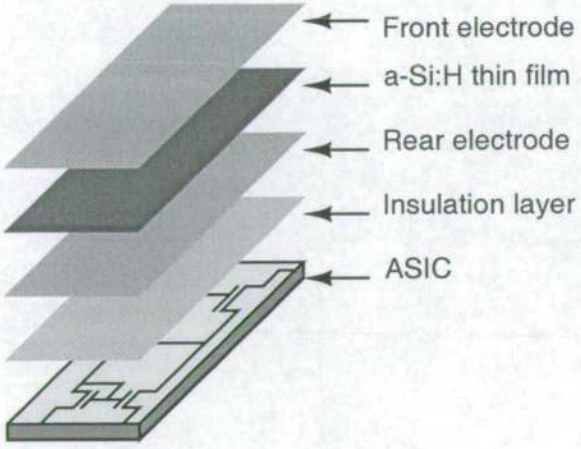


Figure 2.12: *Basic TFA layers .*

Benthien *et al* have shown the potential that 3-D integration using TFA can bring [36]. Their

published work uses a conservative 0.8μm process however small pixel sizes with the inclusion of signal processing circuitry should be possible with a more advanced technology. Another cited advantage is the reduced rise of dark current with temperature compared with crystalline devices. The obvious disadvantage is the cost associated with the extra processing steps required to deposit the amorphous silicon, insulation and electrodes but surprisingly the largest potential drawback is caused by incident illumination. If the light intensity is too intense the amorphous silicon can degrade. This is known as the Staebler-Wronski effect and is permanent.

2.5 Dynamic Range extension techniques in CMOS imagers

Much research has been done to extend the dynamic range of CMOS image sensors but there is still plenty scope to carry out more. The majority of work published in the field has been carried out using imagers operating in linear integrating mode. Multiple exposure, time to saturation or are such examples. In contrast is the continuous time solution, namely the logarithmic imager. Its inherent ability to image high dynamic range scenes make it at first glance an obvious choice. Its poor sensitivity, increased FPN and slow response at low light levels detract from its compression characteristics.

2.5.1 Multiple exposure

A high dynamic range scene can be reconstructed by reading each pixel at two or more different exposure times. The data gathered from the shorter integration times will hold information about the brighter parts of the scene and the longer integration samples will have detail for the darker parts of the scene. A high dynamic range image is formed by combining the data sets. For each pixel the data is chosen to maximise the signal swing without reaching saturation. The linearity lends itself well to colour processing however some form of compression is required if the data is to be viewed on a conventional display. Acquiring two samples per pixel can be fairly easily achieved for low resolution imagers but becomes less easy as resolution increases. When merging the data from two different exposures, the resulting image can look discontinuous if the exposure times are not well matched to the incident light levels.

A dual sampling scheme which uses a top and bottom column parallel readout was proposed by Yadid-Pecht and Fossum in [37] and reviewed in [38]. The basic architecture is shown in Figure 2.13.

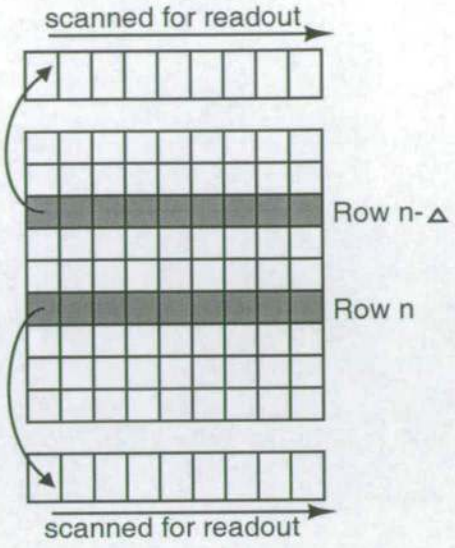


Figure 2.13: *Yadid-Pecht and Fossum's dual sampling scheme.*

Row n is first selected for readout and the pixel's voltages are sampled and held in the lower capacitor bank. Immediately after, row $n - \Delta$ is selected and sampled into the top capacitor bank. The data readout from the lower signal chain is thus the result of the longer exposure period and the data from the top the shorter. Because the sampling time is insignificant compared to the readout time, the frame rate is not reduced. Another advantage of the scheme is its simplicity, allowing the use of a conventional pixel arrangement to optimise fill factor and pixel pitch. A disadvantage is the overhead imposed from the requirement of an off-chip memory. There will be Δ rows of data being readout before a single row has the data from both exposures. The size of memory is thus determined by Δ which also affects the achievable dynamic range. Measurements from the device gave a 64 times increase in dynamic range compared to a single readout. This was achieved using $\Delta = 1$ which may not be optimal for larger resolution devices.

A 1Kx1K resolution imager is presented in [39] [40] and makes two reads per pixel whilst achieving 15fps. The algorithm to reconstruct the image aims to correct for any non-linearity caused by the voltage dependent capacitance of the photodiode. A dynamic range of 92dB is measured by using integration times of 20ms and 640μs respectively. Additional memory is again required to store the two sets of data and to implement the stitching algorithm.

The optimum integration time (from four) and gain (from three) is selected in [41] and stored together with the digitised pixel voltage in a frame memory. The stored information represents a 20 bit linear value which corresponds to a dynamic range of 120dB. Its intended use was in

a driver's assistant system for automotive applications. It was thus useful to have demonstrated operation at elevated temperatures.

An increased frame rate or alternately an increase in the number of read operations can be accomplished by moving the analogue to digital conversion point closer to the pixel. Yang *et al* use a multichannel bit-serial (MCBS) ADC which consists of a 1 bit comparator and latch shared between 4 pixels [42]. The number of samples(k) plus the number of bits per sample(m) combine to give a floating point number of length $m + k$. The slow conversion time allows the use of simple in-pixel circuitry. In subsequent work [43], the authors begin by comparing multiple sampling schemes to a full well capacity adjustment scheme(see Chapter 2.5.4) in terms of the achievable SNR. They conclude that a multiple sampling system can achieve a superior SNR than a well adjustment scheme. In addition the SNR is maximised by limiting the ratio of integration times. Thus it is advantageous to read each pixel a greater number of times. The work also presents design and measurements from a 640x512 imaging array with the pixel level ADC. A dynamic range of 65536:1(96dB) was measured from the sensor which was realised in a 0.35μm process and achieved a 10.5μm pixel pitch with 29% fill factor. Although not mentioned some form of off-chip memory would be required to hold the pixel data for the various exposures.

Later work to include an ADC at the pixel level was done by Kleinfelder *et al* in [20]. The continual reduction in feature sizes allowed the authors to implement a single slope ADC and 8-bit DRAM within a single pixel. A 352x288 array was fabricated in a 0.18μm process. A total of 37 transistors per pixel was translated into a pixel pitch of 9.4μm. Although the ability to increase dynamic range was listed as motivation for the work details on high dynamic range operation were not presented. A disadvantage of the increased pixel complexity was the relatively low fill factor of 15% leading to a low sensitivity of 0.1V/lux.s.

A complete imaging unit with pixel level MCBS ADC is described by Bidermann *et al* in [44]. The system includes an array of 742x554 pixels and 4.9Mb frame buffer. Although multiple sampling achieves a dynamic range greater than 100dB the visualisation of the complete system on-chip clearly shows the overhead of the frame buffer which occupies a significant area of silicon. The total die area is 6.8mmx10.7mm where the pixel pitch is 7μm x 7μm.

A novel approach was presented in [45] and developed in [46] where 2 samples are taken from each pixel with only a single exposure period. The work uses a photogate structure in which

the floating diffusion is used as a light sensitive element in addition to the larger well beneath the photogate. The floating diffusion is used to sense higher illumination levels then readout independently to the signal beneath the photogate. Thus two signals with different sensitivities can be extracted from the same pixel instantaneously. The latter work achieved a dynamic range of 108dB through the use of fusion and compression algorithms that were implemented in an FPGA system requiring 50,000 gates and 18Kbits of memory. The work also proposed Fraunhofer diffraction as an accurate way to measure dynamic range.

In conclusion, multiple sampling schemes can effectively increase the dynamic range of a CMOS image sensor by combining data from the same pixel captured under differing exposures. Multiple sampling of the imaging array requires a fast readout architecture and this has seen conversion to digital signals occurring at the pixel level. The major disadvantage of multiple exposure schemes is the overhead of extra memory.

2.5.2 Locally adaptive exposure

Ginosar and Gnusin implement a simple method of varying the exposure to a pixel. Two integration times are possible, one long and one short. A pixel's exposure time is set dependent on the previous frames data. The older 2μm technology is partly responsible for the large pixel pitch of 60μm but each pixel still requires 13 transistors [47].

2.5.3 Time to saturation

Also known as time-stamping, this method of extending dynamic range lets each pixel integrate freely until it reaches some predetermined level (normally the onset of saturation) at which point the time interval is recorded. There are two approaches to such a system. A pixel will either include the necessary circuitry to store the time stamp or will just signal to another part of the sensor that it has reached the predetermined level. The latter, although achieving a relatively small pixel pitch can suffer from bandwidth problems if many pixels signal to the time-stamping circuitry at the same time. Extra memory may also be required to achieve the correct pixel readout order. In both schemes, as each pixel locally adapts to the illumination the SNR is maximised.

Lulé *et al* have reported an auto adaptive pixel which uses time-stamping combined with a TFA process to create an imager capable of 120dB of dynamic range [48][35]. A comparator,

analogue memory (capacitors) and readout buffers are included in every pixel in the 368x256 array. A block diagram of the pixel is shown in Figure 2.14.

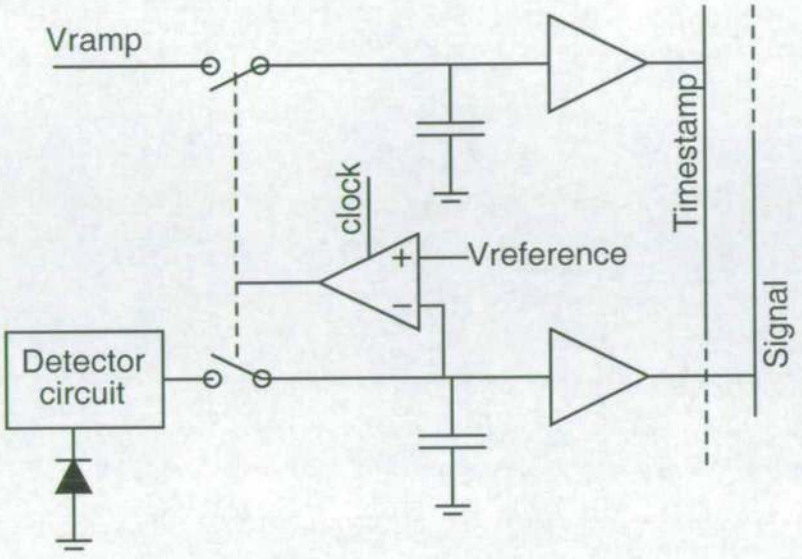


Figure 2.14: *In-pixel time-stamping circuitry.*

The circuit uses a clocked comparator and with each clock cycle the light detector's voltage is compared to a reference level. The pixel size is 40μm x 38μm and incorporates 17 transistors in a 0.7μm technology. The power consumption in such a device could be relatively high since the circuitry in every pixel is always enabled. The power consumption was not reported in the work.

A similar architecture was proposed by Stoppa *et al* in [49][50] which achieved 138dB of dynamic range. The photodiode voltage level is connected to a comparator which toggles when saturation is reached and stores the value of two ramps on two capacitors. The first ramp monotonically decreases whilst the second ramps up and down between its limits N times. This achieves coarse and fine resolution respectively. If the onset of saturation is not reached the photodiode voltage is read as normal. Three readout paths are provided from each pixel which occupies an area of 24.65μm x 24.65μm in a 0.35μm process. In contrast to Lulé, the photo-receptor was integrated horizontally in the pixel thus a fill factor of only 11% was possible. Power dissipation was identified as a key characteristic and steps taken to minimise it. For the 128x64 pixel array the power consumption was 14mW.

Performing the time-stamping outwith the pixel array can also be described as Address Event Representation (AER). Such a sensor is described in [51] where each pixel outputs a 1 bit

request signal to the output bus. When access is granted the address of the pixel is output together with a time stamp. A frame buffer is required to compare each time stamp index with the previous event for each pixel. The sensor reported had a resolution of 80x60 and achieved an array dynamic range of 120dB. For a VGA format using the same architecture a frame buffer of 15Megabytes would be required which imposes a significant overhead on the system.

Hamamoto and Aizawa sample each row of pixels at a fixed frequency in [52][53]. When a pixel saturates a flag is set in preparation for the following read. The device was primarily designed to detect motion and not optimised for dynamic range applications. The minimum sampling period of a pixel was given as 68μs for the 32x32 prototype array but this would rise to around 1ms for a sensor of dimensions 512x512. This sampling period would be too large for high illumination conditions.

A system to observe the interval between successive pixel resets was first proposed by Yang in [54]. The pixel is shown in Figure 2.15 and consists of a photodiode connected to a chain of inverters, the output of which controls the reset of the photodiode. Thus, when the illumination generates sufficient charge for the photodiode to cross the switching point of the first inverter, a pulse is output. This early work demonstrated a 32x32 array in 2μm technology.

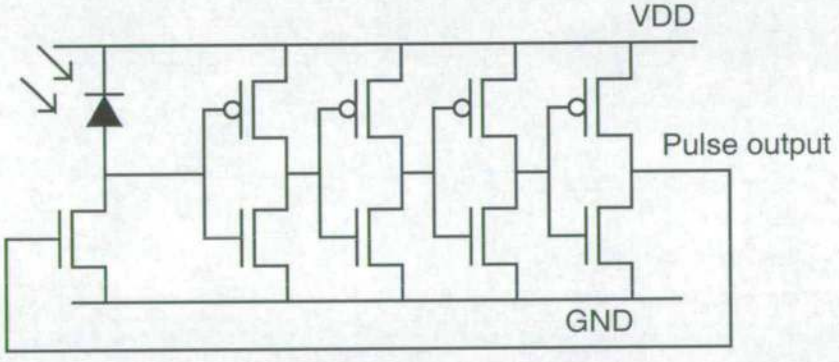


Figure 2.15: *Pixel circuit of Yang.*

A slightly larger array with a pulse generator per pixel was presented by McIlrath in [55] to achieve a similar output to Yang. Each pixel contains a sigma delta converter that resets the photodiode if the voltage on the integration node falls below a threshold level. The pixel thus outputs a logic '1' when the pixel is reset. The pixel is sampled at a high frequency and each read operation resets the output to logic zero. The photo-signal can be determined by the frequency of ones at the output. A dynamic range of 103dB was achieved with a range of output frequencies from 1Hz to 156kHz. Although a relatively small array of 64x64 was tested,

the author believes a 1Kx1K array is achievable with a power consumption of 50mW and the same dynamic range. A measurement under flat illumination was required to create a correction matrix for FPN reduction.

2.5.4 Well adjustment

The original technique was described as a means of increasing the dynamic range of CCD imagers [56] but has been adapted to use in a CMOS system. During the integration time in a linear imager photo-generated charge accumulates in the diffusion area be it a photogate or photodiode type receptor. The maximum charge handling capability of the diffusion directly effects the dynamic range. The method of well adjustment alters the height of a potential barrier such to adjust the well size of the charge sense region. A MOSFET can provide the potential barrier by adjustment of its gate voltage. An initial *high* gate voltage will reset the sensing diffusion then the well size is increased by reducing the gate voltage. The gate voltage is decreased non-linearly, more slowly at first. At any point during the integration period, if the well fills up, further generated charge is able to overcome the barrier potential of the gate and flow to the drain terminal of the MOSFET where it is absorbed. A 256x256 array with a stepped reset voltage was presented by Decker *et al* in [57][58]. The pixel circuit is shown in Figure 2.16.

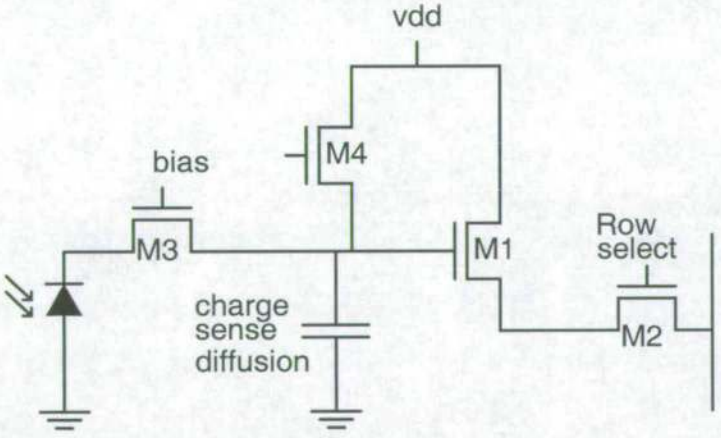


Figure 2.16: *Pixel circuit of Decker* et al.

The pixel incorporates four transistors but the scheme could also be implemented with three by removing device *M3* which is used to increase sensitivity by separating the photodiode from the sensing diffusion. The gate of reset device *M4* is stepped down in voltage by using a shift register cycling through eight analogue levels. Figure 2.17 shows a graph of the accumulated

charge versus time for two different light levels when only two voltage steps are used [59].

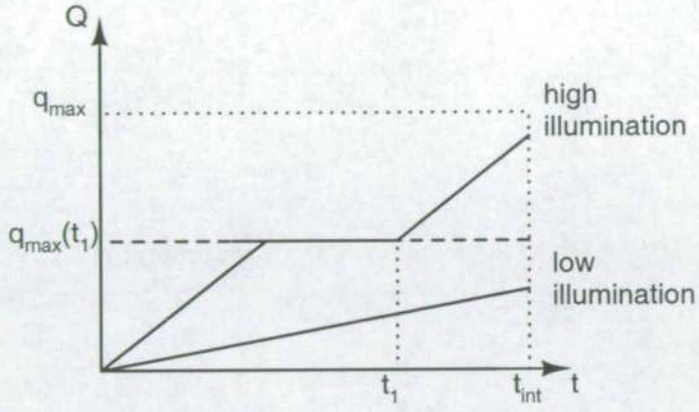


Figure 2.17: *Well adjustment graph.*

The low illumination case of Figure 2.17 never generates sufficient charge to fill the well so behaves as a conventional linear integrating sensor. The high illumination case causes the well to overflow when the potential barrier is relatively low. At time t_1 the barrier is increased and the well begins to fill again. At the end of the integration time the well is not full for either light level. The study in [57] reported a dynamic range of 96dB which is 26dB greater than the conventional linear mode. A similar range is reported in [60] where the well adjustment was implemented in a sensor with a resolution of 1280x1024 with a pixel pitch of 6.7μm.

If the illumination is sufficient for the sense diffusion to fill and cause overflow the response becomes non-linear and this is how the compression is achieved. It should be noted that correlated double sampling cannot be used to remove kTC noise for high illumination levels. Although straightforward to implement, well adjustment causes a reduction in SNR. If the illumination in a pixel is sufficient to cause overflow the SNR will dip [59]. The reduction in SNR (relative to the peak in a conventional integrating imager) is the same as the dynamic range gained.

Ho *et al* [61] report a 1.3M pixel sensor that performs a double reset that is similar to limiting the well capacity. The first reset is performed by raising the gate voltage of the reset device to a voltage, VR1. After the first set exposure period a second reset is applied by raising the gate voltage of the reset device to VR2. VR2 is less than VR1 such that only photodiode voltages below a certain level are reset. The second integration is much shorter than the first. The work achieved a pixel pitch of 5μm with a fill factor of 49% in a 0.35μm process but the full dynamic range was not reported.

The adjustment of the well capacity is achieved in a slightly different manner by Muramatsu

et al in [62] and [63]. Their work uses a 3T pixel with the addition of an analogue memory and access switch. The pixel is shown in Figure 2.18. The first integration period begins with the photodiode and memory capacitor precharged but the access switch OFF. At the end of the first integration period the memory capacitor is briefly shorted to the photodiode causing any collected charge to divide equally between the photodiode and the extra capacitor (Cm=$C_{photodiode}$). The second integration period then begins with the memory access switch OFF. A conventional double sampling readout is performed at the end of integration. Muramatsu *et al* achieved a pixel pitch of 9.3μm and 24% fill factor in a 0.35μm process and thought the Dynamic Range, which is dependent on the ratio of the two integration times, was extendable to 97dB. a downside to this approach is the reduction in low light performance caused by the alteration of the pixel capacitance.

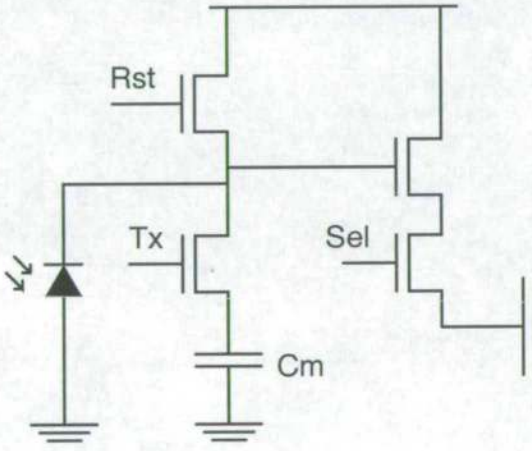


Figure 2.18: *Muramatsu* et al *pixel arrangement.*

2.5.5 Logarithmic sensors

As was briefly mentioned earlier in this chapter, a logarithmic sensor has the inherent ability to image scenes of a high dynamic range. In addition, the simple 3 transistor pixel lends itself well to small pixel sizes with a high fill factor [64]. The absence of a reset signal permits true random access as each pixel's output voltage is continuously available for reading [65] [66] [67]. These characteristics make a logarithmic imager appear as an ideal choice for many high dynamic range applications [24] [68].

Unfortunately, there are many drawbacks with the logarithmic arrangement. Colour reconstruction in integrating sensors rely on the linear response of the data to render an image into standard colour space. The logarithmic compression means colour processing steps cannot be

applied. There has been little work done on the colour rendition in logarithmic imagers. Joseph and Collins begin to address the issue by applying a model to logarithmic data from a real sensor in [69]. The work achieved rendition comparable to a conventional digital camera if the illumination was not too low.

Although the pixels output is available continuously it may not be an accurate reflection of the incident illumination due to lag. At low light levels the generated photo-current can be very small (especially as pixel sizes shrink) thus the time taken to charge/discharge the pixel capacitance can be large. Huppertz *et al* [70] have addressed this limitation by creating a simple inverting amplifier connected between the photodiode and the gate of the load device. The feedback provided by the load device maintains an almost constant voltage across the photodiode thus exhibits a high bandwidth under low illumination. The spatial process variation from multiple devices in the pixel was given as the reason for a further increase in FPN.

Schemes have been proposed to reduce the effect of FPN and can be considered in two categories: off-chip and on-chip. The off-chip methods [65] [66] will include a frame memory in which to store the offsets that have been programmed. Changes over time or temperature variation could reduce the effectiveness of the offsets stored but a small pixel size is maintained. On-chip calibration removes the overhead of a frame memory and involves bringing the pixel into a reference state every time it is read. Sampling the illumination dependent signal and the reference state allows conventional differencing to reduce FPN. If a constant current can be made to flow through the load device and matched across the array, the offsets of each pixel can be learnt. (It has been reported that FPN is not simply the result of offset variation [71]. Gain and illumination dependent errors can also cause FPN but this will be discussed in future sections as to date no logarithmic devices employ on-chip calibration other than offset cancellation.) The requirement to stimulate the load device with a calibration current in addition to the photocurrent can cause problems due to settling times.

Feedback is used to improve the transient response of a logarithmic arrangement in [72]. The source of the load device is held constant and the feedback formed by an amplifier situated in the column and switchable between rows. A set of column current sources are used to generate the reference point but since the photodiode cannot be isolated, high incident illumination could corrupt the calibration. The work claims FPN can be reduced to 0.02% of the full signal swing. However, this was generated from a simulation and since their algorithm only performs a simple differencing operation it is thought this result is unlikely to be achievable in reality.

Kavadias *et al* [73] analyse calibration by pulling a high reference current through the load device but implement a slightly different scheme. The pixel is switched onto a discharged column capacitor for a very short time then sampled just after the column is disconnected, at which point the pixel voltage is said to be independent from the illumination. This method means the photodiode does not need to be isolated from the load device thus the pixel achieves a higher fill factor. However, the remaining FPN is quite high at 2.5% of the total voltage swing. The dynamic range of six decades is compressed into a voltage range of 300mV thus the FPN is 12% when expressed per decade of illumination.

FPN can be further reduced if the calibration current is close to the photocurrent that flows (This is also shown in Chapter 3). Loose *et al* [74] report FPN with an RMS of 3.8% per decade of light intensity when illuminated at $1W/m^2$. The work considers a higher point calibration unnecessary due to low slope variations across the array. The architecture employed uses an analog memory (capacitor) in each pixel to store the offset. The pixel is shown in Figure 2.19 and displays two load devices *M1* and *M2* which conduct the photocurrent. Increasing the number of load devices increases the voltage swing for a given illumination range [75]. The solid line in Figure 2.19 represents circuits located in the pixel whereas the blocks drawn with a dashed line are located in the column.

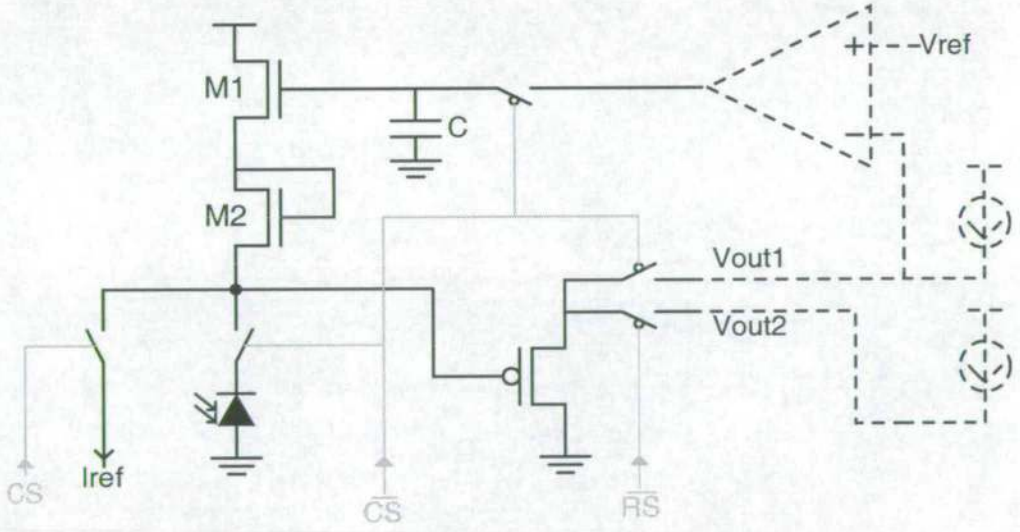


Figure 2.19: *Loose's pixel arrangement.*

During the calibration cycle the photodiode is isolated from the load devices and a reference current is connected in its place. The calibration voltage appears at *Vout1* via the PMOS source follower, and is compared to a reference voltage. The resulting correction voltage is applied

to the gate of *M1*. When the photodiode is re-connected (amplifier and reference current disconnected)the voltage that appears at *Vout2* has the correction voltage applied. The pixel pitch is 24μm in a 0.6μm process but significant space savings will not be possible as each pixel includes N-type and P-type devices.

Alternate approaches to reducing the FPN have been reported. An inverted logarithmic current readout architecture which relies on local matching in the pixel as opposed to global matching of devices across the array is presented in [76]. The logarithmically compressed gate-source voltage of the load device controls the gate-source voltage of a current source. The current is converted to a voltage in the column readout. Although the raw logarithmic image shows improved FPN to conventional arrangements it is still large in comparison to calibrated sensors.

A PMOS device with a floating gate is proposed in [77] but the steps required to trim all the devices in a large array are not trivial. There are also no measured results to show if such a scheme would successfully reduce FPN.

In addition to stacking devices to increase signal swing, variations in the photo-receptor have been proposed. Lai *et al* [78] use a lateral PNP device in place of a photodiode to give up to 4 times increased signal. Absolute FPN also increases but when calculated as a percentage of the signal swing it is shown to have reduced. Calibration is still required to reduce the high levels of FPN.

The work of this thesis focuses on a system that combines linear data with logarithmic data to create a high dynamic range image. To the author's knowledge there has been little work done in this area. Tu *et al* [79] published work that stated a standard 3 transistor pixel array could be operated in linear or logarithmic mode by adjusting the reset voltage. There was no mention of creating an image consisting of linear and logarithmic data and the architecture would not permit pixels of the same line to operate in different modes within the same frame. Fox *et al* [9][80] have detailed a simple arrangement that allows a pixel to operate in logarithmic mode if the incident illumination is sufficient. Figure 2.20 shows the pixel arrangement.

The *pix* node can be precharged high to *Vbias* by pulsing the reset line. *Vbias* is set to a level greater than that required for sub-threshold conduction through *Mlog*. Generated photons will cause the voltage on *pix* to reduce and if the illumination is sufficient *Mlog* will begin to conduct. A steady state condition will be reached where *Mlog* will supply the photocurrent resulting in a logarithmic voltage variation between *vdd* and *pix*. To reduce FPN it would be

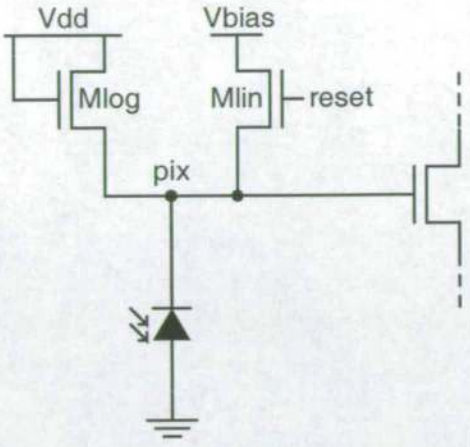


Figure 2.20: *Lin-Log pixel arrangement.*

advantageous to know which mode the pixel was operating. For linear mode simple double sampling could be used but for logarithmic mode a more complex reference generation would be required. Since it is not possible to process the data independently it will be difficult to reduce FPN across the array.

A similar arrangement to the pixel of Figure 2.20 is detailed in [81]. The only difference is the connection of *vbias* and *vdd* and the generation of the reset voltage.

2.6 Conclusion

This chapter has introduced the main blocks of a CMOS image sensor and some of the operational modes possible. Central to every image sensor is a photo-sensitive element which converts the incident illumination into a signal. Normally some form of charge collection is performed at each pixel before conversion to a voltage when readout is selected. The most common pixel structures and their operation were presented. Although linear structures achieve the best SNR and low light performance their full well capacity limits the dynamic range achievable in a single integration period. In contrast to this was the logarithmic pixel which directly converts the photocurrent to a voltage. The compression permits a wide range of illuminances to be captured by sacrificing the SNR. FPN and lag are two other drawbacks.

The second part of the chapter described some techniques to extend the dynamic range in a CMOS sensor. Schemes such as multiple capture and time stamping preserve the linearity of the signals but usually have an added overhead. In the case of the former, additional memory

is usually required to hold intermediate values from the different integration times whereas the latter can suffer from increased pixel pitch or irregular readout format. Compression of the photo-signal permits a wider range of illuminances to be captured. Adjusting the well capacity of the sensing element is one such scheme whereas a logarithmic pixel is another. Due to the simplicity of a conventional logarithmic pixel it is often associated with extended dynamic range applications. However the severity of the drawbacks mean it is not more widely adopted. Efforts to address issues such as FPN can greatly improve image quality but operation, especially at low illumination, is much reduced compared to a linear device.

Having introduced the different operational modes possible it is reasonable to ask if dynamic range could be extended by a combination of different schemes. For example using a linear response to image low illumination and a non-linear technique at increased illumination. The remainder of this thesis discusses combining linear and logarithmic data in a single image.

Chapter 3
Logarithmic calibration and Linear-Logarithmic Fusion

This chapter presents experimental results from the calibration of a CMOS sensor operating in logarithmic mode. It then details how linear and logarithmic images of the same scene can be combined to render a high dynamic range image.

The investigation used a test device fabricated by STMicroelectronics. The CMOS image sensor was VGA resolution with standard 3 transistor active pixels (see Figure 2.7). The array was addressed by column decoders and used a column parallel architecture with an ADC per column. Two rows of on-chip SRAM banks were used to store the ADC codes prior to readout. For flexibility, the sensor was controlled by an FPGA situated on the same PCB as the sensor. The sensor was realised in a 0.35μm process and the pixel pitch was 5.6μm.

The sensor was operated in linear integrating mode by pulsing the reset line to the pixel or alternatively in logarithmic mode by holding the reset line at a voltage near *Vrt*.

3.1 Logarithmic mode

Recalling Equation 2.19 from Chapter 2, the drain current in weak-inversion (neglecting the body effect) is given by:

$$I_{DS} = \frac{W}{L} I_{D0} e^{\frac{V_{GS}}{nV_t}} \left(1 - e^{-(\frac{V_{DS}}{V_t})}\right) \tag{3.1}$$

Again assuming $V_{DS} >> V_t$, Equation 3.1 can be written as

$$I_{DS} = \frac{W}{L} I_{D0} e^{\frac{V_{GS}}{nV_t}} \tag{3.2}$$

The case where the source to bulk voltage (V_{SB}) is not equal to zero will be examined in Chapter 4. The gate-source voltage can be expressed as

$$V_{GS} = nV_t \ln\left(\frac{I_{DS}}{\frac{W}{L}I_{D0}}\right) \tag{3.3}$$

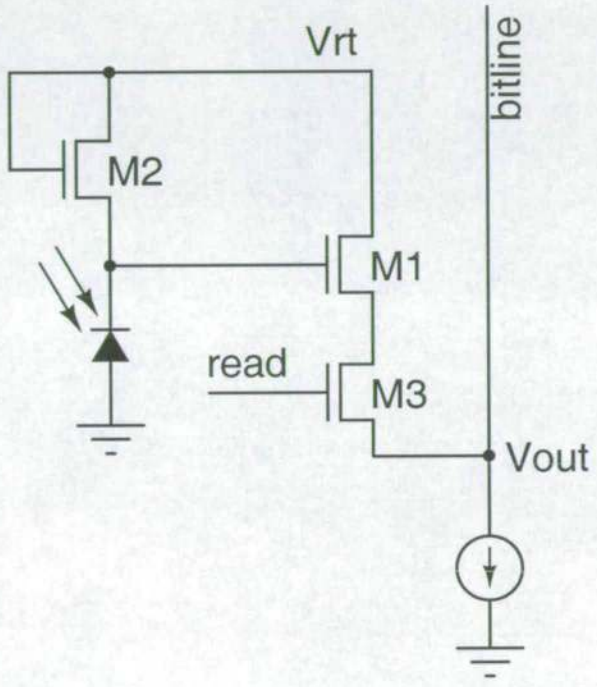


Figure 3.1: *Logarithmic pixel schematic.*

The voltage readout from the circuit of Figure 3.1 is written below. Equation 3.5 assumes device M1 is operating in the saturation region where $I_{DS} = \beta\frac{W}{L}(V_{GS} - V_{th})^2$.

$$V_{out} = Vrt - V_{GS(M2)} - V_{GS(M1)} \tag{3.4}$$

$$= Vrt - nV_t \ln\left(\frac{I_{ph}}{\frac{W}{L}_{(M2)}I_{D0}}\right) - \sqrt{\frac{2I_{DS(M1)}}{\beta\frac{W}{L}_{(M1)}}} + V_{th(M1)} \tag{3.5}$$

where I_{ph} is the photo-generated current flowing through device M2. The notation of $_{(M1)}$ or $_{(M2)}$ signifies to which device each parameter belongs. Considering Equation 3.5 in terms of FPN it is evident that there are many parameters that are liable to variation across a pixel array. Due to the small dimension devices used in a pixel the FPN is expected to be considerable. The

measurement and correction of such FPN is examined in the following sections of this chapter.

3.2 Sensitivity

Having shown in the previous section (and in Chapter 2) that the gate-source voltage of a MOSFET varies as the logarithm of the drain-source current, for low currents, the test sensor was setup to confirm this. In logarithmic mode the reset line to all the pixels in the array was held at approximately 2.7V. This was also the *Vrt* voltage applied to the pixels. The absolute level of the reset line is not important as it simply alters the DC offset of the data. However, it should not be raised above *Vrt* as this could cause the load device to operate in strong inversion. The output voltage was measured for varying levels of incident illumination so that logarithmic operation could be verified and the sensitivity calculated. The sensitivity was also required to enable the FPN to be compared with other published work. As will be shown shortly, FPN in the logarithmic mode is often quoted as a percentage of the sensitivity.

A halogen lamp, neutral density filters, and integrating sphere were used to uniformly illuminate the sensor with varying intensities. The setup is shown in Figure 3.2. As the light meter was not positioned at the same location as the sensor the absolute illuminosity may not have been accurate. If absolute light levels were important then readings would also have to be taken with the light meter positioned at both ports of the integrating sphere and a correction factor found. Since the positioning of the light meter does not affect the ratio of intensities, it was not necessary to find a correction factor.

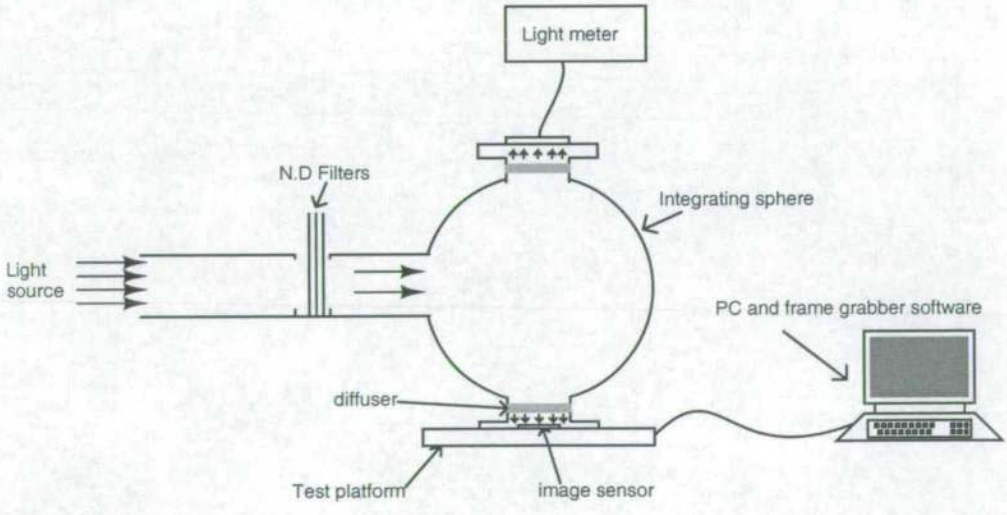


Figure 3.2: *Setup used to measure the logarithmic sensitivity to illumination.*

To focus on the time invariant noise in the image a number of consecutive frames were averaged to reduce the temporal noise. At each illumination level 20 consecutive frames were averaged to reduce the temporal noise by a factor of $\sqrt{20}$. The choice of 20 was a trade off between the reduction of temporal noise and the processing time required. The averaged frame was next processed in software to calculate the mean pixel value and standard deviation of pixel values across the array. The results are shown in Table 3.1 and the mean array value is plotted against the illumination in Figure 3.3.

Illumination (mW/m^2)	Mean (codes)	St.dev codes
885	2192	150.3
726	2179	150.5
496	2158	150.9
200	2098	151.5
3.6	1793	152.4
0.8	1691	152.5

Table 3.1: *Sensitivity data for logarithmic mode(gain=1.45).*

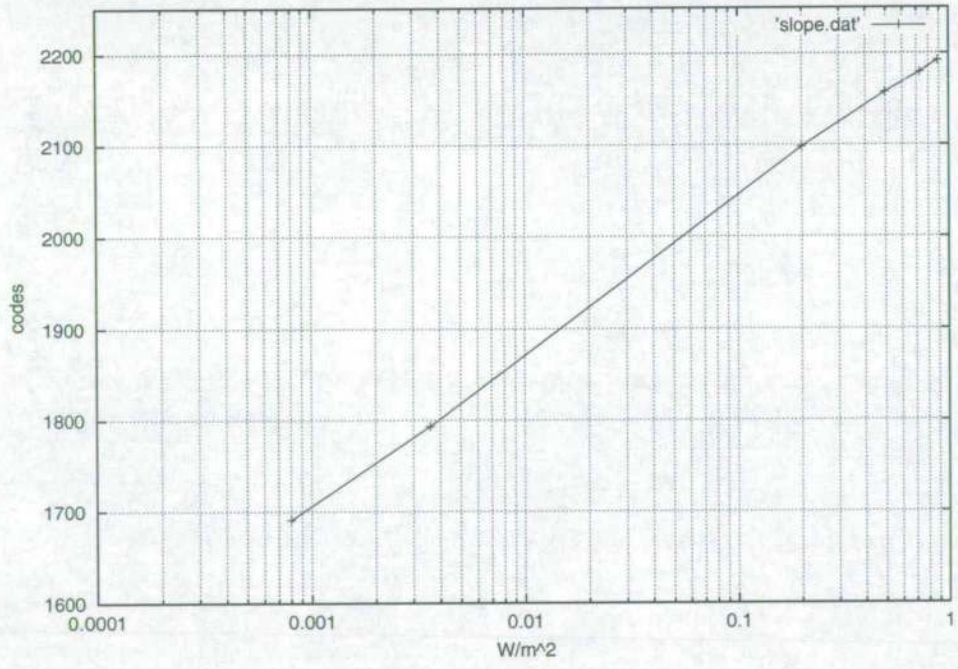


Figure 3.3: *Plot of sensitivity for logarithmic mode (3T device in 0.35μm).*

Using the data from Table 3.1 the sensitivity of the logarithmic mode can be calculated. This is the change in voltage per decade of light intensity.

The gain of 1.45 due to the ADC ramp range was first normalised.

$$\frac{2192.14 - 1690.5}{1.45} = \frac{501.64}{1.45} = 346\text{codes} \tag{3.6}$$

The data spans 3.05 decades of illumination and each code is equivalent to 0.488mV. Thus the sensitivity is given by

$$Sensitivity_{codes} = \frac{346}{3.05} = 113\text{codes/decade} \tag{3.7}$$

$$Sensitivity_{voltage} = 0.488\text{x}Sensitivity_{codes} = 55\text{mV/decade} \tag{3.8}$$

This compares favourably with the output voltage swing reported in [73] and [66] which measured 50mV/decade and 35mV/decade respectively. Loose's work [74] allowed a programmable gain giving a voltage swing between 130mV and 720mV. At the unity gain setting, the high swing of 130mV/decade is achieved by connecting two NMOS devices is series. This has the effect of almost doubling the voltage swing [75].

If the source follower in the pixel is assumed to have a gain of 0.8 (from simulation) the sensitivity at the photodiode is

$$Sensitivity_{Vphdiode} = \frac{1}{0.8}55 = 68.75mV \tag{3.9}$$

The raw FPN given in Table 3.1 can be expressed as a voltage then related to the sensitivity as follows:

$$FPN_{voltage} = \frac{151}{1.45}\text{x}0.488 = 50.8\text{mV} \tag{3.10}$$

$$FPN_{\%decade} = \frac{FPN_{voltage}}{Sensitivity_{voltage}} = \frac{50.8}{55} = 92\% \tag{3.11}$$

Thus the variation is large and amounts to over 90% of the voltage swing per decade of illumination. Such FPN renders an image un-usable as a sample image in Figure 3.4 demonstrates.

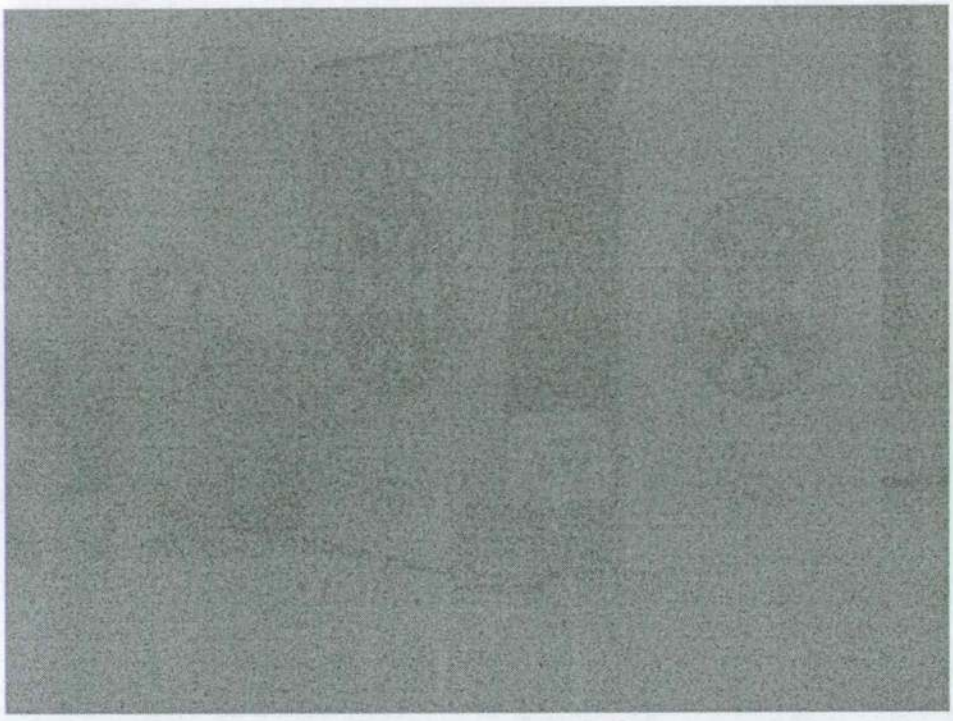


Figure 3.4: *Image captured in logarithmic mode (no calibration performed).*

3.3 Logarithmic Calibration

Section 2.5.5 discussed prior art in calibrating a logarithmic imager and focused on offset cancellation by creating a matched reference state for each pixel. This Section investigates offset calibration then goes on to look at two-parameter calibration. It uses actual data from the 3T test device and implements all the algorithms in software. All reference points for the logarithmic calibration are obtained by uniformly illuminating the device at varying illumination levels as the standard 3T architecture had no means of providing a reference state.

The calibration algorithms used are taken from recently published work by Dileepan Joseph and Steve Collins [71]. Their work, although effective, is not directly applicable to a real-time sensor, due to the number of reference frames (M=24) used in calibration. The remainder of this subsection details the algorithms and shows their performance when a minimum number of reference frames are used. Section 3.3.3 then discusses how to implement such algorithms in a real-time image sensor. Prior to presenting the algorithms the notation is explained.

The response of a j^{th} pixel is modelled by $\hat{y}_{ij}$ and is given by Equation 3.12 in which a, b and c can vary spatially to an illuminance x_i or remain constant.

$$\hat{y}_{ij} = a_j + b_j \ln(c_j + x_i) \tag{3.12}$$

Three cases are examined in [71]:

- a_j varies spatially and b_j and c_j are constants. This is known as offset calibration.
- a_j and b_j vary spatially and c_j is a constant. This is known as offset and gain calibration.
- a_j, b_j and c_j all vary spatially. This is known as offset, gain and bias calibration.

Offset calibration and offset and gain calibration are detailed in the following section. The third case results in a nonlinear solution. Iteration can be used to find the minimum error fit but realisation of such an algorithm on-chip was thought to be too much of an overhead. For the other two cases considered, the Mean Squared Error (MSE) does not have a unique global minimum. The correction of a pixel aims to move its response toward the average response of the pixel array. As stated, the performance of the calibration algorithms were assesed by calibrating uniformly illuminated frames. This permitted the remaining FPN to be calculated in a repeatable fashion and quantified which would not have been possible if actual images were used.

3.3.1 Offset Calibration

The offset of a pixel is proportional to the difference between the pixel's average response and the average response of all the pixels.

$$\hat{y}_{ij} = a_j + b \ln(c + x_i) \tag{3.13}$$

The parameters may be found by minimising the MSE between the actual response y_{ij} and the model, $\hat{y}_{ij}$ to M uniform but different illuminances. N denotes the number of pixels.

$$MSE = \frac{1}{MN} \sum_{i=1}^{M} \sum_{j=1}^{N} (y_{ij} - \hat{y}_{ij})^2 \tag{3.14}$$

But, as mentioned, there is no global minimum, therefore the average response is written and

then used to express the model response.

Average of the pixel array at intensity i

$$\bar{y}_i = \frac{1}{N}\sum_{j=1}^{N} y_{ij} \tag{3.15}$$

$$= \bar{a} + b\log(c + x_i) \tag{3.16}$$

where

$$\bar{a} = \frac{1}{N}\sum_{j=1}^{N} a_j \tag{3.17}$$

Thus the model response is expressed as:

$$\hat{y}_{ij} = a'_j + \bar{y}_i \tag{3.18}$$

where

$$a'_j = a_j - \bar{a} \tag{3.19}$$

Differentiating the MSE with respect to the variable a'_j and setting the result to zero finds the minimum and can be solved for a'_j.

$$\frac{\delta MSE}{\delta a'_j} = \frac{-2}{MN}\sum_{i=1}^{M}(y_{ij} - a'_j - \bar{y}_i) \tag{3.20}$$

giving

$$a'_j = \bar{y}_j - \bar{y} \tag{3.21}$$

with parameters:

- Average per pixel over the intensity range

$$\bar{y}_j = \frac{1}{M}\sum_{i=1}^{M} y_{ij} \tag{3.22}$$

- Average over the intensity range of the pixel array averages

$$\bar{y} = \frac{1}{M}\sum_{i=1}^{M}\bar{y}_i \tag{3.23}$$

Thus, correcting FPN by offset subtraction can be performed on an image y_j as in Equation 3.24

$$y'_j = y_j - a'_j \tag{3.24}$$

This algorithm lends itself to calibration with any number of reference frames(M). Using only two frames with the above algorithm is identical to taking the difference on a pixel by pixel basis of the two frames. This is how a real-time sensor with on-chip offset calibration would function.

Figure 3.5 shows a slightly modified plot of pixel values against the illumination level. Three illumination levels i1, i2 and i3 are shown. Each level creates a corresponding array average ($\bar{y}_i1$, $\bar{y}_i2$, $\bar{y}_i3$) but there will be a spread of individual pixel values around this average. The normal distribution curves aim to show that such a spread exists. Offset correction assumes that the difference between a single pixel value and the array average remains unchanged at different illumination levels.

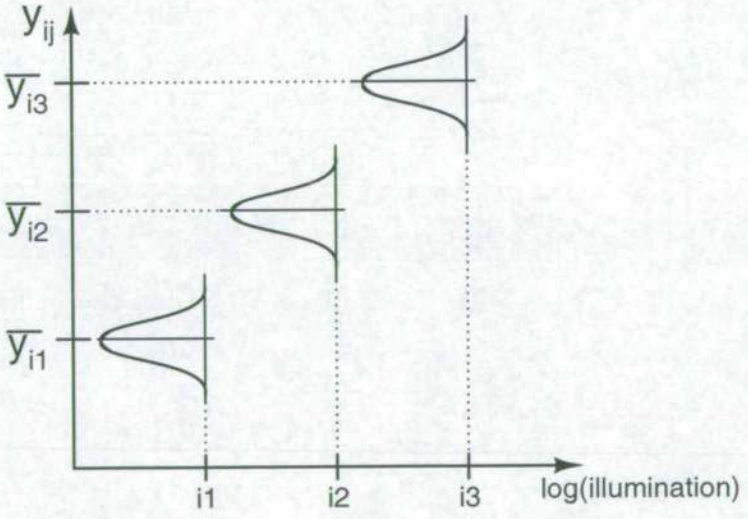


Figure 3.5: *Distribution of pixel values for three different illumination levels.*

Recalling Equation 2.21 and 2.22 from Section 2, if an incident illumination causes a current

of I_{ph} to flow, the voltage after the source follower in Figure 3.1 will be

$$\begin{aligned} V_{photo} &= V_{pix} - V_{GS(M1)} && (3.25)\\ &= Vrt - V_{GS(M2)} - V_{GS(M1)} && (3.26)\\ &= Vrt - nV_t \ln\left[\frac{L}{W}_{(M2)}\frac{I_{ph}}{I_{D1}}\right] + V_{th(M2)} \\ &\quad - \sqrt{\frac{2I_{DS(M1)}}{\beta_{(M1)}\frac{W}{L}(M1)}} + V_{th(M1)} && (3.27) \end{aligned}$$

Similarly if *M2* is now stimulated with a reference current I_{ref}, the voltage after the source follower becomes

$$\begin{aligned} V_{ref} &= Vrt - nV_t \ln\left[\frac{L}{W}(M2)\frac{I_{ref}}{I_{D1}}\right] + V_{th(M2)} \\ &\quad - \sqrt{\frac{2I_{DS(M1)}}{\beta_{(M1)}\frac{W}{L}(M1)}} + V_{th(M1)} && (3.28) \end{aligned}$$

The difference between V_{photo} and V_{ref} is given by

$$\begin{aligned} V_{photo} - V_{ref} &= nV_t \ln\left[\frac{L}{W}(M2)\frac{I_{ref}}{I_{D1}}\right] \\ &\quad -nV_t \ln\left[\frac{L}{W}(M2)\frac{I_{ph}}{I_{D1}}\right] && (3.29)\\ &= nV_t \ln\left[\frac{I_{ref}}{I_{ph}}\right] && (3.30) \end{aligned}$$

Equation 3.30 shows that the difference between the two signal voltages is free from mismatch caused by W, L or I_{D0}. However, a well matched reference current and sub-threshold slope factor are required for this calibration to be effective. In addition, there should be no mismatch in the photodiode response i.e. the same I_{ph} should flow in each pixel if the incident illumination is uniform across the array.

The following graphs plot the remaining FPN (Standard deviation as % of a decade) against the illumination level after offset cancellation. The FPN was calculated after the subtraction of two frames captured under uniform illumination. The illumination level of one of the frames was then altered and the process repeated. The green line shows the illumination level of the reference frame used in each calculation and the red trace plots the remaining FPN at the

different illumination levels. Figure 3.6 shows the condition when the reference frame is at a higher illumination level than the other frames. In contrast Figure 3.7 shows the condition when the reference frame is at a lower illumination level than the others.

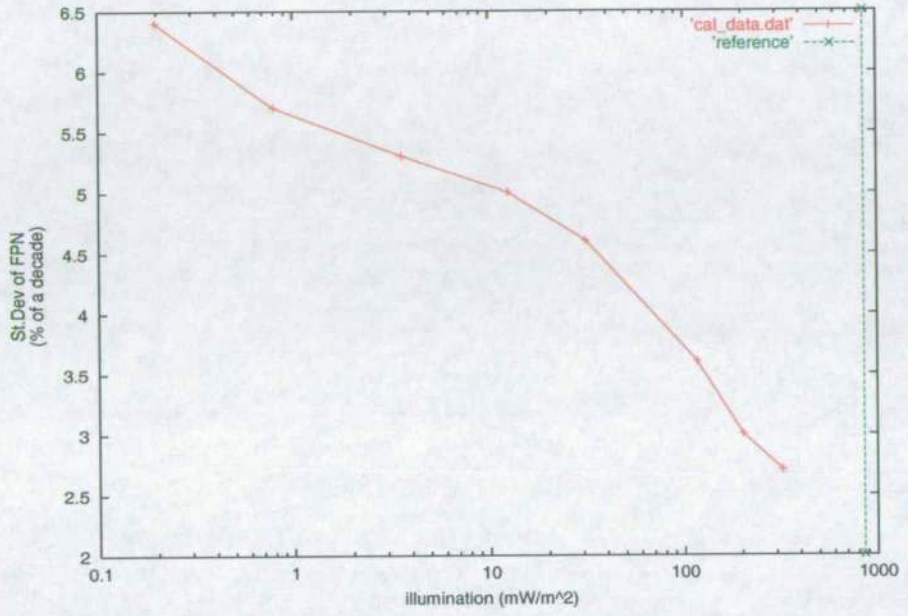


Figure 3.6: *Offset calibration with single reference frame at 873mW/m^2.*

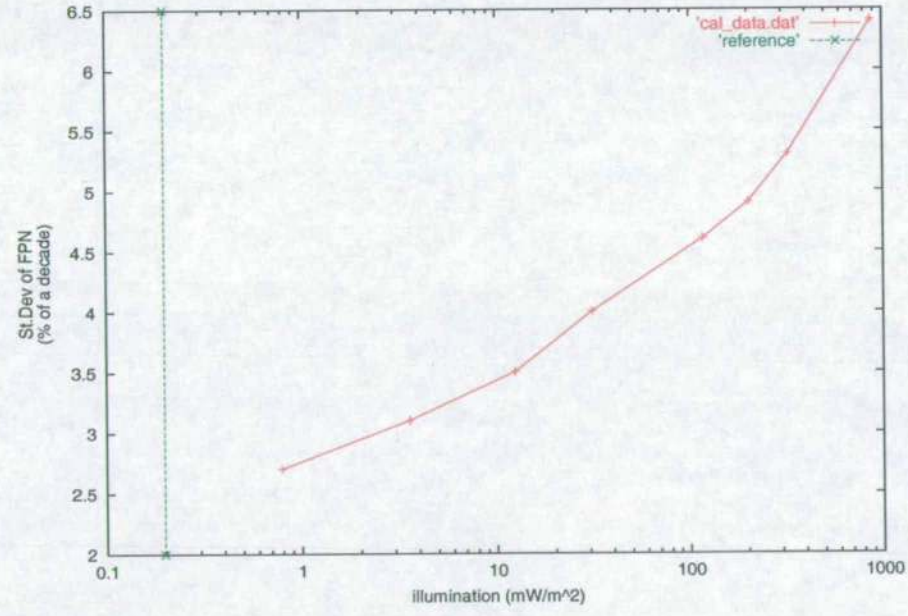


Figure 3.7: *Offset calibration with single reference frame at 0.2mW/m^2.*

The first thing to notice is that in both cases the FPN has been greatly reduced when compared to the raw image. The variation amounting to 92% of a decade before calibration has fallen to somewhere between 2% and 6%. Secondly, the FPN increases as the distance between the reference frame and the frame to be corrected increases. This result is independent to the positioning of the reference frame.

The results suggest that a fairly low remaining FPN is achievable if the reference frame is close to the frame to be corrected. However, in a real working sensor, the scene corrected will not be flat and uniformly illuminated and could have a large dynamic range. It is therefore not possible to choose a reference point close to the value of all pixels. Consequently some pixels get calibrated effectively and others not so.

If offset calibration were to be used in a purely logarithmic sensor the optimum reference point would be at the centre of the dynamic range. For example if the sensor operated over six decades of illumination the reference/calibration point would be a maximum of 3 decades from the actual illumination. From the offset calibration results given above this would result in a worst case FPN around 5.5%/decade.

3.3.2 Offset and Gain Calibration

The results from the simple offset calibration have shown that the FPN is dependent on the proximity of the reference frame to the actual illumination level. This suggest that there is a gain error in addition to offset. Variation in the sub-threshold slope factor, caused by process variations, could account for such a gain error. Figure 3.8 displays the response of a single pixel when an offset error is introduced(red line) and when offset and gain errors exist(blue line). The black line represents a nominal response.

The two parameter calibration from [71] aims to adjust all pixel values such that they become equal to the average of the entire array (for a given illumination).

Consider the average response of a pixel

$$\bar{y}_i \approx \bar{a} + \bar{b}\ln(c + x_i) \tag{3.31}$$

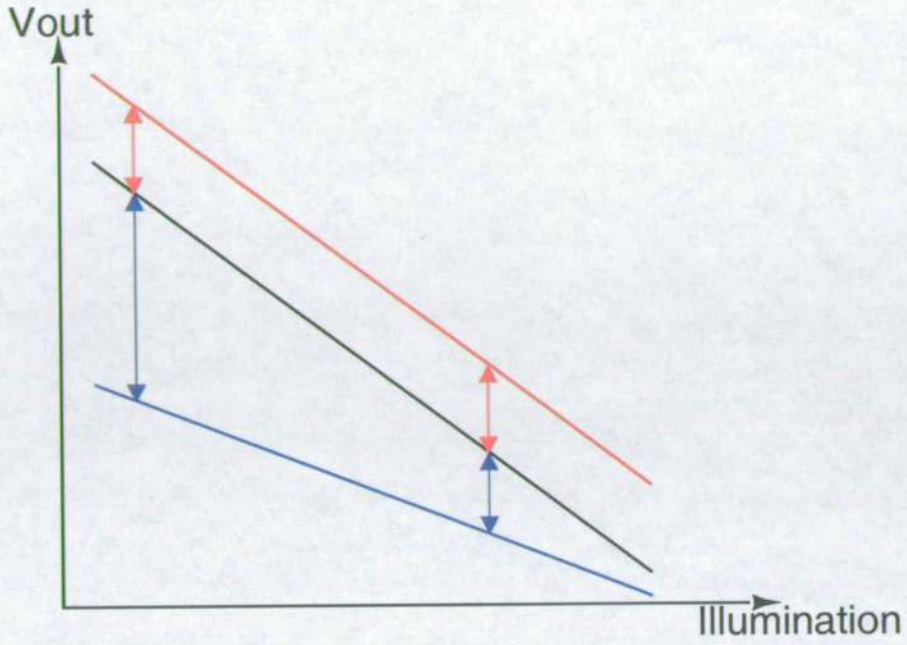


Figure 3.8: *Pixel response:ideal(black), offset variation(red), offset and gain variation(blue).*

where

$$\bar{a} = \frac{1}{N}\sum_{j=1}^{N} a_j \tag{3.32}$$

$$\bar{b} = \frac{1}{N}\sum_{j=1}^{N} b_j \tag{3.33}$$

Comparing Equations 3.12 and 3.31 with c_j = constant:

$$\hat{y}_{iy} = a'_j + b'_j \bar{y}_i \tag{3.34}$$

$$a'_j = a_j - b'_j \bar{a} \tag{3.35}$$

$$b'_j = \frac{b_j}{\bar{b}} \tag{3.36}$$

The MSE is given by Equation 3.37 [82]

$$MSE = \frac{1}{MN}\sum_{i=1}^{M}\sum_{j=1}^{N}(y_{ij} - \hat{y}_{ij})^2 = \frac{1}{MN}\sum_{i=1}^{M}\sum_{j=1}^{N}(y_{ij} - a'_j - b'_j \bar{y}_i)^2 \tag{3.37}$$

and minimised by differentiating with respect to a'_j and b'_j and setting the results to zero.

$$\frac{\partial MSE}{\partial a'_j} = \frac{-2}{MN}\sum_{i=1}^{M}(y_{ij} - a'_j - b'_j\bar{y}_i) = 0 \tag{3.38}$$

$$\frac{\partial MSE}{\partial b'_j} = \frac{-2}{MN}\sum_{i=1}^{M}(y_{ij} - a'_j - b'_j\bar{y}_i)\bar{y}_i = 0 \tag{3.39}$$

a'_j and b'_j can then be solved for and the solution becomes:

$$a'_j = \bar{y}_j - b'_j\bar{y} \tag{3.40}$$

$$b'_j = \frac{\sum_{i=1}^{M}(y_{ij} - \bar{y}_j)(\bar{y}_i - \bar{y})}{\sum_{i=1}^{M}(\bar{y}_i - \bar{y})^2} \tag{3.41}$$

Returning to Equation 3.34 the corrected pixel value is given by:

$$y'_j = \frac{y_j - a'_j}{b'_j} \tag{3.42}$$

The algorithm presented was coded in software to enable processing of raw image data captured in logarithmic mode. Only two reference frames were used (i=2) which is the minimum required to perform 2-parameter calibration. Using the two reference frames supplied the script calculated the offset (a'_j) and gain factor (b'_j) for each pixel in the array then applied Equation 3.42 to the image to be calibrated. The image files were the same as those used in Section 3.3.1. More detail on how the algorithm would be implemented in a real-time system is given is Section 3.3.3.

Figure 3.9 plots the remaining FPN (red line) after two parameter calibration when the reference points(frames) are either side of the illumination level being corrected. The green vertical lines indicate the illumination level of the reference frames whilst the red trace shows the remaining FPN at various illumination levels.

The remaining FPN is much flatter across the range of illumination than in the case of only offset calibration. There is a gradual increase in FPN toward a peak which is almost equidistant from the two reference points which stand almost four decades apart. The calibration

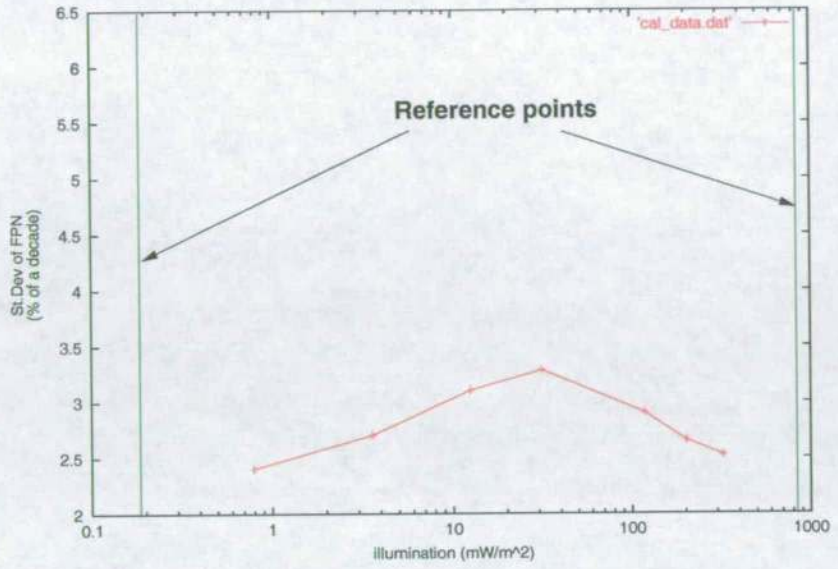


Figure 3.9: *Results of offset and gain calibration (reference points either side of calibration point.*

has reduced the level of FPN to below 4% across this range.

Figure 3.10 shows the case where the reference points are not either side of the illumination level at which the calibration is to be performed. It can be seen that the remaining FPN greatly increases when the calibration point lies outwith the two reference points.

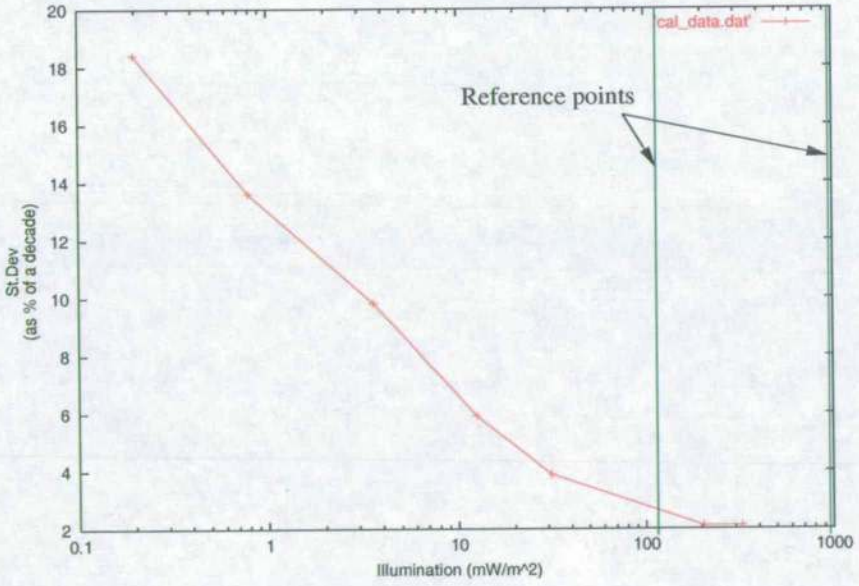


Figure 3.10: *Results of offset and gain calibration (some calibration points not between reference points).*

The algorithm implemented creates a model of the pixel's response between the two reference points and has an associated error. This error increases as the distance between the reference point and the data widens. It also suggests that the FPN is not purely caused by offset and gain variation of the logarithmic converting MOSFET.

To compare single and two parameter calibration Figure 3.11 plots the two sets of data. The vertical green lines again represent the illumination level of the reference points.

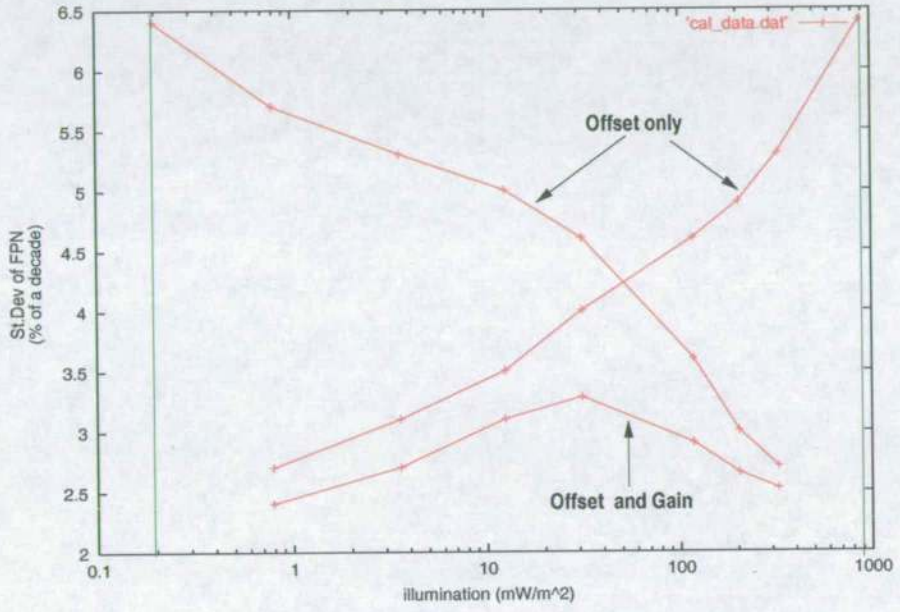


Figure 3.11: *Comparison of single and two parameter calibration.*

If two reference frames are used to perform offset calibration then a flatter reduction in FPN could be achieved. In such a scheme the closest reference frame to the incident illumination level would be used to perform the pixel difference operation however such an implementation would be complex to implement and could introduce new problems. The data would be discontinuous, relating to only one of the reference points. Joining the two sets of data together would be non-trivial.

For the same number of reference points the offset and gain algorithm is able to reduce FPN below that attainable from offset calibration even when the same two reference points are used.

The raw image of Figure 3.4 is shown in Figure 3.12 after two parameter calibration. The same software and reference frames were used but the frame to be corrected was an actual image.

The histogram of the calibrated logarithmic image along with the relative position of the refer-

Figure 3.12: *Logarithmic image after 2-parameter calibration.*

ence points is shown in Figure 3.13. The distance between the two reference points is equivalent to around 2.5 decades of illumination. The green vertical lines again have no meaning in relation to the y-axis scale, they are merely used to show the average code value for the two reference frames.

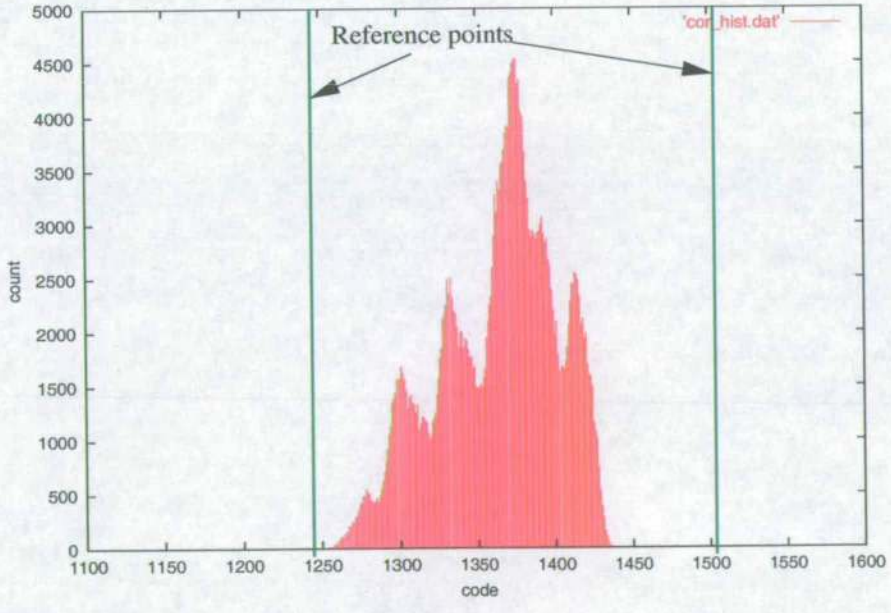


Figure 3.13: *Histogram of 2-parameter calibrated logarithmic image.*

3.3.3 Real-time Implementation

The software implementation has shown that the raw FPN can be greatly reduced using either calibration scheme. However, correction of offset and gain provides a more consistent reduction across a wider range of illumination levels assuming the reference points are correctly positioned. This chapter has used uniformly illuminated images as the reference points but this method does not lend itself to a real practical implementation. As mentioned in Section 2.5.5 logarithmic calibration is usually split into off-chip and on-chip schemes. The former requires a frame memory in which to store the reference point or some correction factor for each pixel. This solution imposes an extra overhead on the complete system as well as reduced performance from ageing or temperature effects. For on-chip calibration, in which only work on offset cancellation has been published, the reference point for each pixel is derived at each pixel. The most effective way to stimulate each pixel is by inducing a matched current. Figure 3.14 shows how a conventional 3T logarithmic pixel could be modified to include a reference generation scheme.

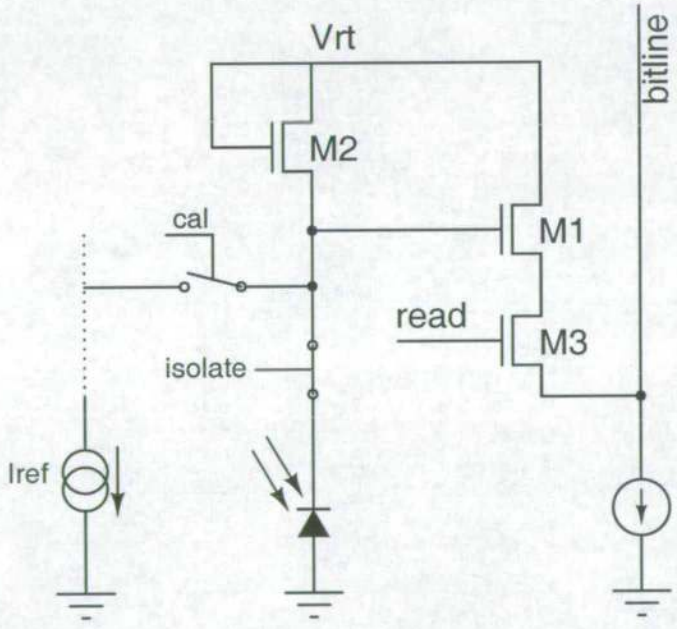


Figure 3.14: *logarithmic pixel with reference generation scheme.*

To bring the pixel into a reference state the switch controlled by *isolate* would be opened whilst closing the switch controlled by *cal*. The column current source pulls the set current through device *M2* and the pixel is read in the usual fashion. If the current is well matched across the pixel array then this will have a similar effect to uniformly illuminating the device. Obviously

only a single row of pixels is brought into the reference state at any single time. After sampling the raw logarithmic value the reference state could then be sampled. The use of a differential architecture would permit the subtraction to be performed during the conversion to a digital code.

Both single and two parameter calibration can be implemented in a real-time sensor without the requirement of a frame memory. However, offset and gain calibration is not as simple to implement as offset calibration. The two-parameter calibration algorithm would require a large amount of circuitry to be implemented in the analogue domain but would likely introduce excessive FPN and noise due to the small signal swings of the logarithmic mode.

For these reasons it was decided that a test device should perform the two parameter calibration in the digital domain. This unfortunately means a reduction in the achievable frame rate as extra ADC cycles are required to get all signals into the digital domain. Three readouts and conversions are required: the actual logarithmic data, the first reference level ($cal1$) and the second reference level ($cal2$). This only requires a memory location large enough to store two rows of data as will be explained in the remainder of this Section.

The challenge for on-chip two-parameter calibration resides in the reference generation. The calibration results from Section 3.3.2 have imposed requirements on the matching for the reference currents. The variation across all pixels in the array should be less than the minimum achievable FPN which implies the current matching should be better than $\sigma = 2\%$. It was also found that the calibration points should lie either side of the actual data point to achieve the best degree of FPN reduction. Thus the design of low sub-threshold currents that settle quickly is required. The design of calibration currents is discussed in Section 5.4

From Section 3.3.2 it can be seen that the two parameter calibration algorithm requires information on the reference points from the entire frame before a single pixel can be corrected. In its current form this algorithm cannot be implemented directly without a frame memory. However, assuming the reference points do not change between frames then information such as array averages can be stored at single memory locations.

Consider Equation 3.43 which represents the processing that needs to be performed for each pixel. It is found by expanding Equation 3.42 for the case when two calibration points are to be used ($i = 2$). The two reference points are given by $cal1$ and $cal2$.

$$y'_j = \frac{raw\_log\_value - \bar{y}_j}{\left[\frac{(cal1-\bar{y}_j)(cal1\_array\_ave-\bar{y})+(cal2-\bar{y}_j)(cal2\_array\_ave-\bar{y})}{(cal1\_array\_ave-\bar{y})^2+(cal2\_array\_ave-\bar{y})^2}\right]} + \bar{y} \tag{3.43}$$

Equation 3.43 requires the following:

- Average of the pixel array at reference points $cal1$ and $cal2$ which are written as $\bar{y}_{i(cal1)}$ and $\bar{y}_{i(cal2)}$
- Average over the illumination range: $\frac{\bar{y}_{i(cal1)}+\bar{y}_{i(cal2)}}{2}$
- Average per pixel over the intensity range: $\bar{y}_j$.

The first two averages listed can be stored in a few registers and accumulated as each frame is read out. Alternately it could be updated less often such as once every 10 or 100 frames. Since the calibration points for each pixel in the array do not change between frames the statistics can be applied to future frames. Temperature and ageing effects will not be a problem due to the short time between the the updating of the averages.

The last average listed can be calculated each time a pixel is read. Is is simply the average of $cal1$ and $cal2$.

A signal flow graph relating to Equation 3.43 is shown in Figure 3.15.

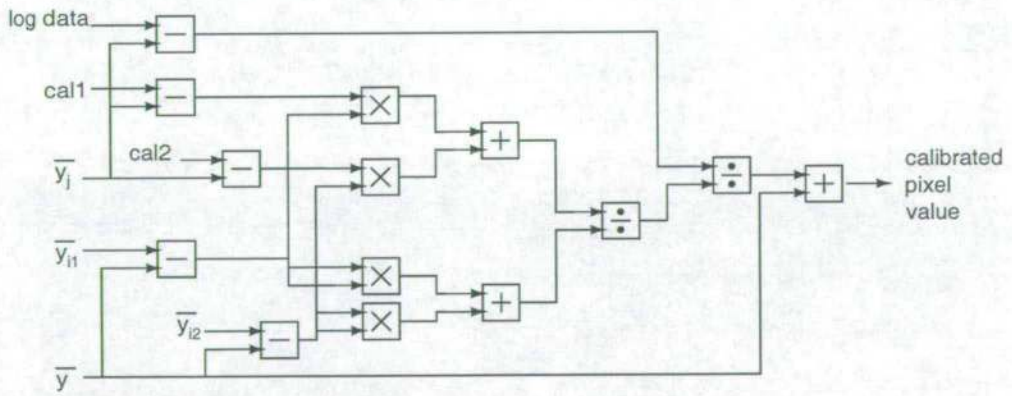


Figure 3.15: *Calibration per pixel*

3.3.4 Conclusion

This Chapter has thus far presented two calibration schemes for reducing FPN in a logarithmic sensor. Both schemes have been implemented in software and their effectiveness assessed on

actual logarithmic data from a CMOS imaging device. The work used a maximum of two reference frames in contrast to the previous literature [71]. Both single and two parameter calibration greatly reduced the raw FPN in an image. Simple offset calibration was most effective if the reference level was close to the actual operating point but two-parameter calibration provided a greater reduction across a wider illumination range. The drawbacks or extra requirements of the two-parameter approach become apparent when considered as part of a real-time imaging device which uses no external memory. Chapter 5 deals with the design of a sensor which can create two reference points and Chapter 6 provides the measurement results.

3.4 Combining images

This section shows how a wide dynamic range image can be constructed by combining linear and logarithmic data from the same scene. The process is first demonstrated using software to manipulate a linear and logarithmic image captured separately before discussing implementation on an actual imaging device.

The algorithm to be presented substitutes logarithmic data for all saturated pixels of the corresponding linear image. If valid linear and logarithmic data exist for a pixel then the linear is used due to its higher SNR. It should be noted that the substitution is always performed on over-exposed linear pixels and never on under-exposed regions. The reason for this choice arises from the SNR of the two modes and their ability to image in extreme lighting conditions. The linear mode has superior low light performance due to the averaging of the photo-signal at the pixel and the SNR of logarithmic mode is maximised at high illumination levels. A logarithmic device may outperform a linear sensor at higher illumination intensities. This is dependent on the minimum exposure time at which the linear sensor can operate.

In a combined linear-logarithmic image the exposure time can directly affect the overall dynamic range. Figure 3.16 aims to show the interaction between illumination, exposure and dynamic range and assumes the linear and logarithmic modes work independently. It can be seen that reducing the exposure moves the linear operating point to a higher illumination level. At the same time the amount of logarithmic data used is reduced. It can be seen that the maximum linear exposure would yield the highest overall dynamic range and at this stage may be considered the best setting.

Figure 3.16 is valid when using linear and logarithmic images captured using conventional

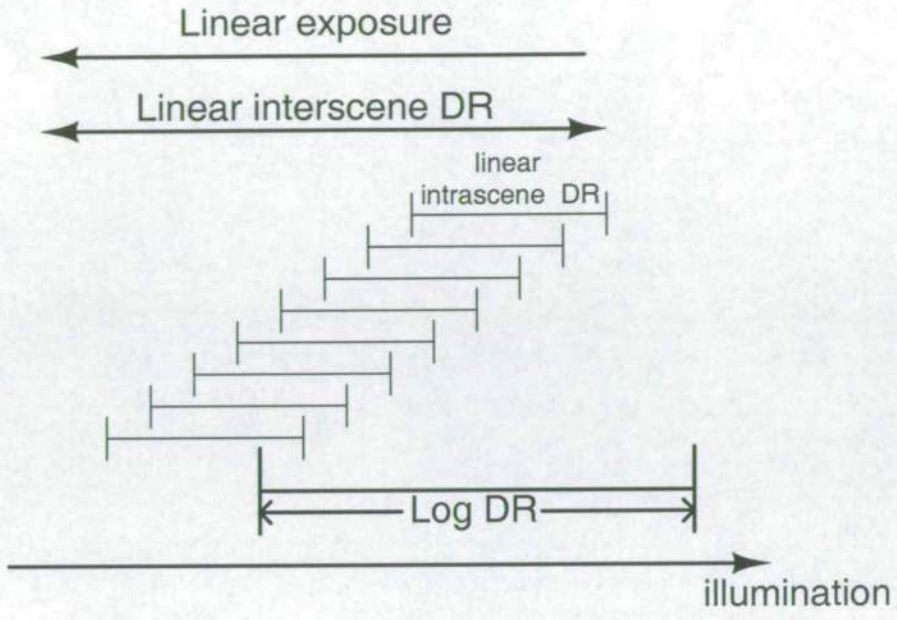


Figure 3.16: *Linear and logarithmic modes of operation.*

operating modes as is performed in this Chapter. It is important to realise that the characteristics of either mode are liable to change if combined on the same sensor. For example the logarithmic range is likely to reduce if the settling time is reduced. Such limitations depend on the design of such a sensor and are covered in Chapter 5.

Prior to commencing the design in silicon it was necessary to verify that a combined linear logarithmic image could be constructed. It was uncertain how data at the crossover point between linear and logarithmic regions would appear in an actual image. The device and setup used was the same as that described in the previous work on calibration except that the sensor was now exposed to an actual scene. A lens was mounted on the device and manually adjusted until the scene was correctly focused. A single linear and logarithmic image was then captured. The time between the images was not negligible as new settings had to be loaded on to the test platform. The logarithmic image was calibrated using the software implementation of the two parameter algorithm. Uniformly illuminated frames were again used as the reference points for the calibration. Scenes with a high dynamic range were chosen as they represent the intended use of such a system. The scene in Figure 3.17 shows the limitation of the linear mode under such conditions. The rightmost facade displaying the university crest and logo is over-exposed causing the text round the crest to be unreadable. In the shadows on the left hand side of the scene the facade and cartoon toy require the longer linear exposure for their lower illumination.

A decrease in the integration period would lose detail captured in the shadows on the left. The histogram of the linear scene is displayed in Figure 3.18. The codes do not begin at zero due to an offset in readout, not because there are no dark areas in the scene.

Figure 3.17: *High dynamic range scene imaged by linear mode.*

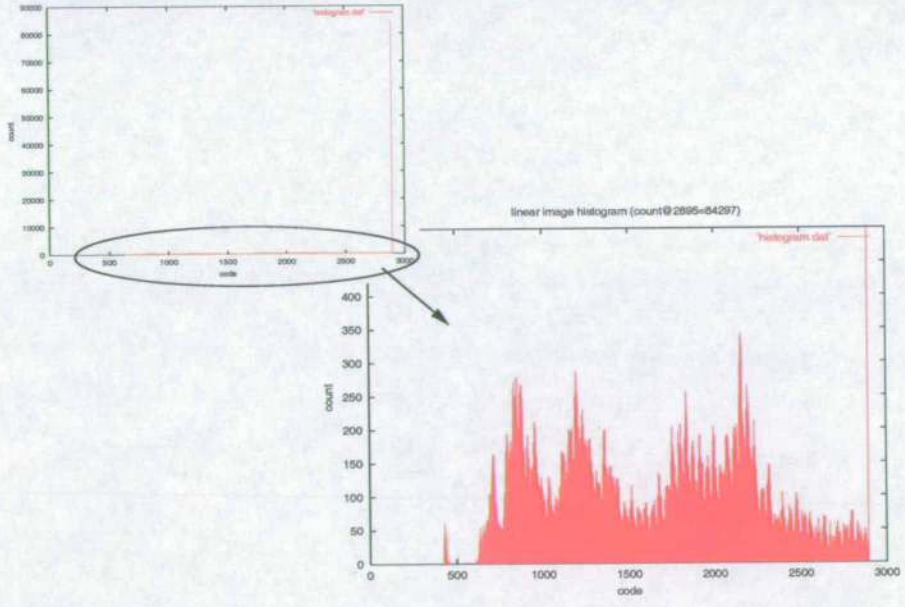


Figure 3.18: *Histogram of linear image (top graph shows count at saturation level).*

Figure 3.19 shows how a typical linear response could be aligned with a logarithmic curve to

extend the dynamic range. The logarithmic curve has been appropriately shifted and a gain applied. The logarithmic compression on the photo-signal produces a reduced voltage swing in the data compared to the linear. Without additional gain the logarithmic data will have a low contrast compared to the linear. The application of gain to the logarithmic data is discussed more fully in Chapter 6.4.1. For a set integration, linear saturation is reached if there is sufficient illumination to discharge the pixel past the lower operating point of the source follower. All pixels that have saturated contain no image data and are useless. Lost information in the saturated pixels of a linear image could be restored if logarithmic data were substituted in their place.

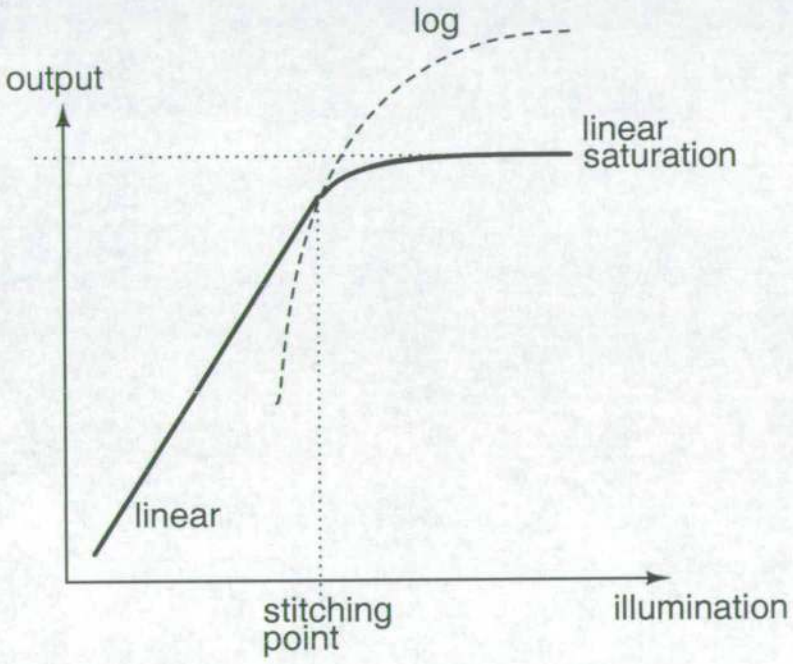


Figure 3.19: *Linear and Logarithmic curve stitching.*

Prior to substitution, the logarithmic data was shifted to align with the linear range. The shift was calculated by comparing non-saturated linear and logarithmic data from the same pixel. This comparison level is labelled as the *stitching point* in Figure 3.19. The stitching point was chosen close to the linear saturation level to maintain as much linear data as possible to benefit from the higher SNR.

Software was used to perform the combination of linear and logarithmic data into a single image. The software took a codes threshold level as an input and then calculated the offset to apply to the logarithmic data as follows:

- Parse the linear image to find the value nearest to the threshold set (this becomes the stitching point). Store the location(s) of these pixels.
- Average the values at the stored locations in the **logarithmic image**
- The difference between the stitching point and the average of the logarithmic values becomes the offset.

A simple boolean substitution was performed on the linear image to instantiate the logarithmic values. If a linear pixel had a value greater than the stitching point then the equivalent pixel value from the logarithmic image was added to the offset then substituted. Figure 3.20 shows the complete image fusion process and Figure 3.21 shows the linear image with the substitution areas blackened.

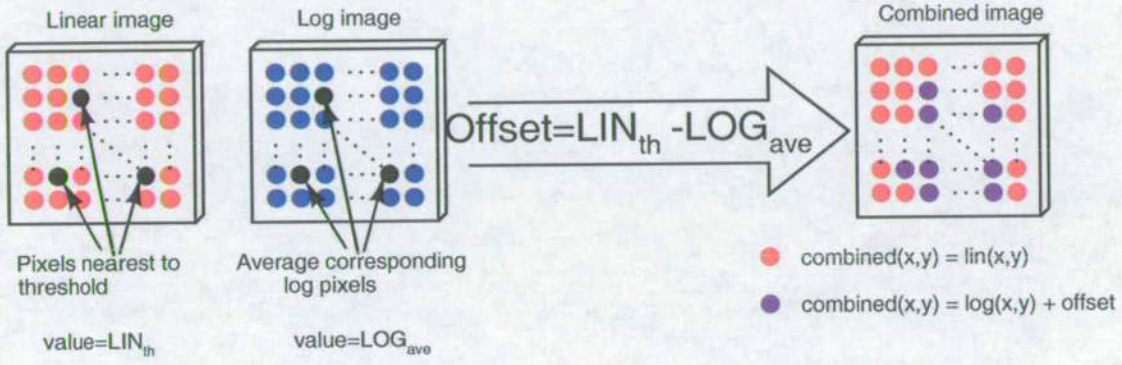


Figure 3.20: *Linear Logarithmic fusion process.*

The fused image in which the logarithmic data has a gain of 16 applied is shown in Figure 3.22.

The combined image has restored information to saturated areas of the linear scene. The text surrounding the university crest on the rightmost facade is now more clearly visible without any loss of information in the shadows on the left of the scene. Figure 3.22 appears darker than the original linear image but this is a limitation of the display. A wider range of data is being viewed in the same display range thus there is a loss of contrast across the scene. Although the logarithmic data is a large improvement in comparison to the saturated pixels, it is still possible to see where the stitching has occurred. The superior SNR of the linear data is the reason for such differences.

Figure 3.21: *Image showing the areas where log data is to be substituted.*

Figure 3.22: *Combined Linear Logarithmic image.*

A histogram of the data in the combined image is shown in Figure 3.23. The stitching point was set at 2300 codes and the difference between the linear and logarithmic data is apparent. Because the logarithmic data has had a gain applied there are missing codes in the histogram. The count is also much higher for the logarithmic data because of its low voltage swing in comparison to linear mode.

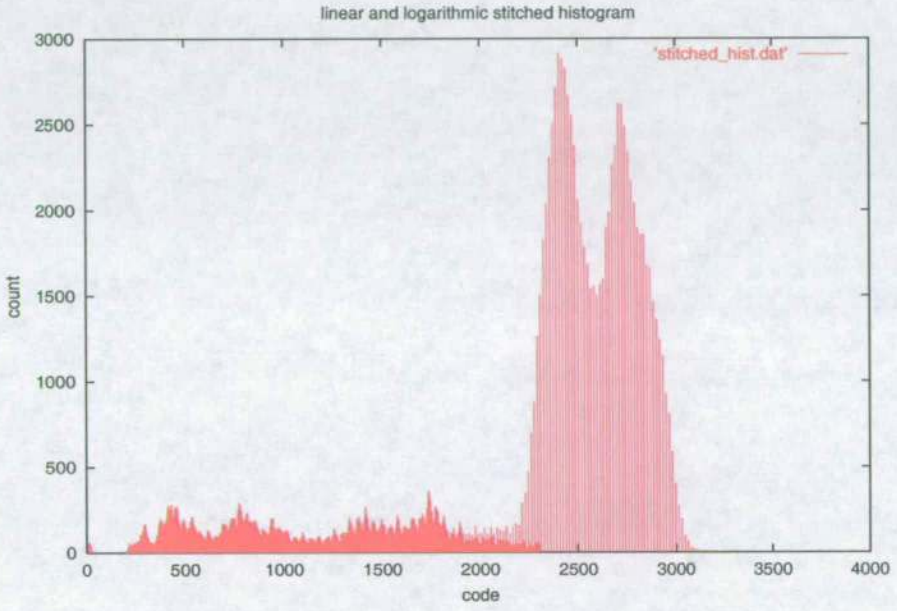


Figure 3.23: *Combined Linear Logarithmic image histogram.*

3.4.1 Real-time Implementation

The software implementation uses two complete frames of data to perform the substitution. Although the algorithm is not complex the requirement to create a mapping between the two sets of data means information on both frames is required. In software the linear image was parsed to find the pixel location(s) nearest to the threshold. However, in a linear-logarithmic device operating in real-time this will not be possible without the use of a frame memory Operation of such a device is likely to be as follows: When a single row in the array is addressed the linear result will be read first and stored in a line memory. Next the logarithmic data will be sampled and the decision on which value to use will be done as the logarithmic data is readout (assuming offset calibration). If logarithmic data is kept, the offset must be added at this stage. This means a single frame lag in the beginning is required such that the offset to apply to the logarithmic data can be calculated. The offset will not need to be re-calculated unless the linear integration time is altered.

3.4.2 Conclusions

The software implementation to substitute logarithmic data into the over exposed regions of a linear image has been confirmed as a way of extending dynamic range. Using linear and logarithmic data captured independently a mapping between the two modes was found from a simple comparison at the chosen linear threshold. The logarithmic data also required extra gain to match the contrast of the linear. The combination of linear and logarithmic data in a single image can be implemented in a real-time imaging device without the requirement of a frame memory. A proposed system to accomplish this is presented in Chapter 5.

Although the sample images clearly demonstrate the dynamic range extension, the lower SNR of the logarithmic data is visible in the final image. Alternate approaches also suffer from mismatch in SNR [83]. Well adjustment in which the reset signal to the pixel is stepped suffers from a dip in the SNR at the stepping point. Multiple capture also suffers from a SNR reduction in the low code areas of each frame. The problem can be improved by capturing more frames at the expense of increased complexity. The SNR of logarithmic mode is low because of the high degree of compression applied to the photo-signal. Chapter 4 discusses the logarithmic voltage swing in more detail.

Chapter 4
Logarithmic Response in a CMOS Imager

This chapter looks in more detail at the logarithmic mode of operation in a CMOS image sensor. Since the compression is a result of the MOSFET operating in the sub-threshold region, the appropriate transistor level equations are further studied. An alternate logarithmic arrangement is also presented and a comparison made with the conventional circuit in terms of voltage swing and transient response. The chapter begins by looking in more detail at the voltage swing obtainable for a given change in drain current. A wider voltage swing will improve the perceived quality of an image due to an increase in the SNR. The body effect, which has been ignored until this point is also discussed. The second half of the Chapter investigates the transient response in logarithmic mode. This is an important performance metric when considering the design of a combined linear-logarithmic CMOS image sensor.

4.1 Sub-threshold operation

A model which details gate, source and drain potentials in terms of the drain current (I_{DS}) is derived in [84] and written below:

$$I_{DS} = \frac{W}{L} I_{D0} e^{\frac{V_{GB}}{nV_t}} \left(e^{-(\frac{V_{SB}}{V_t})} - e^{-(\frac{V_{DB}}{V_t})} \right) \tag{4.1}$$

The model is similar to that used in Chapter 2.4.5 except the terminal potentials are expressed with respect to the bulk voltage. The subscripts ($_{GB}$, $_{SB}$ and $_{DB}$) reflect measurement with respect to the bulk. The arrangement shown in Figure 4.1 is the most widely used logarithmic arrangement. The bulk of the NMOS device is connected to ground, usually by direct contact with the substrate. This difference in potential between the bulk and source terminals causes the body effect. The body effect introduces the term V_{SB}. This phenomenon modulates the drain-source current that flows in the device. Its effect on a device operating in the sub-threshold

region is discussed next. First it is required to derive the output voltage for the circuit in Figure 4.1.

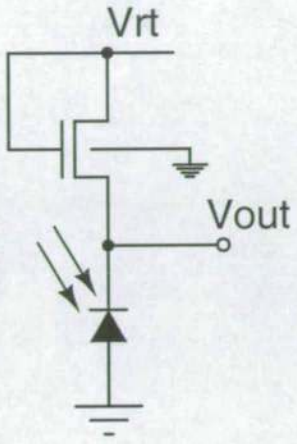


Figure 4.1: *Logarithmic converting device.*

Expanding Equation 4.1 and assuming $V_{DB} >> V_t$ gives

$$I_{DS} = \frac{W}{L} I_{D0} \left(e^{\frac{V_{GS}}{nV_t}} e^{\frac{V_{SB}}{V_t}(\frac{1}{n}-1)} \right) \tag{4.2}$$

Thus the gate source voltage can be expressed as:

$$V_{GS} = nV_t \left[\ln \left(\frac{I_{DS}}{\frac{W}{L} I_{D0}} \right) - \frac{V_{SB}}{V_t} (\frac{1}{n} - 1) \right] \tag{4.3}$$

Equation 4.3 can be written as:

$$V_{GS} = nV_t \ln \left(\frac{I_{DS}}{\frac{W}{L} I_{D0}} \right) - V_{SB}(1-n) \tag{4.4}$$

and the output voltage as:

$$V_{out} = Vrt - V_{GS} \tag{4.5}$$

Now substituting for V_{GS} and noting that $V_{SB} = V_{out}$

$$V_{out} = Vrt - \left(nV_t \ln(\frac{I_{DS}}{\frac{W}{L} I_{D0}}) - V_{out}(1-n) \right) \tag{4.6}$$

$$nV_{out} = Vrt - nV_t \ln \left(\frac{I_{DS}}{\frac{W}{L} I_{D0}} \right) \tag{4.7}$$

$$V_{out} = \frac{Vrt}{n} - V_t \ln \left(\frac{I_{DS}}{\frac{W}{L} I_{D0}} \right) \tag{4.8}$$

This result is now compared to the case when $V_{SB} = 0$. Under such conditions Equation 4.1 becomes:

$$I_{DS} = \frac{W}{L} I_{D0} e^{\frac{V_{GS}}{nV_t}} \tag{4.9}$$

if V_{DB} is again assumed to be $>> V_t$. Developing an expression for the output voltage in the same manner yields Equation 4.10.

$$V_{out} = Vrt - nV_t \ln \left(\frac{L}{W} \frac{I_{DS}}{I_{DO}} \right) \tag{4.10}$$

It can be seen that Equation 4.8 exhibits a lower change in output voltage for the same variation in drain current as compared to Equation 4.10 (assuming $n > 1$). Further discussion of this result is given after a second logarithmic arrangement is considered.

The logarithmic arrangement discussed so far has fixed the gate voltage of the logarithmic converting device. This means the source terminal must vary to reflect the different currents flowing. It is the gate-source voltage that is modulated by the current flowing, thus by using feedback it is possible to fix the source voltage and allow the gate voltage to reflect the current flow.

A pixel designed to detect contrast changes was proposed by Delbruck and Mead in 1996 [85]. The source of the logarithmic converting device controls a simple inverting amplifier which feeds back its output to the gate of the source follower. An adaptive element that sits between the output of the amplifier and the gate of the source follower means the feedback is essentially short circuited on long time scales but open circuit for a high frequency input.

A similar principle has been applied by Huppertz *et al* in [70] with the exclusion of the adaptive element. Their 4 transistor pixel comprises a conventional NMOS device which converts the photo-current into a logarithmic voltage. A simple two transistor inverting amplifier holds the source of the NMOS constant while a final device is used to select different rows.

Figure 4.2 shows an arrangement that encompasses a differential amplifier between the photo-diode and the gate of the NMOS. The source voltage of the logarithmic converting device is held constant at a level determined by *Vref*.

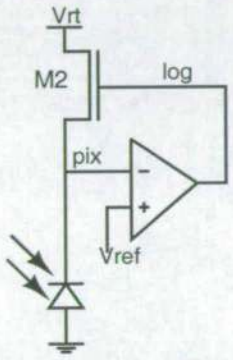


Figure 4.2: *Logarithmic converting device(M2) with feedback amplifier*

Assuming no input offset for the amplifier the logarithmic voltage can be derived as follows:

$$\begin{aligned} V_{log} &= A(Vref - V_{pix}) && (4.11)\\ &= A(Vref - (V_{log} - V_{GS(M2)})) \\ &= \frac{A}{A+1}(Vref + V_{GS(M2)}) && (4.12) \end{aligned}$$

where A is the gain of the amplifier. The gate-source voltage for *M2* will be given by Equation 4.4 except that V_{SB} will be constant and can be replaced by $Vref$. Equation 4.12 becomes

$$\begin{aligned} V_{log} = \; & \tfrac{A}{A+1}(Vref + nV_t \ln(\tfrac{I_{DS}}{\frac{W}{L}I_{D0}}) - Vref(1-n) && (4.13)\\ = \; & \tfrac{A}{A+1}(nVref + nV_t \ln(\tfrac{I_{DS}}{\frac{W}{L}I_{D0}}) && (4.14)\\ = \; & nVref + nV_t \ln(\tfrac{I_{DS}}{\frac{W}{L}I_{D0}}) \qquad \text{if } A >> 1 && (4.15) \end{aligned}$$

Thus Equation 4.15 suggests that the logarithmic output voltage will have a slope greater than the arrangement with the fixed gate for the case when the bulk of *M2* is not connected to its source (Equation 4.8). This is achieved by removing the dependence of the bulk-source voltage on the photo-current level.

The model used to express the gate-source voltage includes terms for the sub-threshold slope factor (n), threshold voltage (V_{th}) and characteristic current (I_{D0}). Until now these terms have been considered to be constant. Tsividis [33] shows that these terms all depend on the bulk-source voltage in a non-trivial manner. For this reason simulation was used to investigate the body effect in sub-threshold.

The two cases studied are shown in Figure 4.3. Circuit (a) shows the conventional logarithmic arrangement where the gate voltage is fixed and the source voltage modulated. ***log_gf*** is the output voltage when the ***g***ate is ***f***ixed. Circuit (b) shows the case where the source is held constant by the addition of a simple inverting amplifier. ***log_sf*** is the output voltage with the ***s***ource ***f***ixed.

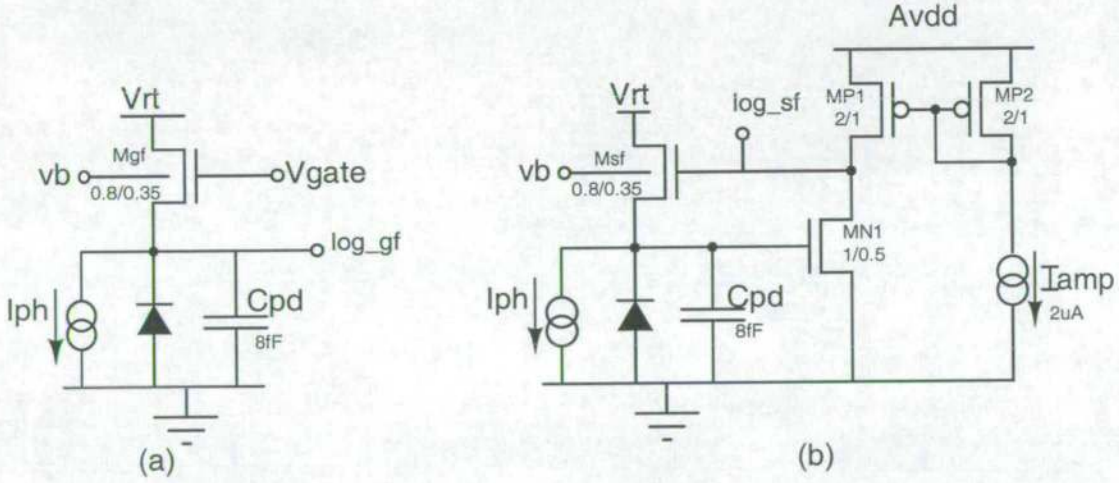


Figure 4.3: *Schematics for simulation: (a) M2 source potential varies, (b) M2 gate potential varies.*

In the simulation performed, Vrt was set to 2.7V, $Avdd$ 3.3V and V_{gate} 2V. The DC conditions of both circuits were plotted as I_{ph} was swept from 100fA to 100pA. The responses are shown in Figure 4.4. It can be observed that the slopes have opposite polarity but in both cases the gate-source voltage increases as a result of an increase in I_{ph}.

The difference in the output voltage range for the simulated cases was recorded and expressed per decade of Iph. Table 4.1 shows the results.

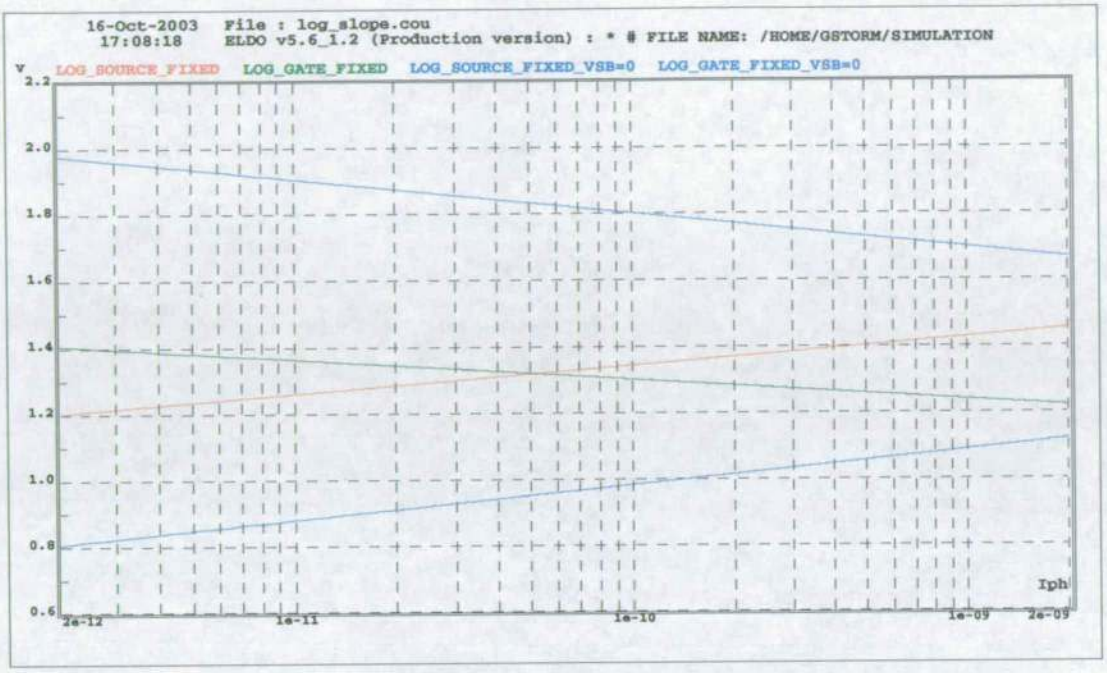


Figure 4.4: *DC sweep results.*

	V_{bulk}=0	V_{BS} =0
circuit (a)	60mV	104mV
circuit (b)	83mV	104mV

Table 4.1: *Logarithmic response for bulk held at 0V and bulk connected to source.*

It can be seen that the lowest logarithmic response occurs when the gate voltage is fixed and the source voltage varies. The change in the bulk-source voltage counteracts the change in the gate-source voltage thus lowering the sensitivity. An increased response is achieved by circuit (b) in which the source voltage is held constant and the gate voltage varies. A high responsivity is shown for both circuits if the bulk is connected to the source. However, such a solution has many drawbacks. To isolate the bulk of M2 from the substrate (which is held at 0V) requires an extra N-well and p-type implant. As an example an ideal implant structure is shown in Figure 4.5.The design rules for such implants mean that the required area will greatly increase even in an advanced process such as 0.18μm. A larger pixel pitch means higher cost for a given resolution.

The connection of bulk to source will also increase the capacitance at the source of M2. From Figure 4.5 it can be seen that the capacitance of the new p implant will now be added to the far smaller source capacitance. This extra capacitance will greatly reduce the transient performance.

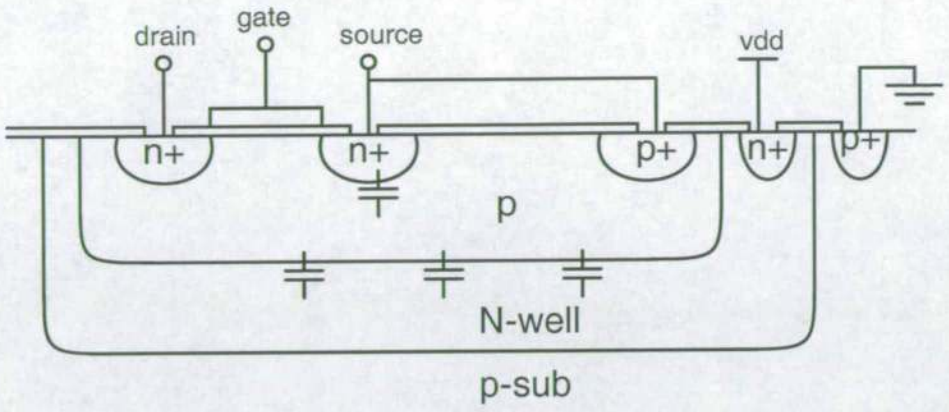


Figure 4.5: *Implants required to connect bulk to source.*

The results from simulation agree quite well with that predicted by the sub-threshold transistor equations although a higher response was expected for circuit (b) even when M2's bulk was not connected to its source. The difference is thought to come from the simplified equations used in the text.

Other techniques also exist to improve the logarithmic signal swing. As shown in Section 2.5.5 [74] [9] two NMOS devices can be stacked to almost double the swing. In theory multiple devices could be stacked but the voltage supplies will impose a limit on the headroom. A reduction in fill factor is also unavoidable.

4.2 Transient performance

The logarithmic schemes [85] [70] that use an amplifier to maintain a constant source-bulk voltage operate continuously in time. Thus their step response is important and needs to be evaluated with respect to abrupt changes in the incident illumination. Such characteristics also determine the settling performance of the circuit if it were switched between being enabled and disabled. For example, a linear integrating mode could be enabled before switching to a logarithmic arrangement within a single pixel. The settling performance of such a logarithmic arrangement would be important if the system was to operate in real time.

The AC response of the two circuits shown in Figure 4.3 is evaluated via small signal analysis then a transient simulation performed. The small signal model for circuit (a) from Figure 4.3 is shown in Figure 4.6.

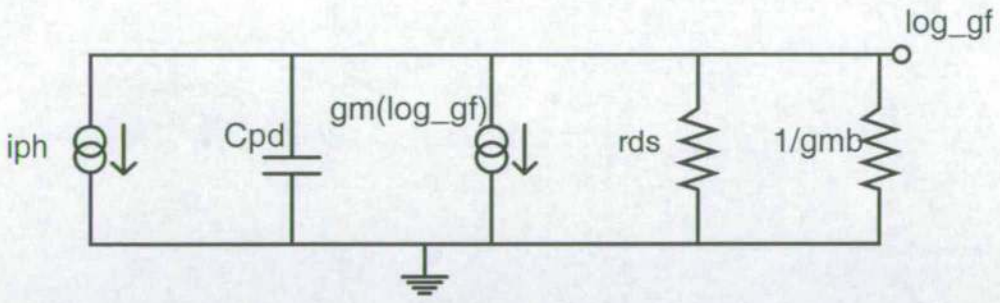


Figure 4.6: *Small signal equivalent circuit for Figure 4.3(a)*

To determine the transfer function of the circuit Kirchoff's current law is applied. Summing the currents leaving the node log_gf produces Equation 4.16.

$$iph + v_{(log\_gf)}sC_{pd} + v_{(log\_gf)}gm + \frac{v_{(log\_gf)}}{rds} + v_{(log\_gf)}gmb = 0 \tag{4.16}$$

Rearranging produces the transfer function

$$\frac{v_{(log\_gf)}}{iph} = \frac{-1}{sC_{pd} + gm + gmb + \frac{1}{rds}} \tag{4.17}$$

Thus there is a pole at approximately $\frac{-gm}{C_{pd}}$.

The transfer function for circuit (b) from Figure 4.3 is determined in the same fashion. The small signal equivalent circuit for schematic (b) is shown in Figure 4.7.

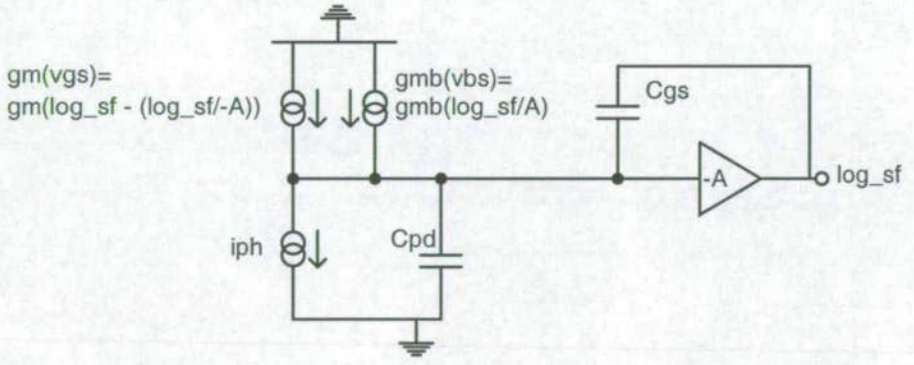


Figure 4.7: *Small signal equivalent circuit for Figure 4.3(b)*

Summing the currents at the input to the amplifier yields

$$0 = v_{(log\_sf)}gm(1+\frac{1}{A}) + gmb\frac{v_{(log\_sf)}}{A} - iph + \frac{v_{(log\_sf)}}{A}sC_{pd} + \left(V_{(log\_sf)} - \frac{v_{(log\_sf)}}{A}\right)sC_{gs} \quad (4.18)$$

$$Aiph = v_{(log\_sf)}\left[gm(A+1) + gmb + sC_{pd} + sC_{gs}(A+1)\right] \quad (4.19)$$

The transfer function can be written

$$\frac{v_{(log\_sf)}}{iph} = \frac{A}{gm(A+1) + gmb + sC_{pd} + sC_{gs}(A+1)} \quad (4.20)$$

$$= \frac{A}{[C_{pd} + C_{gs}(A+1)]\left[s + \frac{gm(A+1)+gmb}{C_{pd}+C_{gs}(A+1)}\right]} \quad (4.21)$$

$$\approx \frac{1}{C_{gs}\left(s + \frac{gm}{C_{gs}}\right)} \quad (4.22)$$

Equation 4.22 has a pole at $\frac{-gm}{C_{gs}}$. This is compared to $\frac{-gm}{C_{pd}}$ for the case when the gate voltage of the logarithmic converting device is held constant. The photodiode capacitance, C_{pd}, will be significantly larger than the overlap capacitance, C_{gs}, of *Msf* thus the pole of circuit(b) will occur at a higher frequency than for circuit (a). This means circuit(b) will respond faster to changes in the photo-current.

Using the circuits shown in Figure 4.3 a transient simulation was performed to confirm the settling performance of the the two arrangements to an abrupt change in the photo-current. Figure 4.8 plots the output voltage of both circuits from Figure 4.3 against time. The bulk voltage was fixed at ground in all cases. The input current, Iph, was stepped upwards at $40\mu s$ then back to its starting value at $400\mu s$. The values of Iph are also shown in Figure 4.8.

The top set of curves show the output from circuit (a) of Figure 4.3 whilst the lower curves show circuit b's response. As mentioned previously the two circuits have opposite polarity thus the step up in *Iph* at 40μs causes the output of circuit (a) to fall and circuit (b) to rise. The opposite changes in output are observed when Iph is stepped down. It is clear that the logarithmic voltage settles quicker in circuit (b) and is most visible for the case when Iph = 1pA. This result agrees with that predicted from the small signal analysis.

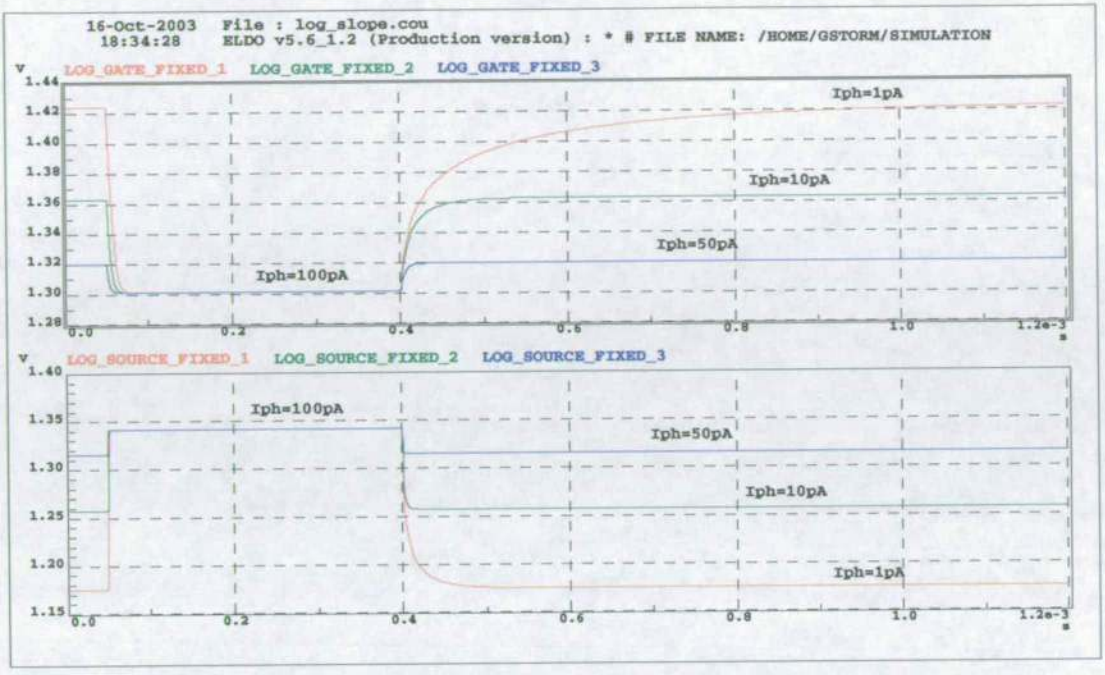


Figure 4.8: *Transient settling results for circuits of Figure 4.3.*

4.3 Conclusion

This chapter has examined the logarithmic response from two different architectures implementable in a CMOS sensor. The conventional 3T arrangement has been compared to a case in which feedback is used to hold the source voltage of the logarithmic converting device constant. Voltage swing and settling time were used as the comparison metrics as they represent two important parameters in an imaging system.

It was shown that the logarithmic sensitivity is reduced by the body effect and the conventional arrangement in which the gate voltage is held constant shows the lowest response. Improved sensitivity can be achieved by fixing the voltage of the source terminal and observing the voltage on the gate. This requires some some form of feedback such as an inverting amplifier. The highest slope is achieved if the bulk is connected to the source regardless of whether the source or gate is fixed. However, the drawbacks of such an implementation are increased area and capacitance.

The circuit incorporating the feedback amplifier was also shown to exhibit the best settling performance. This is the main reason its architecture was adopted for the the final part of this project. Chapter 5 will present the details of a sensor capable of both linear and logarithmic operation.

Chapter 5
Sensor Design

This Chapter provides a full discussion of the circuitry designed to realise a CMOS image sensor that is capable of producing linear and logarithmic data for combination in real-time. Chapter 3 has demonstrated that an image composed of linear and logarithmic data can have a wider dynamic range than the linear alone. This combination does not compromise low light level performance. However, Chapter 3 used linear and logarithmic data captured independently as a proof of concept and is far from a working imager.

The main blocks designed in the CMOS image sensor with combined linear and logarithmic sensing were:

- A new pixel that is switchable between the two modes.
- A logarithmic arrangement that settles quickly.
- A means of calibrating every log pixel such that 2-parameter correction can be implemented.

The device was designed such that logarithmic data could be sampled as soon after the linear data as possible. This means that when a row in the array is addressed the linear data and logarithmic data are read out before the next line is addressed. The readout of logarithmic data may require numerous reads of a pixel if calibration is to be performed. The time permitted per line was constrained to achieve an acceptable frame rate. As mentioned in Chapter 3 the system was designed without the requirement of a framestore for either the linear-logarithmic combination or the logarithmic calibration.

The sensor was designed and fabricated in a 0.18μm process which differs to the 0.35μm technology used for previous measurements (Chapter 3). A more advanced technology allows smaller device sizes and interconnect width thus improves the chip density. In terms of performance it is detrimental to reduce the light sensing areas, however, since the pixels account for the majority of the silicon area a smaller pixel reduces cost.

5.1 Sensor Overview

The floor plan for the test sensor designed is shown in Figure 5.1. The CIF format pixel array is addressed by means of a Y-decoder situated to the left of the array and, dependant on the signal sought, either the logarithmic amplifier or linear current source is connected to the pixels addressed. The signals are sampled in a column parallel architecture. The analogue to digital conversion of the respective signals is also carried out on a per-column basis, with the digital results being stored in one of two sets of SRAM banks. During the subsequent ADC cycle the previous values from SRAM are readout serially, with the X-Decoder addressing each column in turn. The minimum device dimensions of the 0.18μm process were only implementable for the digital logic on the chip due to the maximum voltage ratings. Devices connected to the analogue 3.3V supply had to be formed with double oxide gate thickness which increased their minimum dimension to 0.35μm.

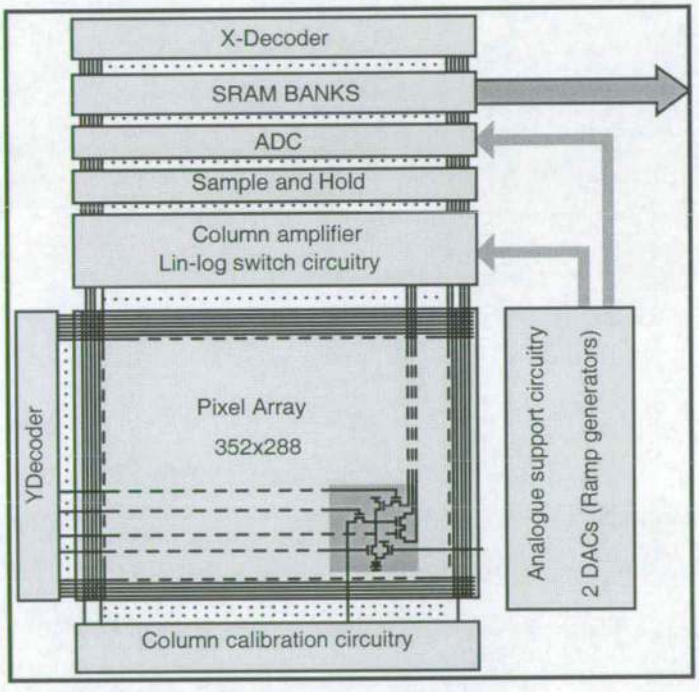


Figure 5.1: *Floorplan of sensor.*

Matched current sources for logarithmic calibration are situated below the pixel array and provide a reference current for the addressed row of pixels. Column calibration and an in-pixel calibration scheme are presented in Section 5.4. Also shown in Figure 5.1 is the analogue control circuitry which includes two DACs. The first DAC is used to supply the ramp to the single slope ADC and the second controls the reference voltage applied to the amplifier used in

logarithmic configuration.

The fabricated device included pre-designed blocks from STMicroeltronics. The ADC, SRAM and DAC are such blocks and have permitted a reduction in design time. Such re-use of core blocks also increases the chances that the first cut of silicon is functional.

The sensor does not include any digital control circuitry to provide the correct sequencing of signals to each block. Instead, the input signals are generated on an FPGA device which is assembled on the same test platform as the sensor. The test setup is shown in Figure 6.1 in Chapter 6. The use of an FPGA reduces the complexity of the test device and does not constrain the timing of inputs. The test platform also includes a number of analogue voltage references. Properly regulated power supplies are an important part of an image sensor although very little is reported in the literature. On-chip voltage references need to handle surges of current. For example when a row is reset or read the reference voltages need to be stable or noise will be injected into the image.

The test device was fabricated to study linear and logarithmic operation combined on a single chip and the associated merits, such as settling time and calibration. It thus makes sense to exclude non-essential circuitry such as the power management.

5.2 Combined Linear-Logarithmic Pixel

The new pixel arrangement is shown in Figure 5.2. It consists of seven N-type MOSFETs labelled *M1* to *M7* and a photodiode *PD1*. There are four vertical access lines labelled *col1* to *col4* and four horizontal control lines, *logsel, isolate, cal/reset* and *read*. *Vrt* and *Vbloom* are reference voltages and are common to all pixels. For the purpose of simulation the schematics included an ideal current source in parallel with the photo-diode. This allowed easy programming of the photocurrent.

5.2.1 Linear operation

The pixel is reset by raising the control line *cal/reset* such that device M4 is ON and *pix* is charged to the voltage of *col4*. *isolate* will also be ON thus the photodiode voltage will be equal to the voltage on *pix*. Simultaneously, M6 is turned ON to precharge the gate of M2 to 0V. This prevents M2 conducting current from *Vrt* to *pix*. The lowering of *cal/reset* starts the

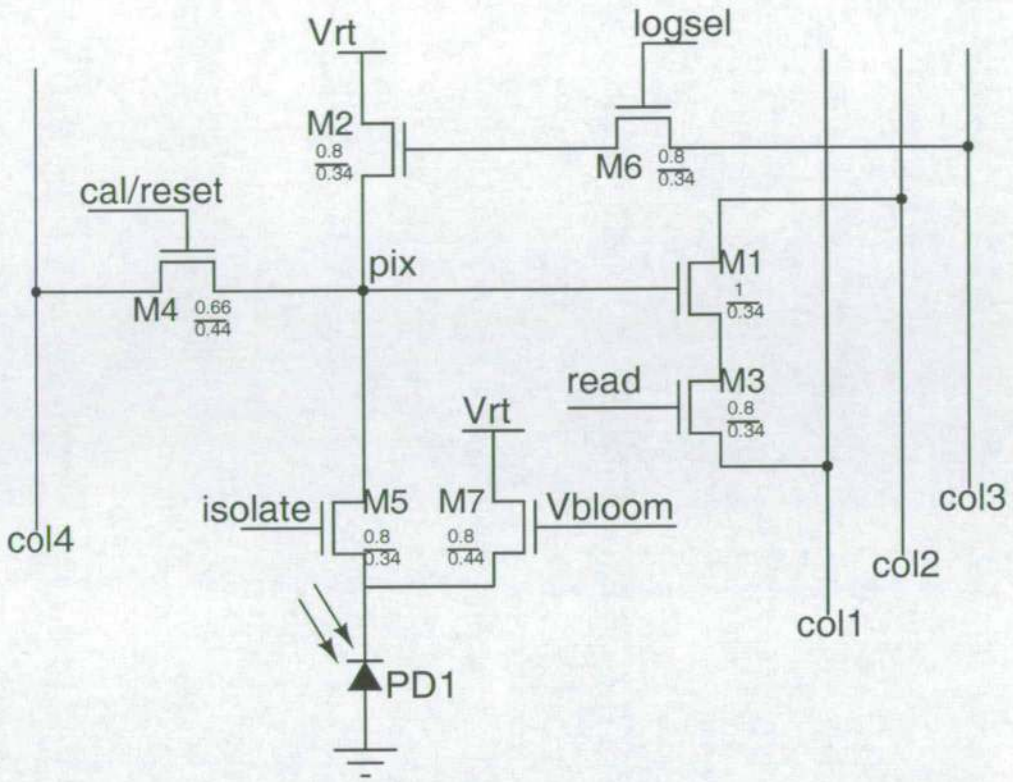


Figure 5.2: *New pixel schematic.*

integration. After the set exposure period the pixel voltage is read out via a conventional source follower: *col2* is raised to *Vrt*, a current source is connected to *col1* and *read* is pulsed high. The timing is shown in Figure 5.3

The reference voltages *Vrt* and *Vbloom* do not vary over time and are fixed at 2.7V and 1V respectively. The use of a separate supply voltage from AVDD with which to reset the pixel aims to reduce noise. *Vrt* is regulated thus should provide a more stable reset voltage than AVDD which has many other blocks connected to it. A noise free signal is not so important for *Vbloom* which is connected to the gate of M7 in every pixel in the array. Device M7 acts as an overflow channel for excess charge generated by the photodiode. Under high levels of illumination it prevents charge spilling to neighbouring pixels. For example, a single white (saturated) pixel may cause the surrounding pixels to become saturated when they shouldn't. This effect is called blooming thus M7 is often referred to as an anti-blooming device.

It can be seen from Figure 5.3 that the read signal is applied during the reset phase. This ensures the pixel is in the same state for reset as it is during the read phase. For example, consider the voltage on *col2*. It will vary during a given pixel's integration period as other rows are selected

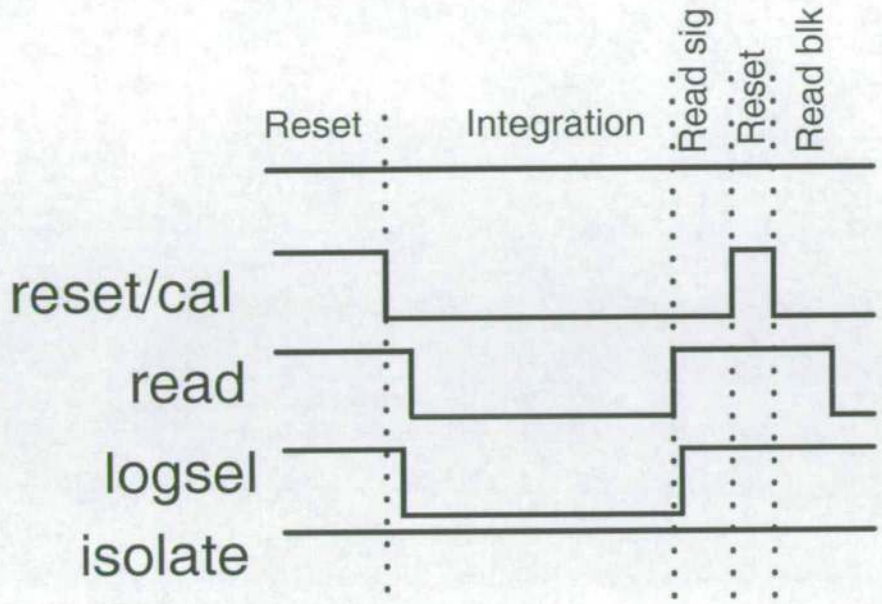


Figure 5.3: *Linear timing.*

and configured in logarithmic mode (see Chapter 5.2.2). This causes charge coupling from *col2* to the pixel via the drain-gate capacitance of M1. As *col2* is returned to *Vrt* (the value it was held at during reset) the charge coupling from the column is cancelled. In a similar fashion, charge coupling can occur from the gate of M2 to *pix*. Although M2 is OFF its gate is not driven for the full exposure period. By returning the gate of M2 to 0V such coupling is cancelled.

5.2.2 Logarithmic operation

To derive a logarithmic result the pixel is switched into the configuration shown in Figure 5.4. Devices *M1* and *M3* from Figure 5.2 become part of the amplifier, the remainder of which is situated in the column.

The amplifier is discussed further in Chapter 5.3. The non-inverting input of the amplifier is held at a reference voltage (*Vref*) which is supplied by one of two on-chip DACs (Chapter 5.5). This causes the node *pix* to settle to this voltage also.

$$Vpix = Vref + V_{offset} \tag{5.1}$$

where V_{offset} is the input offset of the amplifier and may be significant. More detail on the

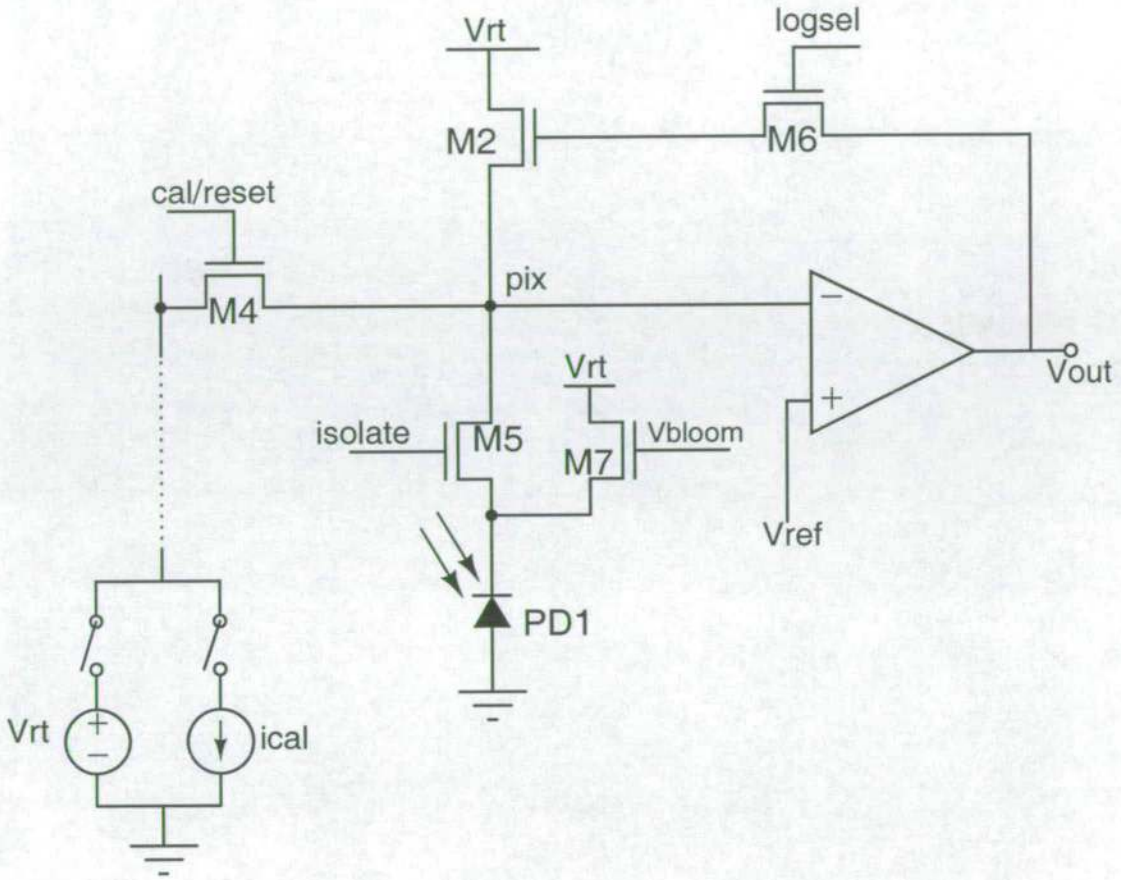


Figure 5.4: *Logarithmic arrangement.*

input offset is given in Chapter 5.3. Photo-current from *PD1* is sourced by device *M2* assuming *M5* and *M6* are ON and *M4* is OFF. The photo-current flowing through M2 sets up a gate-source voltage that is proportional to the logarithm of the photo-current.

$$Vout = Vpix + Vgs_{(M2)} \tag{5.2}$$

Device M4 can connect a current source to *pix* to provide a means of calibrating the logarithmic mode. During such operation *isolate* is lowered such that the photo-current does not corrupt the calibration. Full details of two schemes to generate a reference current are presented in Chapter 5.4. As discussed in Chapter 4.2, the majority of logarithmic pixels suffer from a poor settling time under low illumination. However, the new pixel presented displays an improved settling time with the addition of an amplifier and feedback loop. Chapter 5.3.2 presents more information on the settling performance.

5.2.3 Pixel layout

The size of the pixel greatly affects the cost of an imaging solution since the imaging array normally accounts for the majority of silicon used. However, it is desirable to make the light sensitive area of the pixel as large as possible to maximise the signal thus a tradeoff has to be made. The pixel designed uses 7 transistors but the use of an advanced process with a minimum geometry of 0.18μm enables a competitively sized layout. As mentioned, area is not saved by using smaller transistors because the 3.3V compatible devices specify a minimum geometry of 0.35μm. The area reduction is achieved with the interconnect width and spacing rules which permit a higher density of circuitry in the pixel. The pixel has a 5.6μm pitch with a 33% fill factor. An Nwell/P-substrate photodiode is used providing compatibility with a conventional CMOS process with no special layers. The layout of 2x2 pixel is shown in Figure 5.5. A layer of metal 3 was placed over as much of the circuitry as possible (excluding the photodiode) to prevent light induced currents corrupting the logarithmic calibration.

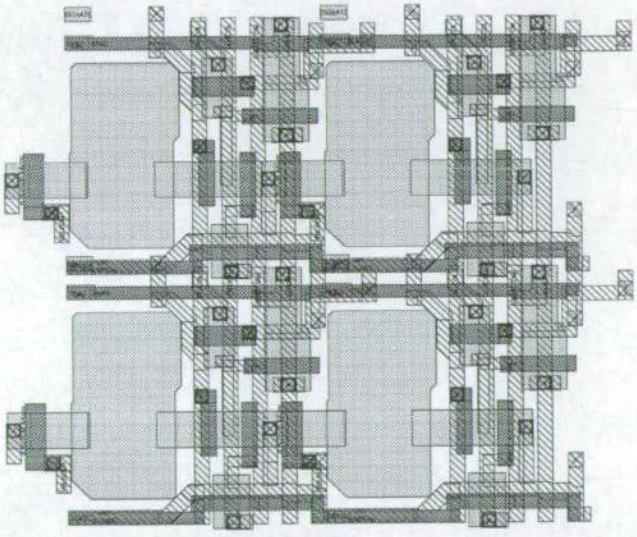


Figure 5.5: *Layout of 2x2 pixels.*

5.2.4 Pixel capacitance

The capacitance shown in Figure 5.6 was taken from a simulation of logarithmic mode.

The capacitance of the photodiode was manually inserted in parallel with the diode and was given a value of 3fF. This value was found from measured data on other test arrays at STMicroelectronics. The total pixel capacitance used in the schematic was therefore 7.2fF. The

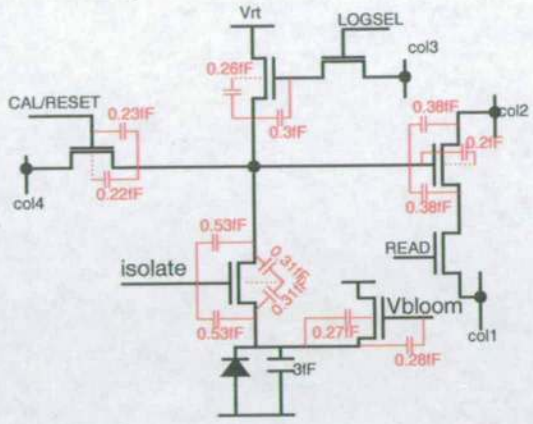


Figure 5.6: *Location of pixel capacitance.*

capacitance was verified by pulling a constant current from *pix* and applying the relationship, $c = i\frac{\delta t}{\delta v}$.

The metal parasitic capacitances associated with *pix* were extracted from the layout and found to be 0.75fF.

5.3 Logarithmic Mode

The column based amplifier used in the test chip has a folded cascode architecture and is displayed in Figure 5.7. The switches are implemented as minimum sized devices of the polarity shown. It can be seen that one side of the differential pair is situated in the pixel whilst the other is in the column. An n-type differential input stage was dictated by the pixel architecture. Due to the spacing rules for devices of a different polarity a p-type device in the pixel would mean a larger pixel.

When simulating the amplifier and pixel configuration it is important to include any column capacitance. Ccol1, Ccol2 and Ccol3 are such capacitance and result from the connection of each row of pixels to the column lines. The capacitance will increase as the number of rows increases. For the CIF array format each column was found to have an inherent capacitance of between 400fF and 500fF. The folded cascode architecture in which the dominant pole occurs at the output node lent itself to this configuration. The compensation capacitance required could be partly provided by the capacitance of *col3*.

The inverting input is formed from device M1 from Figure 5.2 where as the non-inverting input

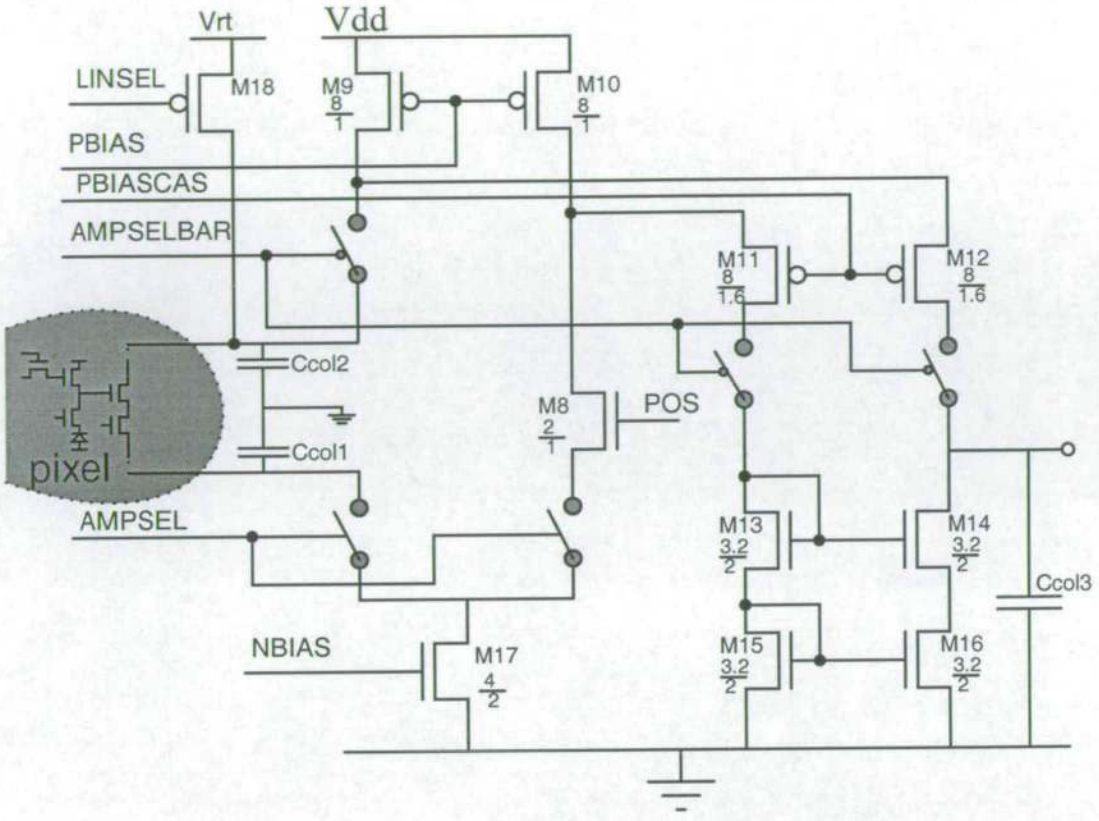


Figure 5.7: *Column based folded cascode amplifier.*

is shown as M8 in Figure 5.7. The only other device not located in the column is device M3 from the pixel which acts as a switch in both linear and logarithmic configurations. Thus, as different rows from the pixel array are read out, different devices will be connected as the inverting input of the amplifier. It is not common for amplifiers to work in such a way with care usually being taken to ensure the input pair are well matched such that the offset of the amplifier is small. In the arrangement shown a high degree of mismatch is to be expected because

1. the input pair are not of the same dimensions($\frac{2}{1}$ and $\frac{1}{0.34}$)
2. the parameters of small devices show a spread in value, particularly over a large area such as a pixel array.
3. the W and L of the input pair are small due to pixel pitch constraints.

The amplifier, although introducing extra offsets, does not reduce the performance of logarithmic mode. The calibration algorithm will remove the amplifier's offset along with others

present in the pixel. The only requirement is that all logarithmic readings from the same pixel must contain the same offset. This is achieved by using the same readout path for each reading.

Recall Equation 4.12 from Chapter 4:

$$V_{log} = \frac{A}{A+1}(Vref + V_{GS(M2)}) \tag{5.3}$$

If the gain of the amplifier is not high enough the $+1$ on the denominator can become significant thus causing a gain error across the array. The need for a high gain was also a reason for choosing the folded cascode architecture.

The amplifier was set to operate with 8μA through *M17* and 9μA through both *M9* and *M10*. This ensured that the cascode devices *M11* and *M12* would not have zero current when one side of the differential pair was off. The simple cascode n-type output was used because a low common mode output was not required.

5.3.1 Stability

When an amplifier is used with some form of feedback it is possible for the circuit to oscillate if not effectively compensated. This section provides details of the simulations performed on the logarithmic arrangement with fedback amplifier to ensure stability.*Gain Margin* and *Phase Margin* are two measures of stability that can be applied to the circuit. In order to avoid oscillations the phase response round a feedback loop must be less than 180^o for gains greater than 1. The *Gain Margin*, GM,is the amount of additional gain permitted before the system becomes unstable. The *Phase Margin*, PM, is the amount of phase lag permitted before the system becomes unstable and is the figure of merit used most commonly in this correspondence.

The amplifier was connected as it would be in the test chip (i.e. device M2 remained in the feedback path). This provided more realistic results as the dc operating levels are set as they would be in the final version. It was required to break the feedback path as shown in Figure 5.8 to extract the open loop characteristics.

The resistor and capacitor allow the correct dc operating point to be achieved but stop any AC signal being passed back into the inverting input of the amplifier. It is crucial that the amplifier is stable under its conditions of operation.

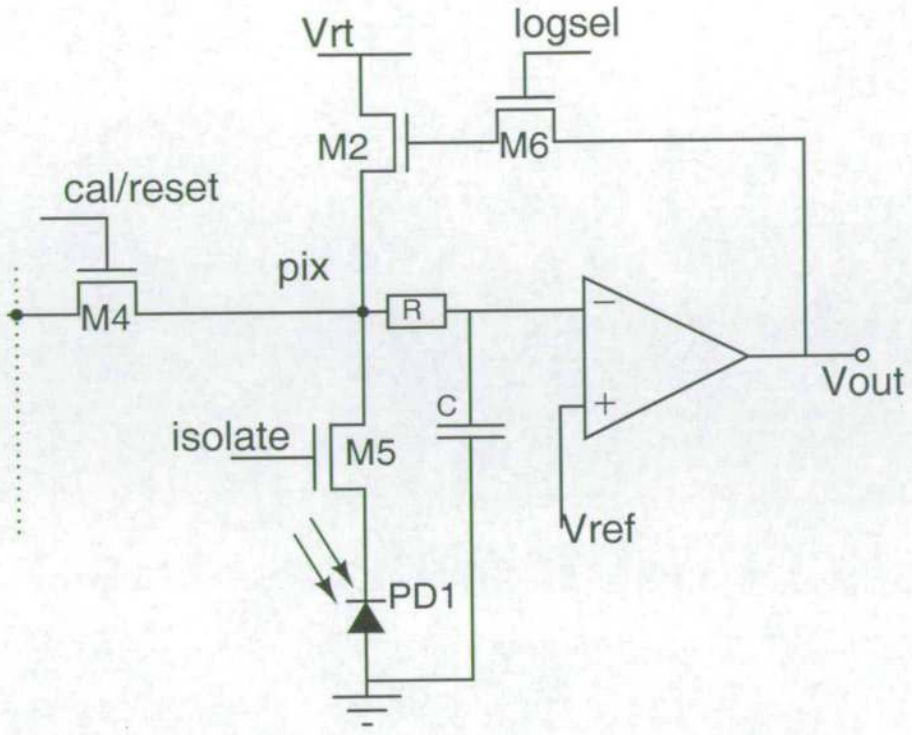


Figure 5.8: *AC analysis schematic.*

As mentioned already the dominant pole occurs at the output of the amplifier and is given by

$$pole = -\frac{1}{R_O C_{col3}} \tag{5.4}$$

where R_O is the output resistance of the amplifier and is given by the parallel combination of $g_{m14}r_{d14}r_{d16}$ and $g_{m12}r_{d12}(r_{d8}//rd10)$.

An AC signal was injected into the non-inverting terminal of the amplifier's of Figure 5.8 and the amplifier's open loop response found by probing the output node. The amplifier's gain and phase response is plotted in Figure 5.9 for three different photocurrents.

The amplifier exhibits an open loop gain of around 90dB and the PM was measured to be around 75^o which should ensure stability. This result was achieved with a capacitance of 1.5pF at the output of the amplifier. This is easily achieved by a combination of the column capacitance due to all the pixel connections and the addition of extra capacitance in the column readout. The column capacitance can be broken down as follows.

Fixed

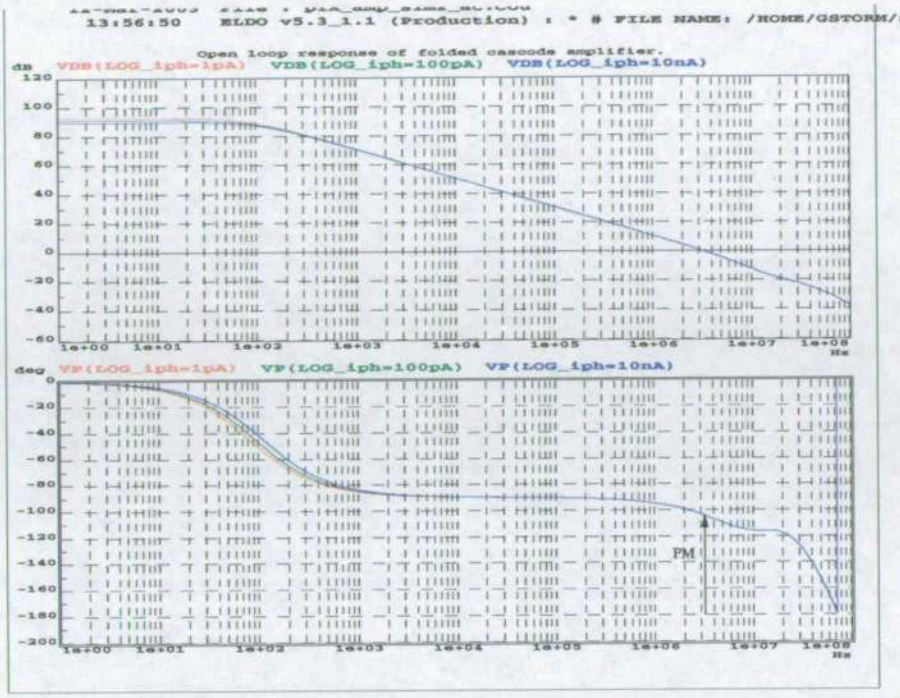


Figure 5.9: *Open loop response of folded cascode amplifier.*

C_{drain} of M6	1.17fF/row	
Therefore, 288 rows gives		337fF
C_{gate} of source follower device in column		40fF
C_{output} of column amplifier		9fF
Parasitic		
C_{drain} of M6	0.23fF/row	
Therefore, 288 rows gives		66fF
Total inherent column capacitance		**452fF**

Extra capacitance required = 1.5pF - 0.452 = 1.048pF

The source follower device in the column buffers the logarithmic signal. The readout path is shown in Figures 5.21 and 5.20.

The feedback from the output of the amplifier to the inverting input forms a source follower where the current flowing in device M2 is the photocurrent. Since the photocurrent is dependent on the incident light, the response of the source follower changes with the light intensity.

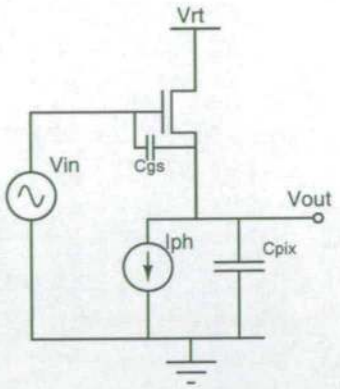


Figure 5.10: *Source follower schematic.*

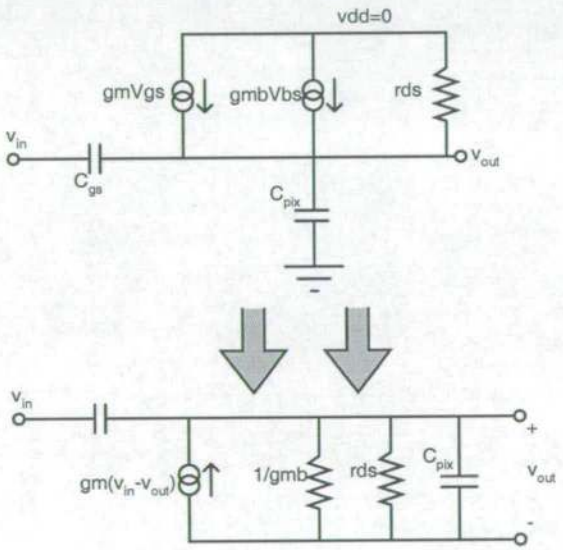


Figure 5.11: *Small signal model for Figure 5.10.*

The AC response is derived by use of the small signal models shown in Figure 5.11. In such a model all static supplies are seen as ground to ac signals. Applying Kirchoff's current law at the output node gives:

$$(v_{in} - v_{out})sC_{gs} = -gm(v_{in} - v_{out}) + v_{out}gmb + \frac{v_{out}}{rds} + v_{out}sC_{pix} \tag{5.5}$$

and rearranging produces:

$$\frac{v_{out}}{v_{in}} = \frac{sC_{gs} + gm}{gm + gmb + gds + s(C_{gs} + C_{pix})} \tag{5.6}$$

Thus there is a pole at $-\frac{-(gm+gmb+gds)}{(C_{gs}+C_{pix})}$ and a zero at $\frac{-gm}{C_{gs}}$. The pole occurs at a lower fre-

quency because the pixel capacitance is much larger than the gate-source capacitance of *M2*. The source follower's AC response is shown in Figure 5.12. The gain and phase response for three different photo-currents is plotted. As predicted, an increase in photo-current increases the frequency at which the pole and zero occur.

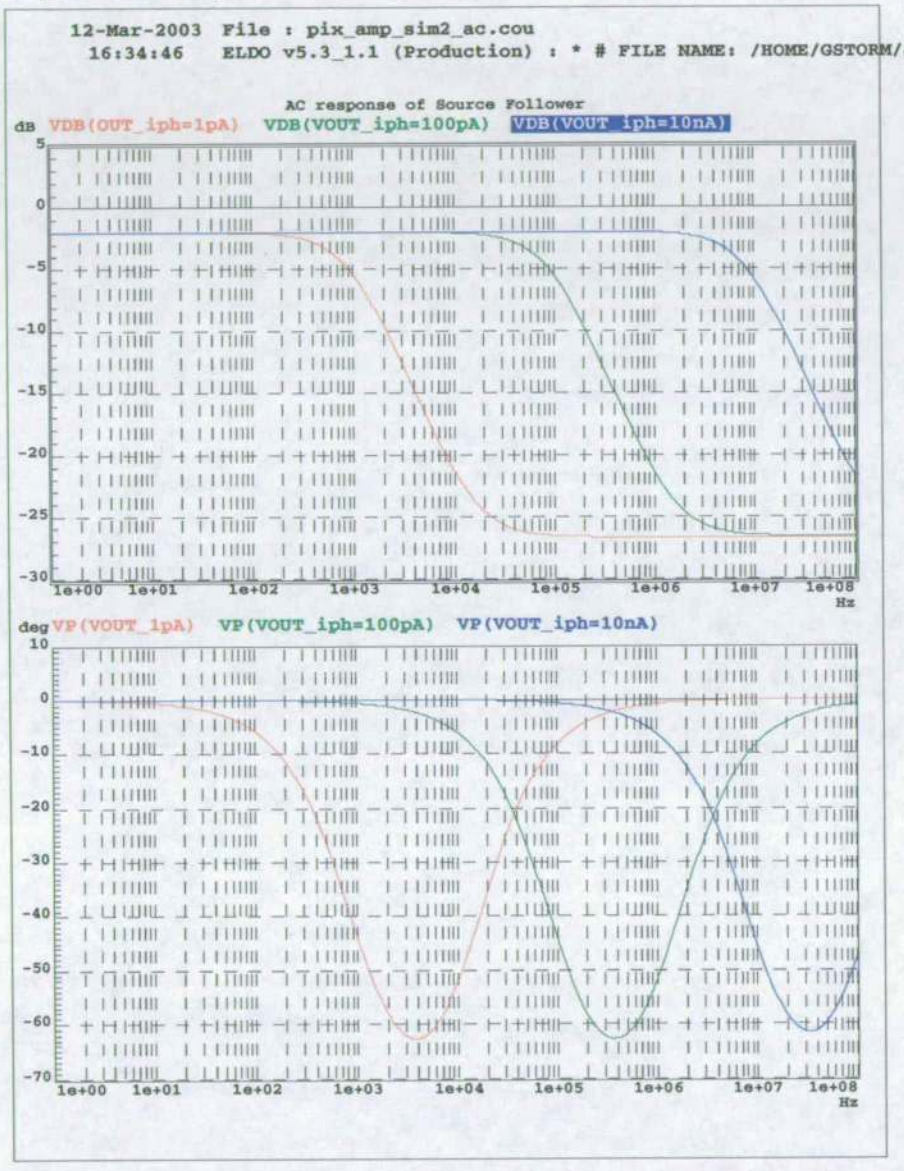


Figure 5.12: *AC response of source follower for different column calibration currents.*

The source follower is a common block in CMOS circuits but usually the current flowing (directly affecting the transconductance, gm) means the pole and zero are located at a frequency outwith the operation of the system. In this application, the current flowing through the source follower device is the photo-current over which the designer does not have control. Figure 5.13 shows the effect that *Cpix* has on the frequency response(iph=50pA). Increasing the capaci-

tance cause a greater phase shift because the distance between the pole and zero is increased. This is an important result as the closed loop response will be the addition of the response of the amplifier and the source follower. It is thus desirable to minimise the pixel capacitance.

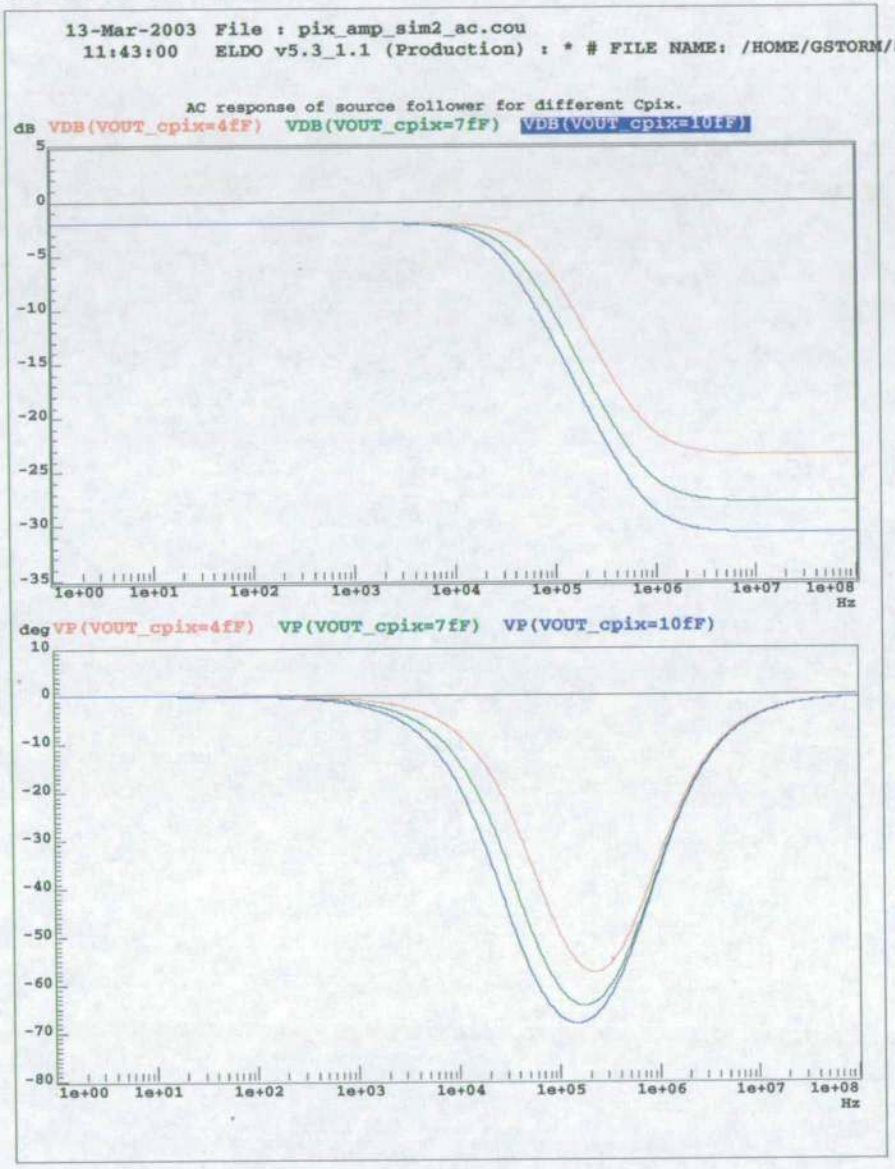


Figure 5.13: *AC response of source follower for different C_{pix}.*

The stability of the logarithmic arrangement must also be ensured when either of the on-chip reference generation schemes are enabled. The details of the calibration schemes are presented fully in Chapter 5.4 but mentioned here for completeness.

The first scheme connects a column current source to the pixel by turning on device *M4*. The *isolate* signal to the pixel is also lowered to prevent the photo-current influencing the reference.

As shown in Figure 5.13, the pixel capacitance greatly influences the stability of the system. The addition of the large column capacitance to the pixel will cause the system to become unstable for all but very high reference currents. To prevent oscillation extra capacitance was situated at the output of the amplifier and made selectable for when the column current sources are connected. The folded cascode arrangement made it simple to add the extra compensation. In addition to slowing down the amplifier, the calibration current from the current sources was only programmable at fairly high levels.

The second calibration scheme uses a voltage ramp to generate a reference current. Under the conditions discussed in Chapter 5.4 (photodiode isolated) the pixel capacitance is greatly reduced and the stability ensured.

The combined response of the amplifier and the source-follower is shown in Figure 5.14. The gain-bandwidth and PM are both influenced by the photo-current. The pole and zero of the source-follower are clearly visible in the phase response and the PM is just above 20^o in places.

The low PM will cause the amplifier to overshoot when it is first connected in the logarithmic arrangement. The settling time is aided by the inclusion of a voltage ramp to absorb the amplifier's overshoot. Further detail is provided in the following section on Settling

5.3.2 Settling time

When switching the pixel into logarithmic mode the overshoot of the amplifier can cause long settling times for low photo-currents. Due to the feedback in the pixel, the node *pix* will attempt to follow the output of the amplifier to maintain a constant gate-source voltage on *M2*. *pix* can charge up quickly with excess current being supplied through device M2 but can only discharge at a rate governed by the photo-current. Thus at low illumination *pix* will increase fast then take a long time to discharge to its settling point. This is shown in Figure 5.15(a) which plots the transient response of the *pix* node and the output node for a photo-current of 100pA. The two traces use different threshold voltages of *M1* from the pixel. The threshold voltages were set to $\pm$200mV of the nominal value to reflect the expected worse case process variation. Regardless of whether the pixel was precharged above or below its settling value the majority of the settling time comes from the discharge of the pixel node.

The switch to logarithmic mode was therefore altered in the following way to eliminate the problem of overshoot.

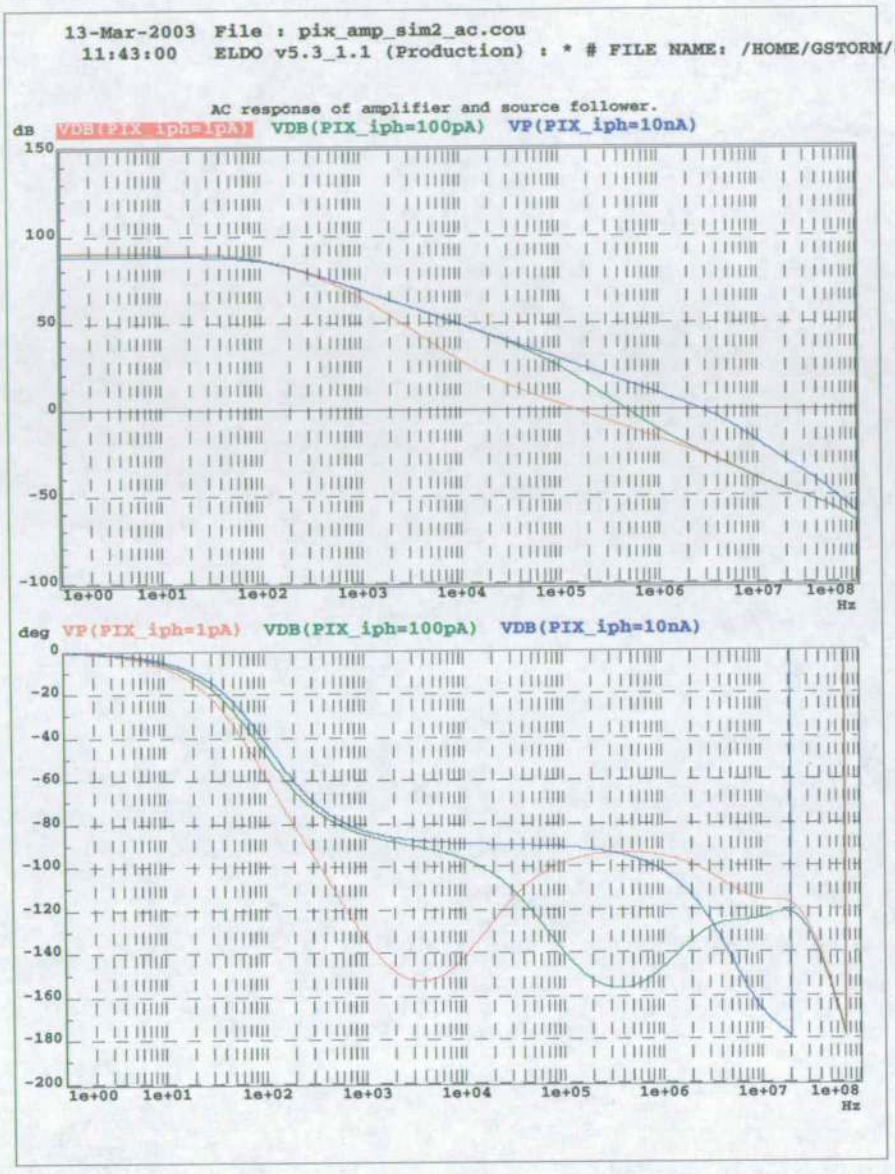


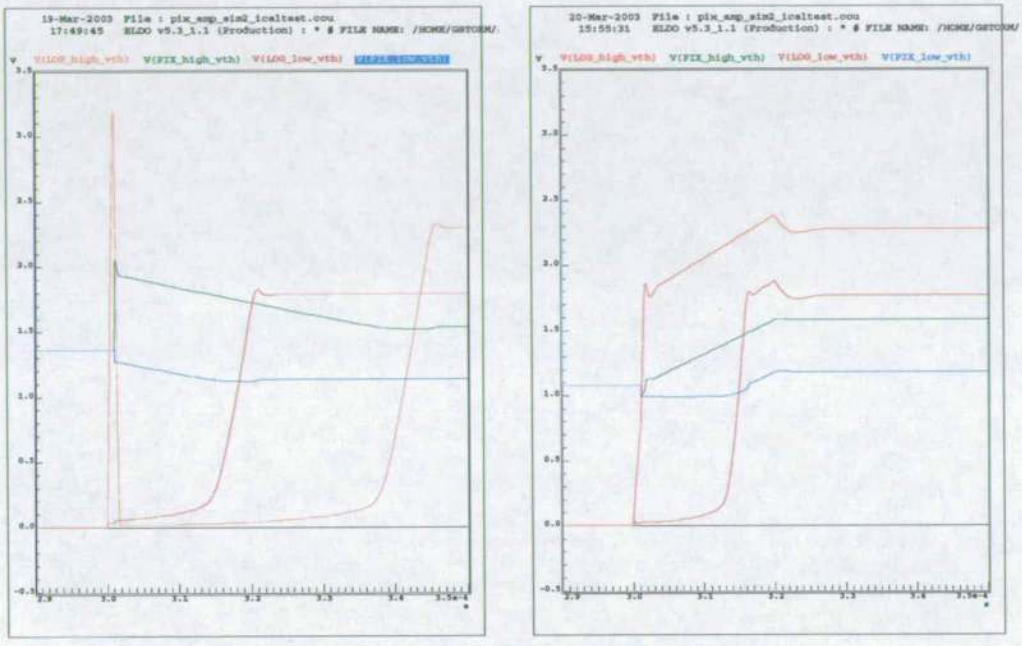
Figure 5.14: *AC response of amplifier and source follower for different photocurrents.*

- *Vref* is set a few hundred mV below its final value
- *logsel* is low (*M6* OFF)
- *pix* is precharged via *M4* to a voltage such that *Vout* is low. The amplifier is now operating in open loop configuration.
- *M4* is turned OFF and *M6* ON.
- *Vref* ramps UP to its final value

The ramping of *Vref* serves to absorb the overshoot caused by the amplifier. As *Vref* increases,

pix does not have to discharge to its settling point. The settling point moves up to meet *Vpix*.

Figure 5.15(b) shows the transient response for the logarithmic mode when an initial voltage ramp is applied. *Vref* is held at 1V until 300us then linearly rises to 1.5V after 320us and remains at 1.5V for the remainder of logarithmic mode.



(a) (b)

Figure 5.15: *Transient response of log arrangement:*
(a) No ramping used(iph=100pA)
(b) Ramping used (iph=10pA).

The oscillations of the output node are just visible as the dc level increases. The photo-current was set to 10pA for the case where the ramping was used. This is ten times less than that used in Figure 5.15(a) but a superior settling time is still achieved.

If a pixel saturates during the linear exposure period then logarithmic data will be substituted during the readout. It is therefore crucial that the logarithmic data for a saturated pixel is valid. In other words, the logarithmic mode must be settled when a reading is made. Unwanted image artifacts would result if a pixel had saturated during the linear exposure and the logarithmic mode were not given enough settling time.

The crossover point at which logarithmic data is substituted for linear needs to be set at a high enough illumination level such that the logarithmic architecture has had time to settle. The

Linear Integration time	Lowest current at which logarithmic mode must settle
33ms	227fA
10ms	750fA
5ms	1.5pA
1ms	7.5pA
500μs	15pA

Table 5.1: *Logarithmic settling requirements for various linear exposures.*

linear exposure period directly sets the lowest photo-current that the logarithmic mode must handle. Table 5.1 gives the photo-currents for five different integration times. The values are derived from Equation 5.7 which relates current, i, capacitance, C and rate of change of voltage, $\frac{\delta V}{\delta t}$.

$$i \approx C\frac{\delta V}{\delta t} \tag{5.7}$$

δV is taken as 1V which is slightly pessimistic (if Vrt is set to 2.7V then there should be nearer 1.5V swing available before the current source connected to the pixel source follower reaches its minimum operating voltage) and C was set to 7.5fF (from Chapter 5.2.4).

33ms is taken as the longest exposure time as this represents the permitted frame time if the sensor is to operate at 30 frames/sec. The logarithmic settling time was set to 50μs as this is the time taken for a single ADC cycle. The logarithmic data is converted by the same ADC as the linear thus will have a single conversion period to settle during the linear conversion. The minimum photo-current at which the logarithmic mode could settle to within 1mV of its final value was found to be between 750fA and 900fA. This result imposes a maximum linear exposure period of around 10ms.

Based on the results of Chapter 3 it was stated that linear-logarithmic combination does not reduce performance at low illumination levels. However, for a real-time sensor with parameters as shown in Table 5.1 the settling performance of the logarithmic mode will determine the longest permissible integration time.

The large offsets (200mV) that could occur between the inverting and non-inverting terminals of the amplifier dictate the range that the reference voltage must ramp. Simulation data was used to

estimate the ramp range required. Based on previous measurements from devices produced by STMicroelectronics a threshold voltage variation of up to ± 200mV was used in the simulation. Table 5.2 shows the settling voltages for node *pix* at different corner conditions[1] and with the variation of the threshold voltage of *M1*. The reference voltage, Vref, was set to 1.5V to ensure the logarithmic output had enough headroom under all conditions. This was determined by the highest logarithmic output which will occur when the ampifier offset, photo-current and threshold voltage of the logarithmic device, *M2*, are all at their maximum values. It is due to the small device dimensions that such large Vth variances occur. This prevented logarithmic devices being stacked to increase the sensitivity.

	Corner condition				
Vth variation	SpSn	FpSn	Typ	SpFn	FpFn
-200mV	1.0868		1.133	1.1812	
+0mV	1.2944		1.341	1.388	
+200mV	1.4868		1.533	1.5812	

Table 5.2: *Pixel voltage for varying process parameters.*

To determine the range and starting voltage for the ramp the highest and lowest settling levels were extracted from Table 5.2. As discussed, the amplifier will firstly be held in open loop configuration at which time the output must be low. Vref must then be ramped high enough to ensure all pixels benefit from the ramp. The extremes were found to occur under SpSn:-200mV and FpFn:+200mV conditions. As the maximum settling voltage is 80mV above the reference voltage it follows that the precharge voltage for the pixel must be more than 80mV above the starting point for Vref. If the starting voltage of the ramp is 1V then the precharge voltage of the pixel must be greater than 1.08V.

The range of the ramp is found by subtracting the lowest settling voltage for pix from the reference voltage:

$$ramprange = Vref - Vpix(min) = 1.5 - 1.08 = 420mV \tag{5.8}$$

Example timings for logarithmic mode are provided in Figure 5.16.

[1]Sp: Slow PMOS device parameters, Sn: Slow NMOS device parameters, Fp: Fast PMOS device parameters, Fn: Fast NMOS device parameters

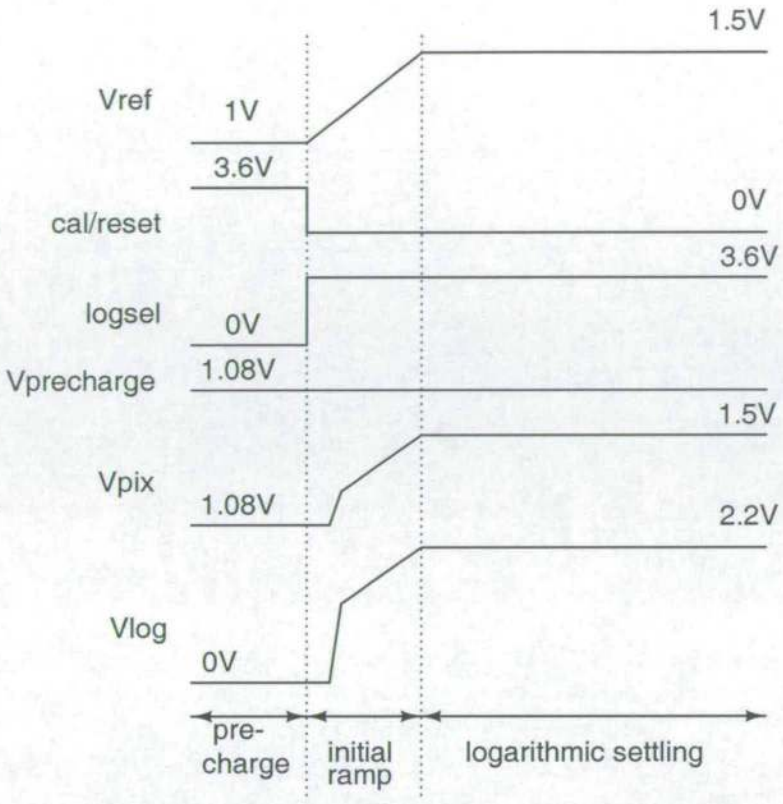


Figure 5.16: *Logarithmic timing and waveforms.*

5.4 Logarithmic Calibration

The lack of a reset voltage prevents any form of conventional double sampling to reduce FPN in logarithmic mode. Chapter 3 presented calibration results for a CMOS sensor configured in logarithmic mode. It detailed how offset and two-parameter algorithms could be used to reduce FPN. Both algorithms relied on placing the pixel into a reference state which was achieved by uniformly illuminating the device. This is not possible in a real-time imager. This Chapter presents two on-chip schemes to induce a reference current through device *M2* from the pixel. The first utilises a current source positioned in each column and is accessed by the corresponding pixel of a given row. The column current sources can be made large and thus well matched but the associated column capacitance will limit the settling time. Since the calibration is to be carried out with sub-threshold currents there will be a trade-off between calibration current and settling time. The second scheme provides a novel means of deriving a reference current and overcomes the settling issues of the column architecture. The method is directly usable with the logarithmic architecture used. It involves ramping the reference voltage to the pixel to induce a constant current and is similar to that presented in Chapter 5.3.2.

5.4.1 Column Calibration

A simple current mirror is shown in Figure 5.17 connected to a column of the pixel array. The current source is connected to the pixel by asserting *cal/reset* (for a particular row) along with *CALENABLE*. The photodiode is isolated from the calibration process by turning OFF device *M5* in the pixel. The calibration current is pulled through device *M2*which in turn sets up the logarithmic output via its gate-source voltage. As shown in Chapter 5.3.1 the current in this configuration needs to be fairly high to ensure the system is stable. Lower calibration currents are also not desirable due to the increased settling time.

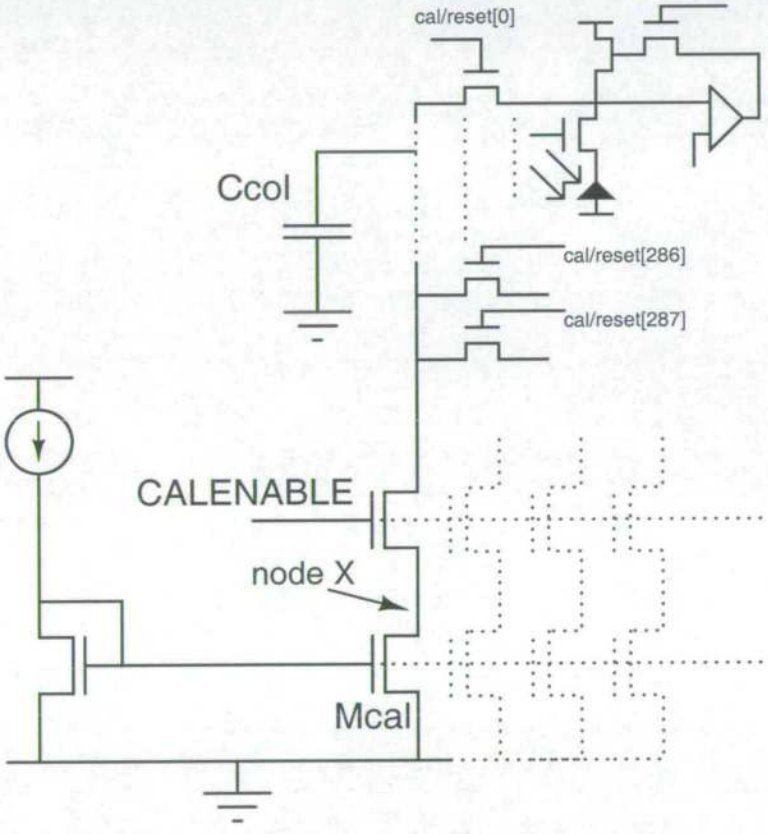


Figure 5.17: *Simple current mirror for column calibration.*

The current that flows in each column needs to be well matched across the array for the calibration process to be effective. If an array of NMOS devices are used to provide the reference current a high degree of mismatch can result if small devices are used. The gate-source voltage will be the same for each device but the current that flows is highly dependent on threshold voltage which can vary considerably.

Methods to cancel this offset were investigated but were found to add too much complica-

tion [86]. Taillefer and Wang [87] use a precharge phase to adjust the gate source voltage on one side of the current mirror such that the currents match. This solution suffered from the problem that each column would need to be 'calibrated' itself thus taking too long.

It was decided to use large devices in the column to improve the matching. The results from Section 3.3.2 were used to set the required performance of the current mirror. The FPN was reduced to between 2 and 3% standard deviation across a uniformly illuminated image. The column current sources were thus required to achieve matching superior than 2%. To achieve such matching the NMOS device dimensions were calculated from foundry supplied data. The devices were sized to $\frac{W}{L} = \frac{9.6}{14}$(in μm).

The configuration shown in Figure 5.17 was found to suffer from capacitive coupling which affected the bias voltage and corrupted the calibration current. When *CALENABLE* is raised node *X* will jump from a very small voltage up to a value close to the reference voltage applied to the non-inverting terminal of the amplifier. This rise in voltage in the column will couple to the gate of device *Mcal* via its gate to drain capacitance. The amount by which the gate voltage moves is given by the ratio of C_{gd} to C_{gate}. To a first approximation for a single column when node *X* jumps by 1V:

$$\Delta V_{gate} = \frac{C_{gd}}{C_{gate} + C_{gd}} \Delta V_{nodeX} \tag{5.9}$$

$$= \frac{3fF}{0.3pF + 3fF} = 0.01V \tag{5.10}$$

The gate capacitance will actually be 360 times larger as all the gates are connected together but this will be cancelled by the gate-drain capacitance of each column. Thus if the voltage on node *X* varies by 1V, the voltage on the gate of *Mcal* will vary by 10mV. This is obviously too high and will cause a change in calibration current well in excess of the 2% required. Due to the large capacitance of all the *Mcal* devices connected(100pF), the recovery time from such coupling creates a large settling time.

$$\delta t = \frac{C}{I}\delta V = \frac{100^{-12}10e^{-3}}{10e^{-9}} \approx 100\mu s \tag{5.11}$$

Thus Equation 5.11 predicts a settling time of around 100μs for a change in gate bias voltage of

10mV. Extra capacitance could be added to the gate of device *Mcal* to reduce the gate voltage variation but the size required would be impractical. For example a factor of 10 improvement would require the capacitance to be increased to 3pF.

For these reasons the circuit shown in Figure 5.18 was implemented instead. It shows the addition of a dummy current path such that the current flowing in *Mcal* is continuous, even when calibration is not being performed. In addition a cascode device is added to reduce the voltage swing on node *X* thus lowering the possible variation in the bias voltage.

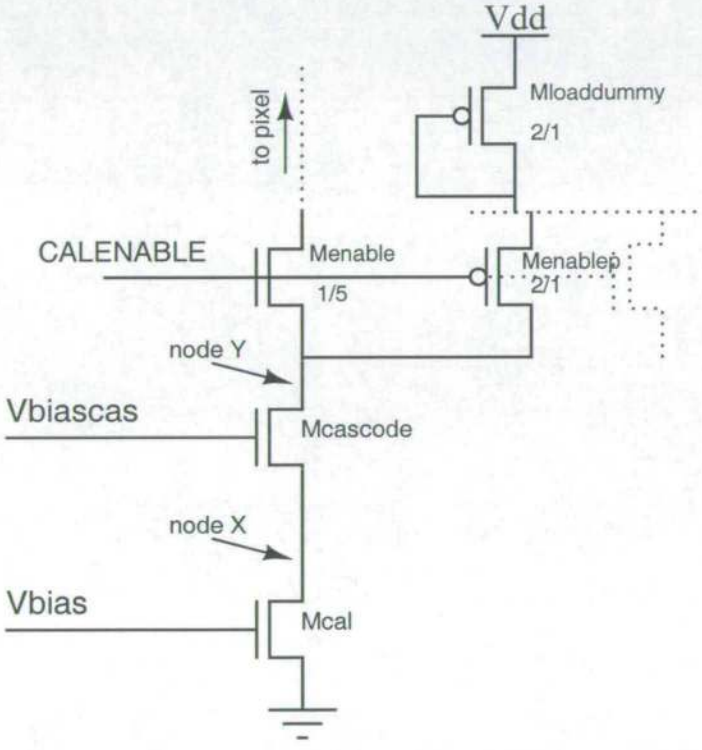


Figure 5.18: *Enhanced current mirror for column calibration.*

It can be seen from Figure 5.18 that node *Y* will be exposed to any voltage swing on the column. There will be the same coupling effect as before but the gate voltage of Mcascode does not have the same influence on the current flowing as that of Mcal. The cascode thus serves to shield node *X* from large voltage variations. The dummy current path is connected when *CALENABLE* is low (i.e no calibration being performed). A PMOS device is turned on which supplies the calibration current for all columns from a single diode connected device. Thus Mcal and Mcascode always have current flowing through them. This reduces the voltage swing on node *Y* and therefore node *X* so the coupling problem is kept to a minimum. Such a scheme will increase the power consumption but the current matching and thus calibration

effectiveness was considered more important.

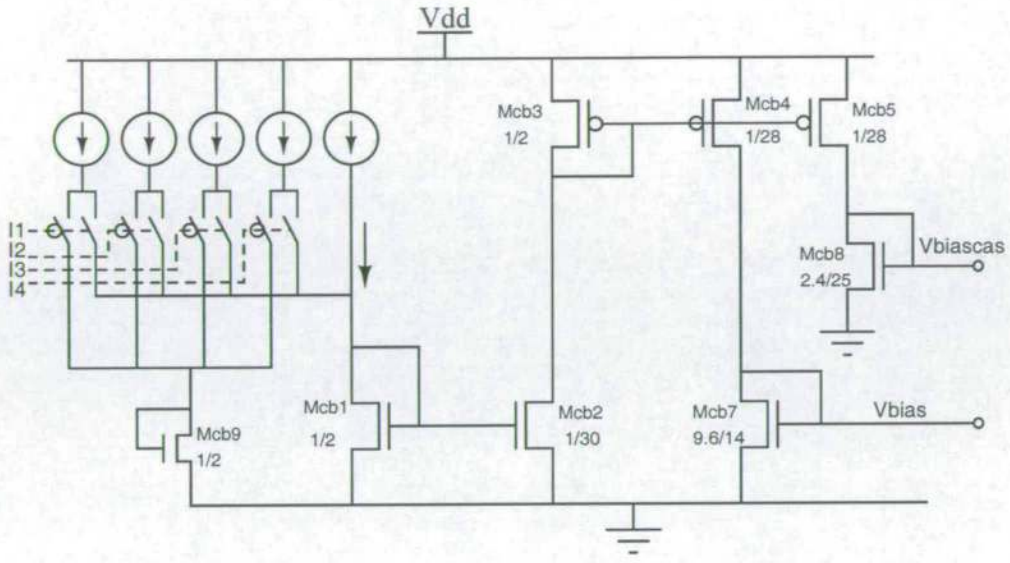


Figure 5.19: *Bias circuitry for column current source.*

The bias voltages *Vbias* and *Vbiascas* from Figure 5.18 are derived from a simple current mirror as shown in Figure 5.19. The input current is selectable with any combination of the 4 current sources possible. *I1*, *I2* and *I3* will each provide 1μA to the input current which translates to around 2nA in the calibration current. *I4* is larger and provides an extra 20nA calibration current. The calibration current is thus programmable between 2nA and 28nA. This very basic current mirror is not accurate in terms of the absolute calibration current generated. However, this is not a problem as it is only necessary that all the pixels are calibrated with the same current, not a specific current.

5.4.2 Ramp calibration

A novel method of generating a matched current across the array has been devised and implemented on the test device. The scheme permits greatly reduced calibration currents to be derived without the settling time problems associated with the column current source approach.

A constant current can be generated if there is a constant rate of change of voltage across a constant capacitance. Recalling Equation 5.7 and knowing the capacitance, a voltage ramp can be programmed to produce a constant current. This technique can be applied to the circuit of Figure 5.4 without modification. Devices *M4* and *M5* are turned OFF and the reference voltage is linearly ramped. The voltage on *pix* will track the reference voltage thus inducing a current

due to the capacitance on *pix*. The current must be supplied by device *M2* thus it is brought into a reference state for calibration. The capacitance seen at the *pix* node will be composed of:

- drain capacitance of *M5*
- drain capacitance of *M4*
- gate capacitance of *M1* (inverting input of amplifier)
- source capacitance of *M2*

and will be extremely small in comparison to the capacitance of a column access line. The capacitance was estimated to be 2.8fF from Figure 5.6. The ramp is generated by one of two on-chip DACs. Assuming the output of the DAC that connects to the pixel is 0.8mV per code and that the ramp operates at a speed of 24MHz the ramp rate is given by:

$$\frac{\delta V}{\delta t} = \frac{0.8e^{-3}}{\frac{1}{24e^{6}}} \tag{5.12}$$

Thus the current that will be generated is given by:

$$i = C\frac{\delta V}{\delta t} = 2.8e^{-15}\frac{0.8e^{-3}}{\frac{1}{24e^{6}}} = 53pA \tag{5.13}$$

During ramp calibration the output must be sampled when the reference voltage reaches the settling level used in normal logarithmic mode. This ensures that the source-bulk voltage of device *M2* is the same for both samples.

5.5 Readout

Both linear and logarithmic signals are sampled onto the same capacitors in the column and then processed by the ADC. Figure 5.20 shows how the different signals are connected to the sample and hold circuitry in the column. Dependant on which mode the pixel is operating, the appropriate select switch will be enabled. Figure 5.21 shows the remainder of the readout chain in each column. The sample and hold capacitors form the input to a comparator which controls what code is written to one of two banks of SRAM.

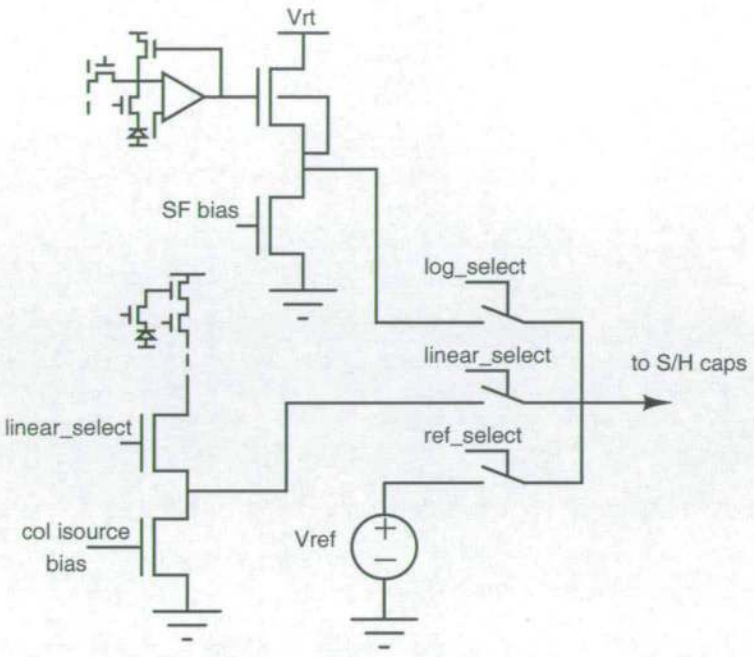


Figure 5.20: *Linear and logarithmic paths to the ADC.*

In the case of linear operation, the pixel voltage after the set exposure period is readout via the pixel source-follower and sampled onto Csig. The *ramp* and *offset* voltages are held at ground potential during the sampling period. The pixel is then reset and released and read for a second time but sampled onto Cblk instead. The offset voltage is now applied to the bottom plate of Cblk and ensures the output of the comparator is high by shifting the voltage at the non-inverting input to a higher voltage than the inverting side. The ramp then begins ramping on the bottom plate of Csig. This causes the inverting input to the comparator to shift toward the non-inverting voltage. When the two inputs become equal the current value of a counter is latched

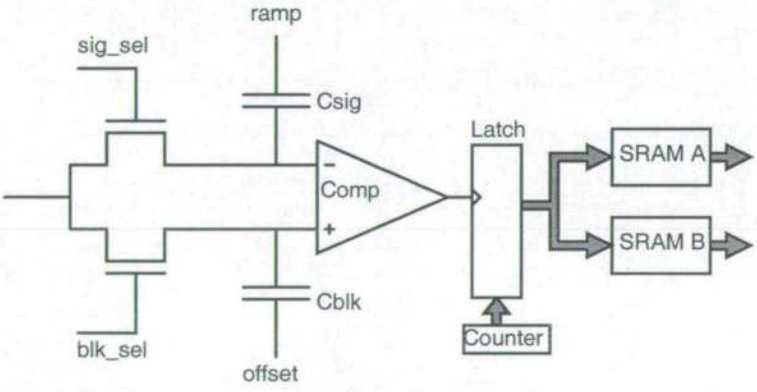


Figure 5.21: *S/H column capacitors and ADC.*

into one of the SRAM banks. During the following ADC cycle the SRAM is read out. Due to the NMOS switches prior to the sample and hold capacitors and the limited range achievable from the DAC the DC level of the logarithmic voltage was lowered. A source follower in the column was used to accomplish this. The column source follower device was situated in its own well so its bulk could be shorted to its source. This minimised the reduction in signal due to the body effect. The column source follower also provides buffering between the column and the pixel. When one of the sample and hold capacitors is selected, charge sharing occurs between the column and the capacitor. This step in voltage on the output would unsettle the logarithmic result at the pixel and undo the work done by the ramp to permit a fast settling time.

5.6 DAC

A schematic representation of the DAC is provided in Figure 5.22.

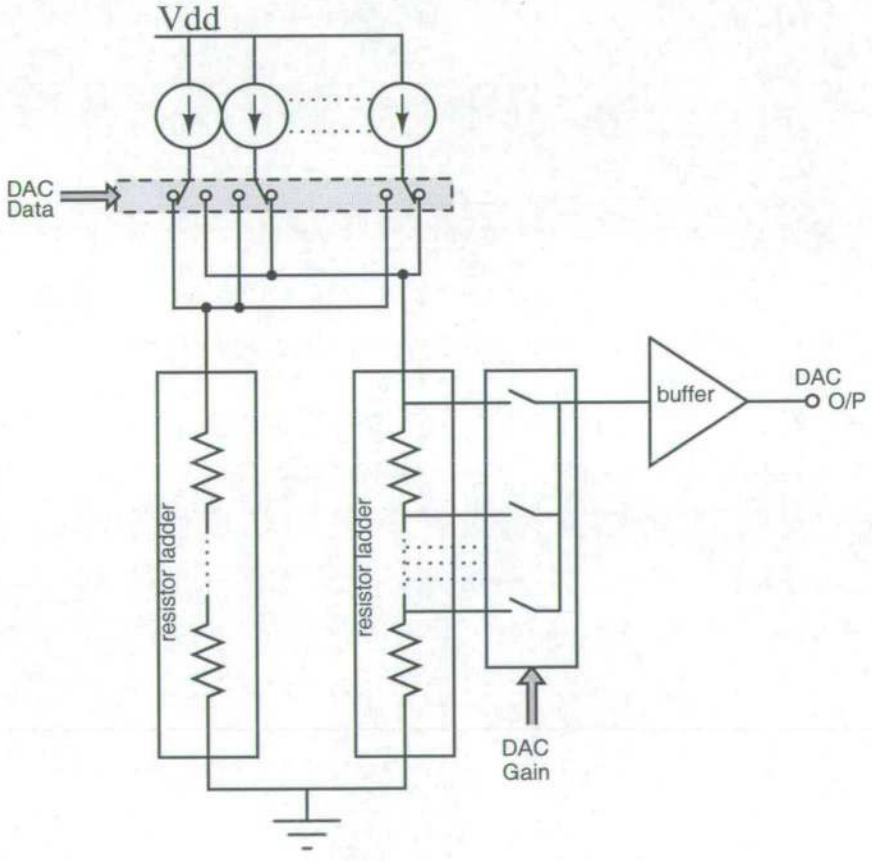


Figure 5.22: *DAC schematic.*

It shows a collection of current sources which can be switched between two matched resistive

ladders, of which the tapped output of one is passed to the output. An offset is also output from the DAC and is derived from a resistor ladder in the same way as the ramp. The offset is a set voltage level up to a few hundred mV and does not ramp.

5.7 Y-decoder

The new combined linear-logarithmic arrangement required the design of a new Y-decoder. A simple multiplexer has been implemented for each horizontal control signal so that maximum flexibility is provided for testing. A control signal has an active and a held state. When a row is selected, the active state is passed to all the pixels of that row and the held state applied to the remainder of the array. A block diagram of the Y-decoder is shown in Figure 5.23.

read, *logsel*, *isolate* and *reset/cal* all require a voltage in excess of the normal supply voltage of 3.3V so that the devices they drive can be fully turned on. The maximum reset voltage of the pixel is 2.7 V. Applying 3.3V to the gate of an NMOS may not completely turn the device fully on to pass the 2.7V. The high drive voltage was generated off-chip on the test board and was set to a default of 3.6V. Level shifters are used in the Y-decoder to make the transition from the digital operating voltage of 1.8V up to 3.6V.

5.8 Timing

The frame rate is determined by the time taken to readout the linear and logarithmic data from an addressed row. When a row is selected for readout the linear signal and reset value are first sampled and held in the column capacitors in preparation for the first ADC cycle. When the conversion is complete the logarithmic signal is then sampled and held in one of the sample and hold capacitors. The raw logarithmic value can be readout by sampling a reference voltage on the second sample and hold capacitor then performing the ADC conversion. The timing is illustrated in Figure 5.24. The time required for each part of the readout is denoted by *T1*, *T2* and *T3*.

T1 is the total time require to sample the linear signal and reset level from the pixel. This is partly determined by pixel's source follower current. *T1* is set to 10μs. The ADC cycle time is set by the slope of the ramp supplied by one of the on-chip DACs. The ADC conversion time *T2* was set to 50μs. *T3* includes the sample and hold time of the logarithmic signal in addition

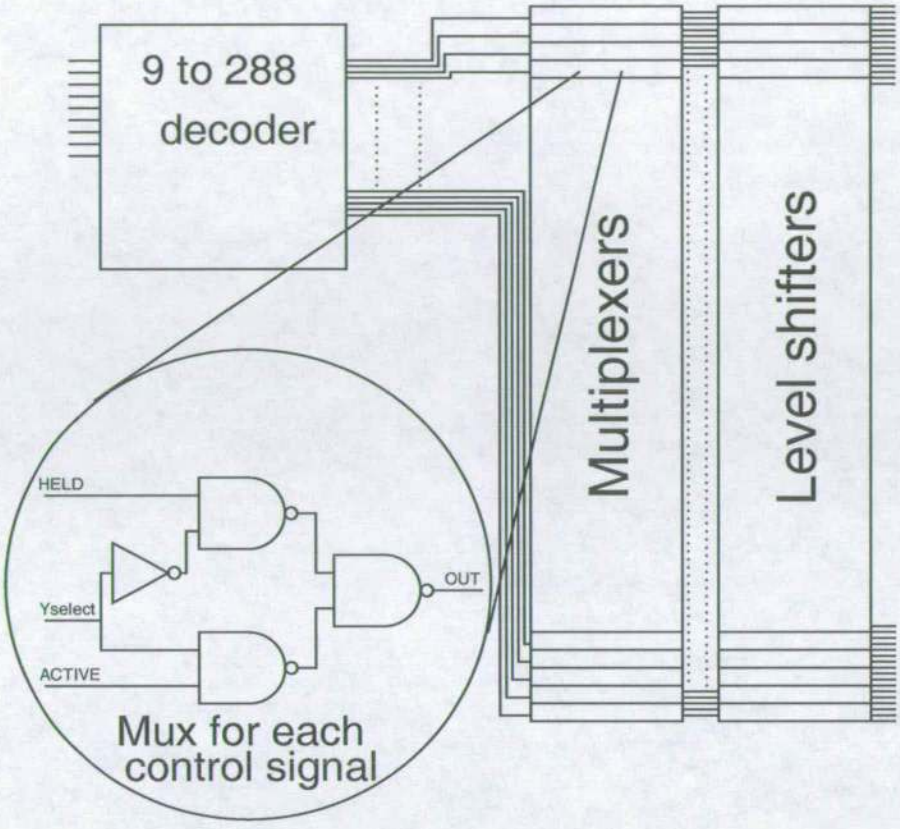


Figure 5.23: *Ydecoder block diagram.*

to the ADC cycle thus will be slightly longer than $50\mu s$. If $T3$ is assumed to be $55\mu s$ the total readout time for an addressed row is $T_{row} = T1 + T2 + T3 = 10 + 50 + 55 = 115\mu s$. For an array with 288 rows the maximum frame rate is 30fps.

Due to the high level of FPN in a raw logarithmic image, the readout scheme presented in

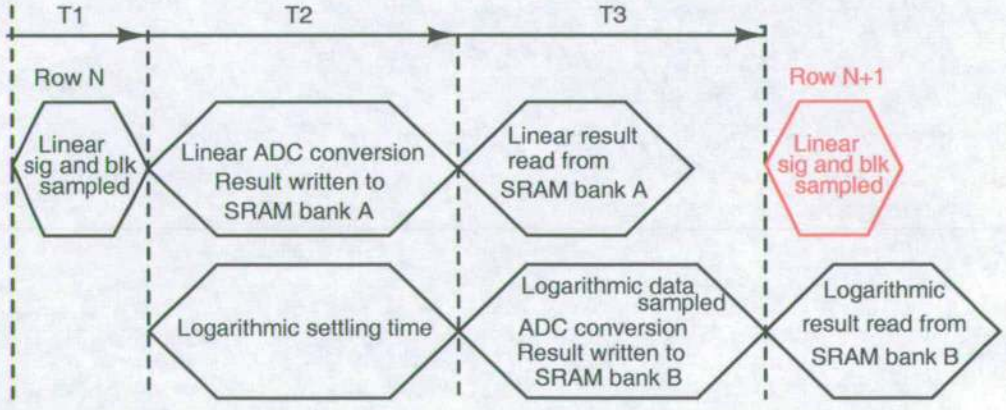


Figure 5.24: *Readout timing: linear data and raw logarithmic data.*

Figure 5.24 is used only for characterisation purposes. To implement either offset calibration or two parameter calibration the readout scheme is modified.

The timing including logarithmic offset calibration is shown in Figure 5.25.

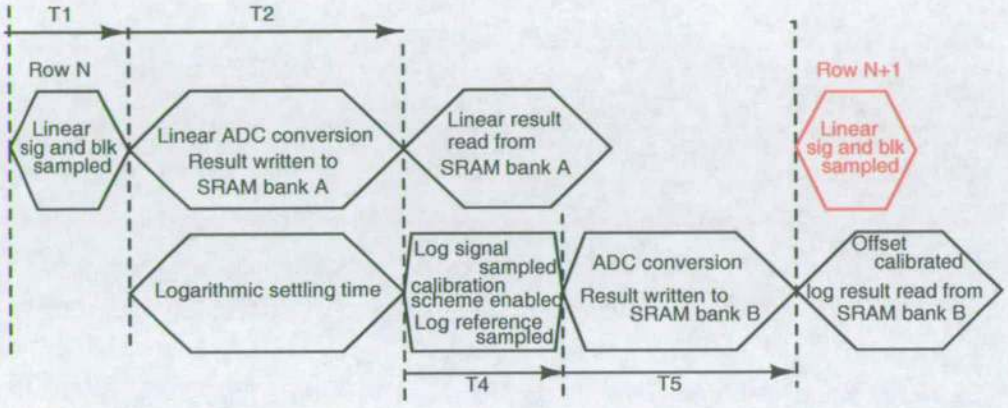


Figure 5.25: *Readout timing: Linear data and offset calibrated logarithmic data.*

The linear data is readout in the same fashion as described above. After the linear ADC conversion the raw logarithmic value is sampled and held but instead of sampling a reference voltage on the second sample and hold capacitor the pixel is switched into one of the reference generation modes and the reference value sampled. There will be a delay of around $20\mu s(T4)$ whilst the column current source settles or the reference voltage to the pixel is ramped. The second ADC conversion begins immediately after the logarithmic reference value is sampled. The digital output contains the difference between the raw logarithmic value and the reference point as required in offset calibration. The logarithmic data does not vary over a wide range of voltages thus it would be possible to reduce the range of the ramp applied to the ADC thus reduce the conversion time. If a response of 70mV/decade is achieved over 6 decades of illumination this only requires a ramp of 420mV compared to the linear range which is greater than 1V. Any offset in the logarithmic data is common to both the raw data and the reference level thus the difference will occupy a greatly reduced range. A reduction in ramp range can not be applied when reading the raw logarithmic value due to possible spread from process variations. Assuming $T4$ is $25\mu s$ and $T5$ is $50\mu s$ the total readout time for a row is $T_{row} = T1 + T2 + T4 + T5 = 10 + 50 + 25 + 50 = 135\mu s$. This equates to a maximum frame rate of 26fps for an array of 288 rows.

The two-parameter algorithm to calibrate the logarithmic data is implemented in the digital domain thus it is necessary to convert the raw logarithmic data, and the two reference points to

digital codes individually. The timing to readout the separate values is shown in Figure 5.26.

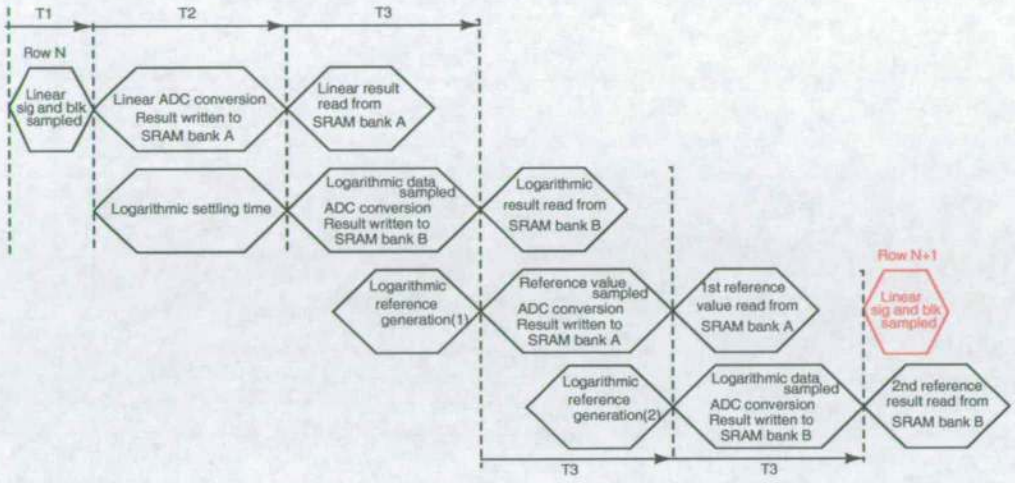


Figure 5.26: *Readout timing: Linear data, raw logarithmic data and two reference points.*

The total readout time for a row is $T_{row} = T1 + T2 + 3(T3) = 10 + 50 + 3(55) = 225\mu s$. This equates to a maximum frame rate of 15fps for an array of 288 rows.

5.9 Other sensor sub-circuits

5.9.1 Analogue output

Two analogue pins were made available to monitor the output of various blocks inside the test device. The first of these is connected to the output of the DAC used to supply the reference voltage to the logarithmic mode. The second multiplexes between the ADC ramp and offset, and the output of eight analogue columns. Such analogue information can greatly aid any debug required as well as allowing a closer look at the settling characteristics. The column outputs are multiplexed to a single signal that passes through a source follower to provide enough drive strength for the pad. The analogue readout for the two pads is shown in Figure 5.27.

5.9.2 I^{2}C register map

The relatively small array size implemented meant that the sensor's minimum size was dictated by the size and spacing of the pads. To minimise the amounted of 'wasted' silicon area the static signals were realised on-chip. A set of register banks were used to hold the values of the

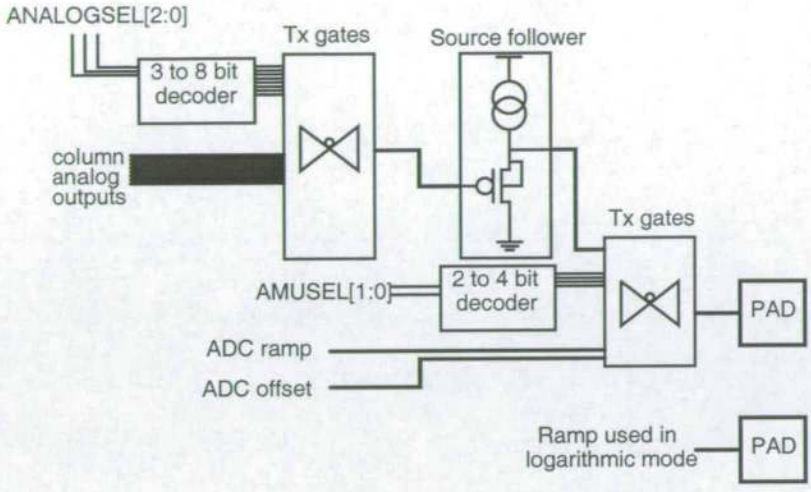


Figure 5.27: *Analogue output multiplexer.*

static signals and their programming was done via a serial interface. An I^2C communications interface was used. The register map consisted of eight registers each a byte in size. Table 5.3 lists the signal names, their location and a description of each.

Index	Bit	Name	Description
0	[3:0]	ICALSEL[3:0]	Calibration current select
	4	CABPD	power down for analogue block
	5	LOGRAMPPD	power down for ramp used in log mode
	[7:6]		NOT USED
1	[1:0]	LOGRAMPSCL[1:0]	Scale for ramp used in log mode
	[7:2]	LOGRAMPGAIN[5:0]	Gain for ramp used in log mode
2	[5:0]		NOT USED
	[7:6]	ICOLSEL[1:0]	Linear mode column current select
3	[1:0][5:7]		NOT USED
	[4:2]	ANALOGSEL[2:0]	Column select for analog output
4	[5:0]	RMPGAIN[5:0]	Gain of ramp used in ADC
	[7:6]	RMPSCL[1:0]	Scale of ramp used in ADC
5	[5:0]	OFFGAIN[5:0]	Gain of the offset used in the ADC
	[7:6]	AMUXSEL[1:0]	Select for analog output
6	[3:0]	RMPOFF[3:0]	Magnitude of offset used in ADC
	[7:4]		NOT USED

Table 5.3: *I^2C Register Map*

5.9.3 Pinout

The test device was bonded in a 180 pin package to enable compatibility with the test platform. Figure 5.28 shows the chip micrograph and Figure 5.29 provides a top level block view of the sensor architecture with a list of all the pin names. The digital control signals are labelled in black and the analogue pins are blue. The remaining pins are supply voltages (violet).

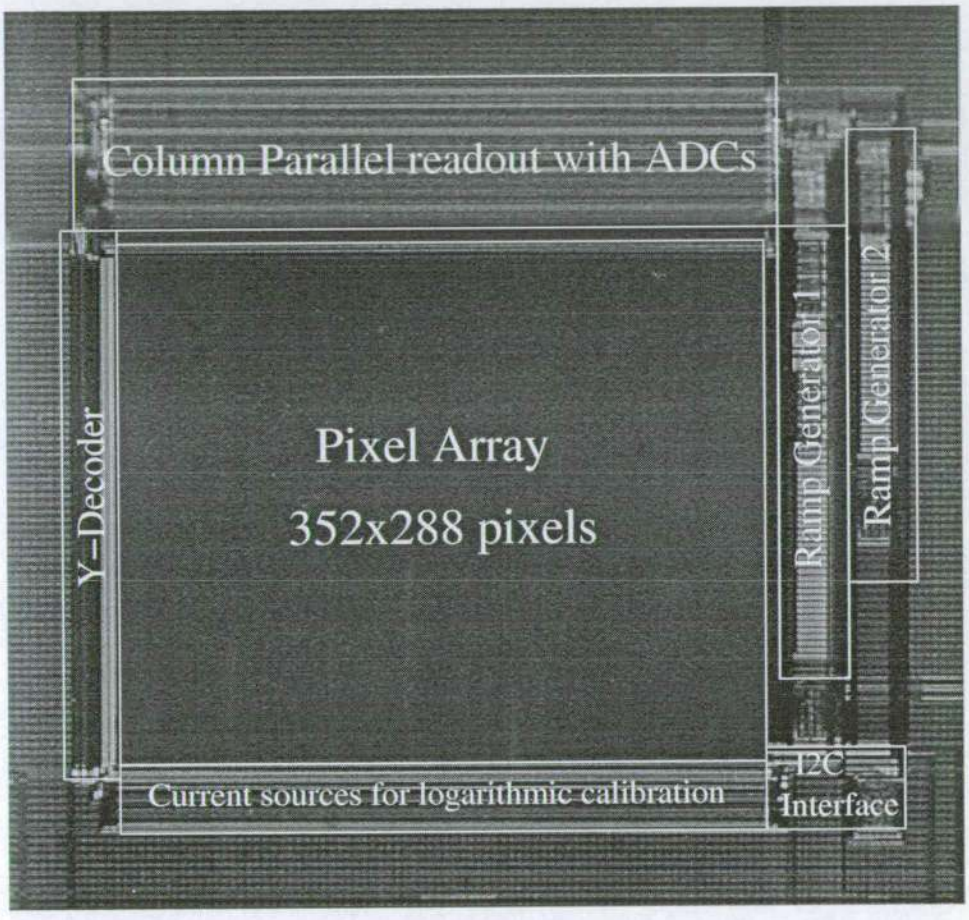


Figure 5.28: *Chip micrograph.*

5.10 Conclusions

A CIF format array CMOS image sensor has been designed which allows independent read-out of linear and logarithmic data. This is achieved from a new 7-transistor pixel that can be switched between the two modes of operation. To improve the settling response in logarithmic mode the source of the logarithmic converting NMOS is held constant and feedback permits its gate voltage to be modulated by the photo-current. A small pixel pitch of 5.6μm x 5.6μm

is achieved by placing the majority of the amplifier in the column circuitry and switching it between pixels of the same column.

Two on-chip reference generation schemes have been implemented as a means of calibrating the logarithmic mode. A set a matched column current sources permit high reference currents to be created whilst a novel voltage ramping scheme has permitted the generation of much smaller reference currents in a usable time period. Offset calibration can be achieved on-chip in the analogue domain by simply differencing the raw logarithmic voltage with the voltage from one of the reference generation schemes. The two-parameter calibration algorithm is however implemented in the digital domain and requires the separate readout of the raw logarithmic value and the two reference levels.

The stitching of the linear and logarithmic data is also done in the digital domain. When a row in the array is addressed the linear data is first sampled, digitised then readout of the chip into a line memory. Logarithmic mode is then enabled and the logarithmic data is readout (calibration either performed on-chip or in digital domain). When the data from both modes is available for a pixel the decision on which to output is made.

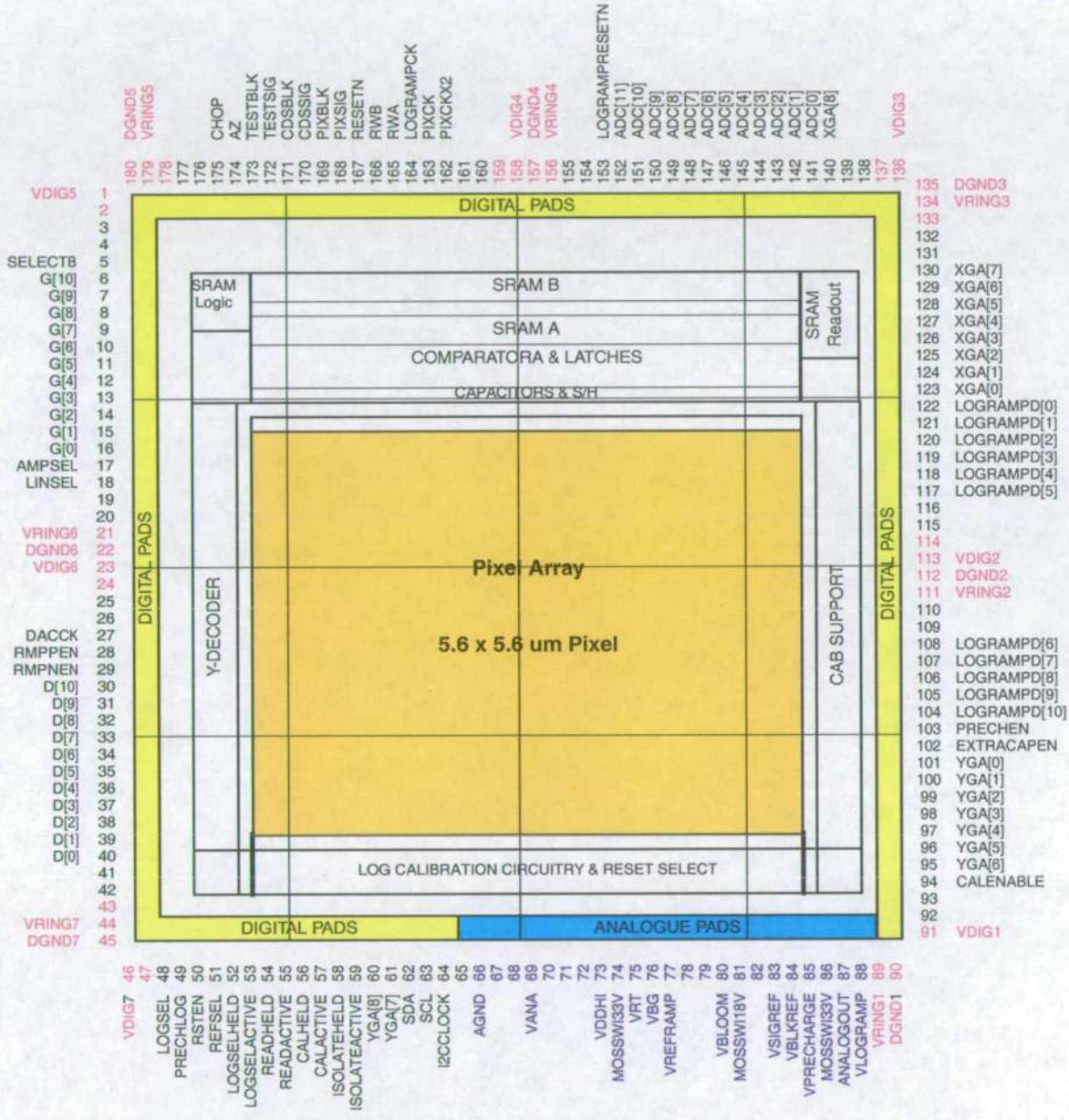


Figure 5.29: *Pinout digram.*

Chapter 6
Sensor Characterisation

The previous design work of a combined linear-logarithmic CMOS image sensor was realised by a fabricated device. This chapter begins by briefly discussing the test-setup before measurements from the linear-logarithmic imager are presented. The two modes have been characterised separately to enable comparison with other imagers. Further detail is also provided for images with linear and logarithmic data combined.

6.1 Test Setup

The linear-logarithmic device was designed to be compatible with an existing test setup. The pad-ring and bonding was arranged such that the 180pin package fitted directly into a printed circuit board(PCB) as shown in Figure 6.1.

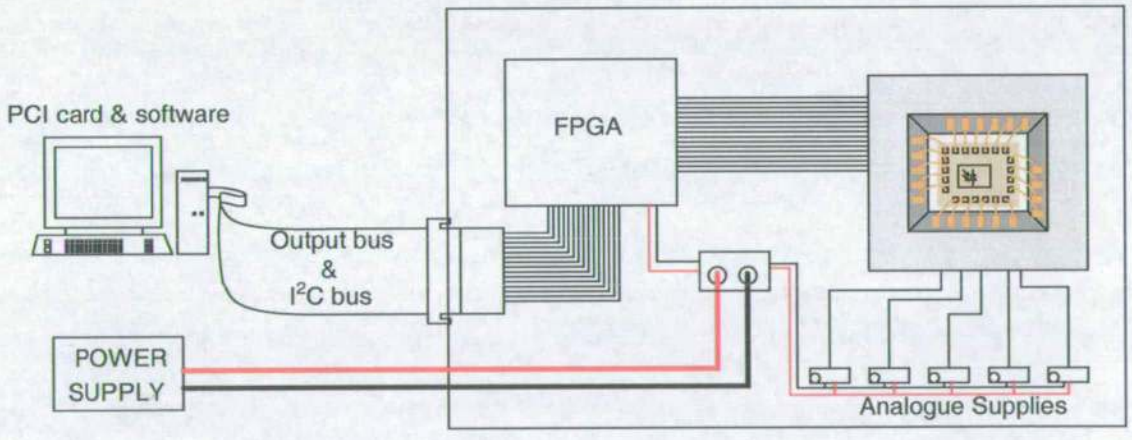


Figure 6.1: *Test setup.*

Potentiometers were used to control the individual analogue reference voltages whilst an FPGA supplied all the digital timing signals. An I^2C connection between the PC and the FPGA provided access to an array of registers such that the timing modes could be altered. The same I^2C connection was also used to access the registers situated on the sensor. The register banks in the FPGA and on the sensor were given different device addresses allowing them to be addressed independently.

The hardware description language, Verilog, was used to create the timing required by the sensor. The signals were coded in Register Transfer logic (RTL) which offers a high level of abstraction. To convert the RTL into a netlist of digital gates, the synthesis tool synplify[1] was used. This synthesis tool is specifically designed for use with FPGAs. Finally, the netlist was fitted into the FPGA using Quartus[2]. Appendix A provides more detail on the FPGA implementation.

6.2 Linear Mode

Illumination dependent noise in an image can be used to determine many parameters. It is first necessary to divide the total noise into its various components. Time invariant noise sources can be considered removed when calculating the per-pixel difference of two images captured under identical conditions. Thus noise sources such as the photon generated signal, dark current signal, and fixed pattern noise are removed. This leaves photon-shot noise, dark current shot noise and readout noise. If the illumination is sufficient, the photon shot noise dominates and the other noise sources can be disregarded.

The methodology is explained in [88] and [89] and briefly reviewed here.

Consider the equation

$$S(DN) = P \times QE \times K^{-1} \tag{6.1}$$

where $S(DN)$ is the averaged signal (represented by a Digital Number) over the affected pixels, P is the mean number of incident photons, QE is the quantum efficiency and K is the conversion factor (e^-/DN). K can be determined by relating the output signal $S(DN)$ to its variance $\sigma_S^2(DN)$.

$$\sigma_S^2(DN) = \left(\frac{\sigma_{PQE}}{K}\right)^2 + \sigma_R^2 \tag{6.2}$$

Equation 6.2 provides an expression for the total noise of the sensor. The photon shot noise σ_{PQE} is multiplied by the gain from the pixel to the ADC and is added to the read noise σ_R^2 which is independent of the incident illumination level. Photon statistics state the noise

[1] EDA tool supplied by Synplicity.
[2] EDA tool supplied by Altera.

is proportional to the number of interacting photons, ${\sigma^2}_{PQE} = PQE$. Therefore, K can be written as:

$$K = \frac{S(DN)}{\sigma^2(DN) - {\sigma^2}_R} \tag{6.3}$$

K is the inverse gain from the photodiode to ADC and is useful in determining other parameters from the sensor.

$$K = (S_P A_{READOUT} A_{ADC})^{-1} \tag{6.4}$$

If known, the gain of the readout and ADC, $A_{READOUT}$ and A_{ADC} respectively, can be used to determine the pixel capacitance, ${S_P}^{-1}$.

The conversion factor can be determined graphically from a plot of the image noise (standard deviation) against the image mean. The resulting curve should resemble that shown in Figure 6.2. The interception of the shot noise slope with the x-axis should reveal the conversion factor. The straight line must be fitted to the data where the photon-shot noise is dominant but also below saturation. An alternate approach is to use Equation 6.3 directly. The saturation or full well level can also be seen from Figure 6.2.

6.2.1 Conversion Factor

Using the setup shown in Figure 3.2, uniformly illuminated images were captured at increasing intensities.Two consecutive images were taken at each illumination level then differenced on a per pixel basis. The variance of the difference frame was then calculated and divided by two to give the variance of a single frame. The image mean was found after subtraction of a frame of zero exposure. Figure 6.3 plots the noise of a single frame, expressed as the standard deviation, against the image mean. This is the photon-transfer curve for the linear mode of the fabricated device.

K was determined using Equation 6.3 for each data point prior to saturation in which the photon-shot noise was dominant. The results were then averaged. K was found to be 64 $e^-/code$. This gave a **full well capacity** in excess of **64000** electrons as the saturation point was slightly greater than 1000 codes.

The pixel capacitance was next calculated knowing the gain of analogue readout path and the

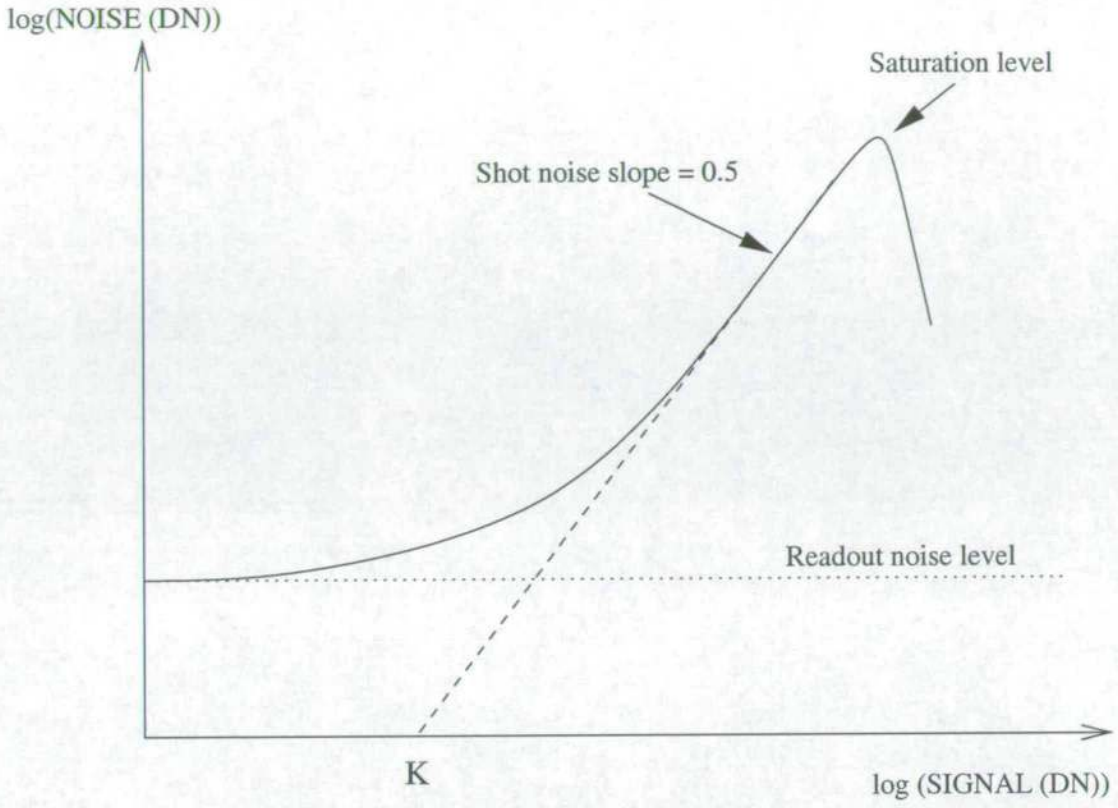


Figure 6.2: *Photon-transfer curve.*

relationship between codes and voltage at the ADC. The first of these is given by the gain of the source follower (A_{SF}) which is part of the pixel and was found to be 0.82 from simulation. The full range of the ADC was set to 2048 codes which were covered by a ramp range of 1.65V. Equation 6.4 thus becomes

$$K = (S_P A_{SF} A_{ADC})^{-1} \tag{6.5}$$

Rearranging and substituting in the above quantities produces

$$\begin{aligned} S_P &= (K A_{SF} A_{ADC})^{-}1 \\ &= (64 \times 0.82 \times \frac{2048}{1.65})^{-}1 \\ &= 15.35 \mu \mathrm{V}/e^{-} \end{aligned} \tag{6.6}$$

The pixel capacitance is found from Equation 6.7 in which q is the charge of an electron and

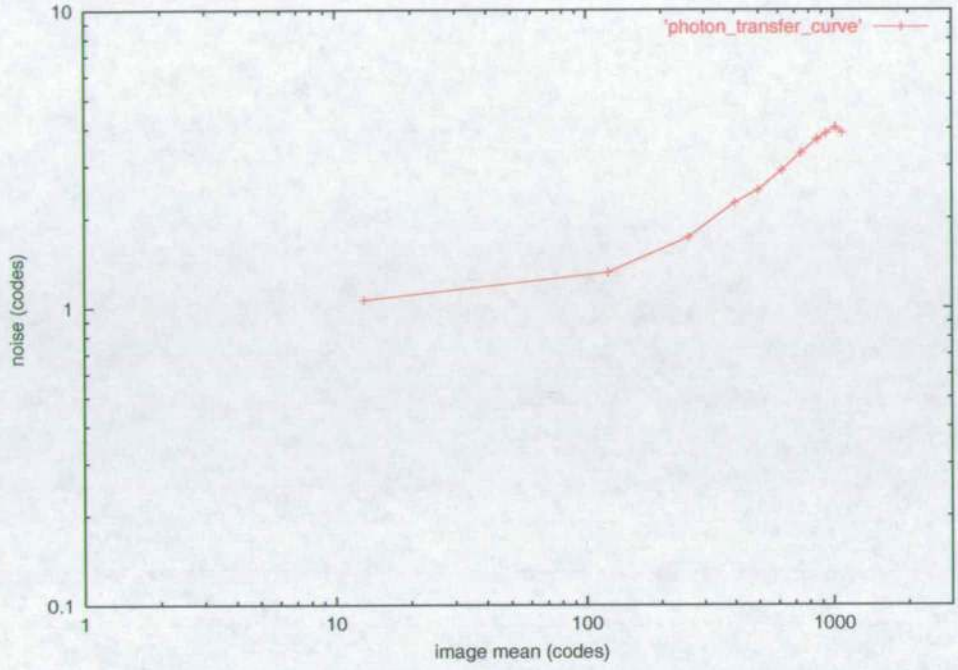


Figure 6.3: *Photon-transfer curve for the test device.*

has the value $1.6\text{x}10^{-19}$C.

$$C_{pix} = \frac{q}{S_P} \tag{6.7}$$

$$= \frac{1.6\text{x}10^{-19}}{15.35\text{x}10^{-6}} \tag{6.8}$$

$$= 10.4\text{x}10^{-15}\text{F} \tag{6.9}$$

The pixel capacitance is slightly higher than the 8fF predicted from the simulation models and layout back in Section 5.2.3. The most likely reason for this is the connection of two N-plus regions to the Nwell photodiode. It is known that highly doped N-diffusion regions have a greater associated capacitance than lower doped N-well areas. The estimation of the total pixel capacitance used a value of 3fF for the photodiode which was measured from a device in which the photodiode had a single connection to highly doped N-diffusion. At the design stage the pixel pitch was prioritised over the pixel capacitance.

The SNR at saturation was calculated using Equation 6.10.

$$SNR(sat) = 20\log_{10}\left(\frac{Signal\_at\_saturation}{Noise\_at\_saturation}\right) \tag{6.10}$$

The number of codes and the noise at saturation was found from Figure 6.3 to be 1019 and 4.02 respectively. This gave a **SNR at saturation of 48.1dB**.

The dynamic range for the linear mode of operation is given by Equation 6.11.

$$Dynamic\_Range = 20\log_{10}\left(\frac{Max\_Signal}{Noise\_floor}\right) \tag{6.11}$$

The maximum signal is the same as the saturation point used to calculate the SNR. The Noise floor is labelled as the 'Readout noise level' in Figure 6.2 and represents the temporal noise of the sensor. This value could have been approximated from the Photon-transfer curve of Figure 6.3 by reading the noise value under low illumination. A more accurate result can be obtained by subtracting two frames of zero exposure, calculating the variance of the resulting image then dividing the answer by two. To further increase accuracy the full ADC range of 2048 codes was set to cover only 0.8V. The **temporal noise** was found to have a standard deviation of **0.95mV**. Converting the saturation point to a voltage and using Equation 6.11 the **Dynamic Range** of the linear mode was found to be **58.7dB**.

6.2.2 Sensitivity

The sensitivity of an imager is commonly expressed in V/lux.s. Because lux is defined over the visual spectrum an IR-filter was used to prevent longer wavelength light influencing the reading. Again, Figure 3.2 shows the test setup used. For a fixed exposure period the illuminance level was varied by changing the Neutral-Density filters placed between the light source and the integrating sphere. This produced the plot shown in Figure 6.4.

A straight line of the form $y = ax + b$ was fitted to the data (using least-squares) and the variables a and b found to be 8.33 and 186 respectively. a represents the constant of proportionality between codes and lux while b is the offset. It was noted that the offset matched the mean codes value obtained from a zero exposure image. The sensitivity was calculated by multiplying the constant of proportionality by the ADC Volts to codes ratio then dividing the answer by the exposure time. The sensitivity was found to be 726mV/lux.s.

The conversion gain of the test device is close to that reported by Krymski and Tu in [90] but significantly lower than the 9V/lux.s also quoted. The paper cites the larger pixel size as a reason for the high responsivity.

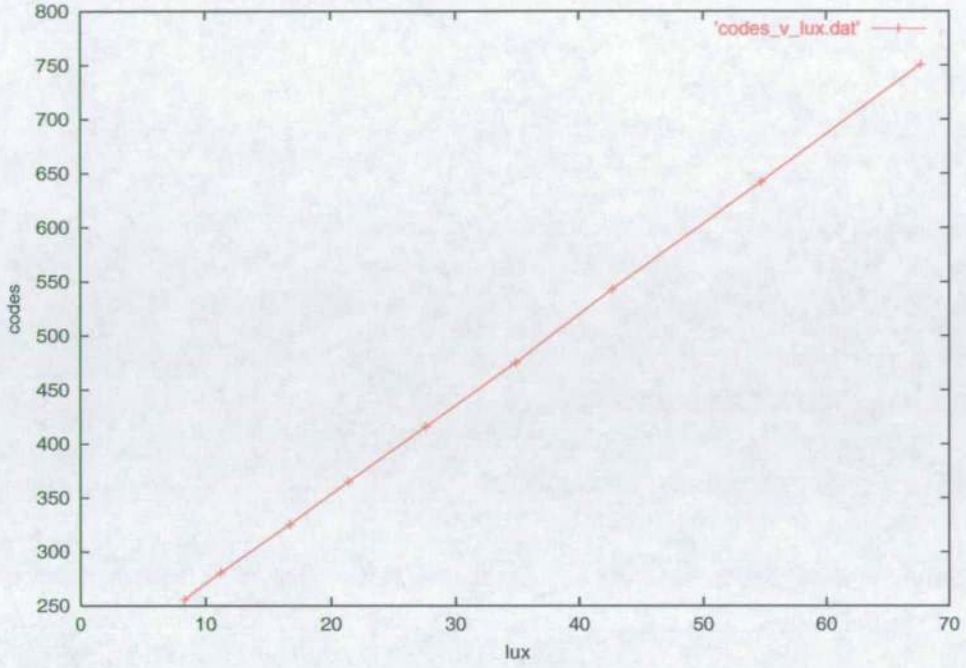


Figure 6.4: *Sensitivity plot for linear mode.*

6.2.3 FPN

The column parallel architecture of the sensor makes it liable to column based FPN. The output path is identical for every pixel in the same column thus offsets between columns will manifest themselves as vertical stripes. To investigate the column FPN all the pixels in a column were averaged and plotted against the column number. Figure 6.5 displays the results for an image captured in the dark and at minimum exposure to minimise the effect of dark current.

The standard deviation was measured to be 10codes which amounts to 3.7mV. The noise is sufficiently high to be visible in a captured image. Section 6.4.5 provides example images. The FPN is partly caused by too low an Auto-Zero (AZ) voltage. The column amplifier at the front end of the ADC uses the AZ phase to store the offsets of the column on internal capacitors. If the AZ voltage on the inputs of the amplifier are too low then the offsets will not be correctly learnt. Unfortunately, a higher AZ voltage reduced the settling performance of the logarithmic mode. This was caused by insufficient drive strength in the source-follower and is described in Section 6.3.2.2.

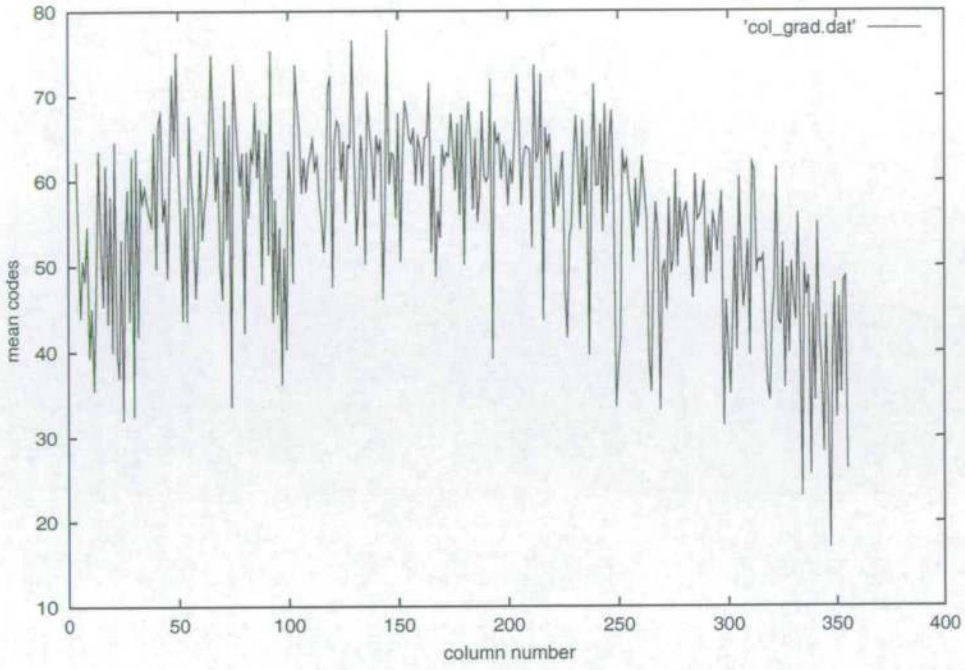


Figure 6.5: *Column averages.*

6.2.4 Dark current

To measure the dark current, a long exposure time was set whilst the sensor was covered to block all incident radiation. A frame of zero exposure was subtracted to remove any offset and FPN. The images were captured at room temperature with an exposure time of 513ms.

Figure 6.6 plots the dark current histogram(red) and a Normal distribution curve (green). Figure 6.7 plots the same information on a logarithmic vertical axis. The mean signal was found to be 49 codes which equates to $0.388fA$. Relating this value to the area of the pixel gives a value of $\mathbf{1.24}nA/cm^2$. It can be seen that the data does not fit the normal distribution well. It is likely a Rayleigh or Poisson distribution would provide a better fit, however, the modelling of the dark current is beyond the scope of this work and is not covered in any more detail. Figure 6.7 shows best the extent to which the outliers extend. In extreme cases the pixel has saturated and would appear white if viewed in an image. Such pixels are known as 'leaky pixels' and a defect correction algorithm would be employed to reduce their effect. However, the performance of the defect correction will reduce as the number of outliers increases. The layout of the pixel is thought to greatly influence the dark current. Similar to the pixel capacitance, it is thought that the two N^+ active connections to the Nwell photodiode increase the dark current.

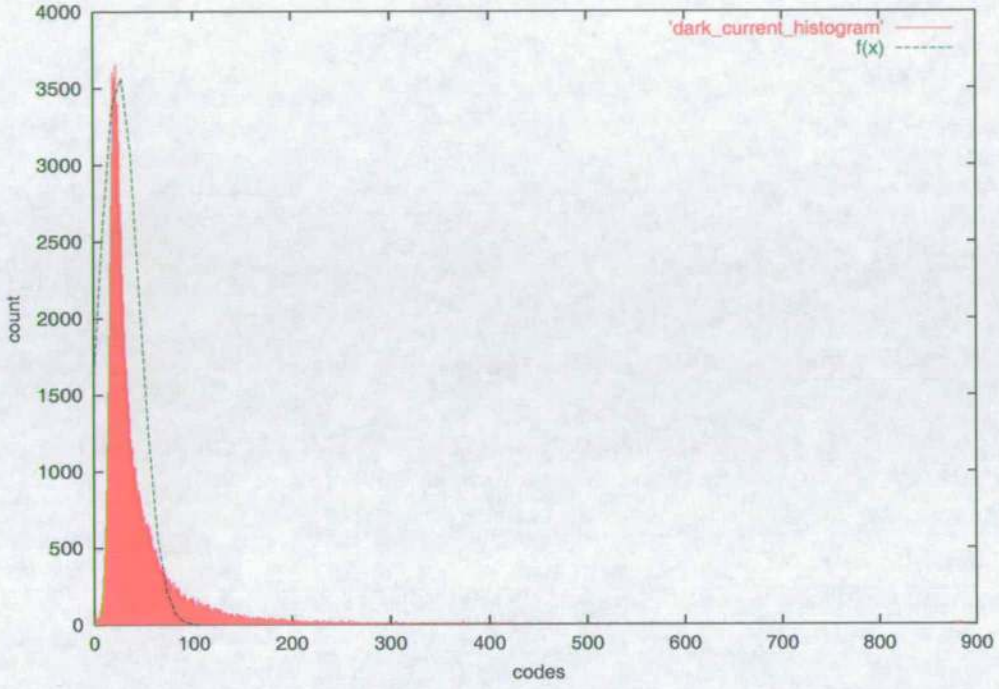


Figure 6.6: *Dark current histogram.*

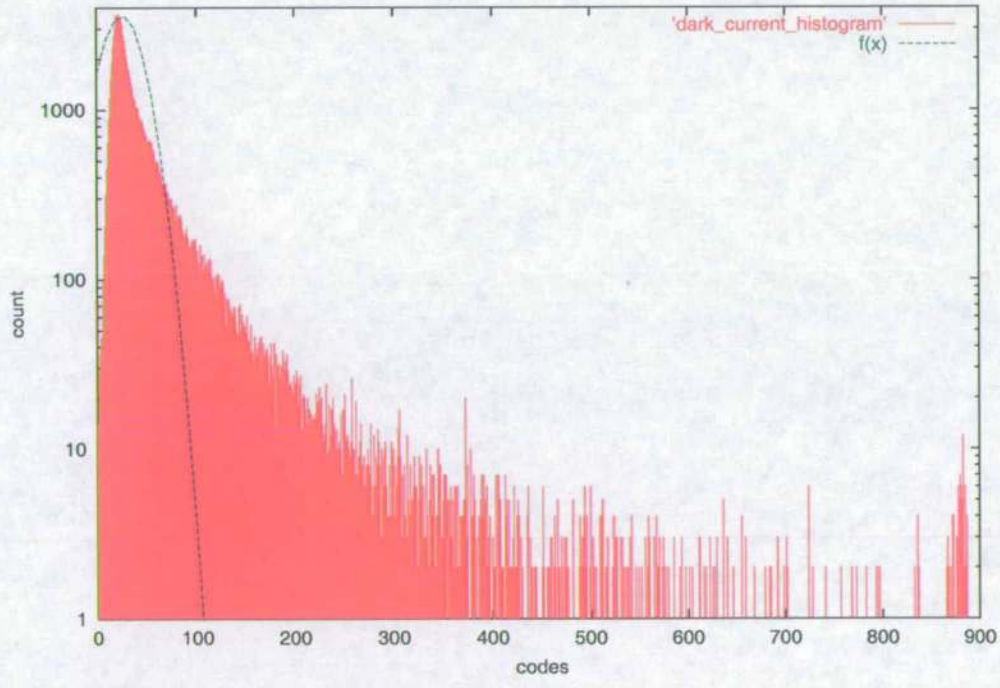
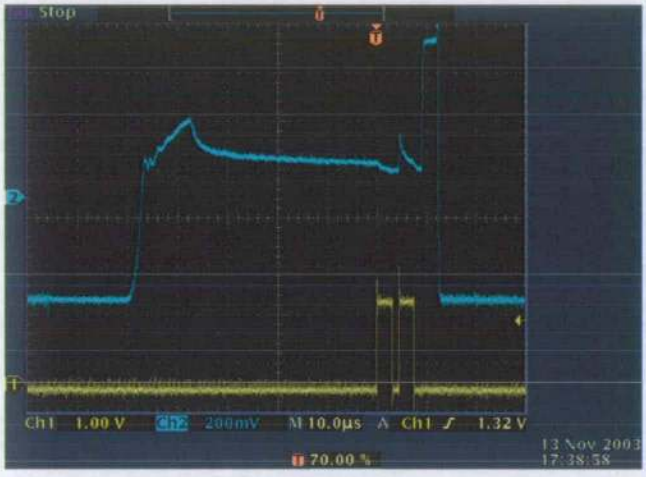


Figure 6.7: *Dark current histogram (red) and Normal distribution (green) plotted on a vertical log scale.*

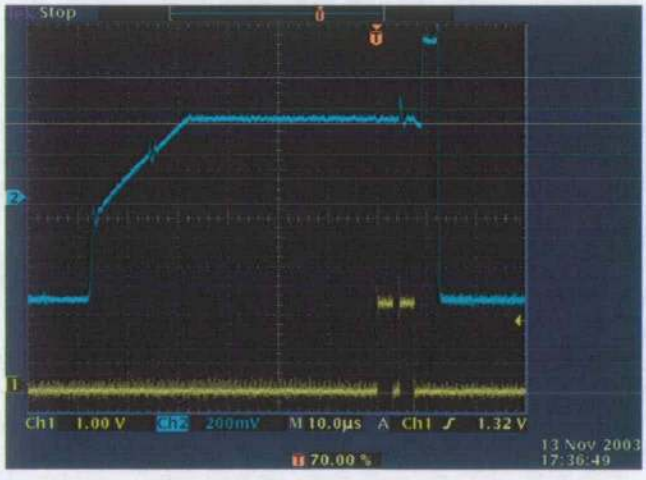
6.3 Logarithmic Mode

In logarithmic mode a feedback loop is created round the pixel by connection of a column based amplifier. The design details of the architecture were given in Chapter 5.2.2. The output voltage, which is the gate-source voltage of the NMOS load device, varies logarithmically with the photo-current.

To observe the switch to logarithmic mode and the initial voltage ramp, the pixel's response was observed through the device's analogue readout. Figure 6.8 shows an oscilloscope trace of a pixel stimulated at two different light intensities.



(a)



(b)

Figure 6.8: *Screenshots of a pixel operating in logarithmic mode (blue trace is the logarithmic output) at (a) low incident illumination, (b) high incident illumination.*

The blue trace shows the column voltage for a single line period and is initially connected to the logarithmic output. In both screen-shots the initial ramping to absorb any overshoot from the amplifier can be clearly seen. At the end of the ramping period the logarithmic voltage settles to its final value in a time proportional to the photo-current. Also shown is the timing of the signal sampling switch (yellow trace), that is activated for the auto-zero phase (first pulse) and for sampling the logarithmic voltage (second pulse). During the sampling phase a glitch can be seen on the logarithmic trace. This is caused by the difference in potential between the auto-zero and the logarithmic voltages. The logarithmic voltage is lower than the voltage used for the auto-zero phase thus when the two are connected there is a glitch as the S/H capacitors discharge. Immediately after sampling the logarithmic signal a reference voltage is sampled onto the second S/H capacitor. The reference level is clearly visible on the blue trace and is purposely greater than the logarithmic voltage to ensure correct operation of the ADC.

The logarithmic response to illumination was calculated using the setup shown in Figure 3.2. Since a single row can only be in logarithmic mode at one time it was important to distinguish the difference between settling time limitations and logarithmic response limitations. A reduced clock frequency was set to provide an extended settling time for logarithmic mode. The transient performance of the logarithmic mode is evaluated in Chapter 6.3.4.

6.3.1 Logarithmic response

Figure 6.9 shows the output of the sensor in logarithmic mode as a function of irradiance. The data follows a straight line because the illumination level is displayed on a logarithmic scale. This confirms the logarithmic compression as the photo-current is converted to a voltage in each pixel. The codes plotted at each illumination level represent the mean over the whole pixel array.

Below about 20mW/m^2 the response begins to deviate from a straight line. This is due to the logarithmic mode not settling in the allocated time. The image acquisition software had a minimum frame rate at which the sensor could operate. This equated to a logarithmic settling time of 7.5ms. For low irradiance levels the logarithmic settling time will exceed this value.

Using the data above an irradiance level of 20mW/m^2 the log slope was calculated to be 100codes/decade. This equates to 80mV/decade. This result compares favourably with Loose [74] and Kavadias'[73] work of which the former achieved 130mV/decade with 2 stacked devices

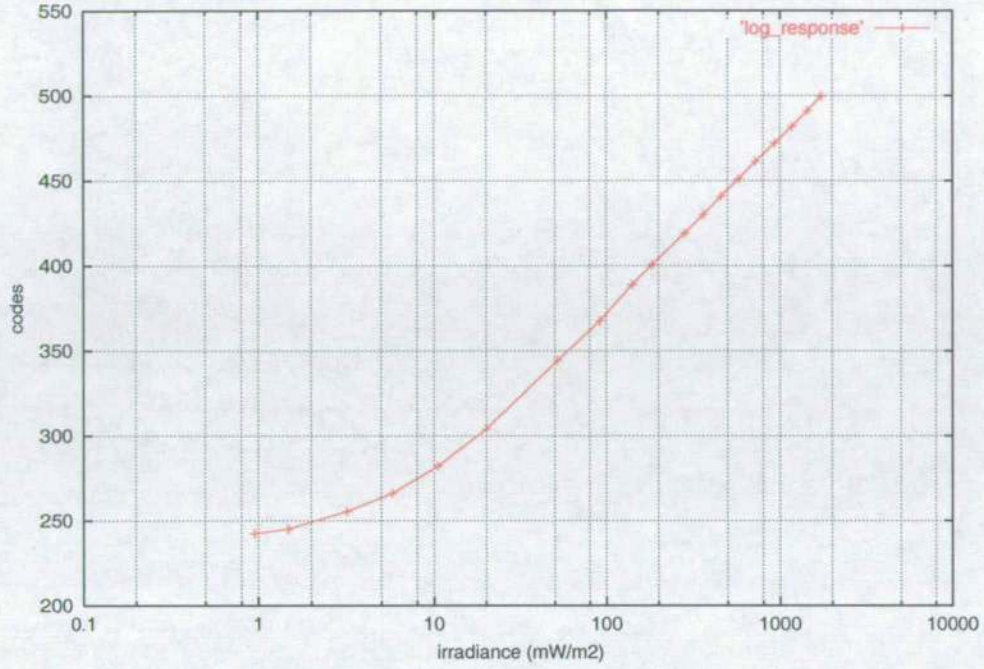


Figure 6.9: *Log response to irradiance.*

(therefore 65mV for a single device) and the latter 50mV/decade. Huppertz *et al* report a slightly superior 84mV/decade which is achieved with feedback (Chapter 4).

To calculate the raw FPN in logarithmic mode a series of 30 frames were averaged on a per pixel basis thus reducing the temporal noise by $\sqrt{30}$. The FPN in the averaged image was then calculated and found to have a standard deviation of 36mV. The ratio of the raw FPN to the logarithmic response is thus 45%. Figure 6.10 shows a histogram for an image captured under uniform illumination of 1423mW/m^2. The raw FPN from the test device is significantly less than the 92% found in Chapter 3. The reason for this is a combination of the new logarithmic architecture and the new 0.18μm technology.

6.3.2 Logarithmic Calibration

The algorithms presented in Chapter 3.3 were used to process the data from the test device. It was possible to perform offset calibration on-chip by sampling the raw logarithmic signal onto the first S/H capacitor then the generated reference point onto the second S/H capacitor. The conversion of the difference produced the offset corrected code.

The 2-parameter correction algorithm required the raw logarithmic value and two reference

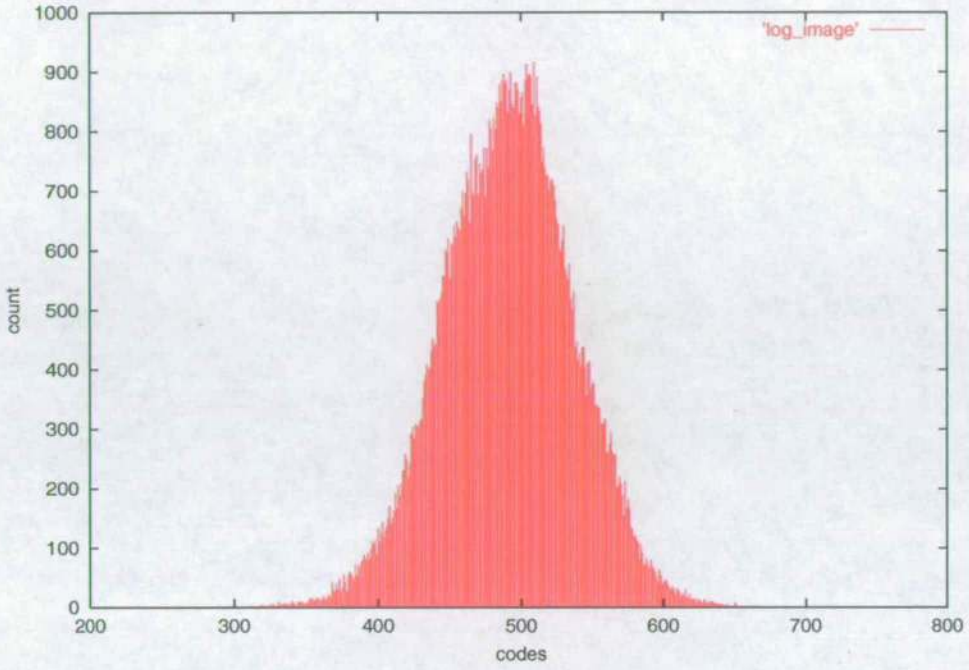


Figure 6.10: *Histogram of raw logarithmic image.*

points as digital codes which could then be processed in the digital readout chain. Unfortunately, time did not permit the algorithm to be implemented in the FPGA thus software was used. The software implementation does not affect the reduction in FPN: it is the generation of the reference points that are important and their read out is unaltered. For real-time operation whilst performing 2-parameter calibration a three line memory would be required. Due to the order of the data the memory would store the linear data, raw logarithmic data and the data from the first reference point.

The results provided in Chapter 3.3 used images captured under uniform irradiance as the reference frames for calibration. The following sections characterise data from the two on-chip reference generation schemes and use it to calibrate raw data. The average of 30 frames was used to reduce the temporal noise so that the effect of the calibration could be more accurately assessed.

6.3.2.1 Column calibration

In this configuration the column current sources were connected to the pixel whilst the photodiode was isolated from the logarithmic converting device. The column current sources were designed to provide a current from 2nA to 28nA depending on the switches *cal1* to *cal4*. If

all switches were set low the reference current was designed to be 2nA and if all were enabled 28nA should have flowed. *cal1*, *cal2* and *cal3* each provided 2nA whilst *cal4* provided 20nA. The programmable reference current was used to calculate the logarithmic response to photocurrent. It was expected to produce the same results as those found when varying the irradiance. Figure 6.11 shows the output recorded for the different settings of *cal1* to *cal4*.

Figure 6.11: *Logarithmic response with programmable column current source.*

The current was varied over the 1.15 decades available and the change in output recorded. The response was calculated to be 100 codes/decade which matches that found when illuminating the device.

All the current sources on the sensor are derived from a Voltage Controlled Current Source (VCCS) which takes an off-chip reference voltage and uses a resistor to create the master current (a bandgap voltage generated on-chip would normally be used as the VCCS reference). *cal1* to *cal4* enables mirrors of this master current thus will vary with the absolute resistor value. This is not a problem if only trying to measure the slope of the response as all currents will be scaled appropriately. Uncertainties result if the absolute current level is to be determined. A simulation at the process corners showed the column current could vary by $\pm 30\%$. This is mainly due to the absolute accuracy of the fabrication process when creating the resistor. The photo-current is estimated in Section 6.3.4 to assess the transient performance of the logarithmic mode.

6.3.2.2 Voltage Ramping to generate a reference current

The second on-chip reference generation scheme used a novel means of generating an in-pixel current. The reference voltage applied to the amplifier was ramped whilst the logarithmic compression device was isolated from the photodiode. It was thought that the matching across the array of the capacitance on the isolated pixel node would directly affect the matching of the reference current. The sampling point of the logarithmic value was also important. When the reference voltage reached its nominal level (i.e its final value during logarithmic mode) the output was sampled. This ensured the body effect was unaltered.

The DAC creates a step input but due to the RC loading this appears as a smooth voltage ramp. The slope can be altered by programming the digital codes that drive the DAC. At the maximum input code value of 2048 the output of the DAC was measured to be 1.67V. Thus the resolution of a single code was 0.815mV.

The sampled value is plotted against the time per code in Figure 6.12. To enable a wider range of slopes to be programmed the clock frequency supplying the chip was also altered. A reference image created from the voltage ramping scheme was measured to have 45codes FPN (St.Dev). This was the same as was measured for the logarithmic mode using uniform illumination. However, since the process variations relating to the load device and amplifier greatly exceed those expected from the current matching, it is not possible from this result alone to determine if the reference point was successfully created. The correction of uniformly illuminated images is performed in the following section and compares the reduction in FPN achievable using the on-chip reference generation schemes and uniform illumination as the reference points.

From Figure 6.12 a slope of 94 codes/decade was measured which corresponds to 75mV/decade. The slope is close to that found when using the halogen light source and the column current sources.

The curve in Figure 6.12 shows a reduced response for voltage ramps exceeding around 10mV/μs. This is caused by the source follower in the column having insufficient drive strength. The S/H capacitors are connected to the output of this source-follower and limit its slew rate. To investigate, a simulation was performed. A 300mV saw tooth waveform was input to the source follower whilst observing the peak to peak output. This was compared with the difference between the DC operating point at the maximum and minimum values of the input waveform.

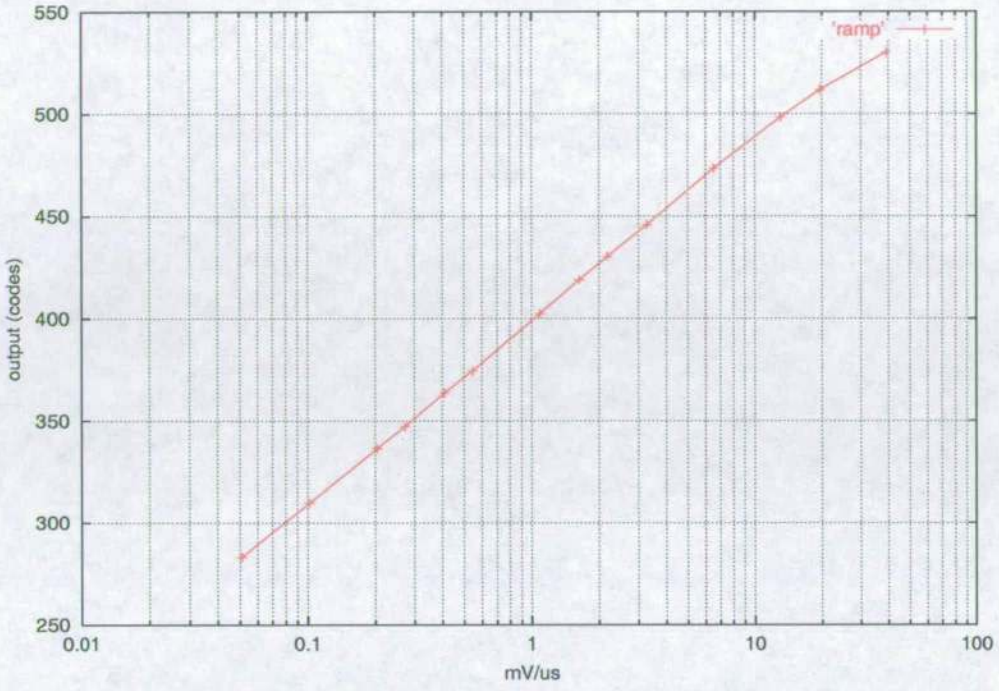


Figure 6.12: *Using the ramp to generate a reference point.*

Table 6.1 shows the output range for different frequencies of the input wave and confirms the source-follower limitation.

dV/dt	Peak to peak output(% of ideal)
300mV/μs	89.5
60mV/μs	97.7
10mV/μs	99.4
7.5mV/μs	99.7

Table 6.1: *Source follower transient characteristics.*

It was envisaged that if the voltage ramp scheme was effective, it would be possible to remove the column current sources. An increased fill factor would then be possible. The transient performance would need to be validated at higher frequencies if such a change were to be implemented.

The pixel capacitance during the ramping phase was estimated to be 3fF from Figure 5.6 of Chapter 5.2.4 (i.e. photodiode isolated from *pix* node and *cal/reset* OFF). Using $I = C\frac{\delta V}{\delta t}$, a 2nA current requires 666mV/μs whilst 1pA requires 0.3mV/us. Whilst the lower reference point is readily achievable, improved buffering would be required for the latter.

6.3.2.3 FPN after calibration

This Chapter investigates the FPN after both offset and 2-parameter calibration. It was shown in Chapter 3.3 that the FPN could be greatly reduced with both algorithms but that the 2-parameter scheme performed better across a wider range of light levels. The results from Chapter 3.3 were achieved by uniformly illuminating the sensor to create the reference points. Since the linear-logarithmic test device uses on-chip reference generation schemes, the results from this Chapter will show how well matched the reference currents are across the array.

Figure 6.13 shows the results for offset calibration with the three different ways of generating a reference point: voltage ramp, column current sources and uniformly illuminated images. The graph plots the standard deviation in codes against the distance between the illumination level and the reference level. Since the sensitivity of the logarithmic mode was measured to be 100 codes per decade of illuminance, the y-axis can also be read as the FPN expressed as a percentage of the sensitivity.

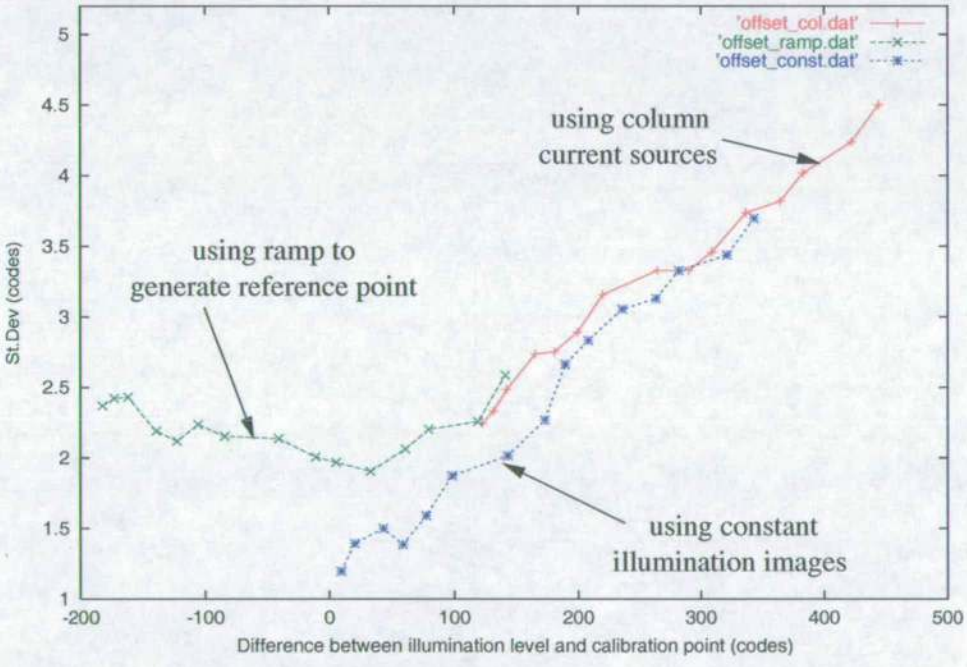


Figure 6.13: *Remaining FPN after offset calibration.*

As expected the FPN is minimised when the reference point is close to the illumination level (difference close to zero). The raw FPN of 45 codes has been reduced to below 3 codes if the calibration point is a maximum of 2 decades (200codes) from the illumination level. All three cases show an increase in the remaining FPN as the distance between the reference point and

the illuminance level increases. As before this is thought to come from slope variations across the array. Using the voltage ramping scheme to create a reference point has reduced the FPN to around 2 codes when the illumination level is close to the reference point. However, the FPN can be further reduced if uniformly illuminated images were used to generate the reference point. This suggests that the matching of currents generated in each pixel by the voltage ramp is around 2%.

For two parameter calibration the standard deviation is plotted against the illumination level with the reference points marked on the plot. Figure 6.14 shows the results from two parameter calibration when the column current sources were used to generate the high reference point and the voltage ramp the lower.

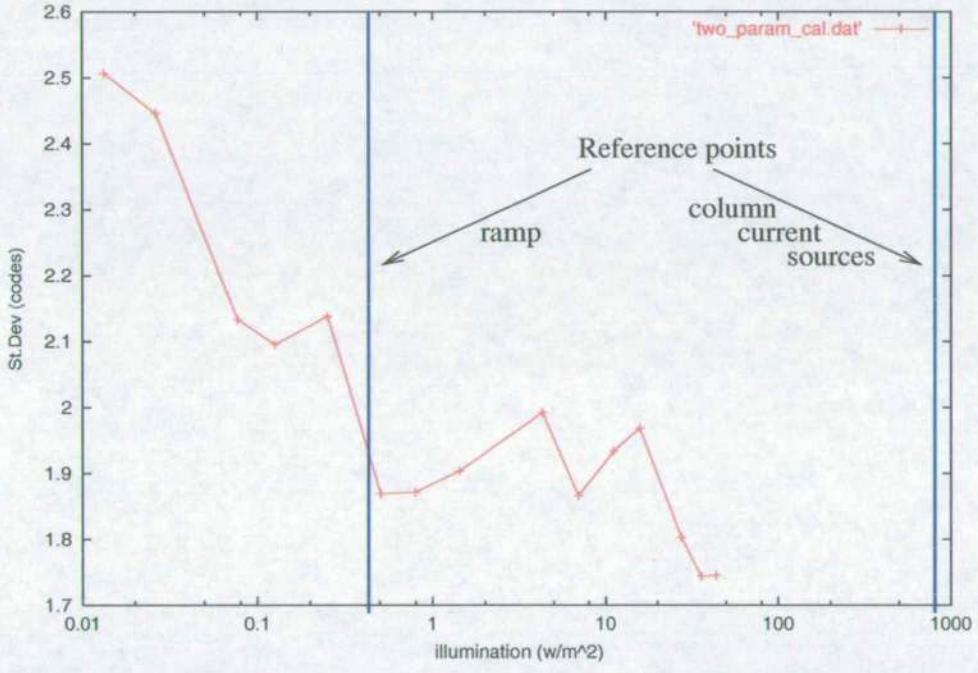


Figure 6.14: *Remaining FPN after two parameter calibration using column current source for the high reference point and the ramp to generate the lower.*

The FPN has been reduced to below 2% for illuminance levels situated between the two reference points. Outside this range the FPN increases but is still $\leq$2.5% at a decade below the lower reference point. To provide a comparison, Figure 6.15 shows the results of two parameter calibration when the reference points were obtained from exposure to a uniform illuminance.

The FPN reduction although slightly superior, is comparable to the results from Figure 6.14. This again demonstrates that the column current sources and the voltage ramp can create well

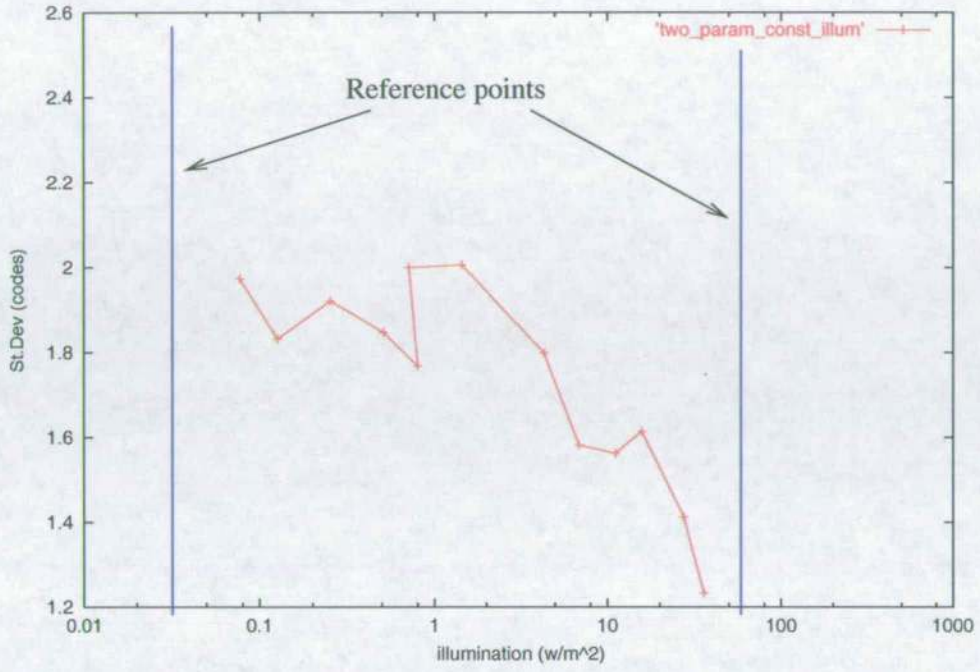


Figure 6.15: *Remaining FPN after two parameter calibration using constant illuminace images as the references*

matched reference currents.

The FPN after 2-parameter calibration with the test device is slightly superior to that found in Chapter 3.3. When the illumination level was between the reference points, the new test device achieved 2% whereas the conventional device from Chapter 3 achieved 3%. This overall performance figure relates the absolute FPN to the logarithmic sensitivity. To compare absolute FPN the results should be expressed in voltages. For the new test device from this Chapter, 2% FPN relates to 1.6mV. From Chapter 3, 3% FPN was equivalent to 1.65mV. Thus the absolute FPN after calibration is very similar.

6.3.3 Temporal Noise

In linear mode the integration period essentially averages the incident illumination over the time period. This increases the signal level with respect to the noise. In contrast, logarithmic mode is continuous in time and suffers from a reduced SNR. The results presented in the previous section have shown what level of FPN reduction is possible with single and two parameter calibration. However, the results were obtained by averaging 30 frames thus reducing the temporal noise by $\sqrt{30}$.

To calculate the temporal noise in logarithmic mode two images were captured under identical conditions and subtracted then the variance of the resulting frame was divided by two to give the noise in a single frame. The sensor was exposed to a uniform illuminance from a current stabilised halogen light source to reduce the effect of flicker noise. The plot shown in Figure 6.16 was found by varying the illuminance level. The bottom x-axis gives the array average in codes (where 100 codes represents a decade of illumination) and the y-axis gives the standard deviation in mV. Recalling that the standard deviation of the FPN was reduced to 1.6mV, it is clear the temporal noise is the limiting factor.

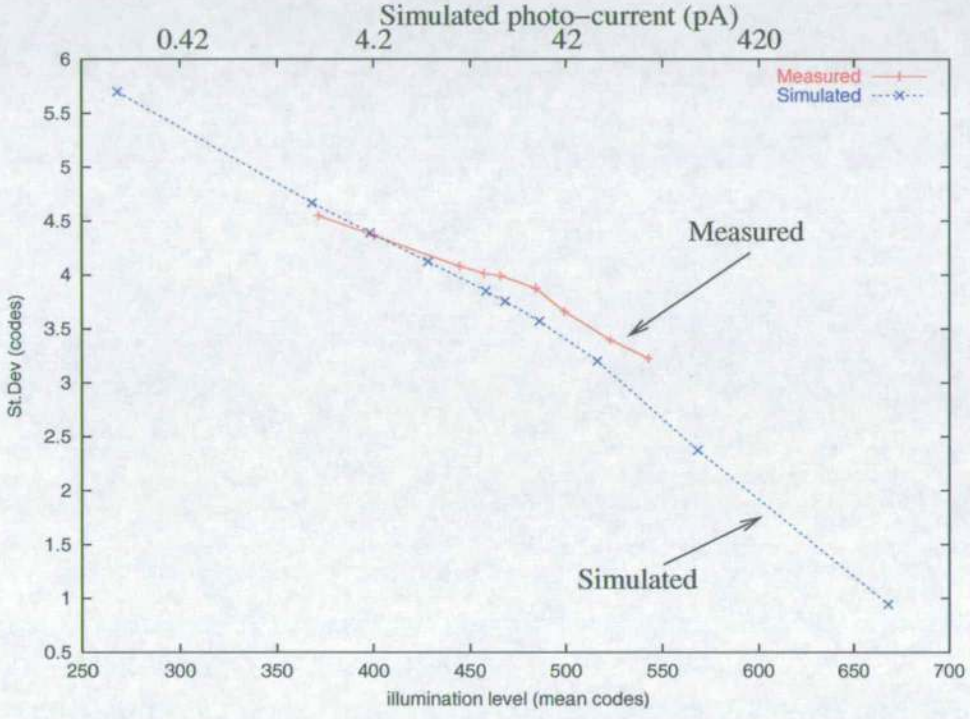


Figure 6.16: *Temporal Noise measured and simulated in logarithmic mode.*

If photon-shot noise were dominant, the noise would be seen to increase for higher light levels. In fact, the opposite was observed. To confirm the measured results a simulation of the noise was performed. The output referred noise is also plotted in Figure 6.16 and the top x-axis provides the photo-currents used. It can be seen that the simulated noise closely matches that measured.

The excessive temporal noise can be explained by examining the frequency response of the amplifier and the feedback (source follower) and remembering that the source follower's bandwidth is proportional to the photo-current. Consider the circuit logarithmic arrangement shown in Figure 6.17.

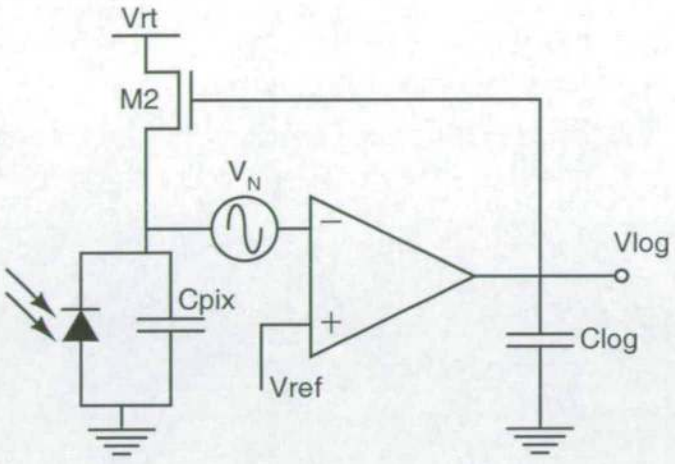


Figure 6.17: *Logarithmic arrangement with input referred noise source.*

At frequencies within the bandwidth of the amplifier and the feedback loop the noise generated by M2 and by the amplifier is subject to a unity gain. However, at frequencies greater than the BW of the source follower but less than the BW of the amplifier the charging and discharging of the pixel capacitance can not be achieved by the photo-current alone. In such cases the current is supplied from the output of the amplifier via the gate-source capacitance of M2. The noise seen at the output is given by:

$$V_{onoise} = \left(1 + \frac{C_{pix}}{C_{gs(M2)}}\right) V_N \tag{6.12}$$

It can be seen the noise is amplified by the ratio of the pixel capacitance(C_{pix}) to the gate-source overlap capacitance ($C_{gs(M2)}$). At frequencies greater than the bandwidth of the amplifier the input referred noise is blocked. Figure 6.18 plots the transfer function from the *pix* node to the output for the circuit of Figure 6.17. The response is plotted for a number of photo-currents. If the photo-current is greater than about 2nA the noise experiences a gain of near unity to the output until the BW of the amplifier is reached and the noise is blocked. However, at lower photo-currents the BW of the source follower is less than the amplifier and the noise begins to get amplified to the output. As the photo-current reduces, the frequency at which the noise begins to be amplified also reduces.

Noise can be reduced by lowering the bandwidth of the circuit. However, a slower settling time would result if the speed of the amplifier were reduced.

If the BW of the amplifier was matched to the BW of the source follower temporal noise could

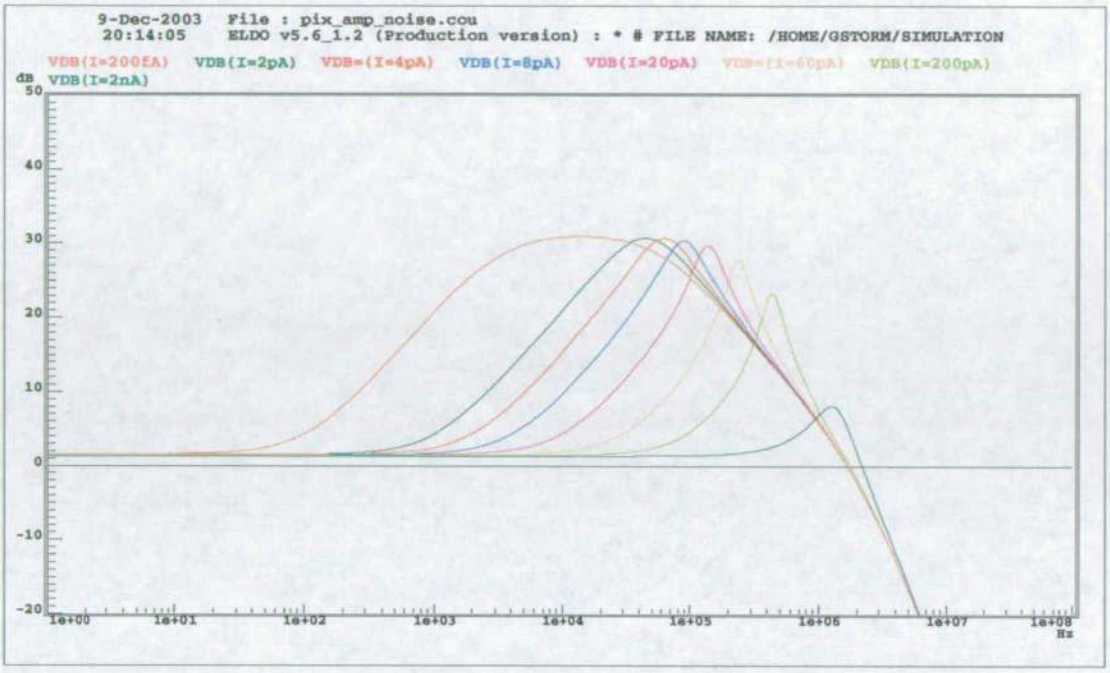


Figure 6.18: *Noise transfer function.*

be reduced but because the photo-current directly influences source follower BW this arrangement is not possible.

One method of reducing the temporal noise is to increase the dimensions of the logarithmic load device and the inverting input device of the amplifier. From Figure 5.2 if *M2* is increased to $\frac{3}{1.5}$ and *M1* to $\frac{2}{1}$ simulation has shown that the noise can be more than halved. This would reduce the temporal noise to a level comparable to the FPN.

A second method of reducing the temporal noise is to increase the absolute photo-current level. This will in turn increase the BW of the source follower. This solution could be achieved by pixel optimisation or by increasing the light sensitive area.

6.3.4 Response time and relative illumination

The response of the logarithmic mode was investigated at various settling times in order to determine the transient performance. Figure 6.19 shows a plot of the output codes against a uniform illuminance for settling times of 43μs, 86μs, 172μs and 258μs. The logarithmic dependence ends at a higher illuminance level as the settling time is decreased.

To estimate the photo-current, the output during column calibration was used as a reference

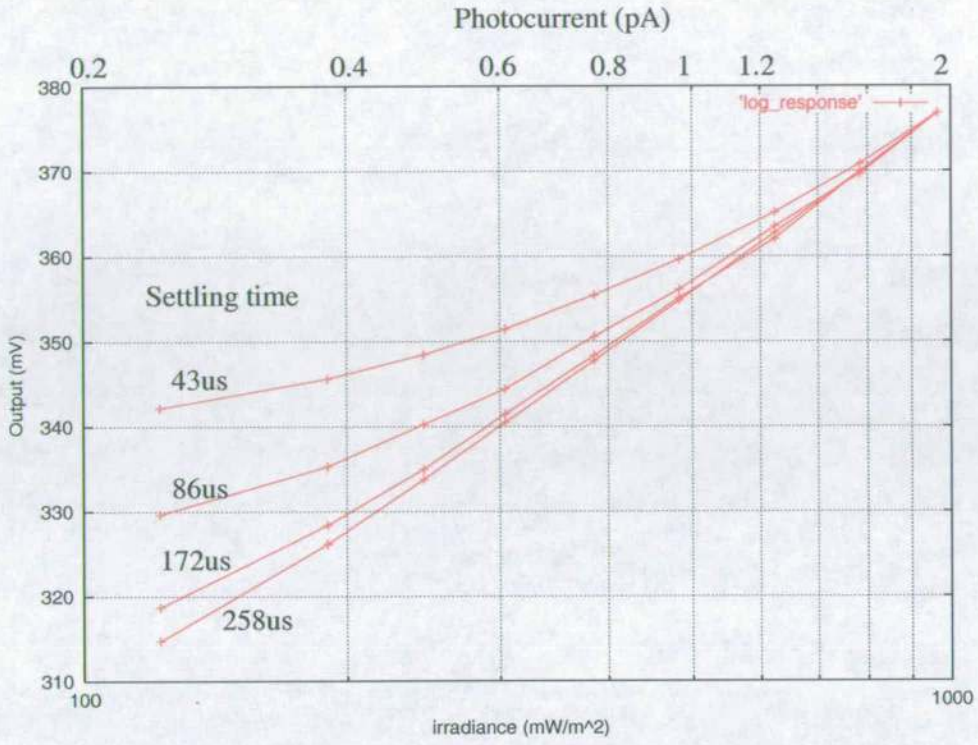


Figure 6.19: *Logarithmic response for varying settling times.*

point. For a settling time of 43μs the logarithmic response was not apparent below about 700mW/m^2. The difference in output between an image captured under a constant irradiance of 700mW/m^2 and an image captured when a reference current was pulled through the logarithmic compression device was found to be 315 codes. Given the logarithmic response of 100 codes/decade this represents 3.15 decades. Assuming the reference current was 2nA (although this could vary by $\pm$30%), the photo-current generated by an irradiance of 700mW/m^2 is 1.4pA. This result is close to that predicted in Section 5.3.2.

700mW/m^2 is a relatively high illumination level in relation to the photo-current and equates to almost 500 lux (multiply W/m^2 by 683). Table 1.1 from Chapter 1.1 relates this value to some typical conditions. The main reason for this is likely to be the size of the photodiode area. As the light sensing area reduces, more light is required to achieve the same photo-current. Although the logarithmic response can extend down to lower currents, the settling time is greatly increased. Another reason for the high relative illumination level could be the density of metal in the pixel. From the cross section view of Figure 6.20 it can be seen that as the angle of incident light deviates from being perpendicular to the silicon surface, it will at some point be reflected and not reach photodiode. This effect worsens as the height of metal in the pixel

increases. Investigation of different structures would be required to optimise the pixel response.

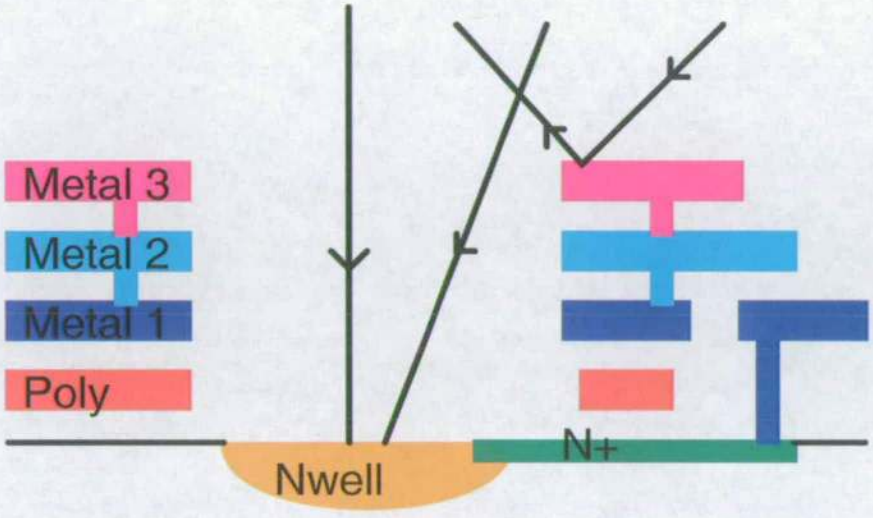


Figure 6.20: *Cross section view of pixel.*

6.3.5 Dynamic Range

The dynamic range in logarithmic mode increases as the settling time is extended. It is thus necessary to define the dynamic range in relation to the operating frequency. The maximum signal was taken to be 28nA which was the highest programmable current during column calibration. The lowest signal was taken to be 1.4pA which is the photo-current that permitted settling in less than 60μs (including initial voltage ramp) and was found from Figure 6.19. These measurements give a **logarithmic dynamic range of 4.25 decades**.

6.4 Combined Linear-Logarithmic operation

A limited system was implemented in the FPGA which enable combined linear-logarithmic images to be streamed in real-time. The logarithmic data was calibrated using offset calibration performed on-chip then the decision on whether to output the linear or the logarithmic data was done in the FPGA.

6.4.1 Combining Data

Chapter 3 stated that gain had to be applied to the logarithmic data before it was substituted for saturated linear data. This section looks in more detail at the gain required. The set of curves shown in Figure 6.21 show linear and logarithmic data plotted against the illumination level.

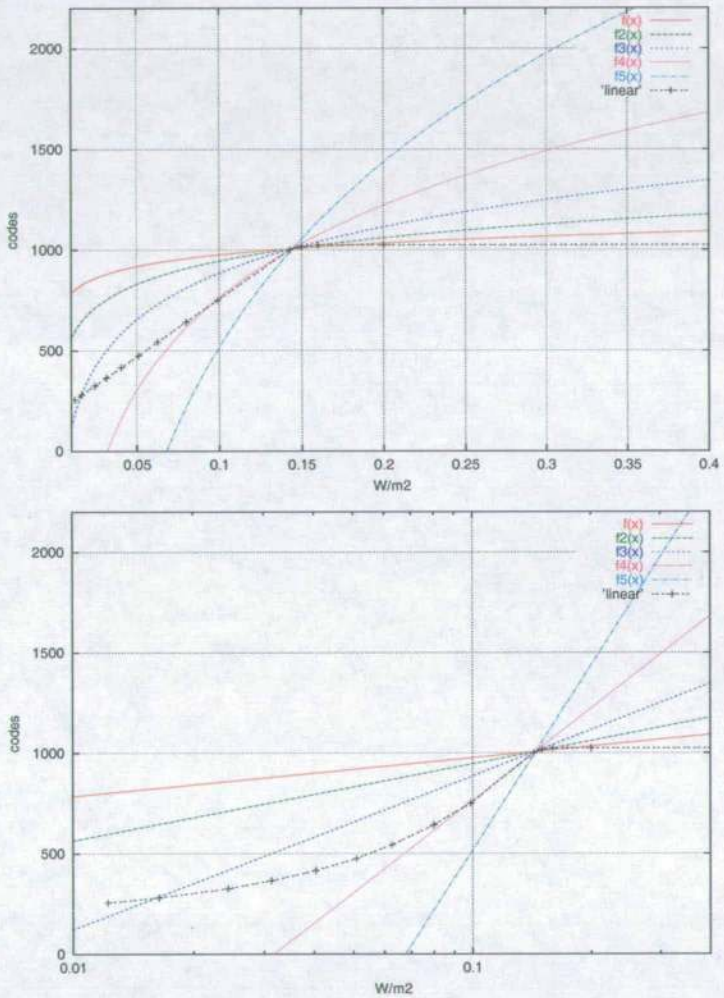


Figure 6.21: *Logarithmic curves fitted to linear data at a stitching point of 1000 codes. f(x), f2(x), f3(x) and f4(x) represent logarithmic data with gains of 2, 4, 8 and 16 respectively.Top graph plotted on linear x-axis, bottom graph on logarithmic x-axis.*

The linear data was captured under a set exposure and shows the expected response until it saturates at 1024 codes. A curve of the form $y = A\ln(Bx) + C$ was fitted to logarithmic data before further gains and offset were applied. The four curves, f(x), f2(x), f3(x) and f4(x), represent the fitted logarithmic curve with gains of 2, 4, 8 and 16 respectively. The logarithmic curves' DC levels were adjusted such that they intersected the linear data at 1000 codes which

was set as the stitching point. It can be seen that the curve with an applied gain of 16 best matches the linear slope at the stitching point. The gain could be more precisely fitted but the change observed in the image would not be significant.

A reduction in the exposure time reduces the slope of the linear data causing it to saturate at a higher illumination level. For a 16 times reduction in the exposure the logarithmic data with a gain of 16 still provided a good match to the linear slope at the stitching point. To better see the effect of different logarithmic gains, six sample images are shown in Figure 6.22. Each image shows linear data except for the top right section which has logarithmic data. Each image is displayed at its full scale (i.e. the minimum code will be black and the highest code white in greyscale) thus as the logarithmic gain is increased its data covers a greater proportion of the codes compared with the linear. This causes the linear data to appear darkened. The image with the logarithmic data gained by 16 provides a good balance between the contrast in the two sets of data.

6.4.2 Power consumption

The power consumption when operating at a 12MHz pixel frequency is shown in Table 6.2. There is an increase of approximately 25% between linear and logarithmic modes of operation. This can be attributed to the column amplifiers that are only connected during logarithmic mode (or the calibration modes).

	Operating Mode			
Circuitry	Linear	Logarithmic	Column calibration	Ramp calibration
digital	5.22mW	5.22mW	5.22mW	5.22mW
analogue	66.58mW	84.37mW	86.42mW	82.51mW

Table 6.2: *Power consumption.*

6.4.3 Frame rate

The Frame rate achievable depends on the logarithmic calibration employed and is the same as that shown in Chapter 5.8. When employing offset calibration of the logarithmic mode, combined linear-logarithmic images can be streamed at 26 fps. When 2-parameter calibration of the logarithmic data is performed, the device can operate at 16 fps.

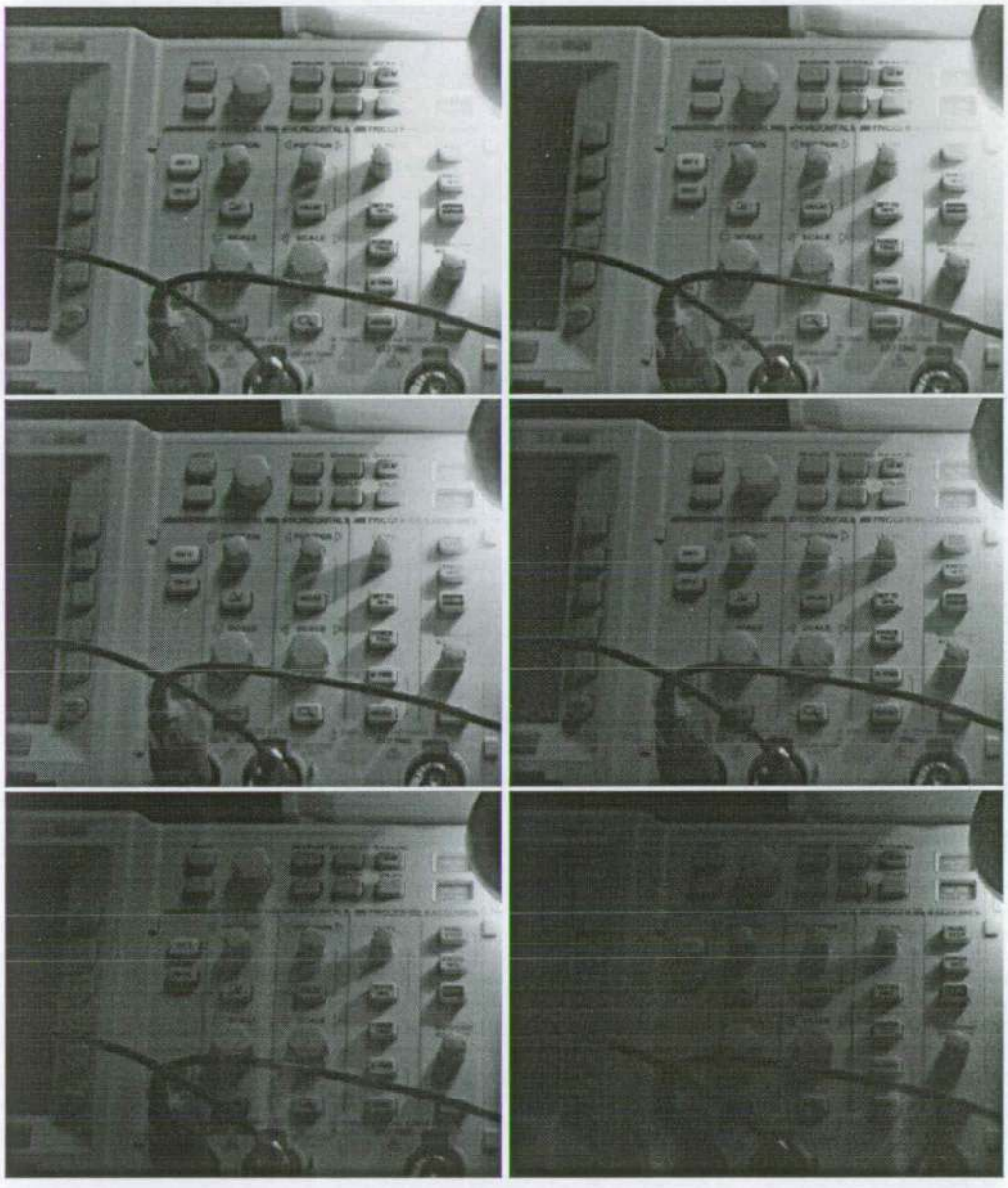


Figure 6.22: *Combined linear-logarithmic images with different gains applied to the logarithmic data. Following the images left to right and top to bottom the gains are 1, 2, 4, 8, 16 and 32.*

6.4.4 Dynamic range

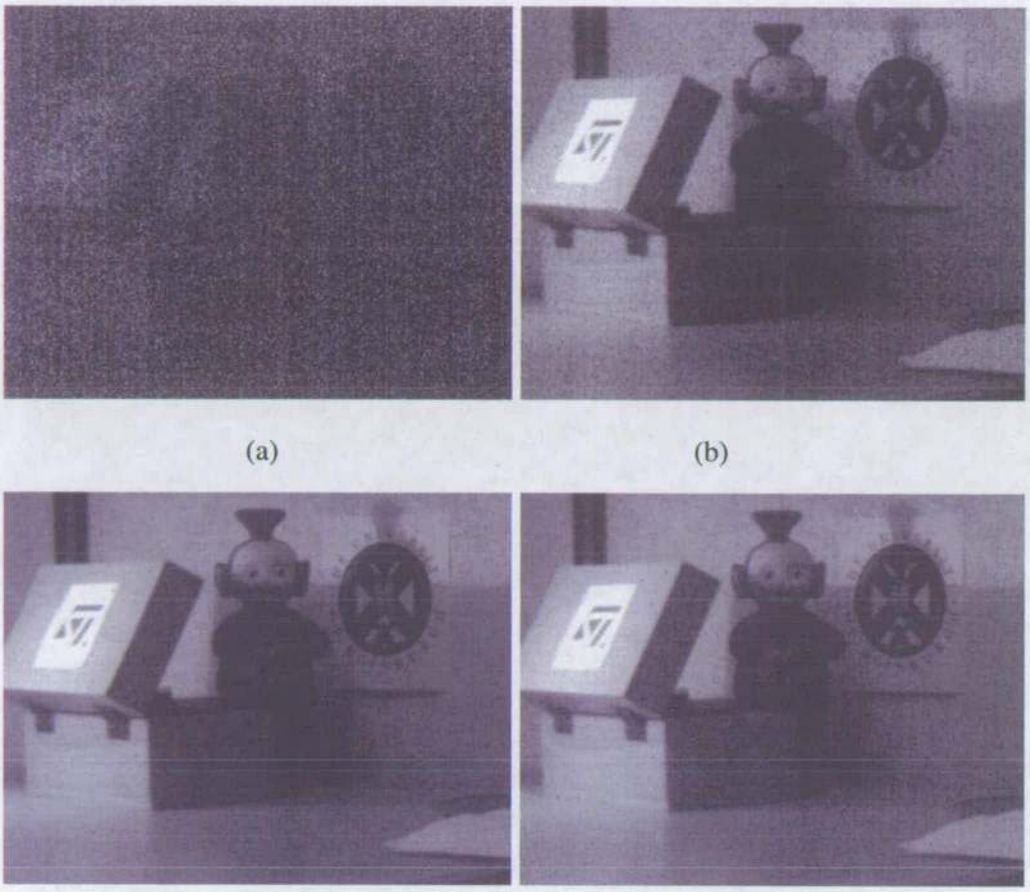
The dynamic range is not dependent on whether offset or two parameter calibration is performed. In both cases the logarithmic settling time is the same. The total dynamic range is found by adding the linear range to the logarithmic range for the given operating conditions. Using the results from Section 6.2.1 and Section 6.3.5 the total Dynamic Range is equal to:

$$\text{linear range} + \text{logarithmic range} = 58\text{dB} + 85\text{dB} = 143\text{dB} \tag{6.13}$$

In reality the full range will be slightly less than this because of the stitching algorithm used. The stitching point between the two sets of data will be just below the saturation point of the linear.

6.4.5 Images

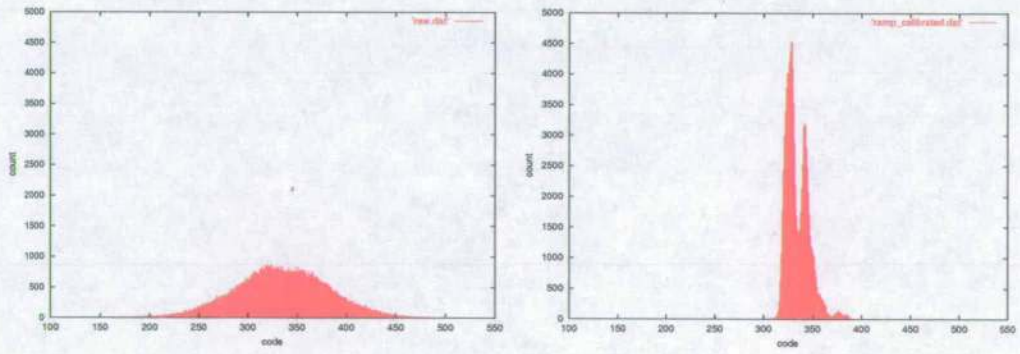
This section shows a collection of high dynamic scenes imaged by the test device. The advantage of combining logarithmic data with the linear should be apparent from the extra detail gained in a scene. Additionally, the effect of logarithmic calibration can be assessed qualitatively with regard to the images. Figure 6.23 begins by showing a scene captured in logarithmic mode. Image (a) displays the raw data before any calibration is applied. The scene is unrecognisable and not usable without correction. Figure 6.23(b) shows the image after offset calibration using the column current sources. The scene is now recognisable and the FPN has been considerably reduced. Offset calibration using the voltage ramp is shown in Figure 6.23(c) and displays improved FPN reduction to image (b). This is because the reference point generated using the voltage ramp is closer to the scene illumination level. The scene average was measured to be 340 codes whilst the reference points had an average value of 480 (voltage ramp) and 777 (column current sources). The histogram for the scene before and after calibration is shown in Figure 6.24. The photo-current can be estimated as in Chapter 6.3.4. If 777 codes equates to a reference current of 2nA, the scene induces an average photo-current of 85fA. Obviously this illumination required an extended settling period for the logarithmic mode. For the logarithmic mode to settle at such illumination levels and maintain a frame rate approaching 30fps an increased responsivity would be required. However, it was not intended for the logarithmic mode to be used at lower illumination levels. Such levels would be imaged by the linear mode.



(a) (b)

(c) (d)

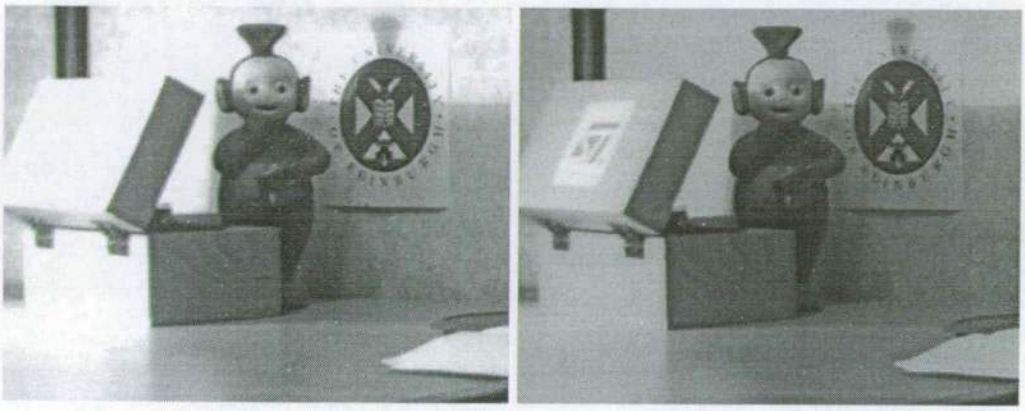
Figure 6.23: *(a)Raw logarithmic image, (b)offset calibration with column reference point, (c)offset calibration with ramp generated calibration point, (d)2-parameter calibration using column and ramp generated reference points.*



(a) (b)

Figure 6.24: *(a)Raw image histogram, (b) Histogram after offset calibration with the ramp generated reference point.*

The scene of Figure 6.23 captured in linear mode is shown in Figure 6.25(a) and the combined linear-logarithmic image in (b). The logarithmic data substituted was FPN corrected using offset calibration with the voltage ramp reference point. The superior SNR in the linear data is evident in comparison to Figure 6.23.



(a) (b)

Figure 6.25: *(a)Linear image, (b) Combined linear-logarithmic image.*

Figure 6.26 is used to show the effect that temporal noise has on the logarithmic mode of operation. The scene shows an oscilloscope, of which the top right is illuminated by a desk lamp. The raw logarithmic image is shown in Figure 6.26(a) and the other images show the scene after offset or two-parameter calibration. In each case the calibration was performed on a single frame of data and on an average of 30 frames. Images (b) and (d) from Figure 6.26 show a single frame after calibration whilst images (c) and (e) show an average of 30 frames after calibration. It is clear that the temporal noise greatly degrades the calibrated image. As was shown in Section 6.3.3 the temporal noise is greater than the level to which the FPN can be corrected.

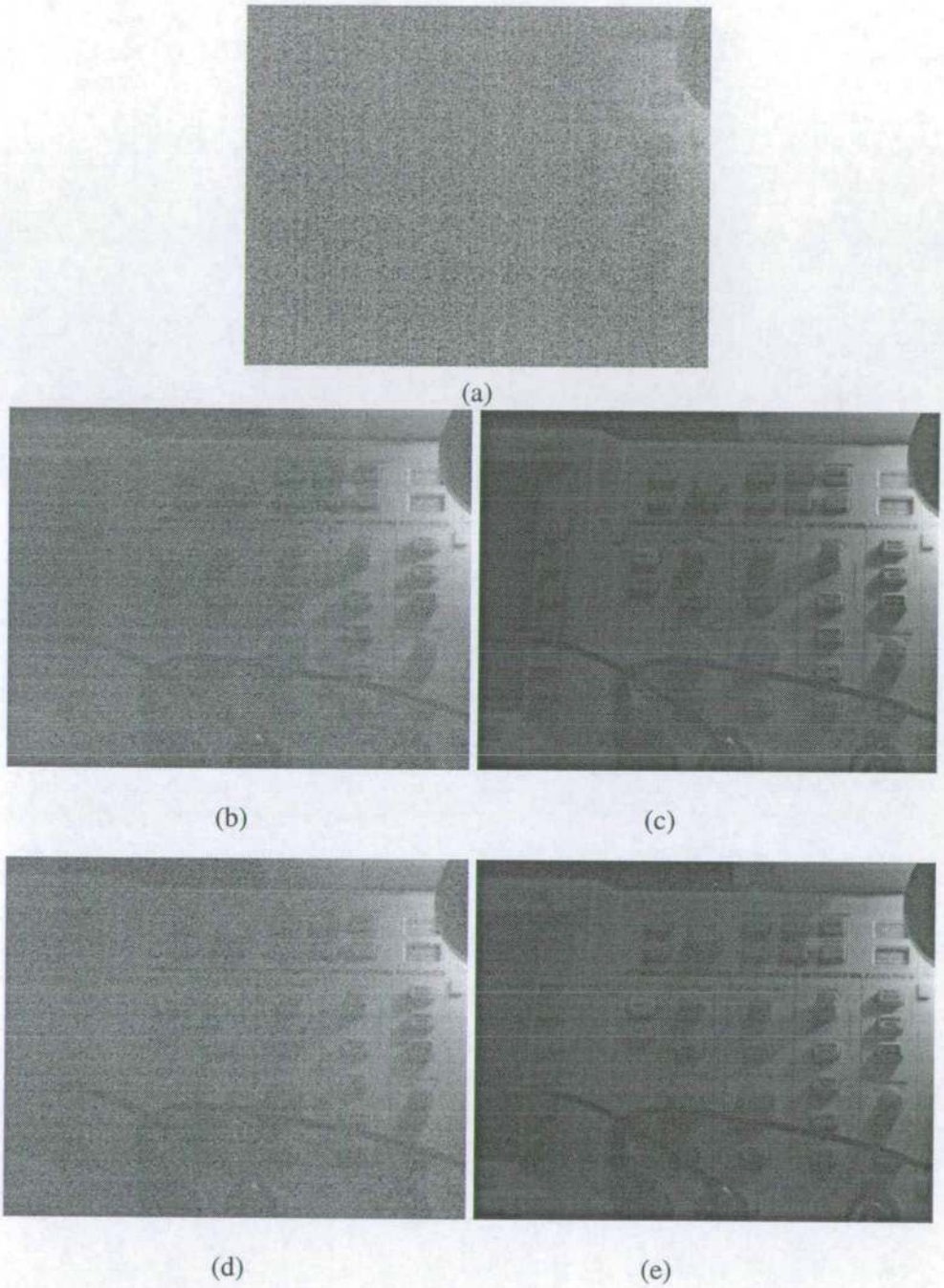


Figure 6.26: *Images in Logarithmic mode: (a)Raw image, (b) offset calibration using ramp (single image), (c) offset calibration using ramp (30 frames average), (d)two-parameter calibration(single image), (e)two-parameter calibration (30 frames average).*

The test device was designed to image high dynamic range scenes, however, the linear mode exhibits breakdown at high levels of incident illumination. The effect is shown in Figure 6.27 where a desk lamp was placed about a meter away from the sensor. The filament of the bulb appears darkened even though it is the brightest part of the scene. In fact it is the extreme intensity that has caused the double sampling scheme to breakdown.

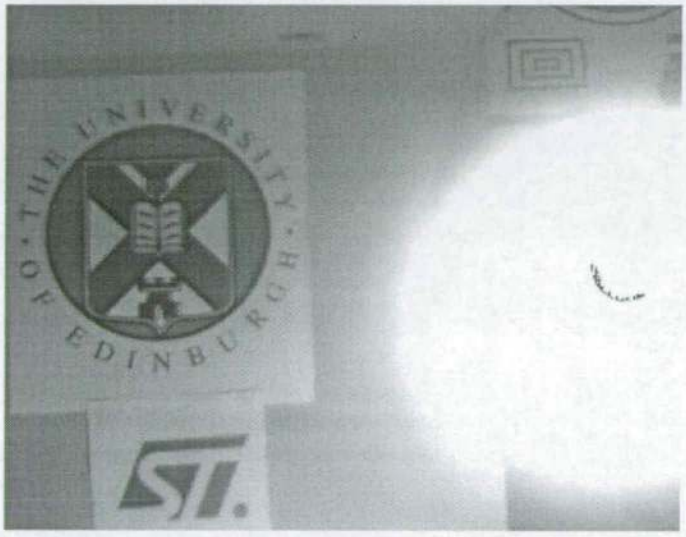
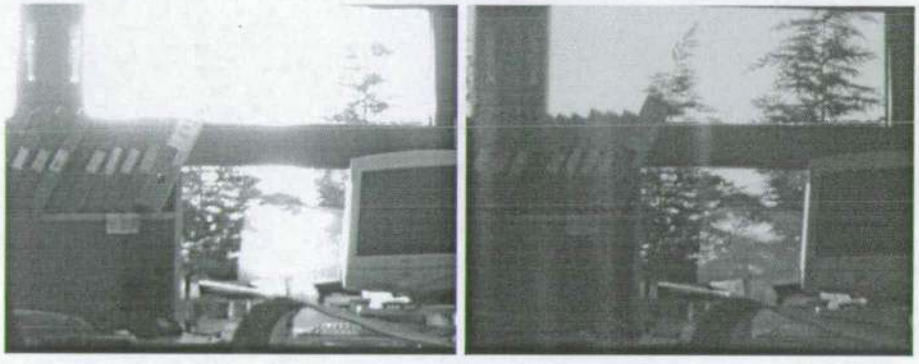


Figure 6.27: *Linear image showing solarization or the black bulb effect.*

The breakdown mechanism is described as follows: The double sampling scheme first samples the signal level, and in the region of the lamp the pixel will have fully discharged. The sample representing the black or reset level is taken very shortly after the pixel is released from reset. However, if the incident illumination is very high, this time period will be sufficient for the pixel to fully or partially discharge. The voltage difference converted by the ADC can therefore be reduced giving a false grey or black pixel value. The effect described is sometimes referred to as solarization or the black bulb effect. Although the mechanisms responsible are thought to be well understood no literature could be found on the phenomenon. A clamping circuit situated in the column can be used to prevent high intensity scenes from appearing reversed. When the reset (or black) level is sampled the clamp will stop the column voltage falling below a set level. Without the clamp circuit a combined linear logarithmic image from the sensor still displays the breakdown. Logarithmic data is only substituted for linear data that has saturated (or close to) thus the black bulb area is not altered. Figure 6.28 shows the scene when the logarithmic data has been substituted for the linear(excluding the black bulb). The filament of the bulb was estimated to generate a photo-current greater than 500pA.

Figure 6.28: *Combined linear-logarithmic image of Figure 6.27.*

Figure 6.29 shows a scene encountered everyday. From inside the office the sensor is pointed toward the window.



(a) (b)

(c)

Figure 6.29: *Window scene (a)Linear image, (b)logarithmic image, (c)combined linear-logarithmic image.*

The illumination range between the indoor office and the outdoors is higher than the linear mode can capture. A reduction in the integration period would lose detail of the objects situated inside. The combined linear-logarithmic image clearly retrieves the detail of the trees without affecting the indoor data.

6.5 Conclusions

The sensor was found to be fully functional in both linear and logarithmic modes enabling a full characterisation. The linear mode performance matched that expected in almost all areas, the exception being the pixel capacitance which was slightly larger than predicted. This has been attributed to an non-optimised layout.

In Logarithmic mode the response of 80mV/decade was a very close match to that predicted from simulation. A similar result was found for the transient response which could settle for photo-currents as low as 1.4pA in a 60us period (including initial voltage ramping).

The simulation of the majority of analogue blocks with accurate models has shown a good correlation with the measured data. However, there are effects that are less easily predicted. For example, FPN due to process variation (especially for minimum sized devices) is far more difficult to predict. This was the case for the on-chip reference generation schemes particularly the in-pixel scheme which relied on the matching of the capacitance on a small node. However, the voltage ramping scheme was shown to provide a matching across array of 2% which is sufficient to greatly reduce the FPN. Using offset and 2-parameter calibration algorithms the FPN was reduced to the level achieved using uniformly illuminated images as the reference.

The relative illumination required to generate photo-currents spanning the usable logarithmic range is quite large. This is the result of a non-optimised pixel and small photodiode area and will worsen if the pixel area is shrunk further.

In the test device temporal noise was shown to be the dominant noise source. The cause of this has been identified and solutions (verified by simulation) have been proposed. With these changes it should be able to reduce temporal noise below the level of FPN.

It has been shown that combining linear and logarithmic data in a single image can widen the dynamic range. A number of images have demonstrated this ability. Dynamic range can be extended to over seven decades whilst maintaining the maximum frame rate of 26fps.

Chapter 7
Summary and Conclusions

This thesis has investigated a method to extend the dynamic range of a CMOS image sensor with minimal overhead added to the overall imaging system. This was achieved by combining linear and logarithmic data,within the readout path of the sensor, in the same image. Logarithmic sensors suffer from FPN that renders a raw image unusable unless some form of correction is applied. Chapter 3 built on previous calibration work on logarithmic sensors and investigated two schemes that could be implemented in a real-time system. It used actual data from a CMOS sensor configured in logarithmic mode. For offset calibration it was found that the effectiveness of the correction was dependent on the distance between the reference point and the illumination level. However, a closely matched reference point and illumination level can not be achieved for all pixels when a high dynamic range scene is imaged. The second scheme, two parameter calibration, consistently reduced FPN if the reference points were either side of the illumination point. This created a challenge to design suitable on-chip reference generation schemes.

The second part of Chapter 3 combined linear and logarithmic data from the same scene into a single image. The combination used a simple boolean substitution of logarithmic data for linear data above a certain threshold. The threshold was set just below the linear saturation level such that valid linear and logarithmic data could be compared and a mapping created between the two data sets.

Chapter 4 compared two logarithmic arrangements in terms of sensitivity and response time. These two characteristics were studied since an improvement in sensitivity increases the signal to noise ratio whilst the response time is important for operation in a real-time system. Simulation results suggested feedback round the conventional logarithmic arrangement would improve the transient performance and the sensitivity.

Chapter 5 provided details on the design of a combined linear-logarithmic test device. A new pixel architecture was implemented to realise the new logarithmic arrangement (based on the results from Chapter 3 and the simulations of Chapter 4) as well as the linear scheme. In

addition to a set of column current sources to generate a logarithmic reference point, a novel means of calibrating the logarithmic mode with a voltage ramp was implemented.

The characterisation results from the test device were presented in Chapter 6. The chip was fully functional in linear and logarithmic mode and achieved a dynamic range in excess of 7 decades when the data was combined.

7.1 Critical discussion

To the author's knowledge this is the first work which combines linear and logarithmic data in the same image. As has been shown in Chapter 6 the test device has been fabricated and effectively demonstrated on high dynamic range scenes. The main advantages are:

- High Dynamic Range at 26fps.
- FPN reduction in logarithmic mode with on-chip calibration schemes.
- No frame memory required for combining data or logarithmic calibration.
- Competitive pixel size.

Disadvantages

- Visible difference in SNR between linear and logarithmic data.
- Increased temporal noise in logarithmic mode.
- Reduced frame rate if 2-parameter logarithmic calibration employed.

The dynamic range has been extended up to about seven decades by substitution of logarithmic data for saturated linear data. This was made possible by addressing two of the main drawbacks in a conventional logarithmic sensor: FPN and settling time. Two on-chip reference generation schemes were used to calibrate the logarithmic data whilst the inclusion of feedback round the pixel greatly improved the transient response compared to a conventional logarithmic arrangement. By situating the logarithmic amplifier in the column and switching it between rows a small pixel pitch was maintained.

To correct FPN a two-parameter correction algorithm was investigated in addition to simple offset calibration. The higher order correction was effective if the reference points could be situated at the maximum and minimum operating levels. The novel use of a voltage ramp and feedback meant low reference currents were achievable in a usable settling time. The extra read outs required for 2-parameter calibration did however reduce the frame rate.

It is reasonable to ask if the reduction in FPN achievable with two-parameter calibration is worth the increased memory requirements and reduction in frame rate? The answer really depends on what is more important in the application. However, in the current design, temporal noise is the dominating noise source thus there is no advantage in further improving FPN from that achievable with offset calibration.

Temporal Noise would have to be improved before the full benefits of the FPN reduction schemes could be seen. Solutions to reduce the noise level have been proposed, namely increasing the dimensions of the noise generating devices and/or increasing the photodiode area. Unfortunately both solutions would increase the pixel pitch.

If low noise is the most important parameter in an application it is unlikey the linear-logarithmic device would be suited. This is mainly due to the low SNR of the logarithmic data. However, if image quality is not critical it may be a viable option. The characterisation of the linear-logarithmic system has enabled a comparison with other systems also aimed at high dynamic range imaging. Firstly, when compared to a multiple capture scheme it compares unfavourably in terms of frame rate, colour sensing, pixel size and SNR. However, the overhead requirements of the linear-logarithmic system are likely to be lower than that of a multiple capture system. To image a wide range of illumination in a multiple capture system the ratio of the longest integration time to the shortest needs to be large. Increasing this ratio also increases the memory requirement as a greater number of pixel values need to be stored. The avoidance of a frame memory can greatly reduce the system cost if the frame memory is to be implemented on-chip.

When a well adjustment scheme is compared to the linear-logarithmic system its simplicity makes it a more attractive option. A smaller pixel pitch is achievable and no extra memory or processing is required. A superior SNR is also likely to be achievable. In terms of colour processing both the well adjustment and the combined linear-logarithmic system produce a non-linear response which is not suited to current reconstruction algorithms. However, another limitation of the well adjustment scheme may be due to FPN. It was stated in [57] that the FPN

followed the shape of the transfer characteristic. Thus it is possible that FPN would worsen significantly if a wider dynamic range were captured. Published work on well adjustment schemes achieve a dynamic range of around 100dB which is significantly less than has been demonstrated by the linear-logarithmic arrangement.

A time to saturation scheme is also likely to provide images with superior SNR than could be achieved with the linear-logarithmic system. However, a time to saturation scheme will either suffer from an increased pixel pitch if the time stamping circuitry is located within each pixel or an irregular readout pattern and/or increased memory requirements if the time stamping is performed outwith the pixel. It is thought that the linear-logarithmic scheme would offer either a reduced pixel pitch or lower memory requirements than the two possible configurations of time to saturation.

7.2 Improvements

By improving the SNR of the logarithmic data the substitution areas in a stitched image should become less visible. At the same time the effect of FPN would also be decreased. Increasing the output voltage per decade change in illumination has previously been achieved by stacking devices and thus increasing the number of gate-source voltage drops. A different method of increasing the logarithmic response was shown in Chapter 4. The scheme connected the bulk of the logarithmic converting device to its source to prevent the body effect. It was not adopted due to the resulting increase in pixel capacitance.

At a later date it was thought to investigate the effect of altering the bulk voltage of the logarithmic converting device. Table 7.1 shows the voltages simulated for the two circuits from Figure 4.3 in Chapter 4.

	V_{bulk}=0.2	V_{bulk}0.4	V_{bulk}0.6
circuit (a)	60mV	60mV	60mV
circuit (b)	87mV	91mV	96mV

Table 7.1: *Logarithmic response for intermediate bulk voltages of Figure 4.3.*

The Table shows an increase in sensitivity for circuit (b) as the bulk voltage was raised toward the source voltage (The source voltage was 0.7V in circuit (b)). This shows that as the potential between the source and bulk was reduced, the logarithmic response increased. No such increase was found for circuit (a). The increased logarithmic response could be realised in two ways:

1. Place the logarithmic converting device in its own well and regulate the supply of the well. However, this would increase the pixel size considerably and care would need to taken to avoid latch-up.

2. Adjust the feedback amplifier such that the reverse bias of the photodiode is reduced. This would require a new amplifier design with a PMOS input stage to accommodate the input common mode but should be possible.

A smaller scale improvement would be to remove the column current sources, column line and device *M4* from within the pixel. Thus all reference currents would be generated from the voltage ramping scheme. This would improve the pixel fill factor. The change would require verification of reference currents at the increased ramp rates which is currently not possible due the slow column buffer.

7.3 Future Work

It is the author's view that future research into a combined linear-logarithmic CMOS image sensor should focus on 3 main areas:

1. Logarithmic response.

2. Dynamic Range.

3. Frame rate.

By extending the logarithmic voltage swing for a given illumination range, the effect of FPN could be reduced. This increase of SNR of the logarithmic data would improve the continuity of a combined linear-logarithmic image. A possible method of achieving this was described in the previous section.

An even wider dynamic range would be possible if the logarithmic settling time were improved. If the logarithmic mode were able to settle for lower photocurrents then the linear mode's maximum exposure could be increased.

The final area of investigation would be operating speed. The current architecture is limited to a maximum frame rate due to the logarithmic settling time required and the multiple ADC cycles.

If it was possible to operate a pixel such that the logarithmic data was available at the same time as the linear, the operating speed could be considerably increased. This could be achieved if the photo-current could be made to flow through the logarithmic converting devices prior to accumulating charge at a given node. Consider the simple example shown in Figure 7.1.

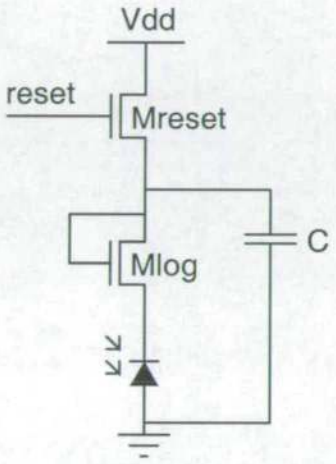


Figure 7.1: *Possible circuit to enable linear and logarithmic readout concurrently.*

The capacitor would be reset to *Vdd* via *Mreset* then would discharge at a rate dependent on the photo-current generated. A non-zero value for *reset* when in its low state would prevent the capacitance fully discharging thus always permitting a logarithmic result to be read. The logarithmic result would be the difference between the voltage on the capacitor and the photodiode voltage.

It may then be possible to place the decision circuitry to select linear or logarithmic data in the analogue domain thus reducing the number of ADC cycles required. Obviously some means of creating the mapping between the two sets of data would be required.

7.4 Concluding remarks

The inherent capability of a logarithmic sensor to image scenes of a wide dynamic range will continue to attract research. This thesis has developed a sensor architecture which employs a logarithmic response only under increased illumination levels where its performance is maximised. The well known drawbacks of FPN and response time have been addressed and improved. The result is a CMOS sensor capable of imaging a wide dynamic range by the on-chip combination of linear and logarithmic data.

Appendix A
Verilog coding for FPGA

The timing of the digital signals for all connections shown in Figure 5.29 were coded in Verilog and downloaded to the FPGA. To permit flexibility, a number of parameters were made programmable via the I^2C interface to the FPGA. The I^2C connections are shown in Figure A.1.

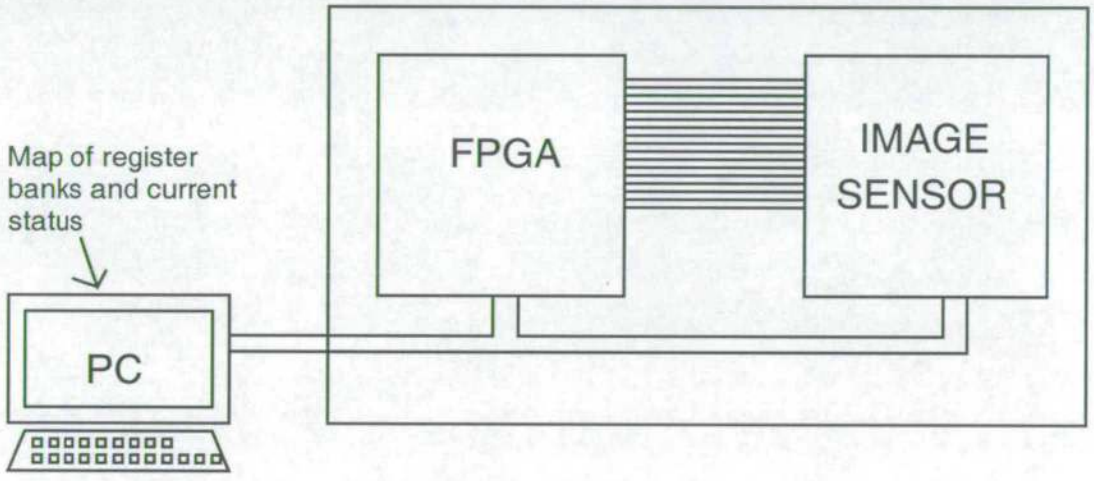


Figure A.1: *I^2C connections.*

A chart showing the main verilog modules is shown in Figure A.2. The top level contains all the connections to the test device and the mapping of the ports on the FPGA. Beneath this the modules are split into 4 main blocks: clock generation, I^2C interface, CAB driver and output coding.

- **clk generator:** generates the main clock from the crystal input source.
- **I^2C interface:** allows the user to change parameters within the timing. This alows greater flexibility during test as less signals need to be hard coded into the FPGA. THE I^2C block is further split into two sections which code/decode the data and store all the internal register values.
- **CAB driver:** This block contains the main line and frame timing signals. Generates timing for pixel, Y-decoder, column readout, ADC, X-decoder.

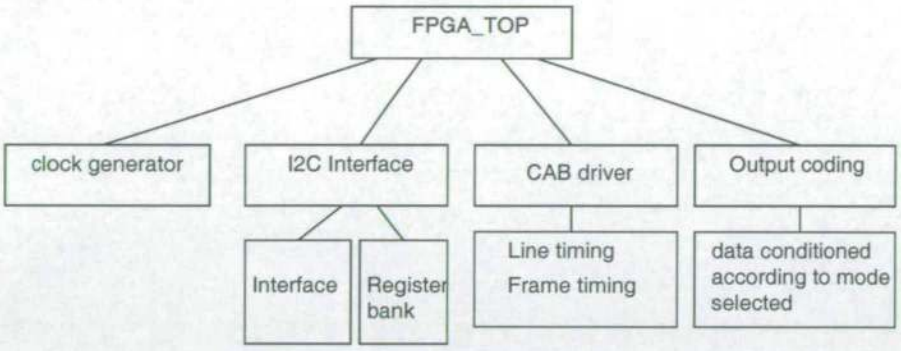


Figure A.2: *FPGA coding hierarchy.*

- **output coding:** Dependent on the operating mode of the pixel the ADC data is conditioned for display. Combination of linear and logarithmic data is also performed here if selected.

As an example of the Verilog code generated, Figures A.3 to A.5 show the output coding block that controls the linear-logarithmic substitution.

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```
////////////////////////////////////////////////
// Module to take linear data then calibrated
// log data and perform substitution where
// necessary.
// Linear data will need to be stored in line memory.
// linear enable, log_enable and log_calcol_enable need to be high.
//
// mode_sequencer = 2'd0: LINEAR MODE IN PIXEL
//                        -Converting log calibrated data, reading out rubbish
//                  2'd1: LOG MODE IN PIXEL
//                        -Converting linear data, reading out calibrtaed log dat
a
//                  2'd2: LOG CALCOL MODE IN PIXEL
//                        -Converting rubbish, reading out linear data
//
// Data comes in as 11 bits but has been clipped at 10 bits (1023 codes)
// Therefore there is an extra bit available for the log data to
// extend above the linear.
//
// Version2: Calculates log offset by averaging all the log
//           pixel values whose linear values are nearest to the linear
//           saturation level.
//
//
module simple_linlog (
                data_in,
                clk_gcc,
                pix_enable,
                reset_n,
                mode_sequencer,
                enable_linlog,
                data_out,
                lin_sat_level,
                xga_binary,
                field_end,
                lin_flag,
                enable_fixed_log_offset,
                fixed_log_offset_value,
                lin_fixed_sub_level,
                prev_mode_delay2,
                reset_linlog_params,
                yga_read_val
                );

input   clk_gcc,
        pix_enable,
        reset_n,
        enable_linlog,
        field_end,
        enable_fixed_log_offset,
        reset_linlog_params;
input [1:0] mode_sequencer,
            prev_mode_delay2;
input [8:0] xga_binary,
            yga_read_val;

input [10:0] data_in,
             lin_sat_level;

input [9:0] fixed_log_offset_value,
            lin_fixed_sub_level;

output [10:0] data_out;
output lin_flag;
```

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Figure A.3: *Example code: Linear-logarithmic substitution(page 1).*

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```
////////////////////////////////////////////
reg [10:0] new_log_offset, new_substitution_level,
          substitution_level, log_offset;
reg [10:0] data_out;
reg [10:0]    linear_data [(362-1):0]/* synthesis syn_ramstyle = "block_ram */;
integer log_accum, log_count;
////////////////////////////////////////////

always @(posedge clk_gcc or negedge reset_n)
        if (!reset_n)begin
                new_log_offset <= 11'd0;
                new_substitution_level <= 11'd0;
                data_out <= 11'd0;
                log_accum <= 0;
                log_count <= 0;
                end
        else if(reset_linlog_params) begin
                // Needs to be asserted longer than field time
                // so log_offset and substitution_level are updated.
                new_log_offset <= 11'd0;
                new_substitution_level <= 11'd0;
                data_out <= 11'd0;
                end
        else if(pix_enable) begin
                if(enable_linlog) begin
                        if(prev_mode_delay2 == 2'd0) begin
                                linear_data[xga_binary] <= data_in;
                                data_out <= data_in;
                                end
                        else if (prev_mode_delay2 == 2'd2 || prev_mode_delay2 ==
 2'd3) begin
                                // Do not use border rows or columns to create lin
log mapping.
                                if(yga_read_val > 9'd4 && yga_read_val < 9'd284) b
egin
                                  // if linear data is nearer saturation than curr
ent substitution level
                                  // then create new log mapping offset.
                                  if (linear_data[xga_binary] > substitution_level
 && linear_data[xga_binary] < lin_sat_level && xga_binary > 10'd4 && xga_binary
<10'd356) begin
                                                if(linear_data[xga_binary] > data_in) be
gin
                                                        if(linear_data[xga_binary] > new
_substitution_level) begin
                                                                new_log_offset <= linear
_data[xga_binary] - data_in;
                                                                new_substitution_level <
= linear_data[xga_binary];
                                                                log_accum <= data_in;
                                                                log_count <= 1;
                                                        end
                                                        else if(linear_data[xga_binary]
== new_substitution_level) begin
                                                                log_accum <= log_accum +
 data_in;
                                                                log_count <= log_count +
 1;
                                                        end
                                                end
                                  end
                                end
```

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Figure A.4: *Example code: Linear-logarithmic substitution(page 2).*

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```
                                ////////////////////////////////////////////////
//////////////
                                // Substitute log data for linear if linear satu
rated       //
                                // if fixed_log offset selected then user has co
ntrol of    //
                                // substitution level and offset applied to log
data.       //
                                ////////////////////////////////////////////////
//////////////
                                if (enable_fixed_log_offset) begin
                                        // Use fixed log offset and fixed substi
tution level
                                        if (linear_data[xga_binary] > lin_fixed_
sub_level)
                                                data_out <= (((data_in + fixed_l
og_offset_value) < 11'd2047)? data_in + fixed_log_offset_value:11'd2047);
                                        else
                                                data_out <= linear_data[xga_bina
ry];
                                end
                                else if (linear_data[xga_binary] > substitution_
level)
                                        data_out <= (((data_in + log_offset) < 1
1'd2047)? data_in + log_offset:11'd2047);
                                else
                                        data_out <= linear_data[xga_binary];
                                end
                        else
                                // invalid data o/p zero
                                data_out <= 11'd0;
                        end
                else
                        // LINLOG combination not selected
                        data_out <= data_in;
                end
reg lin_flag;
always @(negedge field_end)
        if(!reset_n) begin
                log_offset <= 11'd0;
                substitution_level <= 11'd0;
                lin_flag <= 1'b0;
                end
        else begin
                log_offset <= new_substitution_level - (log_accum/log_count);
                substitution_level <= new_substitution_level;
                lin_flag <= 1'b1;
                end

endmodule
```

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Figure A.5: *Example code: Linear-logarithmic substitution(page 3).*

Appendix B
Publications

1. G.G. Storm, J.E.D. Hurwitz, D. Renshaw, K.M. Findlater, R.K. Henderson, M.D. Purcell, "High Dynamic Range Imaging using Combined Linear-Logarithmic Responses from a CMOS Image Sensor", *Workshop on Charge-Coupled Devices and Advanced Image Sensors*, Elmau Germany, May 2003

2. G.G. Storm, J.E.D. Hurwitz, D. Renshaw, K.M. Findlater, R.K. Henderson, M.D. Purcell, "Combined Linear-Logarithmic CMOS Image Sensor", *International Solid-State Circuits Conference*, P6.5, pp 116-117, Feb 2004

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