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# Extended Multilevel Inverter Topology With Reduced Switch Count and Voltage Stress

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**ABSTRACT** For the applications related to the medium/high-power/voltage, Multilevel inverters (MLI) are widely accepted and commercially used. The performance of MLI compare to the conventional two-level inverters is significantly superior due to the insignificant amount of harmonic distortion, lower filter size, requirement of low voltage rating devices, lower electromagnetic interference, etc. However, there are a few disadvantages such as an increased number of components, a complex modulation and control strategy, and issues related to the voltage balancing of capacitors. The present paper proposes a new topology with a lower voltage rating component to improve the performance by remedying the mentioned disadvantages. Compared with existing inverter topologies, (especially higher levels), this topology requires fewer components, fewer dc sources, and gate drives. Further, voltage stress is also low. The overall costs and complexity are therefore greatly reduced, especially for higher voltage levels. The proposed topology has been compared with other similar topologies and the comparison proves the better structure of the proposed topology. To show the working of the proposed topology, a prototype has been developed and tested for a different operating condition with two different modulation techniques. All the results show the adequate performance of the inverter topology at the different real-time environment.

**INDEX TERMS** Multilevel inverter, PWM technique, higher level, reduced switch count.

## I. INTRODUCTION

Multi-level Voltage Source Inverters (MVSIs), known as the 'Rising Power Converter' has been used in a wide variety of high and medium voltage applications during the last decades. Compared with the conventional two-level topologies, this new type of DC-AC converter provides numerous advantages in terms of its high output voltage generation using lower voltage rating devices, lower dv / dt stress, low switching power losses, less input current distortions, and so on [1]–[4]. These attractive features together with the growth of power semiconductors have led to the interface between renewables photovoltaic systems and the utilities using MVSIs for various applications [5], [6].

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The first multi-level topology with separate DC sources was established as a cascaded H-bridge (CHB) in the mid of 1970s. In 1980s, the three-level and five-level Neutral Point Clamped (NPC) structure has been proposed using one DC source. In the 1990s, Flying Capacitor (FC) was introduced which is regarded as the third topology in the classical category of the multilevel inverter topologies. While previously MVSIs were notable to researchers and have been widely used in industrial applications for the past decades, it remained a challenge to develop new, hybrid symmetric or asymmetrical structures to generate more voltage levels that count less components [7]–[9].

The main concerns of NPC and FC include voltage balance, need for a large number of diodes/capacitors, module failure liability due to serial switch connections. Multiple DC source-based CHB gains a strong interest compared to

these single DC MLIs due to their modularity and reliability. Furthermore, symmetric CHB have easier control, while asymmetric topologies can increase the number of levels considerably with a lower device count [10], [11]. However, the CHB required more number of isolated DC voltage sources. The requirement of more semiconductor switches and DC sources is the main constraint for the early proposed MLI. Continuous research has been done in recent years to improve the MLI configuration in all possible ways. Three different varieties of MLIs are investigated, for example, switched DC MLIs, switched-capacitor MLIs, and switched-diode MLIs [12]–[14]. In [15], a symmetric switched DC configuration was suggested with a decreased number of components compared to the traditional circuitry. The backend H-bridge is not used in this topology, hence the voltage stress is on the lower side, however, it still requires isolated sources similar to the CHB for higher voltage level generation. The structures proposed in [16], [17] are modest and cost-effective in the switched DC category. Inherently, these reduced device count topologies can produce both positive and negative polarity of the voltage. Further, a higher number of voltage levels can be achieved by cascading the multiple fundamental units. Optimal structures are revealed in [18], [19] using the integrated H-bridge in the basic units that can generate 15 levels using 16 switches and 7 isolated dc sources. An extension is also possible to generate voltage levels that use different dc sources and with lower voltage stress on switches. In [20]–[22], symmetrical and asymmetrical topologies with different techniques of pulse width modulation (PWM) were introduced and tested. In [23]–[30], compact module topologies based on switched DC were evaluated in order to replace conventional MLIs.

In this paper, a high level of inverter configuration has been proposed. The proposed inverter topology is based on the reduced switch count concept. The proposed topology has been validated using both low and high switching frequency modulation techniques. The paper is organized as: In Section II, the basic module of the proposed topology with its extension has been elaborated. Section III explains the different modulation techniques. Section IV provides the power loss analysis. A detailed comparison has been provided in Section V and experimental results are provided in Section VI. The important outcome of the paper has been summarized in Section VII.

## II. PROPOSED HIGH-LEVEL INVERTER TOPOLOGY

### A. BASIC MODULE OF THE PROPOSED TOPOLOGY

Fig. 1 shows the basic module of the proposed topology. Three voltage sources with eight switches are the main components of the basic module. It consists of two modules with the left side being the high voltage (HV) module and the right side is the low voltage (LV) module. In the HV module, the magnitude of dc voltage sources is $2V_{dc}$ with switches $S_1 - S_3$. The LV side consists of four switches $S_4 - S_7$ with a dc voltage source of magnitude $V_{dc}$. The basic module generates the 11 level output voltage with magnitudes of

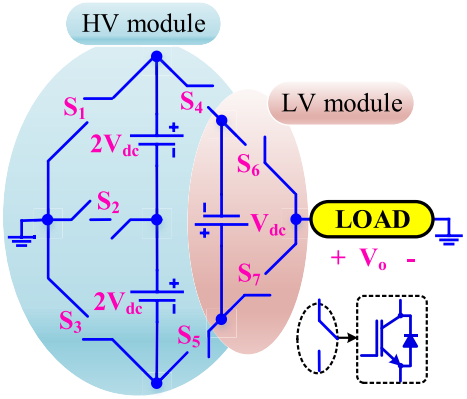


**FIGURE 1.** Basic Module of the proposed topology.

**TABLE 1.** Voltage states for the basic module.

| $S_1$ | $S_2$ | $S_3$ | $S_4$ | $S_5$ | $S_6$ | $S_7$ | $V_o$ |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 1 | 0 | 0 | 1 | $5V_{dc}$ |
| 0 | 0 | 1 | 1 | 0 | 1 | 0 | $4V_{dc}$ |
| 0 | 1 | 0 | 1 | 0 | 0 | 1 | $3V_{dc}$ |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | $2V_{dc}$ |
| 1 | 0 | 0 | 1 | 0 | 0 | 1 | $V_{dc}$ |
| 1 | 0 | 0 | 1 | 0 | 1 | 0 | Zero |
| 0 | 0 | 1 | 0 | 1 | 0 | 1 | |
| 0 | 0 | 1 | 0 | 1 | 1 | 0 | $-V_{dc}$ |
| 0 | 1 | 0 | 0 | 1 | 0 | 1 | $-2V_{dc}$ |
| 0 | 1 | 0 | 0 | 1 | 1 | 0 | $-3V_{dc}$ |
| 1 | 0 | 0 | 0 | 1 | 0 | 1 | $-4V_{dc}$ |
| 1 | 0 | 0 | 0 | 1 | 1 | 0 | $-5V_{dc}$ |

zero, $\pm V_{dc}$, $\pm 2V_{dc}$, $\pm 3V_{dc}$, $\pm 4V_{dc}$, and $\pm 5V_{dc}$. The switch pair ($S_4$, $S_5$) and ($S_6$, $S_7$) of the LV module are operated in a complementary fashion and only one switch from each pair is operated. Table 1 provides the different switching combinations of the basic module. Further, the corresponding connection diagrams for different voltage level generation are given in Fig. 2. As all the switches facilities the bidirectional current flow, the basic module supports the inductive load with reverse current flow. Table 3 gives the information related to the voltage stress (VS) and current stress (CS) of different switches of the proposed topology for different voltage levels with $I_L$ denotes the load current.

### B. STRUCTURE OF THE PROPOSED TOPOLOGY

The proposed topology with N-level output voltage levels is depicted in Fig. 3. The HV module of the proposed topology is the same as that of the basic module and in the LV module, the number of dc voltage sources is increasing in the additive polarity. The magnitude of each dc voltage source on the LV side is selected as $V_{dc}$. Based on the number of dc voltage sources in the LV module, the magnitude of dc voltage

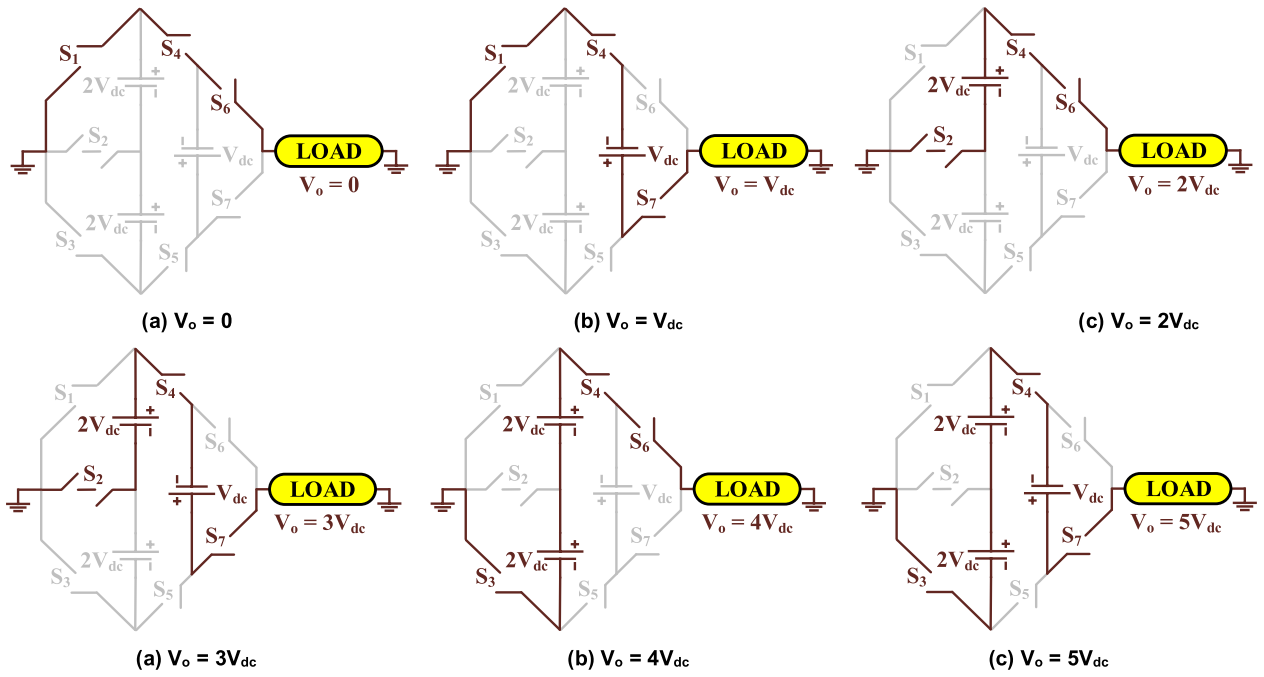


**FIGURE 2.** Switching states of the basic module.

**TABLE 2.** Voltage and current stress of the power switches during ALl possible voltage levels (VS= $\times V_{dc}$).

| Voltage Levels | $S_1$ | | $S_2$ | | $S_3$ | | $S_4$ | | $S_5$ | | $S_6$ | | $S_7$ | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | VS | CS | VS | CS | VS | CS | VS | CS | VS | CS | VS | CS | VS | CS |
| $5V_{dc}$ | 0 | 0 | 2 | 0 | 4 | $I_L$ | 5 | $I_L$ | 0 | 0 | 0 | 0 | 1 | $I_L$ |
| $4V_{dc}$ | 0 | 0 | 2 | 0 | 4 | $I_L$ | 5 | $I_L$ | 0 | 0 | 1 | $I_L$ | 0 | 0 |
| $3V_{dc}$ | 2 | 0 | 0 | $I_L$ | 2 | 0 | 5 | $I_L$ | 0 | 0 | 0 | 0 | 1 | $I_L$ |
| $2V_{dc}$ | 2 | 0 | 0 | $I_L$ | 2 | 0 | 5 | $I_L$ | 0 | 0 | 1 | $I_L$ | 0 | 0 |
| $V_{dc}$ | 4 | $I_L$ | 2 | 0 | 0 | 0 | 5 | $I_L$ | 0 | 0 | 0 | 0 | 1 | $I_L$ |
| 0 | 4 | $I_L$ | 2 | 0 | 0 | 0 | 5 | $I_L$ | 0 | 0 | 1 | $I_L$ | 0 | 0 |
| $-V_{dc}$ | 0 | 0 | 2 | 0 | 4 | $I_L$ | 0 | 0 | 5 | $I_L$ | 0 | $I_L$ | 1 | 0 |
| $-2V_{dc}$ | 2 | 0 | 2 | $I_L$ | 2 | 0 | 0 | 0 | 5 | $I_L$ | 1 | 0 | 0 | $I_L$ |
| $-3V_{dc}$ | 2 | 0 | 0 | $I_L$ | 2 | 0 | 0 | 0 | 5 | $I_L$ | 0 | $I_L$ | 1 | 0 |
| $-4V_{dc}$ | 4 | $I_L$ | 4 | 0 | 0 | 0 | 0 | 0 | 5 | $I_L$ | 1 | 0 | 0 | $I_L$ |
| $-5V_{dc}$ | 4 | $I_L$ | 4 | 0 | 0 | 0 | 0 | 0 | 5 | $I_L$ | 0 | $I_L$ | 1 | 0 |

**TABLE 3.** Comparison of different basic modules with 11 level output voltage.

| Topology | $N_{sw}$ | $N_d$ | $N_{gd}$ | $N_{dc}$ | $N$ | TSV×$V_{dc}$ | TSV/$N_l$ |
|---|---|---|---|---|---|---|---|
| [26] | 14 | 0 | 9 | 5 | 11 | 42 | 3.81 |
| [27] | 8 | 4 | 8 | 5 | 11 | 28 | 2.55 |
| [28] | 7 | 3 | 7 | 4 | 11 | 28 | 2.55 |
| [29] | 14 | 0 | 14 | 4 | 11 | 35 | 3.18 |
| **[P]** | **8** | **0** | **7** | **3** | **11** | **24** | **2.18** |

$N_d$ = number of diodes, [P] = basic module of proposed topology

source $V_1$ is selected as

$$V_1 = (m+1)\,V_{dc} \tag{1}$$

where $m$ is the number of dc voltage sources in the LV module.

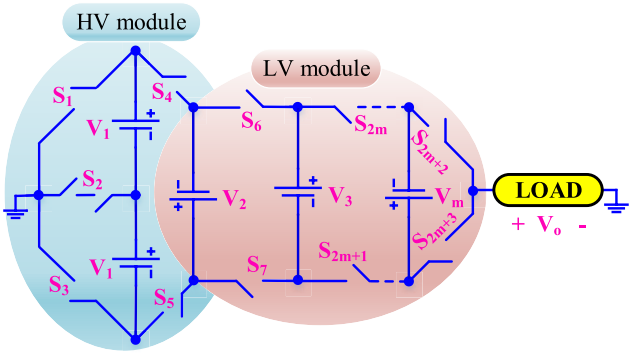


**FIGURE 3.** Proposed Topology.

The total standing voltage (TSV) of the proposed topology can be defined as

$$TSV = TSV_{HV} + TSV_{LV} \tag{2}$$

Based on (1), the required blocking voltage of the switches of HV can be determined as

$$\left.\begin{aligned} V_{S1} &= V_{S3} = 2\,(m+1)\,V_{dc} \\ V_{S2} &= (m+1)\,V_{dc} \end{aligned}\right\} \tag{3}$$

The switched $S_4$ and $S_5$ are the connecting switches between the HV module and the LV module. Therefore these two switches have maximum voltage stress and are given as

$$V_{S4} = V_{S5} = 2\,(m+2)\,V_{dc} \tag{4}$$

Similarly, the maximum blocking voltage of the switches of the LV module is given as

$$\left.\begin{aligned} V_{S6} &= V_{S7} = 2V_{dc} \\ V_{S(2m)} &= V_{S(2m+1)} = 2V_{dc} \\ V_{S(2m+2)} &= V_{S(2m+3)} = V_{dc} \end{aligned}\right\} \tag{5}$$

Therefore, based on the above formulation, the TSV of HV and LV are given as:

$$\begin{aligned} TSV_{HV} &= 2\,(V_{S1} + V_{S2} + V_{S4}) = \{8\,(m+1)+2\}\,V_{dc} \\ TSV_{LV} &= 2\left(V_{S6} + m \times V_{S(2m)} + \ldots + V_{S(2m+2)}\right) \\ &= 2\,(2m+1)\,V_{dc} \end{aligned} \tag{6}$$

From (2) and (6), the TSV of the proposed topology is given as

$$\begin{aligned} TSV &= \{8\,(m+1)+2\}\,V_{dc} + 2\,(2m+1)\,V_{dc} \\ &= 12\,(m+1)\,V_{dc} \end{aligned} \tag{7}$$

For the proposed topology, the equation for different parameters are given as

$$\left.\begin{aligned} N_{sw} &= \frac{1}{3}\,(N+13) \\ N_{gd} &= \frac{1}{3}\,(N+11) \\ N_{dc} &= \frac{1}{6}\,(N+7) \\ TSV &= 2\,(N+1) \end{aligned}\right\} \tag{8}$$

where $N_{sw}$, $N_{gd}$, and $N_{dc}$ denote the total number of switches, gate driver circuits, and dc voltage sources respectively.

## III. MODULATION TECHNIQUES

The PWM technique used for pulse generation was divided into two categories based on the switching frequency: High-frequency switching PWM and fundamental frequency switching PWM technology. Sinusoidal PWM, PWM space vector and PWM hybrid modulation are some examples of high-frequency switching techniques. The number of turns on and off in these PWM techniques are high, due to which the lower order harmonics are shifted to the carrier frequency thus reducing the effect of lower order harmonics. The fundamental switching frequency modulation includes selective harmonic elimination (SHE), nearest level modulation (NLM) or nearest level control (NLC) and optimal switching angle (OSA) modulation. For high power applications, the fundamental switching modulations are mostly preferred due to lower switching losses [31]–[38].

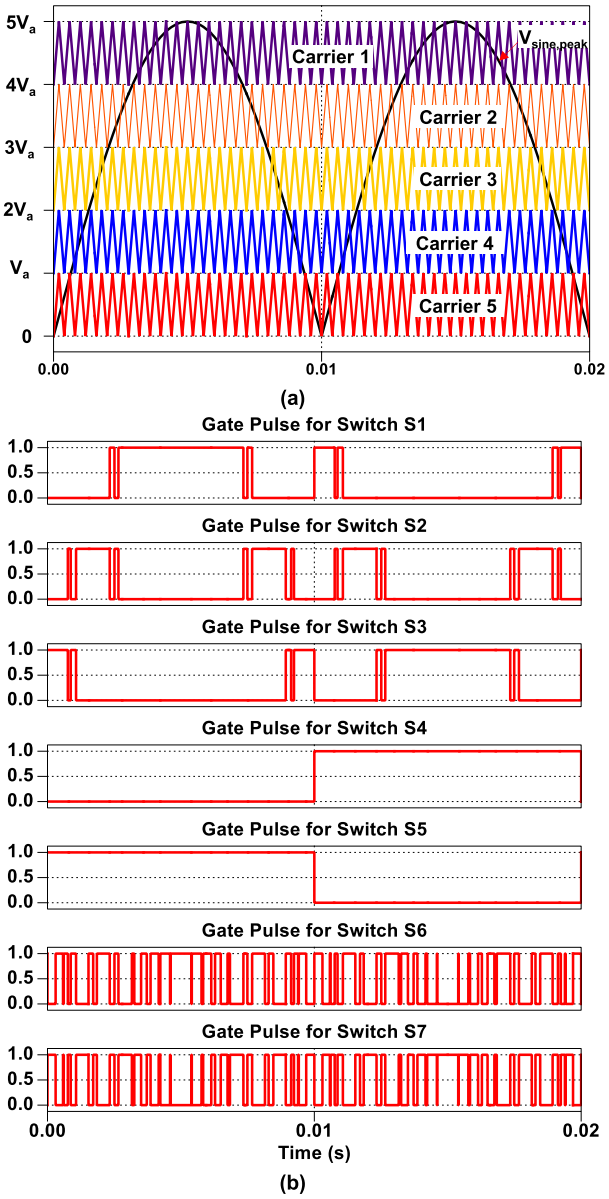


**FIGURE 4.** (a) LS-PWM for 11L and (b) gate pulses for the basic module with LS-PWM.

### A. LEVEL SHIFTED PWM (LS-PWM)

For all switches of the basic module of the proposed topology, the PWM signal can be produced by comparing one modulation waveform with the five carriers waveforms. As shown in Fig. 4 (a), these five high-frequency carrier waves are shifted waveforms corresponding to different levels. The waveform's peak value is $V_{sine,peak}$ and the modulation index (MI) is defined as

$$MI = \frac{V_{ref,peak}}{5V_{car}} \tag{9}$$

Depending on the location of the high-frequency carriers, the PWM signals are produced for the switches $S_1$ to $S_7$. Fig. 4 (b) shows the switching pulses for switches $S_1$ to $S_7$.

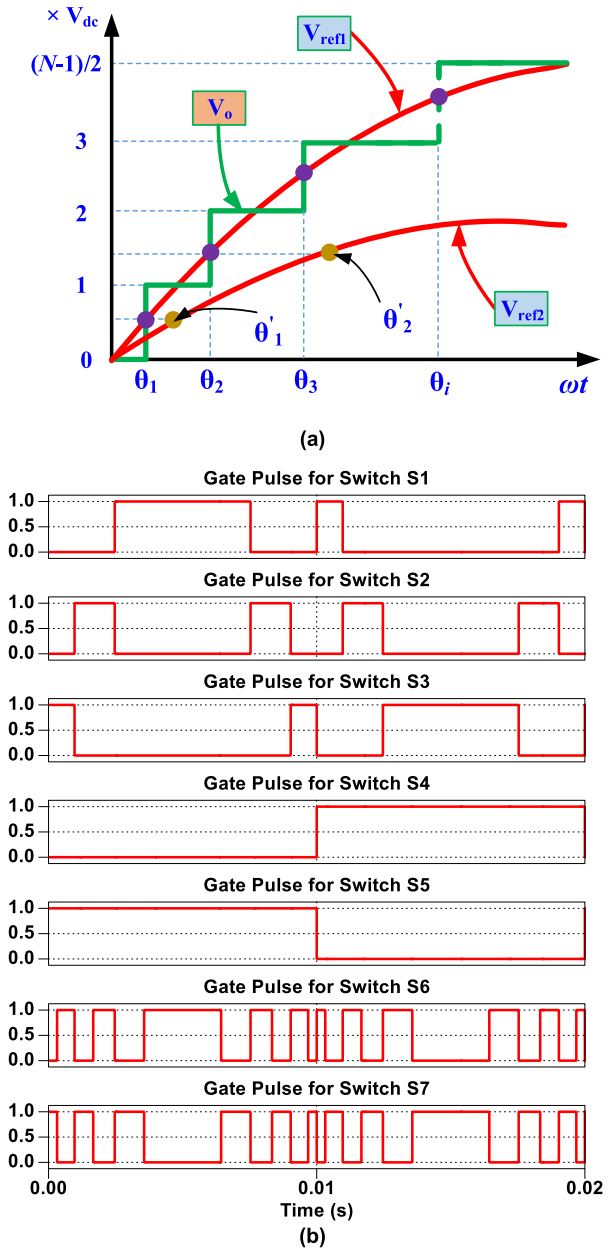


**FIGURE 5.** Illustration of NLC with (a) sampled quarter reference signal and (b) gate pulses with NLCPWM.

## IV. B. NEAREST LEVEL CONTROL PWM (NLCPWM)

The working principle of NLC is illustrated in Fig. 5 (a), where the closest level is selected by comparing the output voltage and reference voltage. In case of float numbers (1.5 $V_{dc}$ or 2.5 $V_{dc}$), the round function is utilized to select the nearest even number (2 $V_{dc}$). The reference signal cuts the rising edge of the output signal into two parts, upper sub-level and lower sub-level, both of which are equal in magnitude as shown in Fig. 5 (a). The firing angle of this technique can be estimated by the expression below:

$$\alpha_i = \sin^{-1}\left(\frac{i-0.5}{n}\right) \tag{10}$$

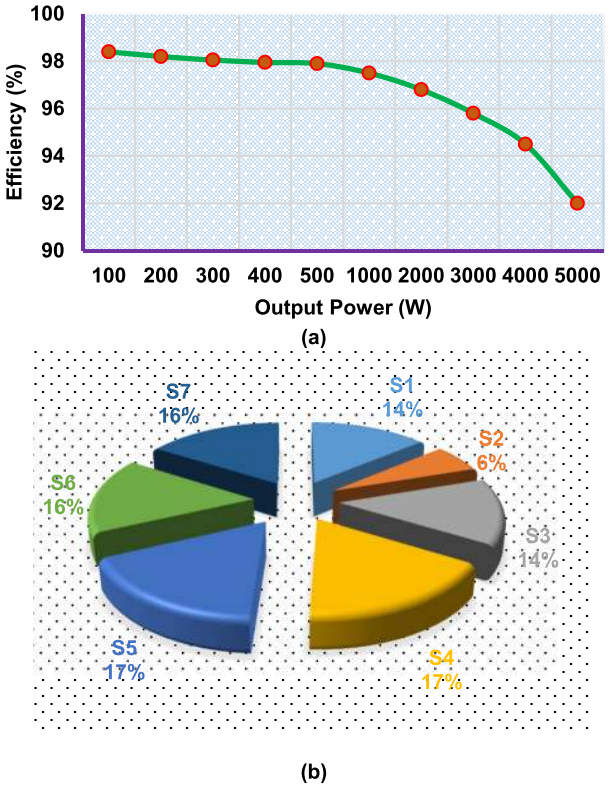


**FIGURE 6.** Power loss analysis with (a) Efficiency plot and (b) Power loss distribution.

where

$$n = \frac{N-1}{2} \quad i = 1,\ 2,\ 3, \ldots\ldots n \tag{11}$$

where, $\alpha_i$ is the switching angle. The NLC can be stretched out to $N$ level and the modulation index ($MI$) of it can also be changed with the reference voltage by the expression below [36].

$$MI = \frac{2}{(N-1)V_{dc}} V_{ref} \tag{12}$$

The generated gate pulse with NLCPWM is illustrated in Fig. 5 (b).

## V. POWER LOSS ANALYSIS

Losses incurred in a converter can be estimated by the accumulation of losses in the different switches and diodes. Power losses of a switch or diode may usually be defined in three groups:

i) OFF state
ii). ON state
iii) Switching state

Because leakage currents during the blocking or OFF state losses are negligible. Therefore, only conduction and switching losses are measured for estimating losses related to the proposed inverter circuitry.

The proposed topology uses eight switches and all of them have their anti-parallel diodes. Therefore, the power loss of the respective anti-parallel diodes must be considered. The conduction losses for the switch ($P_{con,s}$) and diode ($P_{con,d}$)

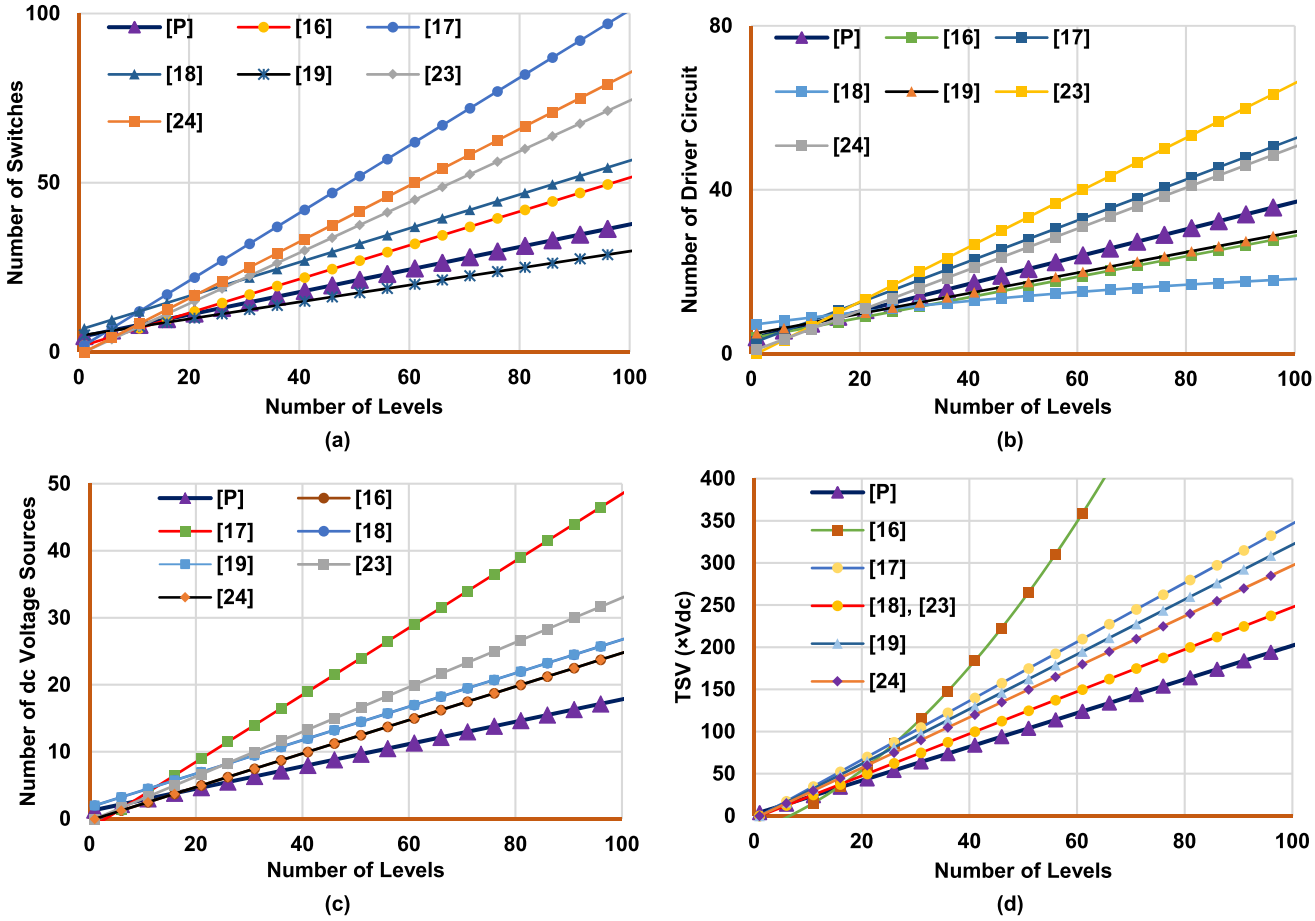


**FIGURE 7.** Comparison of (a) number of switches, (b) number of driver circuit, (c) number of dc voltage sources and (d) TSV with respect to number of levels.

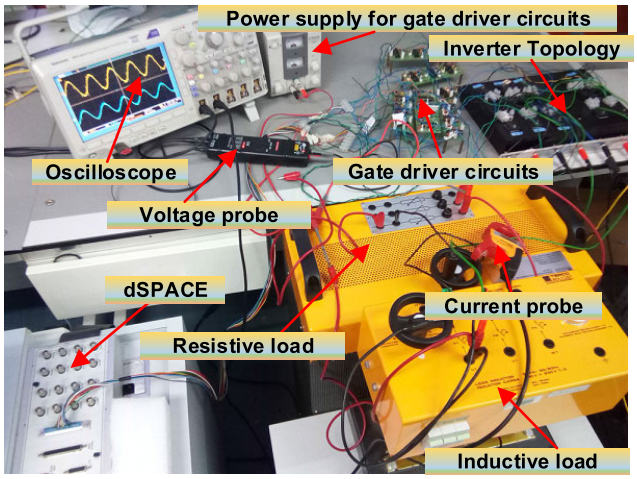


**FIGURE 8.** Experimental setup.

are expressed as follows:

$$P_{con,s} = \left\{V_{ON_s} + R_s i^{\alpha}(t)\right\} i\,(t) \tag{13}$$

$$P_{con,d} = \left\{V_{ON_d} + R_d i(t)\right\} i\,(t) \tag{14}$$

where, $V_{ON,s}$ and $R_s$ denote the voltage drop and the ON-state resistance of a switch, respectively. The similar parameters

**TABLE 4.** Experimental parameter.

| Parameter | Value |
|---|---|
| Step Voltage, $V_{dc}$ | 60V |
| Peak Voltage, $V_{peak}$ | 300V |
| Output frequency | 50 Hz |
| Carrier Frequency (PD-PWM) | 2.5 kHz |
| Load Resistance (R load) | 100Ω, 50Ω |
| Load Inductance (L load) | 100mH |

for the diode are denoted by $V_{ON,d}$ and $R_d$. $i(t)$ is the load current and $\alpha$ is the switch constant.

Now, let $N_s$ and $N_d$ be the number of conducting switches and diodes at any time, then, by using (13) and (14), average conduction losses can be expressed as:

$$P_{con} = \sum_{j=1}^{N_s} \frac{1}{2\pi} \int_0^{2\pi} \left(V_{ON_s} i\,(t) + R_s i^{\alpha}\,(t)\right) dt + \sum_{x=1}^{N_D} \frac{1}{2\pi} \int_0^{2\pi} \left(V_{ON_d} i\,(t) + R_d i^2\,(t)\right) dt \tag{15}$$

A typical switch is taken into account in the calculation of total switching loss, and individual switching losses are

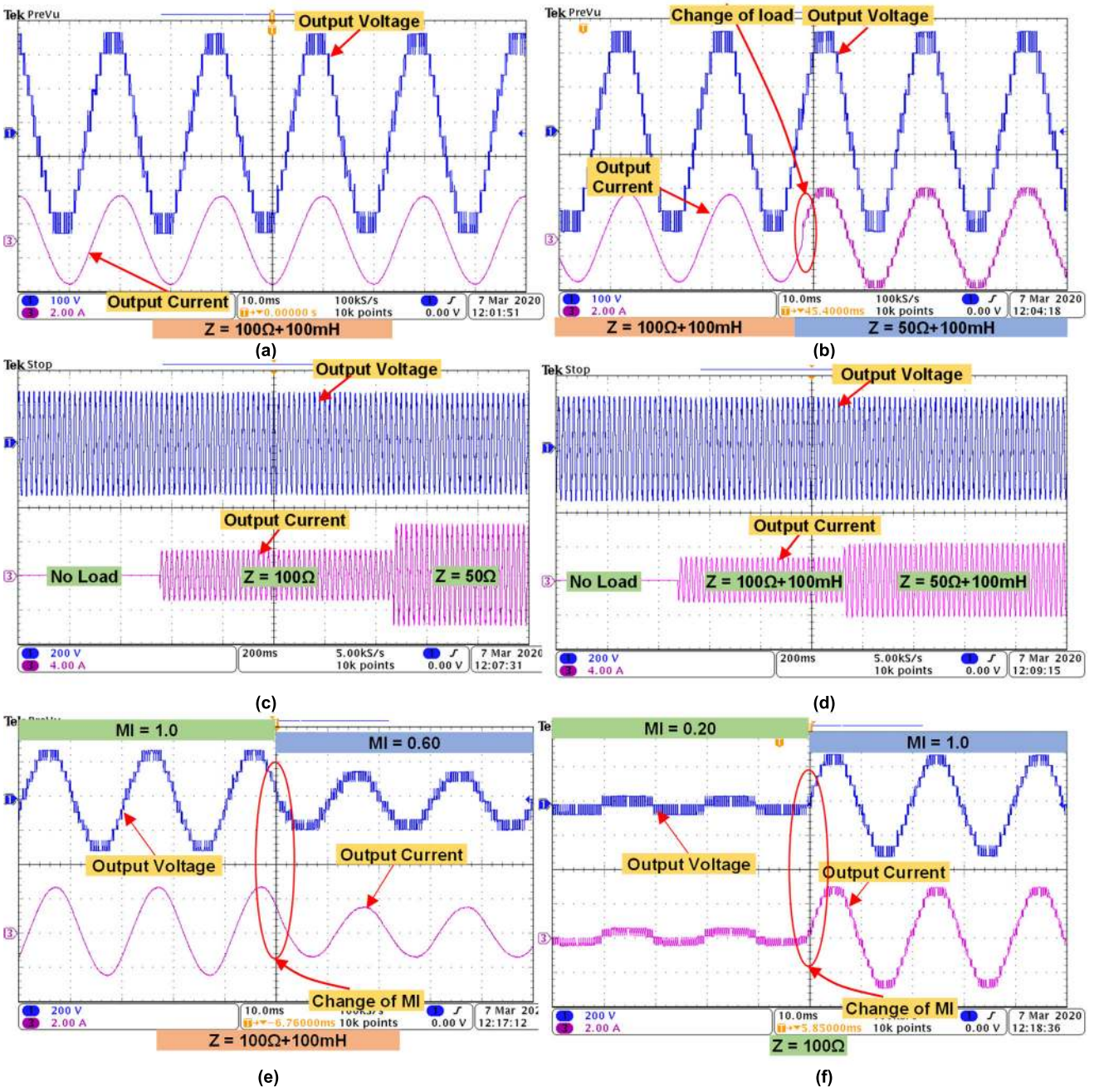


**FIGURE 9.** Experimental results with PD-PWM for (a) RL load, (b) change of load power factor, (c) step change in R load, and (d) step change in RL load, (e) change of MI from 1.0 to 0.60, and (f) change of MI from 0.20 to 1.0.

then added to achieve total inverter switching loss. During the switching period, a linear estimate of the voltage and the current is used to estimate the switching losses on an individual switch [27]. Energy losses during the turn ON and turn OFF are used for the calculation of the switching losses and is given by (16).

$$P_{sw} = \left[\sum_{x=1}^{N_{sw}} (T_{ON_x} E_{ON_x} + T_{OFF_x} E_{OFF_x})\right] \mathrm{x} f \qquad (16)$$

where $T_{ON}$ and $T_{OFF}$ are the turn-ON and turn-OFF time respectively, $E_{ON}$ and $E_{OFF}$ denote the turn-ON and turn-OFF energy losses, respectively and $f$ represents the switching frequency.

Fig. 6 show the different plots for the power loss analysis of the basic module with NLCPWM which has been estimated using PLECS software. The input voltage source magnitude has been selected as 60V and 120V which gives the peak output voltage as 300V. The parameters of switch IKW40N65ES5_IGBT has been considered for the efficiency calculation. As shown in Fig. 6 (a), the basic module gives higher efficiency as the efficiency is 97.5 % at an output power of 1kW. In addition, Fig. 6 (b) provides power loss distribution among different switches.

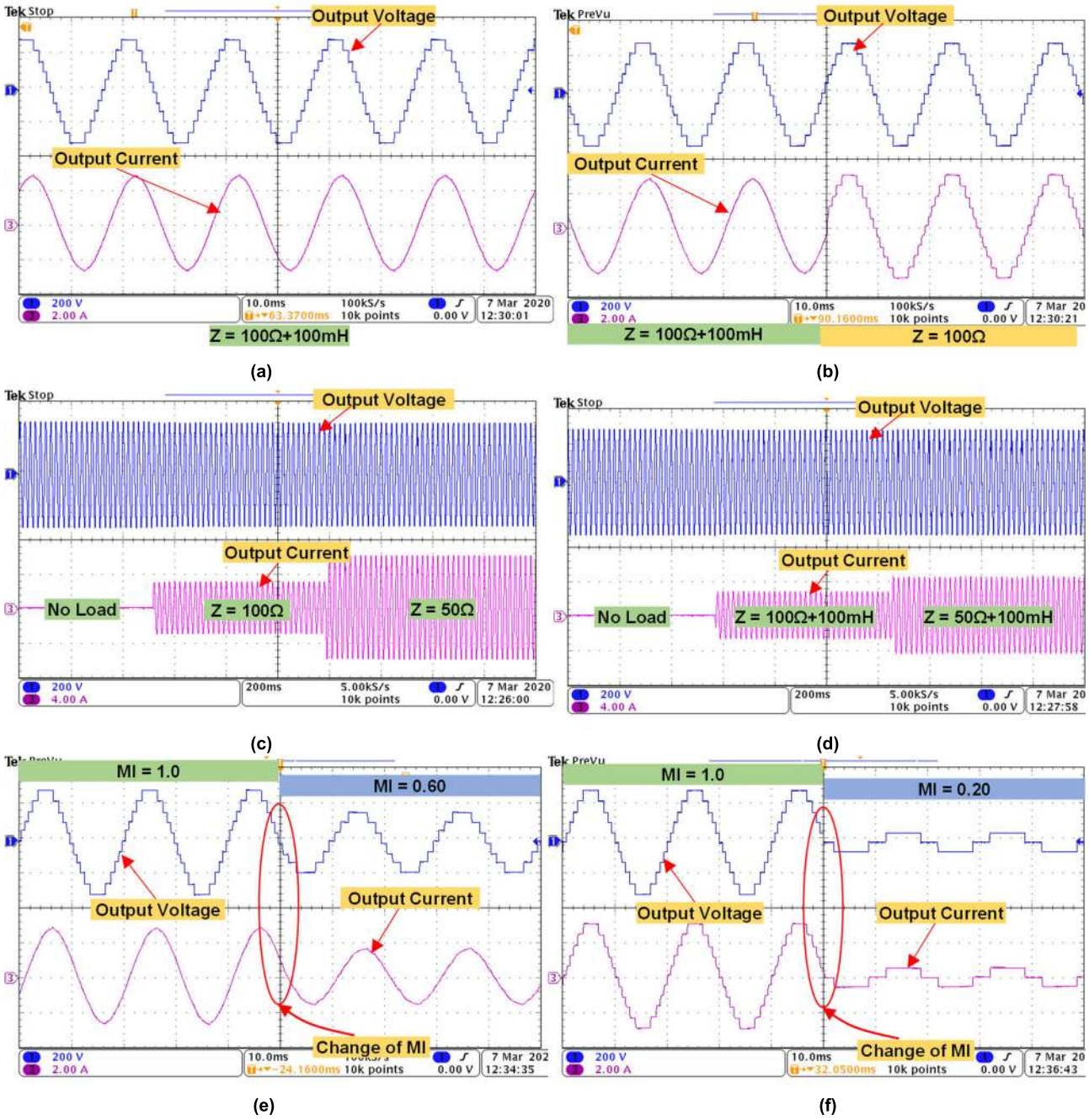


**FIGURE 10.** Experimental results with NLCPWM for (a) RL load, (b) change of load power factor, (c) step change in R load, and (d) step change in RL load, (e) change of MI from 1.0 to 0.60, and (f) change of MI from 1.0 to 0.20.

## VI. COMPARISON OF THE PROPOSED TOPOLOGY

In this section, a comparative study between different topologies that have a similar structure to the proposed one has been provided. Table 3 gives the comparison table for different basic modules with 11 level output voltage. The number of switches for the proposed topology is less except the topology of [28], however, the topology of [28] uses three diodes. Further, the basic module of the proposed topology is such that only three dc voltage sources are required for 11 level output voltage which is lower among other topologies. The value of TSV is also less for the basic module of the proposed topology.

Fig. 7 (a) shows the plot of the number of switches with respect to the number of levels for different topologies. As shown by Fig. 7 (a), the number of switches required for the proposed topology to generate a higher number of levels is low compare to the other topologies except [19]. In [19]. The bidirectional switch in [19] has been configured as a single switch with 4 diodes. The use of diodes reduces the number of switches, however, the overall component count of [19] is higher than the proposed topology. In the proposed topology a bidirectional switch is used with common emitter/source configuration, therefore, the number of driver circuitry required is less than the number of switches. The comparison between

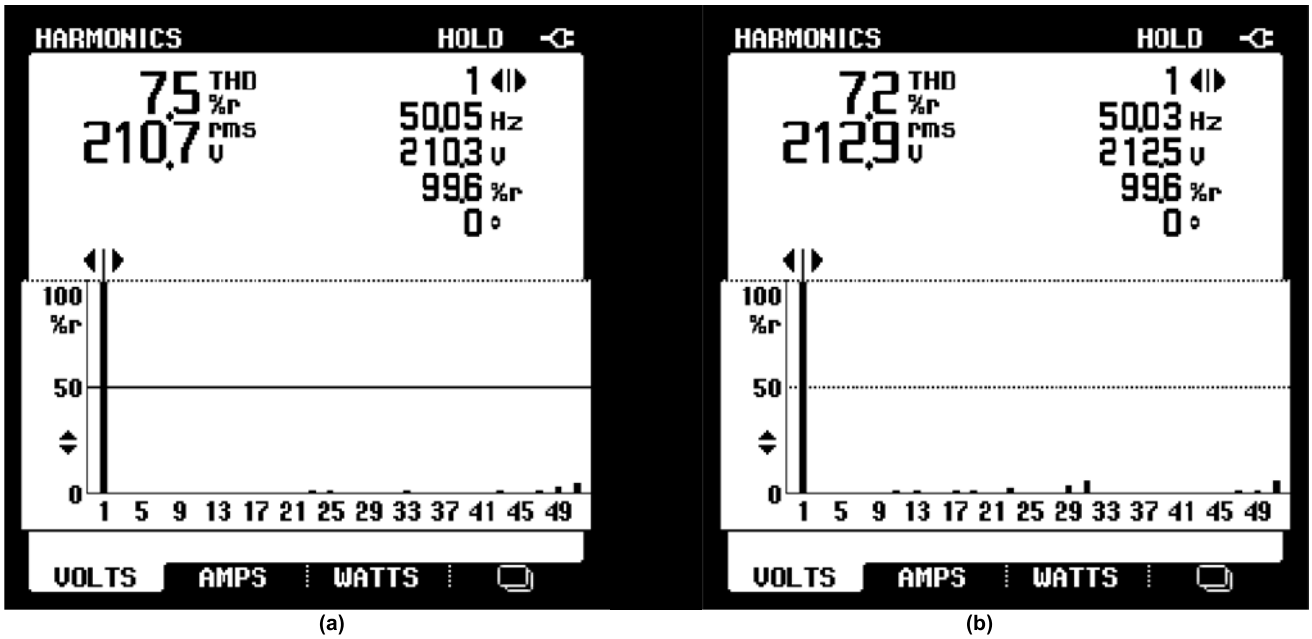


**FIGURE 11.** Harmonic spectrum of output voltage with (a) PD-PWM and (b) NLCPWM.

the number of driver circuitry and the number of levels is illustrated in Fig. 7 (b). Similar to the number of switches, the proposed topology required a lower number of gate driver circuits except for topologies of [16], [18] and [19].

Fig. 7 (c) and (d) show the comparison of the number of voltage source sand TSV of different topologies, respectively. As shown in Fig. 7 (c), the proposed topology requires a lower number of input voltage sources compare to other topologies. Also, the TSV of the proposed topology has a better plot compare to other topologies. Therefore, from Table 3 and Fig. 7, it can be summarized that the proposed topology gives a better alternative for the higher number of levels with a lower number of switches with lower voltage ratings and a lower number of dc voltage sources.

## VII. RESULTS AND DISCUSSION

In this section, the experimental results of the basic module of the proposed topology have been discussed. The basic module generates 11 level output voltage waveform. The basic module has been tested for different operating conditions for both experimental results. For the control of the switches, both NLCPWM and LS-PWM techniques have been used. For the experimental results, an experimental prototype has been developed and shown in Fig. 8. dSPACE controller is used to generating the gate pulses. Table 4 gives the different parameters for the experimental results.

Fig. 9 (a) demonstrate the output voltage and current waveform for an RL load. The magnitude of voltage sources in the HV module is elected as 120V and the voltage source magnitude of the LV module is fixed as 60V. This gives the resultant waveform having 11 levels of step voltage of 60V having a peak magnitude of 300V. The load has a parameter of 100Ω+100mH. Figs. 9 (b), (c) and (d) show the change of current with different loading c-condition with the fixed output voltage. In Fig. 9 (b), the change of load type from R to RL load, i.e., from 100Ω to 100Ω+100mH has been depicted. With purely R load, the power factor (*pf*) of the load is unity whereas, with RL load, the pf is 0.95 lagging. Fig. 9 (c) and (d) show the step change of load with R and RL load respectively. In Fig. 9 (c), the load is changed from no load to 100Ω to 50Ω. This also gives the doubling of the load current. In Fig. 9 (d), the step change is depicted for no-load to 100Ω+100mH to 50Ω+100mH. In this condition, the load *pf* changes from 0.95 lagging to 0.85 lagging.

In Figs. 9 (e) and (f), the magnitude of the output voltage is depicted with the corresponding waveforms of load current. The magnitude of the output voltage can be changed by varying the MI as discussed in Section III. In Fig. 9 (e), the MI is changed from 1.0 to 0.60 with RL load. At 0.60 MI, the number of levels is reduced to 7 with a peak magnitude of 180V. Similarly, with the change of MI from 0.20 to 1.0 with R load is illustrated in Fig. 9 (f). At MI of 0.20, the number of levels is reduced to 3 with a peak output voltage of 60V.

The proposed topology has also been validated with NLCPWM. The different waveforms of output voltage and current with different operating conditions are provided in Fig. 10. The different operating conditions include the change of load *pf*, step change of load, and change of MI. Based on the waveforms from Fig 9 and 10, it can be concluded that the proposed topology can be operated with a different real-time environment with good performance.

Furthermore, the harmonic spectrum of the 11 level output voltage at 50Hz has been illustrated in Fig. 11. The harmonic spectrum with PD-PWM and NLCPWM has been depicted in Fig. 11 (a) and (b) respectively. With the PD-PWM technique with 2.5kHz, the dominant harmonic order is

around the 50th harmonic order. With PD-PWM, THD is 7.5%. With NLCPWM, the THD amount is slightly lower than PD-PWM with a magnitude of 7.2%.

Due to higher voltage stress across the switches of the backend H-bridge, the application of the hybrid MLI topologies in which the backend H-bridge is used for the polarity reversal, in the high-voltage system is less favorable than the traditional CHBMLI topology. Nevertheless, hybrid MLI topologies have become increasingly important in low voltage systems with available commercial MOSFETs or IGBTs up to 1.7 kV blocking voltage. The proposed topology validating its superiority over the latest MLI topologies. Therefore the proposed topology represents a promising alternative for the conventional MLI in low voltage applications. The reason is that, with the same number of dc sources, significantly less switch and source count are required for the proposed topology. Further, the proposed topology can be applied to renewable generation utilizing low-power fuel cells and photovoltaic cells. In addition, the effective use of the battery storage system can be incorporated with the proposed topology for grid-tied or electric vehicle (EV) applications. With the reduced number of control switches in the proposed topology, efficiency improvements along with good quality output voltage waveform are the desirable features in these applications.

## VIII. CONCLUSION

In this paper, a new inverter topology for higher voltage levels has been proposed and discussed in detail. The basic module of the proposed topology generates an 11 level voltage waveform with three voltage sources and 8 switches. The performance of the proposed topology has been shown through the efficiency curve and several experimental results considering various real-time operating conditions. The efficiency of the proposed topology is about 97.5% at an output power of 1kW. Further, the performance of the proposed topology with different operational environments is also satisfactory.

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## REFERENCES

[1] P. R. Bana, K. P. Panda, R. T. Naayagi, P. Siano, and G. Panda, "Recently developed reduced switch multilevel inverter for renewable energy integration and drives application: Topologies, comprehensive analysis and comparative evaluation," *IEEE Access*, vol. 7, pp. 54888–54909, 2019.

[2] M. D. Siddique, S. Mekhilef, N. M. Shah, and M. A. Memon, "Optimal design of a new cascaded multilevel inverter topology with reduced switch count," *IEEE Access*, vol. 7, pp. 24498–24510, 2019.

[3] M. D. Siddique, S. Mekhilef, N. M. Shah, J. S. M. Ali, M. Meraj, A. Iqbal, and M. A. Al-Hitmi, "A new single phase single switched-capacitor based nine-level boost inverter topology with reduced switch count and voltage stress," *IEEE Access*, vol. 7, pp. 174178–174188, 2019.

[4] H. Akagi, "Multilevel converters: Fundamental circuits and systems," *Proc. IEEE*, vol. 105, no. 11, pp. 2048–2065, Nov. 2017.

[5] Y. P. Siwakoti and F. Blaabjerg, "Common-ground-type transformerless inverters for single-phase solar photovoltaic systems," *IEEE Trans. Ind. Electron.*, vol. 65, no. 3, pp. 2100–2111, Mar. 2018.

[6] B. P. Reddy and S. Keerthipati, "A multilevel inverter configuration for an open-end-winding pole-phase-modulated-multiphase induction motor drive using dual inverter principle," *IEEE Trans. Ind. Electron.*, vol. 65, no. 4, pp. 3035–3044, Apr. 2018.

[7] M. Vijeh, M. Rezanejad, E. Samadaei, and K. Bertilsson, "A general review of multilevel inverters based on main submodules: Structural point of view," *IEEE Trans. Power Electron.*, vol. 34, no. 10, pp. 9479–9502, Oct. 2019.

[8] J. S. M. Ali, R. S. Alishah, N. Sandeep, S. H. Hosseini, E. Babaei, K. Vijayakumar, and U. R. Yaragatti, "A new generalized multilevel converter topology based on cascaded connection of basic units," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 7, no. 4, pp. 2498–2512, Dec. 2019.

[9] M. D. Siddique, B. P. Reddy, A. Iqbal, and S. Mekhilef, "Reduced switch count-based N-level boost inverter topology for higher voltage gain," *IET Power Electron.*, vol. 13, no. 15, pp. 3505–3509, Jul. 2020, doi: 10.1049/iet-pel.2020.0359.

[10] M. D. Siddique, S. Mekhilef, N. M. Shah, A. Sarwar, A. Iqbal, M. Tayyab, and M. K. Ansari, "Low switching frequency based asymmetrical multilevel inverter topology with reduced switch count," *IEEE Access*, vol. 7, pp. 86374–86383, 2019.

[11] B. P. Reddy, M. D. Siddique, A. Iqbal, S. Mekhilef, S. Rahman, and P. K. Maroti, "7L-SCBI topology with minimal semiconductor device count," *IET Power Electron.*, vol. 13, no. 14, pp. 3199–3203, Nov. 2020, doi: 10.1049/iet-pel.2020.0313.

[12] R. S. Alishah, D. Nazarpour, S. H. Hosseini, and M. Sabahi, "Novel topologies for symmetric, asymmetric, and cascade switched-diode multilevel converter with minimum number of power electronic components," *IEEE Trans. Ind. Electron.*, vol. 61, no. 10, pp. 5300–5310, Oct. 2014.

[13] M. D. Siddique, B. Alamri, F. A. Salem, M. Orabi, S. Mekhilef, N. M. Shah, N. Sandeep, J. S. M. Ali, A. Iqbal, M. Ahmed, S. S. M. Ghoneim, and M. M. Al-Harthi, "A single DC source nine-level switched-capacitor boost inverter topology with reduced switch count," *IEEE Access*, vol. 8, pp. 5840–5851, 2020.

[14] L. Wang, Q. H. Wu, and W. Tang, "Novel cascaded switched-diode multilevel inverter for renewable energy integration," *IEEE Trans. Energy Convers.*, vol. 32, no. 4, pp. 1574–1582, Dec. 2017.

[15] K. K. Gupta and S. Jain, "A novel multilevel inverter based on switched DC sources," *IEEE Trans. Ind. Electron.*, vol. 61, no. 7, pp. 3269–3278, Jul. 2014.

[16] R. S. Alishah, S. H. Hosseini, E. Babaei, and M. Sabahi, "Optimal design of new cascaded switch-ladder multilevel inverter structure," *IEEE Trans. Ind. Electron.*, vol. 64, no. 3, pp. 2072–2080, Mar. 2017.

[17] R. S. Alishah, D. Nazarpour, S. H. Hosseini, and M. Sabahi, "Reduction of power electronic elements in multilevel converters using a new cascade structure," *IEEE Trans. Ind. Electron.*, vol. 62, no. 1, pp. 256–259, Jan. 2015.

[18] E. Babaei, S. Laali, and Z. Bayat, "A single-phase cascaded multilevel inverter based on a new basic unit with reduced number of power switches," *IEEE Trans. Ind. Electron.*, vol. 62, no. 2, pp. 922–929, Feb. 2015.

[19] S. P. Gautam, S. Gupta, and L. K. Sahu, "Reduction in number of devices for symmetrical and asymmetrical multilevel inverters," *IET Power Electron.*, vol. 9, no. 4, pp. 698–709, Mar. 2016.

[20] M. D. Siddique, A. Iqbal, M. A. Memon, and S. Mekhilef, "A new configurable topology for multilevel inverter with reduced switching components," *IEEE Access*, vol. 8, pp. 188726–188741, 2020, doi: 10.1109/ACCESS.2020.3030951.

[21] M. Saeedian, J. Adabi, and S. M. Hosseini, "Cascaded multilevel inverter based on symmetric–asymmetric DC sources with reduced number of components," *IET Power Electron.*, vol. 10, no. 12, pp. 1468–1478, Oct. 2017.

[22] H. Samsami, A. Taheri, and R. Samanbakhsh, "New bidirectional multilevel inverter topology with staircase cascading for symmetric and asymmetric structures," *IET Power Electron.*, vol. 10, no. 11, pp. 1315–1323, Sep. 2017.

[23] E. Samadaei, S. A. Gholamian, A. Sheikholeslami, and J. Adabi, "An envelope type (E-type) module: Asymmetric multilevel inverters with reduced components," *IEEE Trans. Ind. Electron.*, vol. 63, no. 11, pp. 7148–7156, Nov. 2016.

[24] E. Samadaei, A. Sheikholeslami, S. A. Gholamian, and J. Adabi, "A square T-type (ST-type) module for asymmetrical multilevel inverters," *IEEE Trans. Power Electron.*, vol. 33, no. 2, pp. 987–996, Feb. 2018.
[25] E. Samadaei, M. Kaviani, and K. Bertilsson, "A 13-levels module (K-type) with two DC sources for multilevel inverters," *IEEE Trans. Ind. Electron.*, vol. 66, no. 7, pp. 5186–5196, Jul. 2019.
[26] R. S. Alishah, M. Sabahi, D. Nazarpour, and S. H. Hosseini, "Novel multilevel inverter topologies for medium and high-voltage applications with lower values of blocked voltage by switches," *IET Power Electron.*, vol. 7, no. 12, pp. 3062–3071, Dec. 2014.
[27] R. S. Alishah, D. Nazarpour, M. Sabahi, and S. H. Hosseini, "New hybrid structure for multilevel inverter with fewer number of components for high-voltage levels," *IET Power Electron.*, vol. 7, no. 1, pp. 96–104, Jan. 2014.
[28] R. S. Alishah, D. Nazarpour, M. Sabahi, and S. H. Hosseini, "Switched-diode structure for multilevel converter with reduced number of power electronic devices," *IET Power Electron.*, vol. 7, no. 3, pp. 648–656, Mar. 2014.
[29] R. S. Alishah, D. Nazarpour, and S. H. Hosseini, "Design of new multilevel voltage source inverter structure using fundamental frequency-switching strategy," *Trans. Electr. Electron. Circuits Syst.*, vol. 3, no. 7, pp. 35–41, 2013.
[30] R. S. Alishah, D. Nazarpour, S. H. Hosseini, and M. Sabahi, "Novel single-phase multilevel inverter topology based on cascaded connection of basic units," *Asian Power Electron. J.*, vol. 8, no. 1, pp- 24-29, 2014.
[31] B. Cougo, G. Gateau, T. Meynard, M. Bobrowska-Rafal, and M. Cousineau, "PD modulation scheme for three-phase parallel multilevel inverters," *IEEE Trans. Ind. Electron.*, vol. 59, no. 2, pp. 690–700, Feb. 2012.
[32] A. R. Kumar, M. S. Bhaskar, U. Subramaniam, D. Almakhles, S. Padmanaban, and J. B.-H. Nielsen, "An improved harmonics mitigation scheme for a modular multilevel converter," *IEEE Access*, vol. 7, pp. 147244–147255, 2019.
[33] A. R. Kumar, T. Deepa, S. Padmanaban, and D. P. Kothari, "A guide to nearest level modulation and selective harmonics elimination modulation scheme for multilevel inverters," in *Proc. Innov. Power Adv. Comput. Technol. (i-PACT)*, Vellore, India, Mar. 2019, pp. 1–8.
[34] A. R. Kumar, P. S. Subudhi, T. Deepa, S. Krithiga, S. Padmanaban, and D. P. Kothari, "Simulation analysis of a nearest level modulation scheme for cross-connected sources based MLI," in *Proc. Innov. Power Adv. Comput. Technol. (i-PACT)*, Vellore, India, Mar. 2019, pp. 1–4.
[35] M. D. Siddique, S. Mekhilef, S. Padmanaban, M. A. Memon, and C. Kumar, "Single phase step-up switched-capacitor based multilevel inverter topology with SHEPWM," *IEEE Trans. Ind. Appl.*, early access, Jun. 12, 2020, doi: 10.1109/TIA.2020.3002182.
[36] M. D. Siddique, S. Mekhilef, N. M. Shah, and J. S. M. Ali, "New switched-capacitor-based boost inverter topology with reduced switch count," *J. Power Electron.*, vol. 20, no. 4, pp. 926–937, Jul. 2020.
[37] G. Konstantinou, J. Pou, S. Ceballos, R. Darus, and V. G. Agelidis, "Switching frequency analysis of staircase-modulated modular multilevel converters and equivalent PWM techniques," *IEEE Trans. Power Del.*, vol. 31, no. 1, pp. 28–36, Feb. 2016.
[38] P. M. Meshram and V. B. Borghate, "A simplified nearest level control (NLC) voltage balancing method for modular multilevel converter (MMC)," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 450–462, Jan. 2015.

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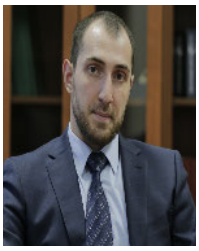

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