

Extension of the Nearest-Three Virtual-Space-Vector PWM to the Four-Level Diode-Clamped dc-ac Converter

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Abstract—Several pulsewidth modulation strategies have been proposed for the three-level three-phase diode-clamped dc-ac converter. Among them, the nearest-three virtual-space-vector (NTV²) pulsewidth modulation (PWM) guarantees the dc-link capacitor voltage balance under any operating condition, provided that the addition of the three phase currents equals zero. This paper extends this modulation concept to the four level converter. The new virtual vectors are presented and practical modulation solutions are defined. Conventional nearest-three space vector (NTV) PWM cannot comprehensively achieve balanced and stable dc-link voltages. The proposed modulation solutions enable the practical use of the four-level converter since they guarantee the dc-link capacitor voltage balance for any operating condition and load, provided that the addition of three-phase currents equals zero. Simulation and experimental results prove the goodness of the presented approach.

I. INTRODUCTION

Multilevel converter topologies [1]-[2] have received special attention during the last two decades due to their significant advantages compared to the conventional two level case. These topologies allow reducing the voltage across the semiconductors without the problems associated to the series interconnection of devices, reduce the harmonic distortion of the output voltage and improve the efficiency of the converter. However, a larger number of semiconductors is needed and the modulation strategy to control them becomes more complex.

Among the possible multilevel topologies, the three-level three-phase diode-clamped dc-ac converter [3] is probably the most popular. Several modulation strategies have been proposed for this converter. Conventional pulsewidth modulations (PWM) are based on the selection of the nearest-three space vectors (NTV). However, as demonstrated in [4], this PWM are not capable of balancing the voltage of the dc-link capacitors under certain operating conditions. On the other hand, the nearest-three virtual-space-vector (NTV²) PWM [5] is capable of controlling the dc-link capacitor voltage balance for any load (linear or non-linear, balanced or unbalanced) and modulation index, provided that the addition of the output three-phase currents equals zero. Reference [6] shows how to interface this modulation with conventional

closed-loop control schemes, and develops a specific control to mitigate possible dc-link voltage balance perturbations.

Several studies have focused on diode-clamped topologies with higher levels, in particular the four-level three-phase diode-clamped dc-ac converter in Fig. 1 [7]–[11]. They conclude that the use of NTV PWM with the four-level converter cannot achieve dc-link capacitor voltage balance under a substantial portion of the converter operating conditions. Eventually, these operating conditions lead to instabilities in the balance, causing the voltage of the middle capacitor to collapse. The limits for balanced and stable operation are specified in [11].

In this paper, the NTV² PWM presented in [5] is extended to the four-level converter. The resulting PWM scheme guarantees the dc-link voltage balance for any modulation index and load, provided that the addition of the three phase currents equals zero. Hence, this modulation enables the practical use of the four-level converter with passive front ends and only requires small dc-link capacitors.

The paper is organized as follows. In Section II the proposed modulation scheme is defined. Section III presents the most interesting particular modulation strategies. In Sections IV and V, the performance of these modulations is analyzed and compared to a reference NTV modulation through both simulations and experiments, and Section VI outlines the conclusions.

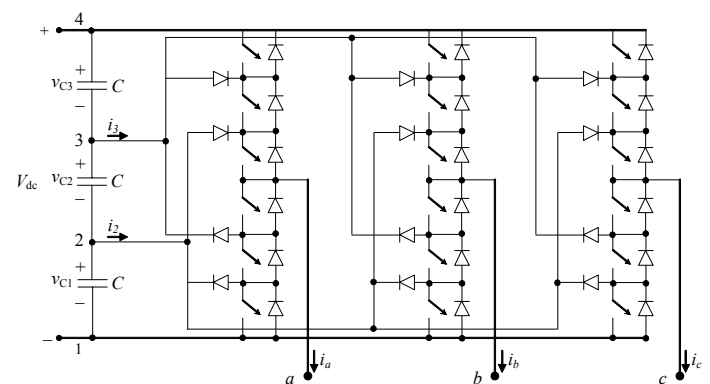


Fig. 1. Four-level three-phase diode-clamped dc-ac converter.

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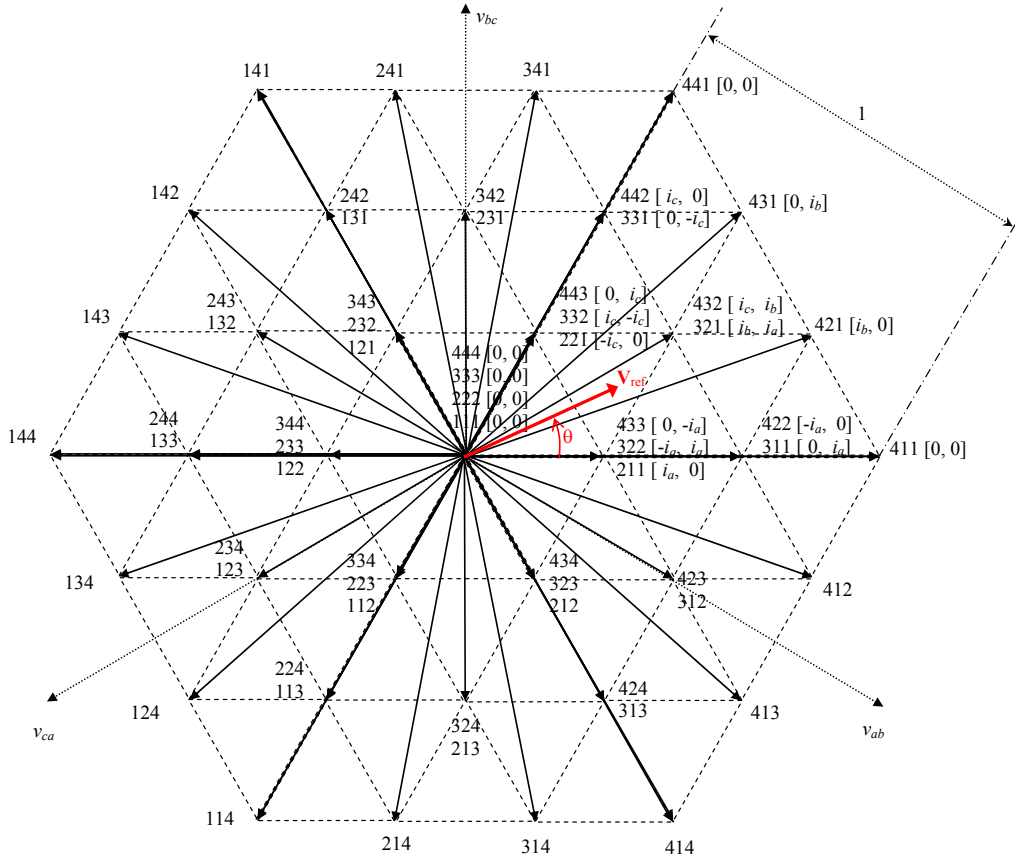


Fig. 2. Normalized space vector diagram for the four-level three-phase diode-clamped dc-ac converter.

II. NEAREST-THREE VIRTUAL-SPACE-VECTOR PWM

A. Virtual Space Vector Definition

Fig. 2 shows the space vector diagram (SVD) for the four-level diode-clamped dc-ac converter. The converter has sixty-four switching states corresponding to all the combinations of connections of each phase to the dc-link points 1, 2, 3 and 4; e.g., 432, corresponding to the connection of phase a to point 4, phase b to 3, and phase c to 2. These switching states define thirty-seven space vectors.

In the conventional NTV PWM, the reference vector (\mathbf{V}_{ref}) = $m \cdot e^{j\theta}$ ($m \in [0, 1]$ for linear modulation) is synthesized in each switching cycle (with period $T_s = 1/f_s$) by a sequence of the nearest three vectors. Whenever a vector can be generated by more than one switching state, an additional selection of one switching state or a combination of several has to be made.

In the first sextant of the SVD of Fig. 2, the midpoint (MP) currents i_2 and i_3 corresponding to each switching state are specified in brackets: $[i_2, i_3]$. Analogous to the three-level case, the average i_2 and average i_3 in every switching cycle must be zero to guarantee the dc-link capacitor voltage balance. In the NTV PWM, whenever redundant switching states are available for a given space vector, the appropriate combination of these switching states must be selected to guarantee that the average MP currents equal zero in every

switching cycle. However, this is not possible for high modulation indexes, especially when the load angle is small ($m_{max} = 0.55$ for a zero load angle [11]).

To achieve full control of the dc-link capacitor voltage balance, a set of new virtual vectors (VV) is defined as a linear combination of the vectors corresponding to certain switching states. The new virtual vectors, shown in Fig. 3 for the first sextant of the SVD, are defined in (1).

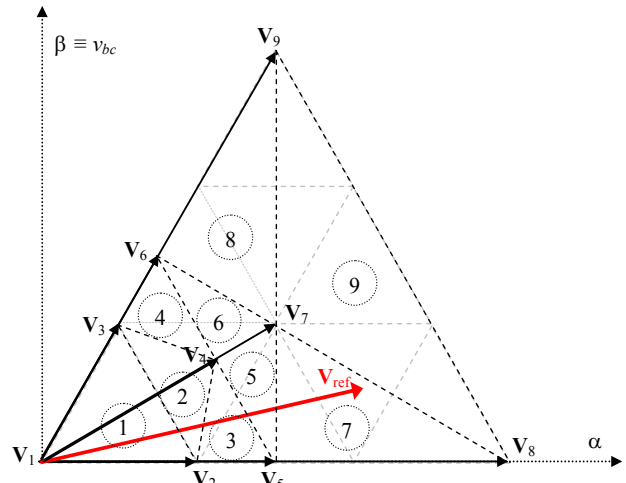


Fig. 3. Virtual space vectors for the first sextant of the SVD.

$$\begin{aligned}
\mathbf{V}_1 &= \frac{1}{2}(333) + \frac{1}{2}(222) = (0,0)_{\alpha\beta} \\
\mathbf{V}_2 &= \frac{1}{3}(433) + \frac{1}{3}(322) + \frac{1}{3}(211) = \left(\frac{2}{3\sqrt{3}}, 0\right)_{\alpha\beta} \\
\mathbf{V}_3 &= \frac{1}{3}(443) + \frac{1}{3}(332) + \frac{1}{3}(221) = \left(\frac{1}{3\sqrt{3}}, \frac{1}{3}\right)_{\alpha\beta} \\
\mathbf{V}_4 &= \frac{1}{4}(443) + \frac{1}{4}(432) + \frac{1}{4}(321) + \frac{1}{4}(211) = \left(\frac{\sqrt{3}}{4}, \frac{1}{4}\right)_{\alpha\beta} \\
\mathbf{V}_{5,1} &= \frac{1}{2}(422) + \frac{1}{2}(211) = \left(\frac{1}{\sqrt{3}}, 0\right)_{\alpha\beta} \\
\mathbf{V}_{5,2} &= \frac{1}{2}(433) + \frac{1}{2}(311) = \left(\frac{1}{\sqrt{3}}, 0\right)_{\alpha\beta} \\
\mathbf{V}_{6,1} &= \frac{1}{2}(442) + \frac{1}{2}(221) = \left(\frac{1}{2\sqrt{3}}, \frac{1}{2}\right)_{\alpha\beta} \\
\mathbf{V}_{6,2} &= \frac{1}{2}(443) + \frac{1}{2}(331) = \left(\frac{1}{2\sqrt{3}}, \frac{1}{2}\right)_{\alpha\beta} \\
\mathbf{V}_{7,1} &= \frac{1}{3}(442) + \frac{1}{3}(421) + \frac{1}{3}(211) = \left(\frac{\sqrt{3}}{3}, \frac{1}{3}\right)_{\alpha\beta} \\
\mathbf{V}_{7,2} &= \frac{1}{3}(443) + \frac{1}{3}(431) + \frac{1}{3}(311) = \left(\frac{\sqrt{3}}{3}, \frac{1}{3}\right)_{\alpha\beta} \\
\mathbf{V}_8 &= (411) = (2/\sqrt{3}, 0)_{\alpha\beta} \\
\mathbf{V}_9 &= (441) = (1/\sqrt{3}, 1)_{\alpha\beta}.
\end{aligned} \tag{1}$$

These vectors have associated average MP currents in every switching cycle equal to zero, due to analogous reasons as those discussed for the three-level converter [5].

Note that virtual vectors \mathbf{V}_5 , \mathbf{V}_6 and \mathbf{V}_7 present redundancy. There are two possible elementary combinations of switching states to define each VV ($\mathbf{V}_{5,1}$ and $\mathbf{V}_{5,2}$ for \mathbf{V}_5 ; $\mathbf{V}_{6,1}$ and $\mathbf{V}_{6,2}$ for \mathbf{V}_6 ; $\mathbf{V}_{7,1}$ and $\mathbf{V}_{7,2}$ for \mathbf{V}_7). In fact, any combination of both elementary options can be used to implement virtual vectors \mathbf{V}_5 , \mathbf{V}_6 and \mathbf{V}_7 :

$$\begin{aligned}
\mathbf{V}_5(x_5) &= x_5 \cdot \mathbf{V}_{5,1} + (1-x_5) \cdot \mathbf{V}_{5,2} \\
&= \frac{x_5}{2}(422) + \frac{x_5}{2}(211) + \frac{1-x_5}{2}(433) + \frac{1-x_5}{2}(311) \\
\mathbf{V}_6(x_6) &= x_6 \cdot \mathbf{V}_{6,1} + (1-x_6) \cdot \mathbf{V}_{6,2} \\
&= \frac{x_6}{2}(442) + \frac{x_6}{2}(221) + \frac{1-x_6}{2}(443) + \frac{1-x_6}{2}(331) \\
\mathbf{V}_7(x_7) &= x_7 \cdot \mathbf{V}_{7,1} + (1-x_7) \cdot \mathbf{V}_{7,2} \\
&= \frac{x_7}{3}(442) + \frac{x_7}{3}(421) + \frac{x_7}{3}(211) + \\
&\quad + \frac{1-x_7}{3}(443) + \frac{1-x_7}{3}(431) + \frac{1-x_7}{3}(311),
\end{aligned} \tag{2}$$

where $x_5, x_6, x_7 \in [0, 1]$.

A particularly interesting combination is obtained when $x = 0.5$, since it represents an equitable combination of all switching states involved.

B. Virtual Space Vector Selection

The synthesis of the reference vector in each switching cycle is performed using the nearest three virtual space vectors. This defines nine small triangular regions in the diagram of Fig. 3. Table I specifies the selected virtual space vectors in the cases where the tip of \mathbf{V}_{ref} is in regions 1–9.

The duty ratio of each selected vector in each switching period is calculated as

$$\begin{aligned}
\mathbf{V}_{\text{ref}} &= d_{VV1} \cdot \mathbf{V}\mathbf{V}_1 + d_{VV2} \cdot \mathbf{V}\mathbf{V}_2 + d_{VV3} \cdot \mathbf{V}\mathbf{V}_3 \\
0 &\leq d_{VVj} \leq 1
\end{aligned} \tag{3}$$

$$d_{VV1} + d_{VV2} + d_{VV3} = 1$$

where $\mathbf{V}\mathbf{V}_j$ corresponds to the j th selected virtual space vector ($j = 1, 2, 3$).

Then, the corresponding duty ratio of the different switching states can be calculated. For the first sextant

$$\begin{aligned}
d_{222} = d_{333} &= \frac{1}{2}d_{V1}, \quad d_{433} = \frac{1}{3}d_{V2} + \frac{1-x_5}{2}d_{V5} \\
d_{322} &= \frac{1}{3}d_{V2}, \quad d_{332} = \frac{1}{3}d_{V3}, \quad d_{432} = \frac{1}{4}d_{V4} \\
d_{211} &= \frac{1}{3}d_{V2} + \frac{1}{4}d_{V4} + \frac{x_5}{2}d_{V5} + \frac{x_7}{3}d_{V7} \\
d_{443} &= \frac{1}{3}d_{V3} + \frac{1}{4}d_{V4} + \frac{1-x_6}{2}d_{V6} + \frac{1-x_7}{3}d_{V7} \\
d_{221} &= \frac{1}{3}d_{V3} + \frac{x_6}{2}d_{V6}, \quad d_{321} = \frac{1}{4}d_{V4}, \quad d_{422} = \frac{x_5}{2}d_{V5} \\
d_{311} &= \frac{1-x_5}{2}d_{V5} + \frac{1-x_7}{3}d_{V7}, \quad d_{442} = \frac{x_6}{2}d_{V6} + \frac{x_7}{3}d_{V7} \\
d_{331} &= \frac{1-x_6}{2}d_{V6}, \quad d_{431} = \frac{x_7}{3}d_{V7} \\
d_{421} &= \frac{x_7}{3}d_{V7}, \quad d_{411} = d_{V8}, \quad d_{441} = d_{V9}.
\end{aligned} \tag{4}$$

C. Switching States Sequence

Finally, the sequence over time within a switching cycle of the application of the different switching states has to be decided. The chosen switching states' order is such that the sequence of connection of each phase to the dc-link points is the symmetrical 4-3-2-1-2-3-4, as shown in Fig. 4. This can be achieved by simply ordering the switching-states three-digit number in descending-ascending order.

TABLE I
SELECTION OF VV FOR EACH TRIANGULAR REGION

Region	Selected VV		
	General NTV ²	NTV ² _A	NTV ² _B
1	$\mathbf{V}_1, \mathbf{V}_2, \mathbf{V}_3$	$\mathbf{V}_1, \mathbf{V}_2, \mathbf{V}_3$	$\mathbf{V}_1, \mathbf{V}_2, \mathbf{V}_3$
2	$\mathbf{V}_2, \mathbf{V}_3, \mathbf{V}_4$	$\mathbf{V}_2, \mathbf{V}_3, \mathbf{V}_4$	$\mathbf{V}_2, \mathbf{V}_3, \mathbf{V}_4$
3	$\mathbf{V}_2, \mathbf{V}_4, \mathbf{V}_5$	$\mathbf{V}_2, \mathbf{V}_4, \mathbf{V}_5(0.5)$	$\mathbf{V}_2, \mathbf{V}_4, \mathbf{V}_5(0.5)$
4	$\mathbf{V}_3, \mathbf{V}_4, \mathbf{V}_6$	$\mathbf{V}_3, \mathbf{V}_4, \mathbf{V}_6(0.5)$	$\mathbf{V}_3, \mathbf{V}_4, \mathbf{V}_6(0.5)$
5	$\mathbf{V}_4, \mathbf{V}_5, \mathbf{V}_7$	$\mathbf{V}_4, \mathbf{V}_5(1), \mathbf{V}_7(1)$	$\mathbf{V}_5(1), \mathbf{V}_6(1), \mathbf{V}_7(1)$
6	$\mathbf{V}_4, \mathbf{V}_6, \mathbf{V}_7$	$\mathbf{V}_4, \mathbf{V}_6(1), \mathbf{V}_7(1)$	$\mathbf{V}_5(1), \mathbf{V}_6(1), \mathbf{V}_7(1)$
7	$\mathbf{V}_5, \mathbf{V}_7, \mathbf{V}_8$	$\mathbf{V}_5(1), \mathbf{V}_7(1), \mathbf{V}_8$	$\mathbf{V}_5(1), \mathbf{V}_7(1), \mathbf{V}_8$
8	$\mathbf{V}_6, \mathbf{V}_7, \mathbf{V}_9$	$\mathbf{V}_6(1), \mathbf{V}_7(1), \mathbf{V}_9$	$\mathbf{V}_6(1), \mathbf{V}_7(1), \mathbf{V}_9$
9	$\mathbf{V}_7, \mathbf{V}_8, \mathbf{V}_9$	$\mathbf{V}_7(0.5), \mathbf{V}_8, \mathbf{V}_9$	$\mathbf{V}_7(0.5), \mathbf{V}_8, \mathbf{V}_9$

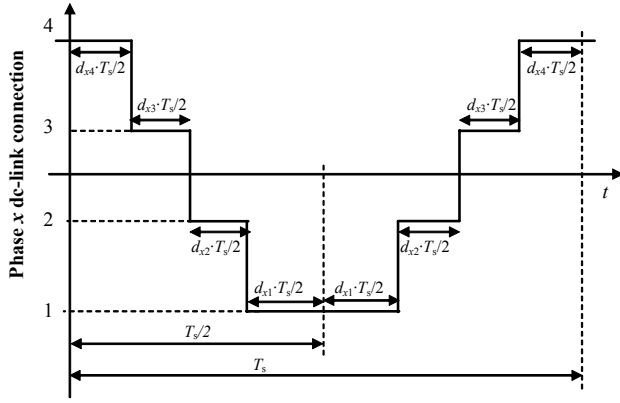


Fig. 4. Selected sequence of connection of phase x (a, b or c) to each of the dc-link points (1, 2, 3, and 4).

Therefore, a practical implementation of the proposed modulation strategy only requires the computation of duty ratios $d_{a1}, d_{b1}, d_{c1}, d_{a2}, d_{b2}, d_{c2}, d_{a3}, d_{b3}, d_{c3}, d_{a4}, d_{b4}, d_{c4}$ (where d_{xy} is the duty ratio of the phase x connection to the dc-link point y), as the addition of the appropriate switching state duty ratios calculated in Section II.B. For example, in the first sextant, to obtain d_{a2}

$$d_{a2} = d_{222} + d_{221} + d_{211}. \quad (5)$$

D. Phase Duty-Ratio Expressions

Fig. 5 shows the simulated duty ratios d_{a1} and d_{a4} , for any NTV² PWM, $m = 0.8$ and a line period. The simple pattern observed for d_{a4} can be mathematically expressed as

$$\begin{aligned} 0 \leq \theta < 2\pi/3: & \quad d_{a4} = m \cdot \cos(\theta - \pi/6) \\ 2\pi/3 \leq \theta < 4\pi/3: & \quad d_{a4} = 0 \\ 4\pi/3 \leq \theta < 2\pi: & \quad d_{a4} = m \cdot \cos(\theta + \pi/6). \end{aligned} \quad (6)$$

The expression for duty ratio d_{a1} is the same as (6) but phase-shifted 180°. The expressions for the b and c phase duty ratios are the same as for phase a, but phase shifted 120° and 240°, respectively. These expressions allow obtaining directly $d_{a1}, d_{b1}, d_{c1}, d_{a4}, d_{b4}, d_{c4}$ as a function of the reference vector length m and angle θ , without the need of identifying the triangle in which the reference vector is located and then performing calculations (3)–(5). This significantly simplifies the computations. Note that these expressions are the same as for $d_{an}, d_{bn}, d_{cn}, d_{ap}, d_{bp}, d_{cp}$ in the three-level converter [5].

The expressions for $d_{a2}, d_{b2}, d_{c2}, d_{a3}, d_{b3}, d_{c3}$ depend upon the selection of x_5, x_6 , and x_7 .

III. PARTICULAR MODULATION STRATEGIES

In the preceding Section, we have presented the general NTV² PWM for the four-level three-phase dc-ac converter. In order to determine a particular modulation strategy, we still need to select the proper value of x_5, x_6, x_7 ; i.e., which combination of the redundant VV we will use to implement V_5, V_6 and V_7 . A choice of $x_5, x_6, x_7 = 0.5$ seems to be good a priori, since all possible redundant VV are then equally employed in approximating the reference vector.

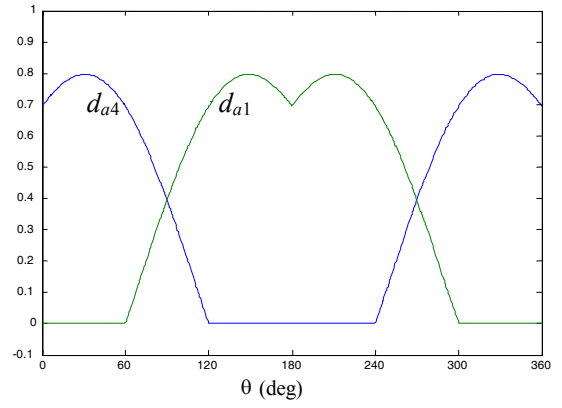


Fig. 5. d_{a1} and d_{a4} as a function of θ ($m = 0.8$).

The resulting expressions for d_{a2} and d_{a3} are very simple:

$$d_{a2} = d_{a3} = \frac{1 - d_{a1} - d_{a4}}{2}. \quad (7)$$

However, in triangles 5–8 this solution leads to employ a set of switching states that cannot follow the sequence defined in Fig. 4, and the number of switching transitions in these four triangles would be much higher than in others. An alternative could be to set $x_5, x_6, x_7 = 1$ (or = 0) in regions 5–8, defining what we designate as the NTV²_A modulation solution (see Table I). Still, this solution presents a pattern for the phase duty-ratios d_{a2} and d_{a3} in regions 5 and 6 that can be simplified if we select virtual vectors V_5, V_6 , and V_7 in both regions, defining what we designate as the NTV²_B modulation solution (see Table I). Since we are not selecting the true nearest three VV in triangles 5 and 6, the output voltage distortion will increase slightly, but not significantly. As a result, solution NTV²_B presents a fairly simple duty-ratio pattern. For the first sextant:

$$\begin{aligned} \text{Regions 1–4 and 9: } & \quad d_{a2} = d_{a3} = \frac{1 - d_{a1} - d_{a4}}{2} \\ \text{Regions 5–8: } & \quad d_{a2} = 1 - d_{a1} - d_{a4} \\ & \quad d_{a3} = 0. \end{aligned} \quad (8)$$

Solution NTV²_A presents 7 pairs of switching transitions (one switch turns off and another turns on) in regions 1–6 and 9 per half switching cycle. In regions 7 and 8 presents only 6 pairs of switching transitions. Solution NTV²_B presents 7 pairs of switching transitions in regions 1–4 and 9. In regions 5–8, it only presents 6. Therefore, solution NTV²_B is also superior from the point of view of switching transitions.

IV. SIMULATION RESULTS

The performance of the proposed modulation has been verified through simulation. The converter has been modeled in Matlab-Simulink and simulations have been carried out in open loop. The performance of the proposed modulation is compared to a particular NTV PWM. In this modulation used as a reference for comparison, the duty ratio assigned to each space vector is equally shared in every switching cycle by all associated switching states. Fig. 6 presents the results of the

comparison at $m = 0.75$ for the phase a duty ratios and the dc-link capacitor voltages. As expected, the proposed modulation guarantees the dc-link balance while the NTV PWM not only can not guarantee the balance but also leads to the collapse of v_{C2} . In Fig. 7, we observe that the dc-link voltage balance is achieved at the expense of a higher output voltage distortion compared to what one would obtain from a NTV PWM if the dc-link capacitors were replaced by dc voltage sources.

V. EXPERIMENTAL RESULTS

Experimental tests have been conducted to verify the performance observed in simulations. A 1 kW prototype has been used for this purpose. The converter is operated in open loop, with a dc power supply connected between dc-link points 1 and 4 and a three-phase series R-L load connected to the ac side. The computation of the nine independent phase duty-ratios is performed by the embedded PowerPC of dSpace

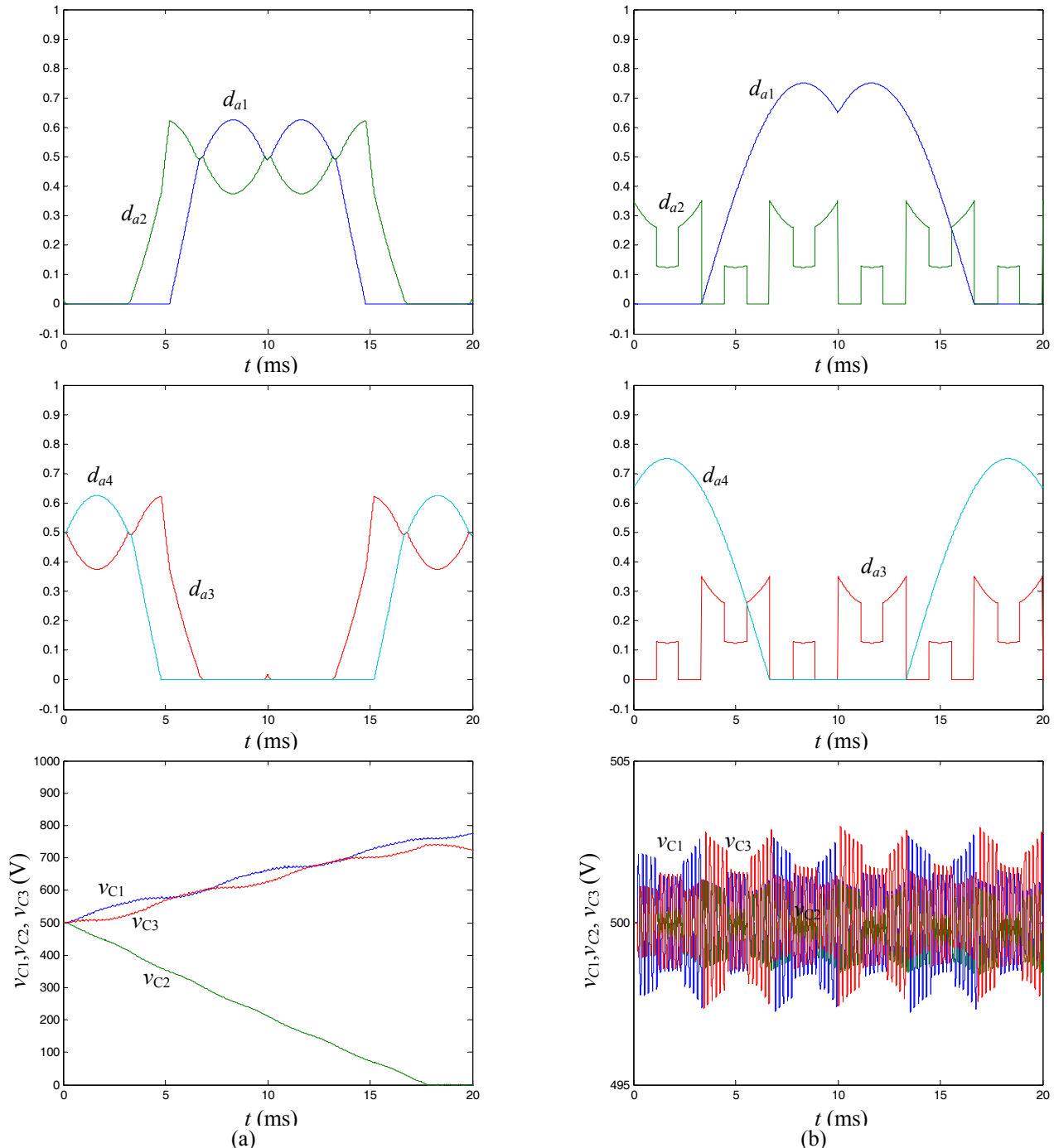


Fig. 6. Simulation results for d_{a1} , d_{a2} , d_{a3} , d_{a4} , v_{C1} , v_{C2} and v_{C3} in the following conditions: $V_{dc} = 1500$ V, $m = 0.75$, $C = 0.5$ mF, $f_s = 5$ kHz, and a linear and balanced load with per-phase impedance $Z_L = 10.5 \Omega \angle 17.5^\circ$ (series R-L load). (a) Reference NTV PWM. (b) Proposed NTV²_A and NTV²_B PWM.

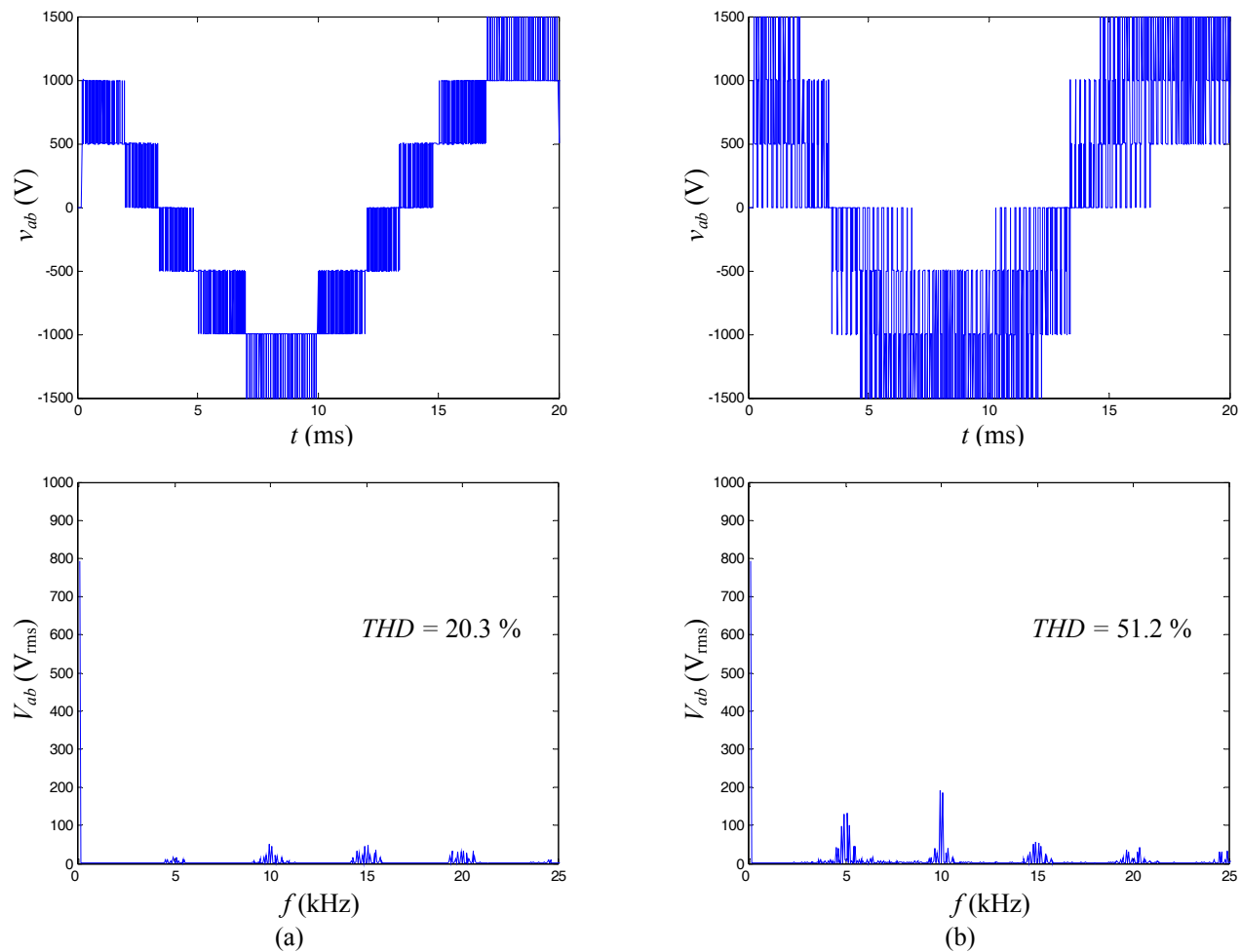


Fig. 7. Simulation results for output voltage v_{ab} , and $\text{FFT}(v_{ab})$ in the following conditions: $V_{pn} = 1500$ V, $m = 0.75$, $C = \infty$, $f_s = 5$ kHz, and a linear and balanced load with per-phase impedance $Z_L = 10.5 \Omega \angle 17.5^\circ$ (series R - L load). (a) Reference NTV PWM. (b) Proposed NTV²_A and NTV²_B PWM.

DS1103. This information is sent to an Altera EPF10K70 programmable logic device in charge of generating the eighteen switch control signals.

In Fig. 8, we can observe that the NTV PWM used as a reference for comparison leads to the collapse of the middle capacitor voltage. The same would occur with any other NTV PWM. On the other hand, in the proposed NTV² PWM all three capacitor voltages are fairly balanced in the absence of a closed-loop control.

VI. CONCLUSIONS

A new modulation approach for the comprehensive control of the dc-link capacitor voltage balance in the four-level three-phase diode-clamped dc-ac converter has been presented (patent pending). The dc-link voltage balancing is achieved for any load (linear or nonlinear, balanced or unbalanced) over the full range of converter output voltage and for all load power factors provided that $i_a + i_b + i_c = 0$. Thus, the proposed modulation not only enables the use of the four-level diode-clamped converter with passive front ends, but also allows

operating with small dc-link capacitors. The dc-link capacitance required to limit the voltage ripple across these capacitors diminishes as the switching frequency increases, eventually allowing the use of non-electrolytic capacitors.

Practical modulation strategies have been defined. The phase duty-ratio of these strategies can be described with simple mathematical expressions, leading to a very compact computation implementation. These expressions are only dependent on the modulation index and reference vector angle. In particular, they do not depend on the load. Therefore, no knowledge of the load is required to implement the proposed modulation.

The benefits of the proposed solution over conventional NTV PWM have been verified through simulation and experiments. These benefits are obtained at an expense of a higher output-voltage high-frequency distortion, compared to a NTV PWM applied to a converter with dc voltage sources replacing the dc-link capacitors. This distortion, however, can be easily attenuated using an adequate filter.

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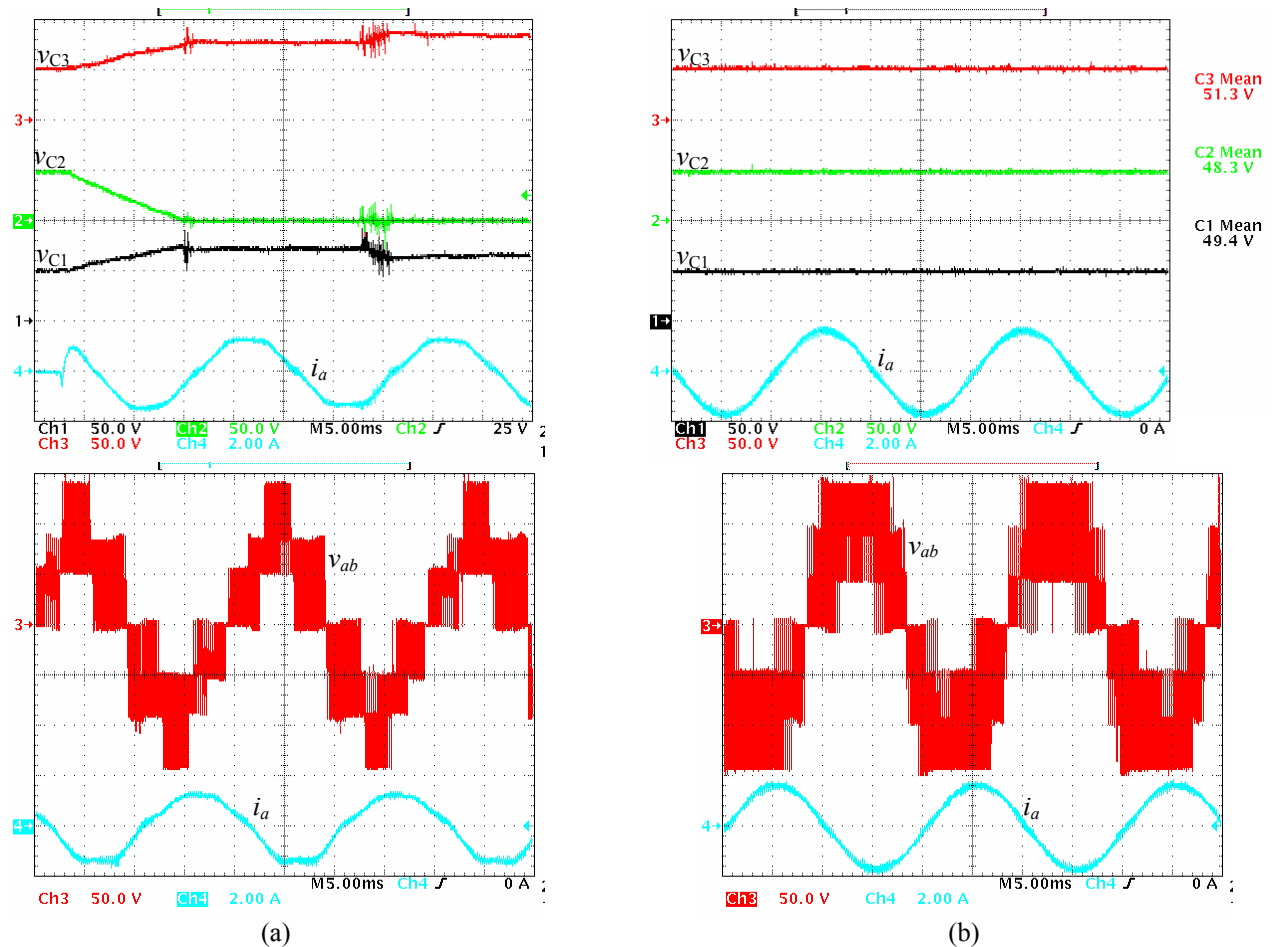


Fig. 8. Experimental results for v_{C1} , v_{C2} , v_{C3} , i_a and v_{ab} in the following conditions: $V_{dc} = 150$ V, $m = 0.75$, $C = 102$ μ F, $f_s = 5$ kHz, and a linear and balanced load with per-phase impedance $Z_L = 33.5 \Omega \angle 8.5^\circ$ (series R-L load). (a) Reference NTV PWM. (b) Proposed NTV²_A and NTV²_B PWM.