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Extension Options for 193nm Immersion Lithography

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The extension of 193nm immersion lithography (193i) has become a requirement due to the current lack of convergence of economic viability and technological capability for any other lithographic technology, at least through the 22nm node. Double patterning is currently the only direct path to 22nm without any clear showstoppers. This technology is expensive because it includes additional costly processing steps. For 22nm and beyond, technical issues such as the need to reduce line edge roughness (LER) or line width roughness (LWR) may drive innovation in lithography. The evaluation of non-chemically amplified photoresist systems may be used to trade resist sensitivity for improved LER and resolution. This work will describe the trade-offs of the candidate technologies for 22nm and beyond and specifically the efforts of several groups to extend 193nm immersion lithography.

Keywords: Next Generation Lithography, 193nm Immersion lithograph, Double Patterning, Double Exposure, non-Chemically Amplified Resist

1. Introduction

Since the emergence of the semiconductor industry, photolithography has set the innovation curve by which the industry has charted its advance. Now the photolithography community finds itself far behind the curve, trying to catch up even as new technology nodes continue to be implemented despite delays in new wavelength source or tool availability. It would be highly inaccurate to state that there has been no innovation in lithography or that the industry has been offered only one option to enable scaling beyond the 32nm node. The three main candidates for next generation lithography (NGL) are extreme ultraviolet (EUV),[1-2] electron beam (EB),[3-5] and nanoimprint lithography (NIL).[6-7] Each of these techniques offers some advantage going forward and illustrates the degree to which the industry has been innovative. However, each also has multiple issues that impede catching up to and passing the innovation curve, thus making implementation in main stream CMOS production unlikely in the near-term. Since none of these techniques is emerging as a clear leader for NGL, the continued optimization of 193nm immersion lithography is necessary to drive the economics of the semiconductor industry.

Clearly, 193nm immersion lithography with some version of double patterning (DP) technology has come to the fore as the key and necessary technology to enable the 22nm node.[8-13] The additional cost of DP technology has kept pressure on the lithographic community to find other options to reduce cost of ownership (COO). Additionally, the lack of any chemically amplified resist (CAR) meeting LER/LWR requirements for 22nm line/space (L/S) has prompted the industry to reinvestigate non-chemically amplified resist systems (nCARs).[14-17] Currently, only NIL, EB, and a DP approach have shown any results close to the required values of LER/LWR for 22nm.[18-19]

2. Next generation lithography technologies

The three major candidates to supplant 193nm immersion lithography—EUV, NIL, and EB—all have some attractive features that make their development compelling.[1] Table 1 shows some of the main advantages and disadvantages of these NGL techniques. For example, EUV promises a relaxed k_1 as we once again realize sub-wavelength imaging. Scalability and a simplified optical proximity correction (OPC)

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Table 1 Summary of NGL techniques

NGL Technique	Advantages	Disadvantages
EUVL	Enables return to high k_1 lithography Easy to moderate OPC Imaging shown to 22nm node	Poor source power (throughput) No mask making infrastructure No mask metrology infrastructure Mask design complicated by mask 3D effects Poor LER/LWR for ≤22nm node No demonstration for sub 22nm node High system maintenance costs Tool Costs 70-100M$ making the opportunity of other patterning options more attractive
EB	Narrow e-beams allow high resolution direct write Eliminates high cost mask requirements for optical litho Meets ITRS requirement for LER/LWR for 22nm	Writing speed requirement $\geq 10^6$ beams for 32nm; ~100 demonstrated Proximity effects LER/LWR poor below 22nm hp Cost of multi-e-beam system may rival EUVL
NIL	Base tool is inexpensive Meets ITRS requirement for LER/LWR for 22nm High aspect ratios can be patterned. Provides cost benefit for certain applications (HDD for example)	Throughput in CMOS based processing Defectivity (template and wafer) Template cost, lifetime, cleaning Template manufacturing infrastructure Overlay below 22nm hp

were also promises of this NGL platform. Recent results, however, have shown that the EUV light source power produced after normalization is only enough for about five hours of full manufacturing time, assuming 100 wafers per hour, 100 watts at intermediate focus, and a resist sensitivity of 10mJ/cm^2.[2] An exceptional demonstration of EUV imaging was recently shown[20] that produced 22nm contacts on a 80nm pitch. Unfortunately, these contacts needed an approximately 47 mJ/cm^2 dose to print; making the total normalized available continuous manuacturing time for EUVL just over an hour. This throughput is clearly unacceptable by any measure for economically viable volume manufacturing.

Additionally, this technique is not likely to be available until at least the 15–16 nm node.[21,22] For EUV to be introduced at this node, a higher numerical aperture (NA) of at least 0.34 will be required, causing an increased obscuration[23,24] and thus necessitating an even more powerful source. Several other issues will also be difficult to overcome in a reasonable timeframe, including the lack of metrology and mask infrastructure.[25]

EUV photoresist development has achieved resists that are approaching the dose goal of 10mJ/cm^2, but these resists are still far from the International Technology Roadmap for Semiconductors (ITRS) LER/LWR requirements for the 22 or 16nm nodes. The LER/LWR problem, in fact, seems endemic to the CAR systems in use today.[26-28] Even the use of molecular glass-based resists has not shown an improvement in ER/LWR for sub-45nm applications.[29,30]

As feature dimensions get smaller, the critical aspect ratio (AR) at which pattern collapse occurs dictates that the resist film becomes thinner with reduced critical feature dimension as shown in Figure 1.[31-35]

There is general agreement that this trend arises from the capillary forces on the patterns, adhesion failure between the resist and substrate, and deformation related to the mechanical properties of the resist.[33] The feature dimensions for the 22 and 15nm nodes will require that this decreasing trend in critical AR be continued.

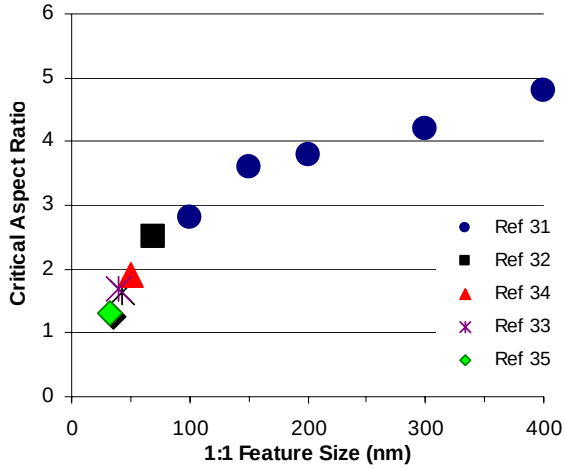


Figure 1. Illustration of the trend for the critical aspect ratio vs. resist feature size

The trend of decreasing film thickness is equally troubling for LER/LWR, since LER/LWR has been shown to increase as the resist film becomes thinner.[36-38] Figure 2 compares the general trend for LER with film thickness in conventional CAR systems.[33, 38-43] This trend, which has been noted by multiple groups, is independent of wavelength.[36,38] Although the data exhibit a significant spread, the overall trend is clear. For EUV, this trend is especially grim since introduction at the 15nm node would mean a resist film less than 40nm thick. The film thickness effect for decreasing critical aspect ratio and increasing LWR is in addition to the resolution, sensitivity, and LWR tradeoff already observed with CARs.[44]

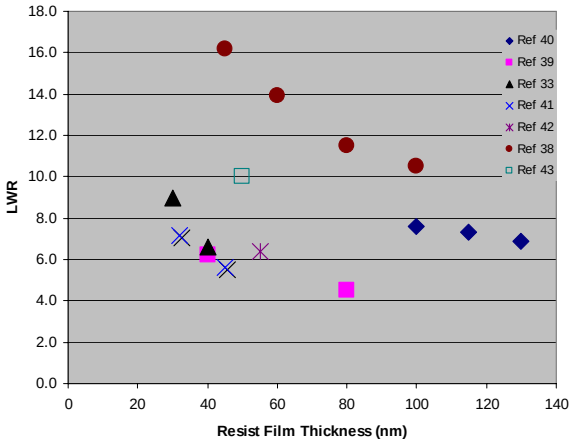


Figure 2. General trend of LER/LWR in CAR systems vs. decreasing film thickness

Fundamental work on thin film effects in polymers has shown increased free volume with decreasing thickness.[17] This effect could account for the mechanical aspects of pattern collapse that reduce the critical AR and could also explain the increase in LWR because of enhanced diffusion of acid in thinner, less dense resist films.

One possible opportunity to circumvent the LWR vs. film thickness trend is to use a non-CAR (nCAR) system, eliminating the diffusion blur. This, however, would likely require a significant increase in dose compared to conventional CAR systems and EUV already has a shortage of photons.

The two other NGL techniques can both reduce LER/LWR. NIL and EB have demonstrated LER values in the 2–3nm range[18,45], which is good enough for 32nm but not the nodes beyond.

EB direct write lithography has recently regained interest as an NGL technique.[3-5] As shown in Table 1, it can eliminate costly photomasks. The increasing cost of masks with each generation has put an especially onerous economic burden on companies producing few wafers per mask set. The promise of EB lithography is particularly applicable for such manufacturers.[3-5]

Fundamentally, EB lithography has had limited application due to the write speed, making it useful for mask writing or very small volume applications. The total write time is described by equation 1,

$$(D)(A)= [(C)(t)/S]^2= Q, \qquad (1)$$

where D is dose in Coulombs/cm^2, A is exposed area in cm^2, C is beam current in Amperes, S is the step size, and Q is the total charge of incident electrons. In addition to the write time problem is the growing data density with each subsequent technology node, which makes leapfrogging EB over other techniques unlikely.[46] Already for the sub-90nm node, a multi-terabit data stream will be required-an additional challenge to throughput.[46]

The required data stream will increase by three orders of magnitude by the 15–16nm node, at which EB lithography would most likely find a possible insertion point.

Currently, some multi-beam systems have over 100 directed beams,[3] but the throughput with these systems for just the 32nm node would be less than a wafer per hour at best. To get to 10–12 wafers per hour, $\geq 10^6$ beams are needed for reasonable throughput. This technological challenge seems difficult for the industry to achieve in a timeframe of a few years. EB may be considered for just a small fraction of wafer area on a specific critical feature, which may prove economical if tool costs are low. This type of application may be an economic niche for EBL.

However, other issues must still be addressed, such as proximity effects and the need for all beams to be maintained at the same intensity and uniformity.[46,47] Resist blur at the required lowered energies for direct write EB may also prove a fundamental limit below 20nm.[47].

Any effort put into multi-EB technology will not be lost as the technology advancements will work their way into other applications. The true market niche for multi-EB systems may be back in its roots, which is mask writing or template writing for NIL. With substantial effort, the current multi-beam systems could be applied to accelerate the mask-making process. This could reduce mask costs for the entire industry, and this reduction in cost may prove essential as the

semiconductor industry migrates to double patterning lithography.

NIL has also proven itself a worthy contender for NGL (see Table 1). Its pace of advancement over the past few years has been stunning.[6,7,18,48] In less than a decade, NIL has gone from the drawing board to a major application in the disc drive industry.[7] The technique seems particularly well suited to 32nm technology and to applications requiring low LER/LWR and high ARs. Many issues still need to be addressed for broad applicability in CMOS manufacturing. Defectivity, overlay, throughput, and template cost are among key issues that must be overcome if NIL will become a mainstream lithographic technique.[18] Of particular interest is directivity for the sub-32nm node applications and the open question of whether "plug" defectivity will increase with decreasing feature size.[18] Studies in this area have yet to be completed.

NIL is still evolving and its broad application to CMOS manufacturing is still very much in question. Further areas in which this technology will be used, such as hybrid applications,[6] will no doubt emerge. For now, however, any economically feasible application of NIL or the other NGL technologies for mainstream CMOS manufacturing remains unlikely for the 22nm node and questionable for the 15nm. The lack of alternative lithography technologies implies that the only current solution for these technology nodes is some form of DP lithography.

3. Double patterning lithography

DP is a relative newcomer to lithography, brought on by necessity rather than any desire to embrace the processing methodology. Table 2 shows an overview of some of the pros and cons for different DPL technologies. Opportunity costs have made some form of DP technology the inevitable bridge to 22nm and perhaps beyond. The predicted COO[49] is nearly competitive with EUVL, assuming a 100 wafer per hour (WPH) throughput for EUVL. If we assume a more realistic 10 WPH throughput for EUVL, based on current data,[1,2,20] the COO for DPL is then significantly lower. This is an intuitive result since existing infrastructure is being used for DPL. What is unclear is the exact DPL or combination of DPL approaches that will provide the best resolution and the best economics for the 22nm node and beyond.

Figure 3 shows a couple of variations on the technology. One of the initial DP efforts was a litho-etch, litho-etch (LELE) approach that requires two etch steps.[50] Developed subsequently, the litho-freeze process requires only one etch step and uses a track process to "freeze" the resist before a second resist coat and exposure.[8,48,49] Because the freeze uses a chemical modification of the first exposed/developed resist, it is not adversely affected by subsequent lithography processing.[8,51-53] The COO for this DP approach should be less than for LELE since fewer processing steps are needed.

Table 2 Summary of DPL techniques

Double patterning /exposure approach	Advantages	Disadvantages
LELE	No fundamental limitations ≥ 22nm	Costly extra processing Challenging overlay for ≤ 22nm
LFL	No fundamental limitations ≥ 22nm Intermediate processing possible on track	Costly extra processing Challenging overlay for ≤ 22nm
SADP	Single critical exposure No overlay issues More cost effective than LELE or LFE Currently applicable to memory	2D design is quite challenging Significant extra processing required
DTD	Improved cost effectiveness	New materials development required Negative-tone materials historically difficult Does not currently meet 32nm requirements Challenging overlay for ≤ 22nm LER/LWR may be a showstopper
DE	Best overall cost No overlay issues	Materials not currently available Material integration may be difficult No intrinsic improvement for LER/LWR may limit applicability below 32nm

DPL has already shown that it is lithography's bridge for the 22nm node,[54] producing a 6T SRAM cell < 0.1μm^2 nearly six months before a similarly scaled SRAM was produced using EUVL.[20]

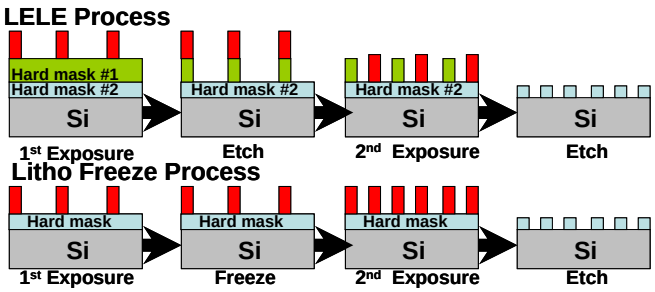


Figure 3 Schematic of two varieties of double patterning approaches

Another variation of DPL is the self-aligned double patterning (SADP) process.[55-57] Figure 4 shows the basic flow of the process: With SADP the resist is exposed followed by development; then a masking material is deposited and etched to form sidewall spacers. The resist material from the exposure step is then removed, and the substrate etched using the remaining spacers as a mask. Finally, the residual spacers are removed leaving the final pattern.

The advantages of the SADP process are that only one critical exposure is needed and overlay poses no issues. Further, critical dimension uniformities (CDUs) and LER/LWR are shown to be improved over any conventional lithography process, meeting the ITRS requirements for the 22nm node.[55-58]

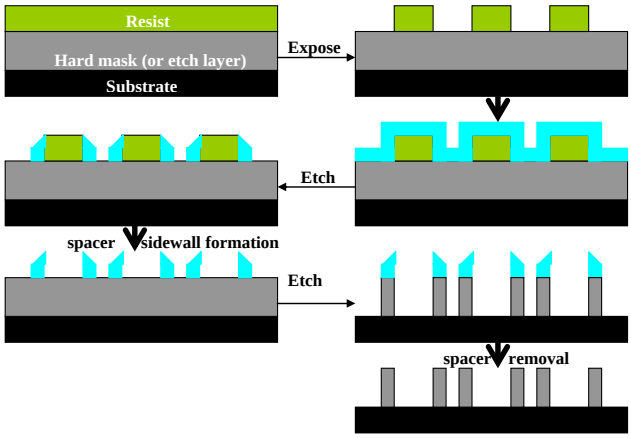


Figure 4 Schematic of the general process flow for SADP

The main limiting factor for a broad implementation of this technique is that it is not well suited to non-uniform designs.[10] Recently, however, a proposed gridded design scheme with SADP has suggested a path to 16nm on a 44nm pitch for logic.[59] Additionally, a method for contact formation using SADP has been proposed,[60] indicating that further development may enable this DP technique to have broader applicability.

Another promising contender for DPL is dual tone development (DTD),[61] in which a conventional exposure is followed by two development steps.[61] In positive tone development, all material that has been exposed to some threshold dose is removed, while in negative tone development, all material that has seen a threshold lower than a specific dose is removed.

DTD may be a path to reduced COO. However, many materials issues must be overcome.[61] Additionally, LER/LWR has been related in some measure to the development process[39,62], and the combination of two development processes may result in unacceptable LER/LWR.

In spite of the COO of DPL[63], some form of DPL will be used for 32nm and 22nm and likely beyond because it poses no fundamental showstoppers to implementation.[50-53,57] Some believe that this technology will take us to the end of the semiconductor roadmap.[64,54]

4. Materials and process for extending 193nm immersion lithography

Even with the advent of DPL, additional drivers are pushing an exploration of other ways to extend or enhance 193nm immersion lithography. At SEMATECH, several projects are focusing on extension. They fall into three categories: double exposure (DE) materials, non-chemically amplified resists (nCARs), and inorganic resists.

4.1 Double exposure materials

DE materials were conceived of as a cost mitigation alternative to DPL. In DE, the wafer is not removed from the lithography tool, thus eliminating the DPL overlay issue. No time-consuming, costly intermediate processing steps and no additional expensive equipment are needed. In DE, a conventional resist contains material(s) that have a nonlinear response in a multi-photon process at 193nm. The intermediate state, two-photon photoacid generator (PAG) (ISTP) approach was developed by the Willson group at the University of Texas (UT) and Jeffrey Byers at

SEMATECH.[66] The ISTP material using electron transfer and "latent sensitizer" sensitization was devised as shown in Figure 5. The materials are returned to the initial state by exposure to a second wavelength in the lithography tool before the second 193nm exposure. After this, the wafer completes standard processing. In collaboration with the Turro group at Columbia University, a proof-of-principle was achieved[67]

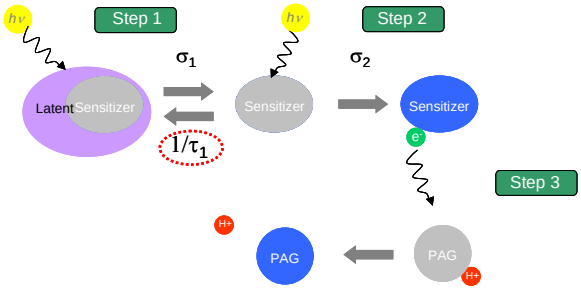


Figure 5 Schematic of ISTP approach

Additional efforts in DE materials have been supported by Intel.[68] Their approach is the same as described above. If successful, it may provide the best means to achieve imaging for the 32nm and 22nm nodes.

However, this approach has several possible drawbacks. First, the necessary materials do not yet exist. Second, even if these materials are developed, their integration into a working resist system in a timeframe useful for integration into 32nm processing will be challenging. Since this process will use diffusion, LER/LWR may limit the utility of this approach beyond the 32nm node.

4.2 Non-chemically amplified resists

With the milestone works by Willson *et al.*,[69-71] on chemically amplified resist, work in an area to supplant CARs seems almost heresy. However, since much work[15, 72,73] over the years from the Willson Group at UT has concentrated on nCAR systems, perhaps the sin may be forgiven. The development of nCARs has been ongoing for some time. Successful nCAR systems have been developed for 193nm[15,16,74]; however, these systems are typically too insensitive or require special development solvents or conditions to be considered for a manufacturing process. Past photospeed requirements for resists have prevented the use of such systems in manufacturing.

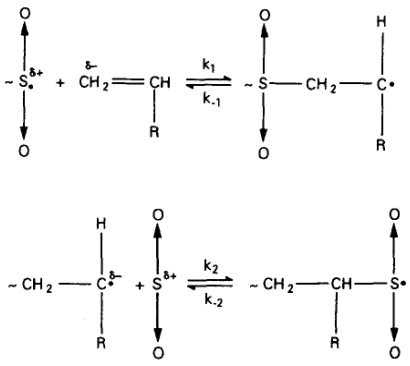
Over the past 10 years, 193nm power has steadily improved to where there is now more power than is required for exposure.[75] This additional power can be used for less sensitive resists in the hope that LER/LWR and resolution can be improved in the tradeoff with sensitivity as described by G.M. Gallatin.[44]

SEMATECH is supporting researchers exploring two distinct approaches that are believed to be the only paths that will provide the contrast needed for a high performance resist.

The first path is to adapt a previous approach using a photosensitive dissolution inhibitor.[76,77] Very good contrast can be achieved by logarithmic changes in dissolution rate versus the unexposed film.[76,77] The expectation is that because such thin films (≤40nm) will be used for 22nm and beyond, several of the systems used for i-line resists may now be worth investigation. Absorbance values of 10–18/μm may be acceptable as these values will still allow light to reach the bottom of the resist in very thin films.

The second approach uses a polymer with a ceiling temperature, T_c, that will promote depolymerization after a photo-induced chain scission event. H. Ito and C.G. Willson have described such a system, polyphthaldehyde (PPA).[78,79] After exposure with 193nm, either the blocking group is removed or a main-chain scission occurs. In either case, the polymer chain completely unzips while the unexposed polymer remains intact. However, the PPA system has an absorbance of 30/μm at 193nm; hence, it is not useful as a nCAR at 193nm. Several other systems with T_c below or close to room temperature are being investigated.

The polyolefin sulfones offer a more transparent alternative to the PPA system. Scheme 1 shows the generic mechanism for the forward and reverse reaction of sulfur dioxide and an alpha-olefin. Above the ceiling temperature (T_c), the reverse reactions dominate.[80]



Scheme 1 Mechanism for polymerisation of SO_2 and alpha-olefins. Above T_c, the reverse reactions dominate.

Although this is not an attractive scheme for lithography in general due to the release of SO_2, immersion lithography could eliminate this concern since SO_2 is highly soluble in water. Work within the Whittaker group at the University of Queensland is focusing on developing these systems.[17]

The main goal of the nCAR development is to produce a system with improved LER/LWR by eliminating the CAR diffusion process. It is unclear whether this will be enough to significantly mitigate LER/LWR at smaller feature sizes. Recent nCAR studies have shown LER/LWR improvement to have mixed results.[15,28,81] In parallel, the non-resist contributions to LER/LWR must be considered.[40,,82]

4.3 Inorganic resists

The final area of SEMATECH's efforts to extend 193nm focuses on developing an inorganic resist. For example, hydrogen silsesquioxane (HSQ) has been used for many years as a resist.[83,84]

The goal of our work here is to take a material developed for another project[85] and create a new inorganic resist. The properties of the material will improve etch resistance, depth of focus (DOF), and LER/LWR. Recently, a similar composition of materials was evaluated as an inorganic resist with promising results.[86]

Solids content and absorbance requirements have been achieved in casting solution and film. The dimensions of the inorganic nanomaterial are between 1–2nm, which is expected to help with LER/LWR in the exposed film. The exact operational mode of the material is currently under study.

5. Summary

The need to extend 193nm immersion lithography arises from the lack of a suitable NGL technology. No NGL is likely to be ready for economical mainstream CMOS manufacturing before the 16nm node. Further, catching up to the technological curve is difficult, especially when the curve is not static. In the interim, some form of DPL technologies will carry the industry through at least the 32 and 22nm nodes. This time window will allow additional development and competition among DPL technologies, making them more cost-effective.

As the extension of 193nm immersion lithography now stretches out to the horizon, new materials will continue to be needed. Projects will continue to focus on solving fundamental resist issues such as LER/LWR and etch resistance, aiding in strategies to enable cost-effective lithography for the next node.

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