Hindawi Publishing Corporation
Modelling and Simulation in Engineering
Volume 2008, Article ID 593042, 8 pages
doi:10.1155/2008/593042

Research Article

Extra-High-Voltage DC-DC Boost Converters Topology with Simple Control Strategy

P. Sanjeevikumar[1] and K. Rajambal[2]

[1] *Project Engineer, Simulation Solutions, Chennai, India*
[2] *Department of Electrical and Electronics, Pondicherry Engineering College, Pondicherry 605014, India*

Correspondence should be addressed to P. Sanjeevikumar, sanjeevi_12@yahoo.co.in

Received 4 June 2007; Accepted 21 January 2008

Recommended by Ivan Zelinka

This paper presents the topology of operating DC-DC buck converter in boost mode for extra-high-voltage applications. Traditional DC-DC boost converters are used in high-voltage applications, but they are not economical due to the limited output voltage, efficiency and they require two sensors with complex control algorithm. Moreover, due to the effect of parasitic elements the output voltage and power transfer efficiency of DC-DC converters are limited. These limitations are overcome by using the voltage lift technique, opens a good way to improve the performance characteristics of DC-DC converter. The technique is applied to DC-DC converter and a simplified control algorithm in this paper. The performance of the controller is studied for both line and load disturbances. These converters perform positive DC-DC voltage increasing conversion with high power density, high efficiency, low cost in simple structure, small ripples, and wide range of control. Simulation results along theoretical analysis are provided to verify its performance.

1. Introducton

Proceeding to the paper work [1], other two topologies are developed for extra-high-voltage applications. Traditional DC-DC boost converters are used in extra-high-voltage applications. But they are not economical due to the limited output voltage, efficiency, and they require two sensors with complex control algorithm. Because of the effect of parasitic elements, the output voltage and transfer efficiency of DC-DC converters are limited. Voltage lift technique is a popular method widely applied in electronic circuit design. It has been successfully employed in DC-DC converter [1–5] applications in recent years, and opened a way to design high-voltage gain converters. The output voltage increases stage-by-stage along the geometric progression. So to overcome these limitations and to make the DC-DC converter with a simple control loop, a new technique called voltage lift technique is used [6–11].

In this paper, a new series of DC-DC converter topologies is analyzed which is different from classical boost converter. This paper introduces positive output boost converters employed with voltage lift technique that implements the output voltage increase in a simple geometric progression. They also effectively enhance the voltage transfer gain as per power-law terms. The performance of this DC-DC converter is superior to classical DC-DC with reduced control scheme. The performance of this DC-DC converter is superior to classical DC-DC with the following advantages.

(i) It performs similar to classical DC-DC boost converter with comparatively high-voltage transfer ratio.

(ii) Wide range of control with smooth ripple at the output voltage is an added advantage of this proposed converter.

(iii) High power density with high efficiency than classical boost converter.

(iv) Closed-loop controller requires only one sensor.

In this paper, the operation and mathematical analysis of the proposed converters I and II are presented. An algorithm is developed to generate PWM pulses for the N-channel MOSFET. The simulation model of the converter is developed in

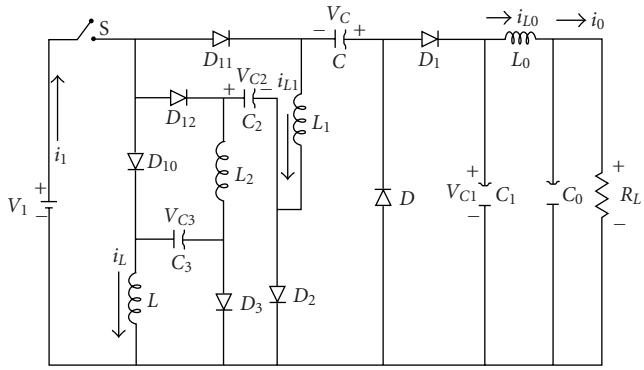

Figure 1: Topology-I of DC-DC boost converter.

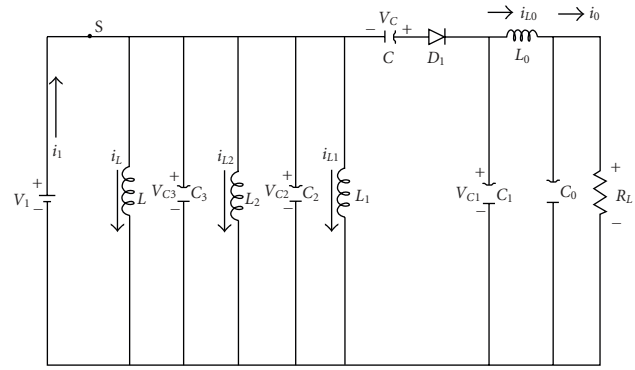

Figure 2: Topology-I (switch-ON equivalent circuit).

MATLAB7 using simulink toolbox. Simulation is carried out to study the performance of the converter under line and load disturbances. The simulation results are presented and they closely match with the theoretical results. The effectiveness of the converter is shown by comparing the performance with the classical boost converter.

2. Boost Converter Circuits

2.1. Topology-I

The proposed topology of new series of boost converter is derived from the DC-DC boost converter circuit. Topology-I is a boost converter circuit with the voltage lift components, that is, additional three stages of inductor and capacitor along with the basic circuit are shown in Figure 1. In this topology, the switch S is N-channel power MOSFET device (NMOS) and it is driven by a pulse-width-modulated (PWM) switching signal with variable frequency f and conduction duty k. For this circuit, the load is usually resistive, $R = V_0/I_0$.

The basic principle of this circuit in boosting up the output voltage is charging and discharging reactive elements into a load, controlling the levels of charge, and consequently the output voltage by switching the DC supply in and out of the circuit at very high frequencies. They include a freewheeling diode to protect the switch from the inductors high reverse currents, and this also ensures that the generated inductor energy is applied to the load. Capacitors are connected in parallel with the load to filter output ripple and maintain a constant output voltage.

It consists of passive components: one static switch S, diodes, four inductors L, L_0, L_1, L_2, and capacitors C, C_0, C_1, C_2, and C_3. Capacitors C_2 and C_3 perform the characteristics to lift the capacitor voltage V_C. The directions of all voltages and currents are defined and shown in Figure 1. We will assume that all the components are ideal and the capacitors are large enough. We also assume that the circuits operate in continuous conduction mode. The output voltage and current are V_0 and I_0 the input voltage and current are V_1 and I_1.

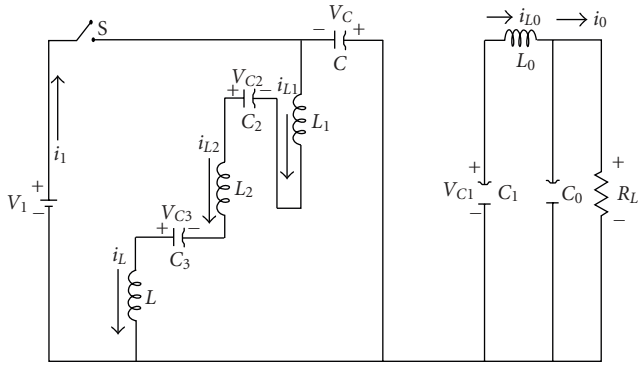

Figure 3: Topology-I (switch-OFF equivalent circuit).

2.2. Analysis of Topology-I

When switch S is turned ON, its equivalent circuit is shown in Figure 2. The source instantaneous current is equal to $i_{L1} + i_{L0} + i_{C2} + i_{L2} + i_{C3} + i_L$. The load current flows from the addition of two voltages. That is, the source voltage V_1 and the voltage across the capacitor C during ON period. Also the capacitors C_2 and C_3 are charged to the input voltage under switch-ON condition. All the inductor current rises during switch-ON period. When switch S is turned OFF, source current is equal to zero. The stored energy in the inductors L_1, L_2, and L and the capacitorsC_2 and C_3 discharges and charge the capacitor C with the direction as shown in Figure 3. Simultaneously, current i_{L0} flows through the load, which is sustained by the inductor L_0. Currents i_L, i_{L1}, and i_{L2} decrease during switch-OFF period.

In steady state, the average inductor voltages over a period are zero. Thus

$$V_{C0} = V_0. \tag{1}$$

The inductor current i_L increases in the switch-on period and decreases in the switch-off period. The corresponding voltages across L are V_1, and $-V_{L\text{-OFF}}$.

Therefore,

$$\begin{aligned} kTV_1 &= (1-k)\,TV_{L\text{-OFF}}, \\ V_{L\text{-OFF}} &= \left[\frac{k}{1-k}\right] V_1. \end{aligned} \tag{2}$$

Similarly,

$$V_{L1\text{-OFF}} = \left[\frac{k}{1-k}\right]V_1,$$
$$V_{L2\text{-OFF}} = \left[\frac{k}{1-k}\right]V_1. \tag{3}$$

During switch-on period, the voltage across capacitor C_1 is equal to the source voltage plus the voltage across C. Since we assume that C and C_1 are sufficiently large, during switch-on period,

$$V_{C0} = V_1 + V_{C1}. \tag{4}$$

Therefore, from switch-off period equivalent circuit,

$$V_C = V_{C\text{-OFF}} = V_{L\text{-OFF}} + V_{L1\text{-OFF}} + V_{L2\text{-OFF}} + V_{C2} + V_{C3},$$
$$V_C = \left(\frac{k}{1-k}\right)V_1 + \left(\frac{k}{1-k}\right)V_1 + \left(\frac{k}{1-k}\right)V_1 + V_1 + V_1,$$
$$V_C = \frac{3k}{1-k}V_1 + 2V_1,$$
$$V_0 = V_C + V_1,$$
$$V_0 = \left[\frac{3}{1-k}\right]V_1. \tag{5}$$

The voltage transfer gain of continuous conduction mode (CCM) is

$$M = \frac{V_0}{V_1} = \frac{3}{1-k}. \tag{6}$$

The output voltage, current, and the voltage transfer gain are summarized as follows:

$$V_0 = \left[\frac{3}{1-k}\right]V_1,$$
$$i_0 = \left[\frac{1-k}{3}\right]i_1, \tag{7}$$
$$M = \frac{3}{1-k}.$$

Average voltages are

$$V_C = \left[\frac{2+k}{1-k}\right]V_1,$$
$$V_{C1} = V_0, \tag{8}$$
$$V_{C2} = V_{C3} = V_1.$$

Average currents are

$$i_{L0} = i_0,$$
$$i_{L1} = i_{L2} = i_L = \left[\frac{1}{1-k}\right]i_0. \tag{9}$$

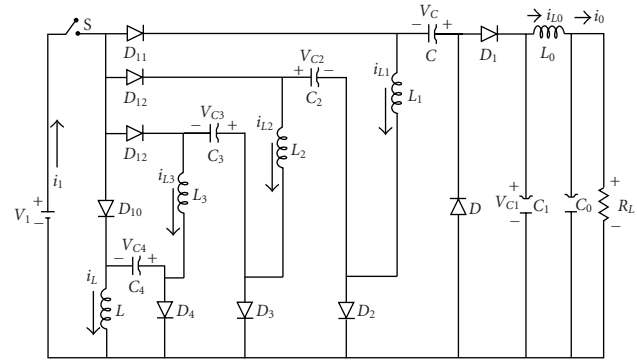

Figure 4: Topology-II of DC-DC boost converter.

2.3. Topology-II

Topology-II of the DC-DC boost converter is derived from topology-I. Topology-II is the same as topology-I circuit with the additional voltage lift components, that is, capacitor and inductors in addition to that of the topology-I circuit. The output voltage and current of this converter are smooth. The output voltage of this converter is four times that of the input source voltage. It consists of a static switch S, diodes D, D_1, D_2, D_3, D_4, D_{10}, D_{11}, D_{12}, and D_{13}, inductors L, L_0, L_1, L_2, and L_3 capacitors C, C_1, C_2, C_3, and C_4, and the output capacitor C_0. It can be seen that there are one capacitor C_4, one inductor L_3, and two diodes D_4 and D_{13} added into the circuit. Capacitors C_1, C_2, C_3, and C_4 perform characteristics to lift the capacitor voltage Vc by four times that of source voltage V_S. The directions of all voltages and currents are defined and shown in the Figure 4.

It is assumed that all the components are ideal and the capacitors are large enough. It is also assumed that the circuits operate in continuous conduction mode. The output voltage and current are V_0 and I_0, while the input voltage and current are V_I and I_1. Topology-II performs a positive-to-positive DC-DC step-up voltage conversion with high efficiency, high power density and cheap topology in a simple structure.

2.4. Analysis of Topology-II

When switch S is turned ON, the equivalent circuit is shown in Figure 5. The source instantaneous current is equal to $i_{L1} + i_{L0} + i_{C2} + i_{L2} + i_{C3} + i_L + i_{C4} + i_{L3}$. The load current flows from the addition of two voltages, That is, the source voltage V_1 and the voltage across the capacitor C during switch-ON period. Also the capacitors C_2, C_3, and C_4 are charged to the input voltage under switch-ON condition. All the inductor current rises during switch-ON period. When switch S turned OFF, source current is equal to zero and equivalent circuit is shown in Figure 6. The stored energy in the inductors L_1, L_2, L_3, and L and the capacitors C_2, C_3, and C_4 discharges and charges the capacitor C with the direction as shown in Figure 6. Simultaneously, current i_{L0} flows through the load, which is sustained by the inductor

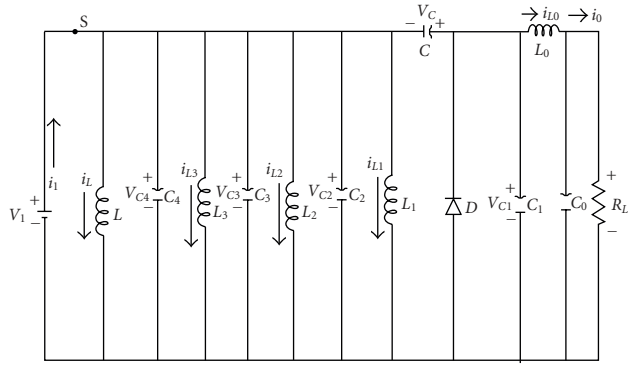

Figure 5: Topology-II (switch-ON equivalent circuit).

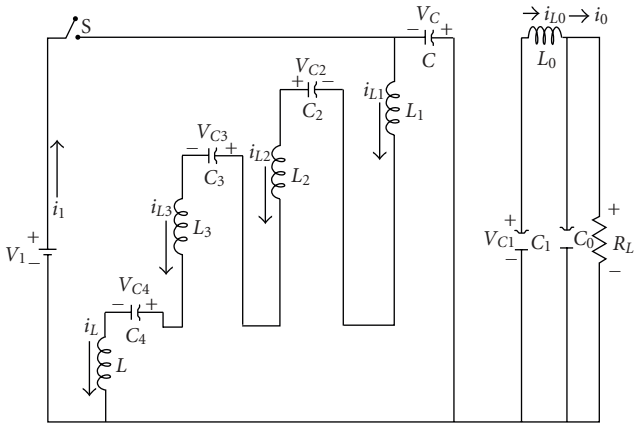

Figure 6: Topology-II (switch-OFF equivalent circuit).

L_0. All the inductor currents decrease during the switch-OFF period.

Under steady state, the average inductor voltages over a period are zero. Thus

$$V_{C0} = V_0. \tag{10}$$

During switch-on period,

$$V_{C2} = V_{C3} = V_{C4} = V_1. \tag{11}$$

Also

$$V_0 = V_{C1} = V_C + V_1. \tag{12}$$

The inductor current I_L increases in the switch-on period and decreases in the switch-off period. The corresponding voltages across L are V_1 and $-V_{L\text{-OFF}}$.

Therefore,

$$\begin{aligned} kTV_1 &= (1-k)TV_{L\text{-OFF}}, \\ V_{L\text{-OFF}} &= \left[\frac{k}{1-k}\right]V_1. \end{aligned} \tag{13}$$

Similarly, for $L_1, L_2,$ and L_3,

$$\begin{aligned} V_{L1\text{-OFF}} &= \left[\frac{k}{1-k}\right]V_1, \\ V_{L2\text{-OFF}} &= \left[\frac{k}{1-k}\right]V_1, \\ V_{L3\text{-OFF}} &= \left[\frac{k}{1-k}\right]V_1. \end{aligned} \tag{14}$$

From switch-off period equivalent circuit,

$$\begin{aligned} V_C &= V_{C\text{-OFF}} = V_{L\text{-OFF}} + V_{L1\text{-OFF}} + V_{L2\text{-OFF}} \\ &\quad + V_{L3\text{-OFF}} + V_{C2} + V_{C3} + V_{C4}, \\ V_C &= \frac{4k}{1-k}V_1 + 3V_1, \\ V_0 &= V_C + V_1, \\ V_0 &= \left[\frac{4k}{1-k}\right]V_1. \end{aligned} \tag{15}$$

The output voltage, current, and voltage transfer gain are summarized below

$$\begin{aligned} V_0 &= \left[\frac{4}{1-k}\right]V_1, \\ i_0 &= \left[\frac{1-k}{4}\right]i_1, \\ M_0 &= \frac{4}{1-k}. \end{aligned} \tag{16}$$

Average voltages are

$$\begin{aligned} V_C &= \left[\frac{3+k}{1-k}\right]V_1, \\ V_{C1} &= V_0, \\ V_{C2} &= V_{C3} = V_{C4} = V_1. \end{aligned} \tag{17}$$

Average currents are

$$\begin{aligned} i_{L0} &= i_0, \\ i_L &= \left[\frac{k}{1-k}\right]i_0, \\ i_{L1} &= i_{L2} = i_{L3} = i_L + i_{L0} = \left[\frac{1}{1-k}\right]i_0. \end{aligned} \tag{18}$$

Table 1 illustrates the comparison between the analyzed DC-DC converters with the classical boost converter. From the table, it is clear that the proposed converter topology produces higher output DC voltage.

3. Closed-Loop Controller for Proposed Boost Converter

Closed-loop control scheme for the proposed DC-DC boost converter topology is shown in Figures 7 and 8. The control

Table 1: Performance comparison of the proposed DC-DC boost converter with classical boost converter.

DC-DC converters	Output voltage (V_0) (volts)	Output current (i_0) (amps)
Classical boost converter	$V_0 = [k/(1-k)]V_1$	$i_0 = [(1-k)/k]i_1$
Boost converter topology-I	$V_0 = [3/(1-k)]V_1$	$i_0 = [(1-k)/3]i_1$
Boost converter topology-II	$V_0 = [4/(1-k)]V_1$	$i_0 = [(1-k)/4]i_1$

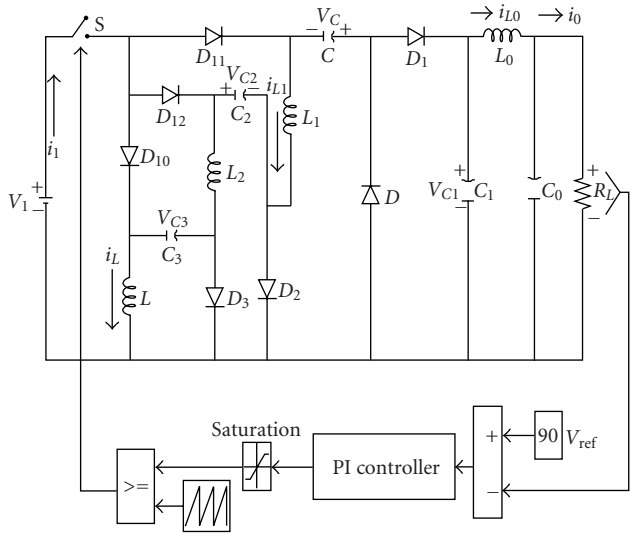

Figure 7: Closed-loop controller for topology-I DC-DC boost converter.

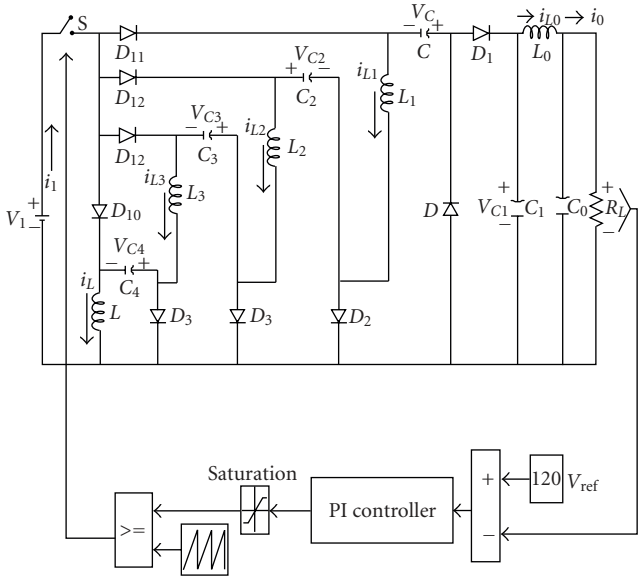

Figure 8: Closed-loop controller for topology-II DC-DC boost converter.

scheme essentially consists of only one voltage sensor with simple control structure when compared with classical DC-DC boost converter which requires both voltage and current sensors. DC voltage of the load is fed back and compared with V_{dc} reference voltage and the error is given to the PI controller to stabilize the error and the signal obtained from the controller is the modulating signal for the PWM scheme. Signal from the PI controller is compared with high frequency ramp signal to produce required pulse for the N-channel MOSFET switch to obtain the reference DC voltage at the load. In this paper, for the above model of the converter [12, 13] using the Ziegler-Nichols method 1 is (S-shaped curve technique) applied to design the PI controller.

Step input is applied to the plant model and the response is the S shaped curve. By drawing the tangent to the S-shaped curve at its inflection point with reference to X-axis, the time delay L and time constant $T$are calculated. Using [12] Ziegler-Nichols chart, the value of the K_p and $T_i$is calculated. The PI controller designed by the above method is tested under different disturbance conditions and results are provided for the feasibility. Closed control schemes for both topologies are the same and tuning parametersK_p and K_i are different.

4. Simulation Results

Simulation results of the proposed DC-DC boost converter topologies with simplified controller scheme are presented

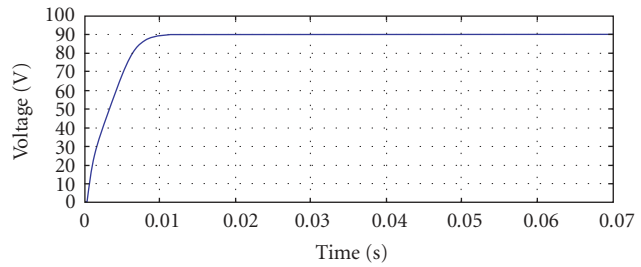

Figure 9: Output voltage at rated condition for topology-I.

and discussed further. Design of inductance and capacitance is based on 5% ripple at the output [14] and the values are the same for both load and lift part of the circuit.

Simulation parameters taken for analysis are
Input voltage V_1 = 10 volts,
Inductance = 100 μH,
Capacitance = 5 μF,
Load resistance = 44 ohms,
Duty ratio k = 0.6666,
Switching frequency = 50 KHz.
PI controller transfer function:

$$\text{Topology-I: } G(s) = \frac{0.065684(\text{S}+5500.2)}{\text{S}},$$
$$\text{Topology-II: } G(s) = \frac{0.065011(\text{S}+9000)}{\text{S}}. \quad (19)$$

Table 2: Comparison of simulation result of the proposed converters with classical converter at steady state condition for rated load.

Duty ratio (k)	Output voltage (V_0) classical converter	Output voltage (V_0) proposed topology-I	Output voltage (V_0) proposed topology-II
0.1	1.11	33.33	44.44
0.2	2.5	37.5	50
0.3	4.28	42.85	57.14
0.4	6.66	50	66.66
0.5	10	60	80
0.6	15	75	100
0.7	23.33	100	133.33
0.8	40	150	200
0.9	90	300	400

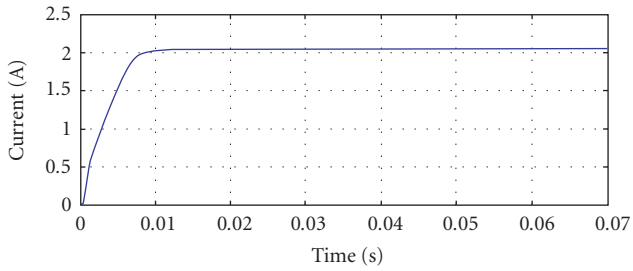

Figure 10: Output current at rated condition for topology-I.

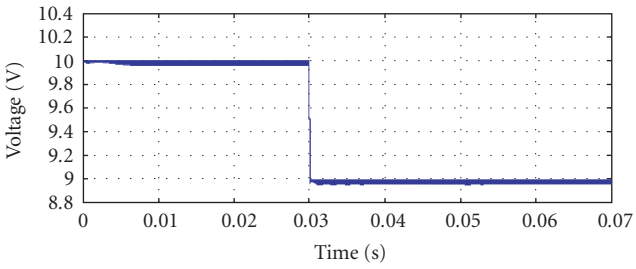

Figure 11: Line disturbance at 0.03 second for the topology-I.

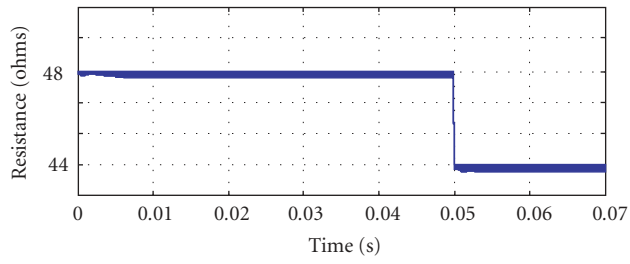

Figure 12: Load disturbance at 0.06 second for the topology-I.

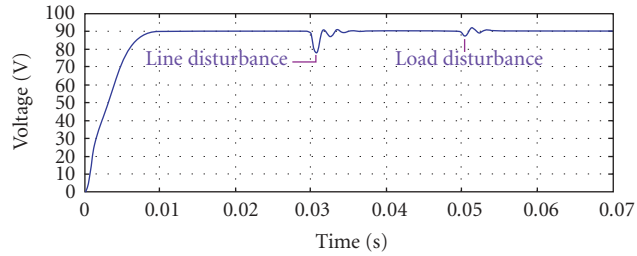

Figure 13: Output voltage of the topology-I for line and load disturbances.

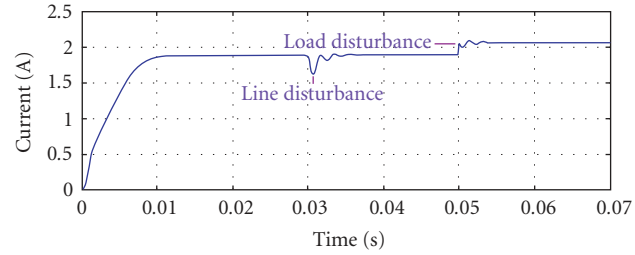

Figure 14: Output current of the topology-I under line and load disturbances.

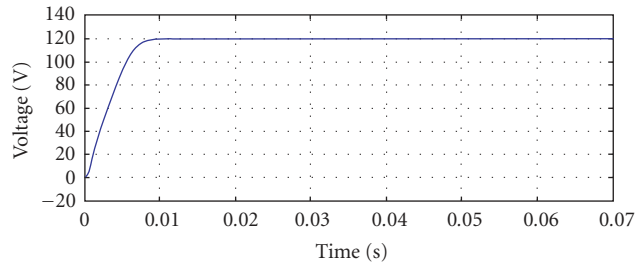

Figure 15: Output voltage at rated condition for topology-II.

Figure 9 depicts the output voltage of the converter at rated condition, maintaining 90 volts at 44 ohms load resistance, and the corresponding output current of 2.045 amperes is shown in Figure 10. Figure 11 shows the line voltage variation applied to topology-I, initially 10 volts is maintained and introduced a change to 9 volts at 0.03 second, for analyzing the line disturbance performance. Figure 12 shows the load resistance variation applied to topology-I, initially 48 ohms are maintained and introduced a change to 44 ohms at 0.05 second, for analyzing the load disturbance performance. Figure 13 illustrates the output voltage for topology-I under both line and load disturbances,

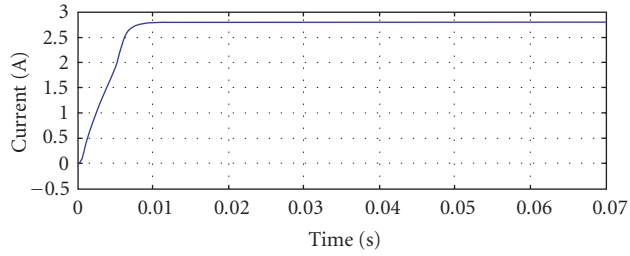

Figure 16: Output current at rated condition for topology-II.

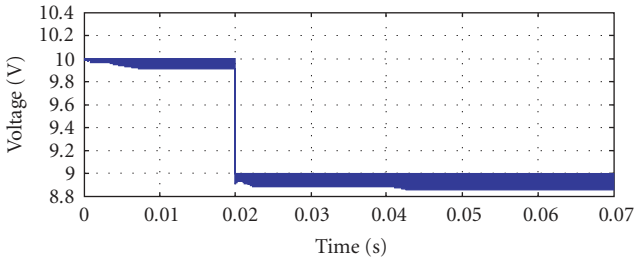

Figure 17: Line disturbance at 0.02 second for topology-II.

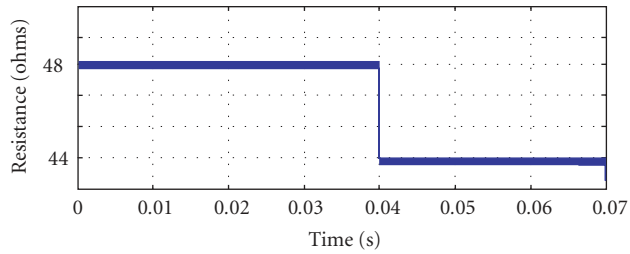

Figure 18: Load disturbance at 0.04 second for topology-II.

the output voltage stabilized in 0.005 second for both distortion conditions by the closed-loop controller. Figure 14 illustrates the output current for topology-I under line and load disturbances, as load resistance decreases from 48 ohms to 44 ohms at 0.05 second the load current increases from 1.875 amperes to 2.045 amperes.

Figure 15 depicts the output voltage of the converter at rated condition, maintaining 120 volts at 44 ohms load resistance and the corresponding output current of 2.7272 amperes is shown in Figure 16. Figure 17 shows the line voltage variation applied to topology-I, initially 10 volts are maintained and introduced a change to 9 volts at 0.02 second, for analyzing the line disturbance performance. Figure 18 shows the load resistance variation applied to topology-I, initially 48 ohms are maintained and introduced a change to 44 ohms at 0.04 second, for analyzing the load disturbance performance. Figure 19 illustrates the output voltage for topology-I under both line and load disturbances, the output voltage stabilized in 0.005 second for both distortion conditions by the closed-loop controller. Figure 20 illustrates the output current for topology-I under line and load disturbances, as load resistance decreases from 48 ohms

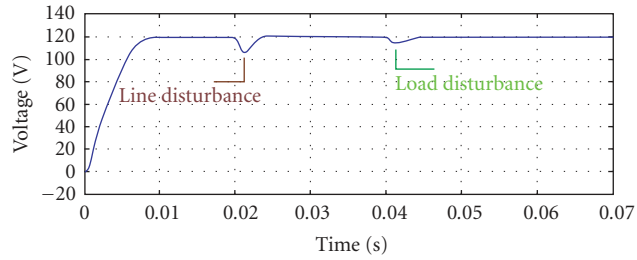

Figure 19: Output voltage of the topology-II for line and load disturbances.

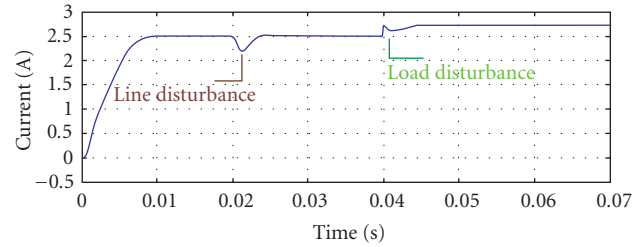

Figure 20: Output current of topology-II under line and load disturbances.

to 44 ohms at 0.05 second the load current increases from 2.5 amperes to 2.7272 amperes.

5. Effectiveness of the Proposed Converter

The effectiveness of the proposed converter topologies is shown in Table 2 by comparing the simulation results with classical boost converter. It is seen from Table 2 that the output voltage varies from 33.33 volts to 300 volts for topology-I and 44.44 volts to 400 volts for topology-II, respectively, for a duty ratio of 0.1 to 0.9. However, the classical converter produces only a maximum of 90 volts. This shows that the proposed converter provides higher output voltage.

6. Conclusions

A new series of DC-DC boost converter topologies are proposed. The topologies use voltage lift technique to obtain higher output voltage than the classical boost converter for the same duty ratio. The technique also overcomes the effect of parasitic elements and minimizes the ripple in the output voltage. A simplified controller with one sensor is designed to maintain the output voltage at the required level for the load and line disturbances. Simulation results validate the theoretical analysis. The proposed converter topologies find application in computer peripheral circuits, medical equipments, and industrial applications which require higher DC voltages.

References

[1] K. Prabakaran, P. Pavani, I. Ramadevi, J. Kumaravel, and P. Sanjeevikumar, "DC-DC boost converter topologies for high voltage applications," in *Proceedings of the National Conference on Trends in Instruments and System Design Automation*, Karunya University, Coimbatore, India, 2007.

[2] F. L. Luo and H. Ye, "Positive output super-lift converters," *IEEE Transactions on Power Electronics*, vol. 18, no. 1, pp. 105–113, 2003.

[3] Y. He and F. L. Luo, "Analysis of Luo converters with voltage-lift circuit," *IEE Proceedings: Electric Power Applications*, vol. 152, no. 5, pp. 1239–1252, 2005.

[4] Y. He and F. L. Luo, "Study of slide mode controller for DC-DC converter," in *Proceedings of the International Conference on Power System Technology (POWERCON '04)*, Singapore, November 2004.

[5] F. L. Luo and H. Ye, "Ultra-lift Luo-converter," in *Proceedings of the International Conference on Power System Technology (POWERCON '04)*, vol. 1, pp. 81–86, Singapore, November 2004.

[6] X. Chen, F. L. Luo, and H. Ye, "Modified positive output Luo converters," in *Proceedings of the 3rd IEEE International Conference on Power Electronics and Drive Systems (PEDS '99)*, vol. 1, pp. 450–455, Kowloon, Hong Kong, July 1999.

[7] F. L. Luo, "Luo-converters, a series of new DC-DC step-up (Boost) conversion circuits," in *Proceedings of the 2nd IEEE International Conference on Power Electronics and Drive Systems (PEDS '97)*, vol. 2, pp. 882–888, Singapore, May 1997.

[8] F. L. Luo and X. F. Chen, "Self-lift DC-DC converters," in *Proceedings of the 2nd IEEE International Conference on Power Electronics Drives and Energy Systems for Industrial Growth (PEDES '98)*, vol. 1, pp. 441–446, Perth, Australia, November-December 1998.

[9] F. L. Luo, "Luo-converters, voltage lift technique," in *Proceedings of the 29th IEEE Annual Power Electronics Specialists Conference (PESC '98)*, vol. 2, pp. 1783–1789, Fukuoka, Japan, May 1998.

[10] F. L. Luo, "Re-lift converter: design, test, simulation and stability analysis," *IEE Proceedings: Electric Power Applications*, vol. 145, no. 4, pp. 315–325, 1998.

[11] F. L. Luo, "Re-lift circuit: a new DC-DC step-up (Boost) converter," *Electronics Letters*, vol. 33, no. 1, pp. 5–7, 1997.

[12] K. Ogata, *Modern Control Engineering*, Prentice-Hall, New Delhi, India, 2nd edition, 1996.

[13] K. M. Smedley and S. Cuk, "Dynamics of one-cycle controlled Cuk converters," *IEEE Transactions on Power Electronics*, vol. 10, no. 6, pp. 634–639, 1995.

[14] M. H. Rashid, *Power Electronics: Circuits, Devices and Applications*, Prentice-Hall, Englewood Cliffs, NJ, USA, 2nd edition, 1993.