Extraction and Modeling of Self-Heating and Mutual Thermal Coupling Impedance of Bipolar Transistors

Nebojša Nenadović, *Student Member, IEEE*, Slobodan Mijalković, *Senior Member, IEEE*, Lis K. Nanver, *Member, IEEE*, Lode K. J. Vandamme, Vincenzo d'Alessandro, Hugo Schellevis, and Jan W. Slotboom, *Member, IEEE*

***Abstract*—A measurement system comprised of an ultra-low-distortion function generator, lock-in amplifier, and semiconductor parameter analyzer is used for sensitive extraction of the small-signal thermal impedance network of bipolar devices and circuits. The extraction procedure is demonstrated through measurements on several silicon-on-glass NPN test structures. Behavioral modeling of the mutual thermal coupling obtained by fitting a multipole rational complex function to measured data is presented.**

***Index Terms*—Bipolar transistor, electrothermal modeling, self-heating, silicon-on-glass, thermal coupling, thermal impedance.**

I. Introduction

ELECTROTHERMAL effects play a major role in the performance of modern semiconductor devices and integrated circuits. Thermal issues are especially important for radio frequency (RF) bipolar technologies for several reasons. First, RF bipolar transistors operate at very large current densities in order to push the high-frequency performance to the limits [1]. Second, there is a positive feedback between the collector current and temperature of a bipolar transistor that can induce thermal instabilities [2]–[7]. Third, reduction of the parasitic capacitances of the active devices and increase in the level of integration in RF systems is achieved by decreasing the parasitic coupling to the Si substrate. This is often done by introducing silicon-on-insulator (SOI) substrates and deep trench isolation. Unfortunately, such solutions entail a tremendous reduction in the heat spreading from the active device regions [8]–[12]. Furthermore, emerging technologies based on three-dimensional (3-D) integration [13] and substrate transfer [14], [15], despite being electrically very attractive, continue degrading the heat spreading, influence self-heating and mutual thermal coupling, and increase the circuit operating temperature. It is, therefore, very important to accurately describe electrothermal feedback within a single device, and equally important to understand and describe electrothermal coupling within a circuit composed of such devices.

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N. Nenadović, L. K. Nanver, H. Schellevis, and J. W. Slotboom are with the Laboratory of ECTM, DIMES, Delft University of Technology, 2600 GB Delft, The Netherlands (e-mail: n.nenadovic@dimes.tudelft.nl).

S. Mijalković is with the Laboratory of HiTeC, DIMES, Delft University of Technology, 2600 GB Delft, The Netherlands.

L. K. J. Vandamme is with the Department of Electrical Engineering, Eindhoven University of Technology, 5600 MB Eindhoven, The Netherlands.

V. d'Alessandro is with the Department of Electronics and Telecommunications Engineering, University of Naples "Federico II", 80125 Naples, Italy.

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Various dc measurement techniques for extraction of the self-heating thermal resistance R_{TH} are proposed in the literature [7], [16]–[19]. When steady-state thermal models are utilized for characterization of RF devices and circuits, the temperature instantaneously follows the power dissipation signal, and dynamic thermal behavior is disregarded. To describe dynamic behavior, thermal impedance rather than thermal resistance must be characterized. In general, transient [20]–[24] and ac measurement techniques [25]–[27] are used for extraction of the self-heating thermal impedance, Z_{TH}. It has been shown that thermal response is always limited to low frequencies with a thermal cutoff frequency f_{TH} in the range from a few kilohertz to about 1 MHz. Therefore, single-tone RF signals are unaffected by dynamic electrothermal effects. However, in the case of narrow-band signals, like EDGE GSM where channel separation can be as small as 25 kHz, modulated signals can completely fall into the region below f_{TH} [28]. Even for wider channels, signals below the thermal cutoff frequency appear in the spectrum [29], [30], and it has been demonstrated that the value of the third-order intermodulation coefficient IMD3 is dependent on the tone spacing. Therefore, the standard IM3 characterization technique based on wide tone spacing may not fully represent the linearity performance of PAs [29]. Thermal impedance data is thus needed for complete electrothermal characterization of RF amplifiers. For example, the thermal memory effect caused by the dynamic thermal behavior seriously limits the maximum achievable cancellation performance of the predistortion linearization method [28], [31]. Moreover, when designing circuits, it is very important to perform an overall electrothermal analysis, in which not only self-heating but also mutual thermal coupling impedance is taken into account. A few techniques for extraction of the thermal coupling resistance [32] and impedance [21] have been reported.

In this paper, a novel ac measurement technique is presented, with which an accurate extraction of both the small-signal self-heating and mutual thermal coupling impedance is made possible. To achieve a very high sensitivity measurement, an ultra-low distortion function generator and parameter analyzer are used for accurate biasing of the devices under test, while a lock-in amplifier and base-emitter thermometer are combined to measure small-signal temperature variation at a given reference frequency. A wide range of bipolar technologies can be electrothermally characterized by this method. Here, the accuracy of the system is demonstrated by measurements of different silicon-on-glass test structures [15].

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The measured frequency-sampled thermal impedance data is obtained in a wide frequency range. To model this for circuit design purposes, a general behavioral modeling approach based on a rational transfer function is adopted in this paper. As indicated above, such thermal models are needed for accurate characterization of RF devices and circuits. Moreover, they are necessary for analysis of devices used in power switching applications, differential amplifier stages, and current mirrors [33]. Also, they are useful for studying the device thermal structure including thin-film interfaces, die attachments, and heat sinks [34], and for sensor applications [35], [36].

II. Small-Signal Thermal Impedance Network

In this section, the small-signal thermal impedance network, which will be extracted in Sections III–V, is introduced and the individual components are defined. In a multiport system shown in Fig. 1, each port represents either a single transistor as a part of a complex circuit or a cell in a multicellular device. In both cases, the number of ports can be very large. For the sake of simplicity, however, a two-port system is considered in the following.

The small-signal two-port thermal impedance network in the complex domain is defined as

$$\begin{aligned} \underline{t}_1 &= \underline{t}_{11} + \underline{t}_{12} = \underline{z}_{TH11}\underline{p}_1 + \underline{z}_{TH12}\underline{p}_2 \\ \underline{t}_2 &= \underline{t}_{21} + \underline{t}_{22} = \underline{z}_{TH21}\underline{p}_1 + \underline{z}_{TH22}\underline{p}_2 \end{aligned} \quad (1)$$

where $\underline{z}_{TH11}$ and $\underline{z}_{TH22}$ are the self-heating thermal impedances, $\underline{z}_{TH12}$ and $\underline{z}_{TH21}$ the mutual thermal coupling impedances, $\underline{p}_1$ and $\underline{p}_2$ the power dissipations, and $\underline{t}_1$ and $\underline{t}_2$ the temperature variations at ports 1 and 2, respectively. It is assumed that the temperatures $\underline{t}_1$ and $\underline{t}_2$ are small in magnitude, and thus a linear relationship between the power and temperature is adopted in (1). Moreover, in a linear approximation, the superposition principle holds and therefore the temperature $\underline{t}_1$ ($\underline{t}_2$) consists of the self-heating term $\underline{t}_{11}$ ($\underline{t}_{22}$) and mutual thermal coupling term $\underline{t}_{12}$ ($\underline{t}_{21}$). However, since the systems of devices under consideration are composed of silicon and/or other semiconductor and dielectric materials, which have temperature-dependent thermal conductivities [37], the thermal impedance coefficients are not constant with temperature [38]. Thus, the linearity principles used in (1) do not hold in general, but even in the case of large-signal excitations, for which large temperature changes can be generated within the system, it is often still useful to adopt the small-signal compact models of the thermal impedance network, and this is done in almost all practical cases. A few attempts to include nonlinearity in the analytical thermal resistance/impedance models have been reported in the literature [38], [39], but such models are very complex and even for bulk technologies they have much less practical value than linear models. An alternative approach in nonlinear thermal impedance modeling is the database (or look-up table) modeling method based on measured small-signal thermal impedance data. Such a thermal database model coupled with an electrical model (compact or database [40]) can then be used for accurate large-signal electrothermal analysis of devices and circuits. With the lock-in measurement technique presented here, the small-signal thermal impedance data at constant temperature can be extracted versus frequency and used to create thermal impedance models.

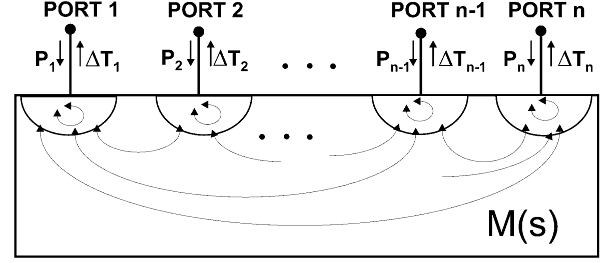

Fig. 1. Schematic of coupled thermal interaction in a multiport system.

III. Measurement System and Extraction Procedure

The measurement system is shown in Fig. 2. In the present experiments, two identical neighboring devices, D1 and D2, are probed on-wafer using a Cascade probing station equipped with a thermal chuck. The setups in Fig. 2(a) and (b) are used for $\underline{z}_{TH11}$ and $\underline{z}_{TH21}$ extraction, respectively. By exchanging D1 with D2 in the same setups, the other two thermal impedance coefficients, $\underline{z}_{TH22}$ and $\underline{z}_{TH12}$, can be extracted.

A. Biasing Setup

In Fig. 2(a) and (b), the device D1 is biased in a common-base configuration. The constant emitter current I_{E1} is forced through the transistor by an HP 4156B Parameter Analyzer. A SR-DS360 ultra-low-distortion function generator is used to bias the collector of this device: an offset dc voltage $V_{CB1} > 0$ is applied along with the ac signal v_{cb1} at frequency f_K.

The transistor is biased in forward active mode where the current gain β is much larger than 1, and thus $I_{C1} \simeq I_{E1}$. The transistor dissipates a dc power $P_1 = V_{CE1}I_{E1}$, and an ac power at frequency f_K expressed in the complex domain as

$$\begin{aligned} \underline{p}_1 &= I_{C1}\underline{v}_{ce1} + \underline{i}_{c1}V_{CE1} \\ &\simeq I_{E1}\underline{v}_{ce1} + \underline{v}_{cb1}I_{E1}\frac{V_{CE1}}{V_A\beta} \simeq I_{E1}\underline{v}_{ce1} \end{aligned} \quad (2)$$

where V_A is the Early voltage. The term $\underline{i}_{c1}V_{CE1}$ can be readily calculated from the low-frequency small-signal hybrid-pi equivalent circuit of a bipolar transistor biased in a common-base configuration with a forced dc emitter current. Since $V_{CE1}/V_A\beta \ll 1$, $\underline{i}_{c1}V_{CE1}$ can be neglected with respect to $I_{C1}\underline{v}_{ce1}$.

Due to the generated power dissipation, the temperature of the chip changes with respect to ambient. In a linear approximation, only those frequencies that are present in the power excitation are induced in the temperature spectrum. This means that P_1 induces dc temperature components $\Delta T_{1,DC}$ and $\Delta T_{2,DC}$ in devices D1 and D2, respectively, while $\underline{p}_1$ induces ac temperatures at frequency f_K, and $\underline{t}_1$ and $\underline{t}_2$ at devices D1 and D2, respectively. Thus, the temperatures of devices D1 and D2, expressed in time domain, are

$$\begin{aligned} T_1(\tau) &= T_0 + \Delta T_{1,DC} + t_1(\tau) \\ T_2(\tau) &= T_0 + \Delta T_{2,DC} + t_2(\tau) \end{aligned} \quad (3)$$

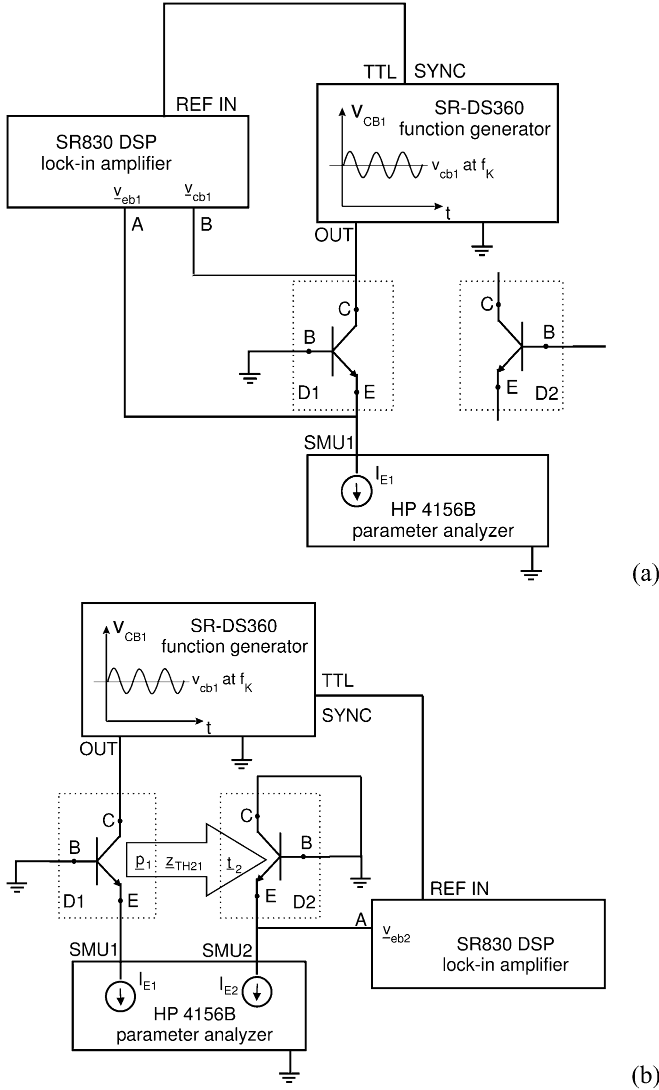

Fig. 2. Schematic of the measurement setup: configuration for (a) $\underline{z}_{TH11}$ measurement and (b) $\underline{z}_{TH21}$ measurement.

where T_0 is the thermal chuck temperature, $t_1(\tau)$ and $t_2(\tau)$ the small-signal temperatures in time domain at D1 and D2, respectively, and τ the time.

For the purpose of detecting the temperature $\underline{t}_2$, the device D2 is biased as shown in Fig. 2(b): a constant current I_{E2} is forced through the emitter, while the collector is shorted to the base.

B. Base-Emitter Voltage Thermometer

The temperature variations of a transistor can be measured by monitoring the base-emitter voltage. In the forward active regime with the collector (or emitter) current kept constant, the base-emitter voltage decreases as the device temperature increases. From the V_{BE}–T characteristics at the collector currents of interest, the base-emitter voltage temperature coefficient

$$\varphi = \left.\frac{\partial V_{BE}}{\partial T}\right|_{I_C} \tag{4}$$

can be extracted. It is demonstrated in [7] that the coefficient φ is temperature independent and therefore the measured changes in the base-emitter voltage divided by φ will give the temperature change with respect to ambient.

Under forward active operation for a fixed I_{E1} and a small-signal excitation $\underline{v}_{cb1}$, as in the setups from Fig. 2(a) and (b), two concurrent mechanisms influence $\underline{v}_{eb1}$: one is the Early effect (*electrical feedback*) and the other is the self-heating effect (*thermal feedback*) [41]. At the low frequencies of interest, only thermal feedback influences $\underline{v}_{eb2}$ for a fixed I_{E2} since D1 and D2 are electrically isolated. The compensation for the Early effect will be treated in Section III-C.

C. Extraction of the Thermal Impedance Network Coefficients

In Fig. 2(a), an SR830 DSP lock-in amplifier is connected to device D1 so that $\underline{v}_{eb1}$ is measured through channel A and $\underline{v}_{ec1}$ through A–B. This instrument isolates the magnitude and phase of the input signals at a given reference frequency even when the signals are obscured by noise sources that are orders of magnitude larger. The TTL signal at frequency f_K is taken from the function generator and used as the reference input for the SR830 DSP. Thus, the lock-in amplifier detects the signals $\underline{v}_{eb1}$ and $\underline{v}_{ec1}$ that have the same frequency as the excitation $\underline{v}_{cb1}$. Since $\underline{v}_{eb1}$ and $\underline{v}_{ec1}$ can be translated into $\underline{t}_1$ and $\underline{p}_1$, respectively, this combination of ultra-low-distortion function generator and lock-in amplifier gives a sensitive means of determining the small-signal self-heating thermal impedance.

The thermal component of the V_{BE}-V_{CB} electrothermal feedback is extracted after compensating the measured $\underline{v}_{eb1}$ for the Early effect, as follows:

$$\underline{v}_{eb1,\text{thermal}} = \underline{v}_{eb1} - \underline{v}_{eb1,\text{electrical}} = \underline{v}_{eb1} - \underline{v}_{cb1}\frac{V_T}{V_A} \tag{5}$$

where $V_T \approx 26$ mV is the thermal voltage. The Early voltage V_A can be extracted from the isothermal (measured in pulsed mode) device characteristics. The calculated $\underline{v}_{eb1,\text{thermal}}$ is converted into the temperature $\underline{t}_1$ as follows:

$$\underline{t}_1 = -\frac{\underline{v}_{eb1,\text{thermal}}}{\varphi_1} \tag{6}$$

where φ_1 is given by (4) with $I_C = I_{C1} = I_{E1}$. Using (2), the measured $\underline{v}_{ec1} = -\underline{v}_{ce1}$ is converted into $\underline{p}_1$ and thus, the self-heating thermal impedance in complex domain is determined as

$$\underline{z}_{TH11} = \frac{\underline{t}_1}{\underline{p}_1} = -\frac{\underline{v}_{eb1,\text{thermal}}}{\varphi_1 I_{E1}\underline{v}_{ce1}} = \frac{\underline{v}_{eb1,\text{thermal}}}{\varphi_1 I_{E1}\underline{v}_{ec1}}. \tag{7}$$

To determine $\underline{t}_2$, the device D2 is biased and the lock-in amplifier is reconnected as shown in Fig. 2(b). As is explained in Section II, only thermal feedback influences $\underline{v}_{eb2}$, and thus $\underline{v}_{eb2} = \underline{v}_{eb2,\text{thermal}}$. The measured $\underline{v}_{eb2,\text{thermal}}$ is then converted into the temperature $\underline{t}_2$:

$$\underline{t}_2 = -\frac{\underline{v}_{eb2,\text{thermal}}}{\varphi_2} \tag{8}$$

TABLE I
LIST OF TEST STRUCTURES AND CORRESPONDING THERMAL IMPEDANCES EXTRACTED AT $f_K = 1$ Hz

Test structure	isolation type	Distance d [μm]	Abs($\underline{z}_{TH11}$) [K/W]	Abs($\underline{z}_{TH21}$) [K/W]
J-6	junction	6	15235	8912
J-36	junction	36	15085	4200
J-56	junction	56	14713	2607
T-6	trench	6	15506	7260
T-36	trench	36	16761	2654
T-56	trench	56	16870	1470

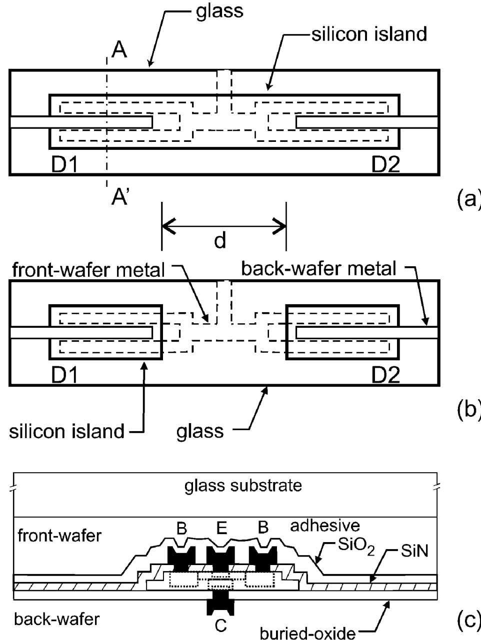

Fig. 3. Schematics of the test structures fabricated in silicon-on-glass bipolar technology: back-wafer views where D1 and D2 are separated by (a) junction isolation and (b) trench isolation. (c) The cross section along A-A′ axis in (a).

where φ_2 is given by (4) with $I_C = I_{C2} = I_{E2}$. The complex mutual thermal coupling impedance is then found to be

$$\underline{z}_{TH21} = \frac{\underline{t}_2}{\underline{p}_1} = -\frac{\underline{v}_{eb2,\mathrm{thermal}}}{\varphi_2 I_{E1} \underline{v}_{ce1}} = \frac{\underline{v}_{eb2,\mathrm{thermal}}}{\varphi_2 I_{E1} \underline{v}_{ec1}}. \tag{9}$$

IV. MEASUREMENT EXAMPLES

A. Silicon-on-Glass NPN Test Structures

The silicon-on-glass NPN test structures were designed and fabricated as shown in Fig. 3. They are comprised of a pair of identical silicon-on-glass bipolar NPNs each with an emitter area $A_E = 20 \times 1$ μm^2 [15]. During silicon-on-glass device and circuit fabrication, the silicon substrate is replaced by a glass wafer. Pure electrically, this results in the elimination of the substrate losses and a reduction of the active device parasitic capacitances and resistances. However, the thermal impedance of a silicon-on-glass transistor is much higher than that of the corresponding bulk-silicon device, mainly due to very low thermal conductivity of glass (more than 100 times lower than that of silicon).

The transistor pairs forming the test structures are placed in a trenched silicon island, while the region between them is either junction or trench isolated, as shown in Fig. 3(a) and (b), respectively. The distance d between D1 and D2 is either 6, 36, or 56 μm. The details of the test structures are listed in Table I. In the junction isolated test structures (J-6, J-36, and J-56), D1 and D2 are thermally connected by a silicon region, which has a good thermal conductivity. On the other hand, the trench between the trench isolated devices (T-6, T-36, and T-56) is filled with poor thermal conductors: silicon nitride and silicon oxide. For these devices, d is the trench width between D1 and D2. The trenches are etched all the way to the buried oxide to give a perfect electrical isolation of each silicon island that have a size of $0.64 \times 10 \times 23$ μm^3.

B. V_{BE} Thermometer Calibration

All the transistors in the test structures are electrically identical. A transistor with the lowest thermal resistance was therefore chosen to calibrate the V_{BE} thermometer. Gummel plots were measured at different substrate temperatures ranging from 300 K to 380 K, which amply cover the temperature range of interest. The measurements were performed in isothermal (pulsed) mode and for $V_{CB} = 0$ V. Fig. 4 shows the base-emitter voltage as a function of temperature for different fixed current densities. The base-emitter voltage temperature coefficient φ is given by the differential of each curve, the absolute value of which increases as the current density decreases.

C. Device Biasing

After the calibration was performed, the test structures were connected according to the measurement setup as shown in Fig. 2. The following voltages and currents were applied at the devices' terminals: $V_{CB1} = 0.5$ V, $\underline{v}_{cb1} = 0.1$ V, $I_{E1} = 1$ mA, and $I_{E2} = 1$ μA. The emitter current of D2 is set to be very low, for the first, to minimize the self-heating and second, to maximize the sensitivity for $\underline{t}_2$ detection. Using the calibration curves from Fig. 4, φ_1 and φ_2 were found to be -1.5 mV/K and -2.1 mV/K, respectively. f_K was varied from 1 Hz up to 100 kHz, which is almost the full frequency range of the available equipment.

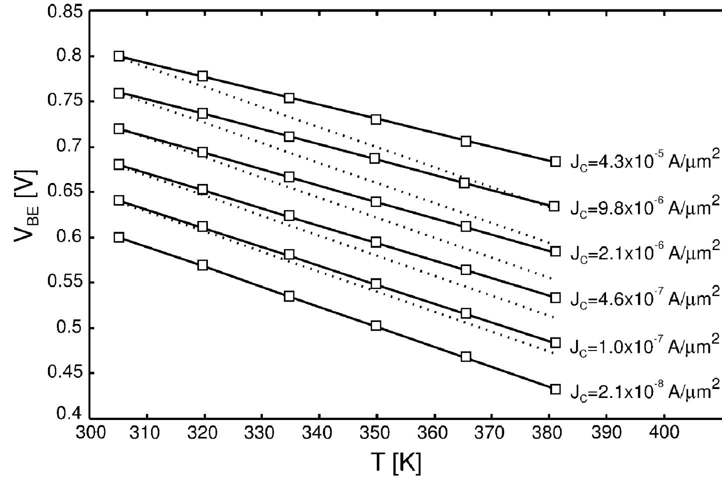

Fig. 4. Base-emitter voltage as a function of temperature for various values of collector-current density. The base-emitter voltage temperature coefficient φ is extracted as the slope of measurement results (squares). For comparison, curves having the same slope as the one with the lowest current density are also included (dotted lines).

D. Measurement Results and Discussion

The thermal resistance of the present transistors is known to be at most about 1.5×10^4 K/W [15], so the small-signal power $|\underline{p}_1| \approx 0.1$ mW, calculated by (2), does not introduce a temperature swing $|\underline{t}_1|$ larger than $\sim$1.5 K over the measured frequency range. This is so low that a temperature-induced nonlinearity in the heat propagation can be neglected.

The magnitude of $\underline{t}_2$ can be much smaller than that of $\underline{t}_1$. For instance, for a given power $|\underline{p}_1| = 0.1$ mW and at high f_K, the magnitude of $\underline{t}_2$ can be as low as a few milliKelvins. Even though the sensitivity of the base-emitter thermometer is maximized ($\varphi_2 = -2.1$ mV/K) by setting I_{E2} to only 1 μA, $\underline{v}_{be2}$ is still very low, in the microvolt range for the frequencies where $|\underline{t}_2|$ is in order of 1 mK. Therefore, an extremely sensitive measurement technique, as is achieved here with the lock-in amplifier, is imperative for this type of measurement.

The thermal impedances $\underline{z}_{TH11}$ and $\underline{z}_{TH21}$ of the test structure T-6 are extracted and the magnitudes are shown in log-log scale in Fig. 5. No variations in the extracted thermal impedance values were detected for $|\underline{p}_1|$ ranging from 0.05 mW to 0.3 mW. The frequency range provided by the available instruments is seen to be adequate to fully cover the spectrum of $\underline{z}_{TH21}$. Nevertheless, as displayed in Fig. 5, only low-frequency values of $\underline{z}_{TH11}$ can be measured. To fully cover the spectrum of $\underline{z}_{TH11}$ for this particular device, as well as for a wide range of devices made in other technologies including bulk-silicon [21], the upper frequency limit has to be raised. This can be done by using a lock-in amplifier that can measure the signals up to 10 MHz. Alternatively, the presented measurement technique could be combined with other, faster ac techniques, such as the one given in [27]. Fig. 6 shows the extracted magnitude and real and imaginary part of $\underline{z}_{TH21}$ for the trench isolated test structures. The thermal chuck temperature was set to $T_0 = 22$ °C. Thermal coupling between transistors D1 and D2 is seen to be strongly influenced by the distance between them. Compared to T-6, the coupling in T-36 and T-56 is reduced by 65% and 80%, respectively. For the junction isolated structures, which have a stronger thermal coupling, the reduction with distance is lower: compared to J-6, the thermal coupling in J-36 and J-56 is reduced by 55% and 70%, respectively. Fig. 7 compares the magnitudes of $\underline{z}_{TH21}$ for the test structures of both types. The extraction results show that the electrically isolated devices from T-6 are only 20% less thermally coupled than the corresponding J-6 devices. The difference grows higher if the trench width d increases: it becomes 36% for $d = 36$ μm and 43% for $d = 56$ μm. This means that good thermal isolation of the trenched devices can only be achieved with trenches of the order of 100 μm or wider, even though the pure electrical isolation is perfect for all distances. Table I summarizes the magnitudes of extracted $\underline{z}_{TH11}$ and $\underline{z}_{TH21}$ at 1 Hz for the devices analyzed. The increase in $|\underline{z}_{TH11}|$ as a result of introducing trench isolation is much smaller than what has been observed in bulk-silicon processes [8]. This is because the glass substrate is placing the greatest restriction on the heat transfer.

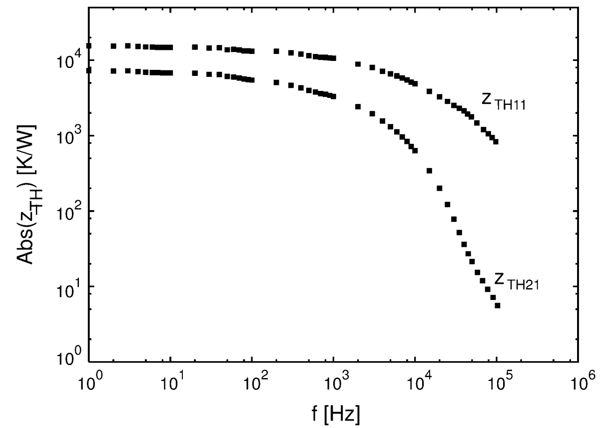

Fig. 5. Extracted magnitude of $\underline{z}_{TH11}$ and $\underline{z}_{TH21}$ for the test structure T-6.

Fig. 8 shows the magnitude of $\underline{z}_{TH21}$ that is extracted for the test structure J-36 at three different thermal chuck temperatures T_0: 22 °C, 70 °C, and 110 °C. Since the thermal conductivity of silicon decreases as the temperature increases, and the thermal conductivity of glass and other dielectric materials surrounding the test structure increases as the temperature increases [37], it is plausible that the extracted mutual thermal coupling impedance of J-36 is lower at higher temperatures. Nevertheless, the change in $\underline{z}_{TH21}$ is not dramatic and the

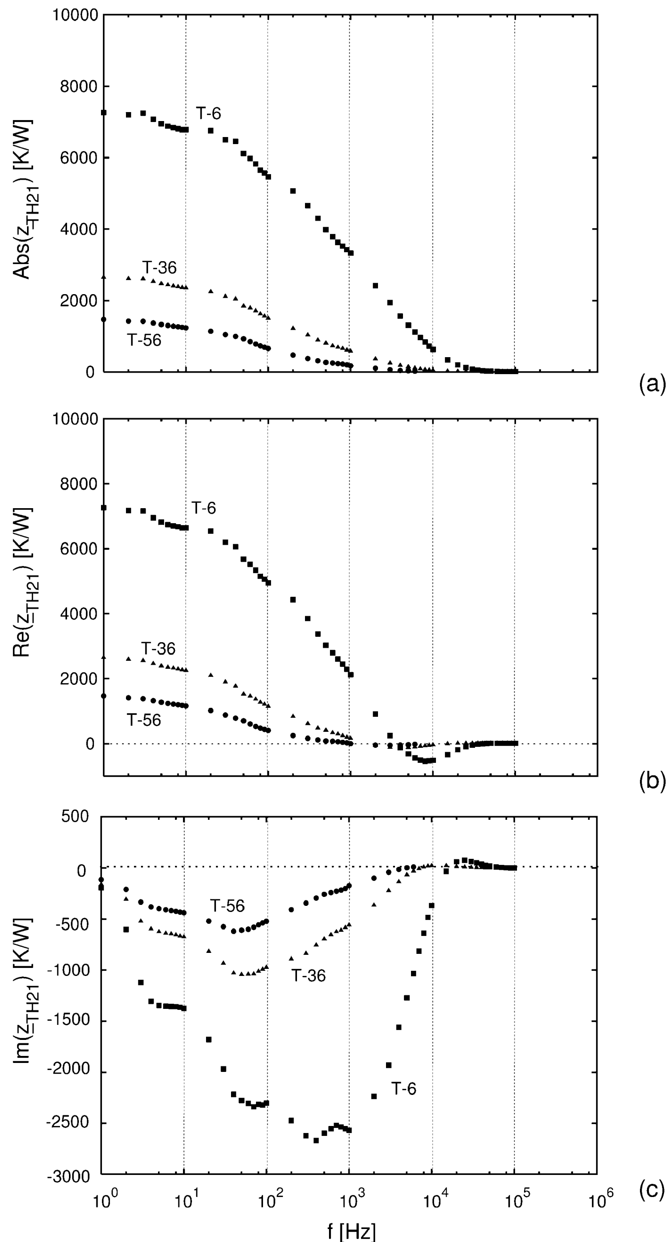

Fig. 6. Extracted (a) magnitude, (b) real and (c) imaginary part of $\underline{z}_{TH21}$ for the test structures T-6, T-36, and T-56.

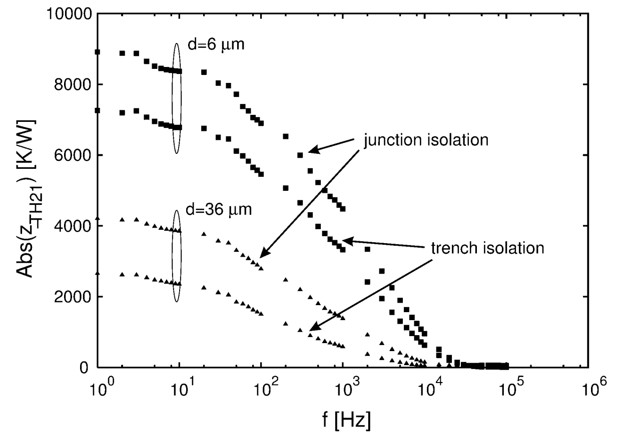

Fig. 7. Comparison between magnitudes of the mutual thermal coupling impedance $\underline{z}_{TH21}$ for the trench and junction isolated test structures.

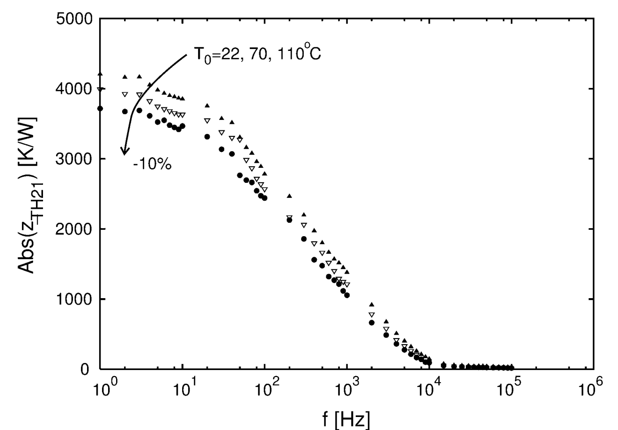

Fig. 8. Temperature dependence of the extracted magnitude of $\underline{z}_{TH21}$ for the test structure J-36.

room temperature thermal impedance value can be utilized to a very good approximation over a wide temperature range. Likewise, a weak temperature dependence is measured for the self-heating thermal impedance $\underline{z}_{TH11}$. The thermal impedances have also been measured at different bias points and only minor changes are detected. Under normal operating regimes, the small changes of the thermal impedance can be attributed to modification in the operating temperature and not to the size modulation of the heat source [42], [43]. This means that experimental small-signal thermal impedance data can be used with sufficient accuracy also for the large-signal modeling of the silicon-on-glass transistors. For other technologies and operating conditions this may not always be the case. In the most general situation, small-signal thermal impedance data should be measured versus bias, temperature and frequency, and used to create a look-up table thermal impedance model suitable for large-signal analysis. Nevertheless, for many purposes it is often enough to adopt a linear approximation and thus measure the thermal impedance versus frequency at a single bias point and temperature.

V. Modeling the Small-Signal Thermal Impedance Network

All the presented experimental results illustrate the capability of the proposed measurement system to accurately measure small-signal thermal impedances and detect changes in the self-heating and mutual thermal coupling caused by even very small changes in the device surrounding. In order to predict electrothermal circuit behavior, an accurate thermal model and the associated procedures for parameter extraction should be formulated. This section presents an approach to generating linear time-invariant (LTI) thermal models from the measured complex thermal impedance data in a wide-band frequency range.

The continuous LTI model has several equivalent representations that can be converted to each other through a straightforward procedure. The most important LTI model formulations are: time domain state-space equations, frequency domain rational transfer functions, or passive electrical analog circuits. The last formulation is particularly appealing from the implementation point of view due to its compatibility with standard

circuit simulation techniques. However, it should be emphasized that modern circuit simulators also accept frequency domain transfer functions as a model formulation either directly or via analog (and mixed-signal) hardware description languages like Verilog-AMS [44] or VHDL-AMS [45].

In simple cases of self-heating modeling, it is often possible to directly identify the lumped thermal resistors and capacitors in the equivalent thermal network from time [9] or frequency response data [27]. However, for the multiport thermal problems, with mutual thermal coupling, it is not evident how to *a priori* construct a lumped network topology with an optimal number of lumped elements. Moreover, in the circuits of higher complexity the extraction procedure can be seriously complicated by the high correlation between large numbers of resistance and capacitance parameters. An effective alternative modeling methodology is to identify the thermal multiport LTI model in the rational transfer function representation. In the case of a p-port network, the rational transfer function of order n is

$$\underline{H}(s,P) = \frac{\sum_{k=1}^{n} \mathbf{b}_k\, s^{n-k}}{s^n + \sum_{k=1}^{n} a_k s^{n-k}} \tag{10}$$

where $P = (a_1, a_2, \ldots, a_n, \mathbf{b}_1, \mathbf{b}_2, \ldots, \mathbf{b}_n)$ with $a_i \in \mathbb{R}$ and $\mathbf{b}_i \in \mathbb{R}^{p \times p}$, and s represents the complex frequency. The order n of the rational transfer function from (10) also defines the number of poles in the network description. The total number of model parameters that should be extracted is $n(p^2+1)$. Without any loss of generality in the sequel, only the modeling of a nondiagonal thermal impedance matrix element, $\underline{z}_{TH21}$, will be considered as an example.

A variety of methods have been proposed for the parametric identification of transfer functions in the real frequency domain. A survey of such methods is given in [46]. Here, we have employed a robust method based on the nonlinear least square method minimizing the quadratic cost function

$$K_{NLS} = \sum_{k=0}^{m} \left| \underline{\mathbf{z}}_{TH}(\omega_k) - \underline{H}(j\omega_k, P) \right|^2 \tag{11}$$

where m is the number of sampled real frequencies $\omega_k = 2\pi f_k$. In order to minimize the condition number of the Jacobian matrices underlying the governing Gauss–Newton optimization algorithm, the frequency range is appropriately scaled. Before the rational function model with extracted parameters is used in circuit simulations, it is important to check its passivity by inspecting the eigenvalues of the full impedance matrix. In principle, the parameter extraction procedure can be enhanced to become a constrained optimization procedure that automatically enforces the thermal network passivity [47].

Fig. 9(a) and (b) gives a comparison of extracted and modeled real and imaginary parts of the mutual thermal coupling impedance $\underline{z}_{TH21}$ as a function of frequency for the test structure J-36. Similar results are achieved for all the other test structures. A high degree of complexity of the transfer function (rational function of order $n = 9$) is needed to achieve sufficiently accurate fitting across the whole measured frequency range from 1 Hz to 100 kHz.

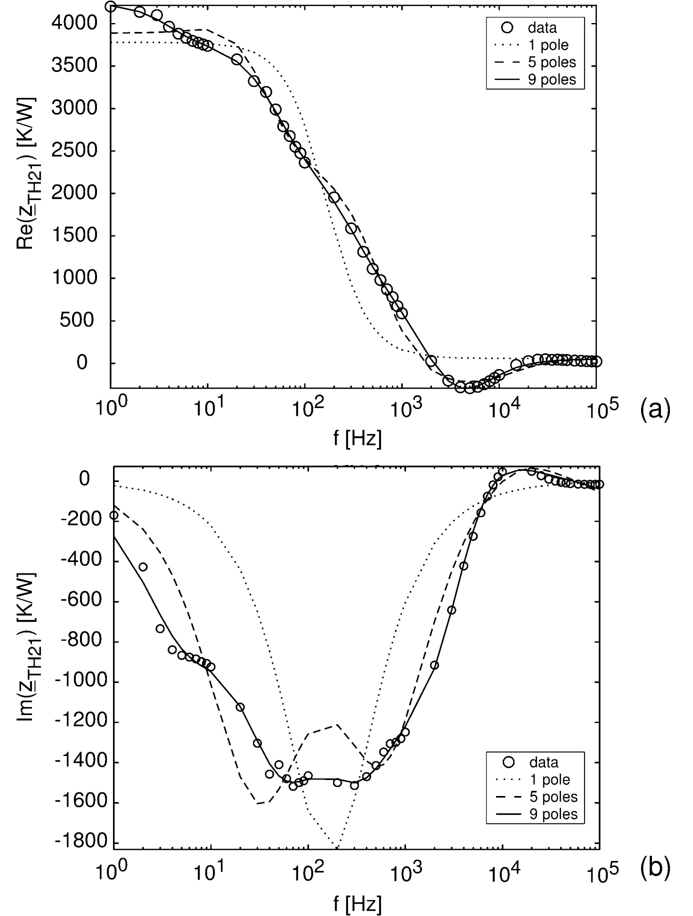

Fig. 9. Extracted and modeled (a) real part and (b) imaginary part of $\underline{z}_{TH21}$ for the test structure J-36.

VI. Conclusion

With the presented measurement technique, both the diagonal and nondiagonal elements of the small-signal thermal impedance matrix, which originate from the self-heating and mutual thermal coupling, respectively, can be extracted. To achieve a very high sensitivity measurement, an ultra-low distortion function generator, parameter analyzer, and lock-in amplifier are combined to bias the devices under test and measure small-signal temperature variation at a given reference frequency. The accuracy of the measurement system and the extraction procedure are demonstrated by measurements on silicon-on-glass NPN test structures, where small differences in the device surroundings are clearly detected as correspondingly small changes in the thermal impedances. The results show that this technique can be a powerful tool for the electrothermal optimization of device and circuit process technology.

Moreover, the presented measurement method can supply data for establishing accurate thermal impedance models. Here, a linear modeling approach is adopted based on fitting a multipole rational complex function to the measured data. The generated behavioral models can be directly used by circuit simulators and thus enable electrothermal analysis of semiconductor devices and circuits. Alternatively, for very accurate nonlinear thermal modeling, look-up table models have been proposed, which can be created from the small-signal experimental data measured by the presented lock-in technique.

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Nebojša Nenadović (S'02) was born in Belgrade, Serbia and Montenegro, in 1976. In September 2000, he received the M.Sc. degree (*cum laude*) in electrical engineering from the University of Belgrade, Serbia and Montenegro, after which he joined the Laboratory of Electronic Components, Technology and Materials of DIMES, Delft University of Technology, The Netherlands, where he is currently pursuing the Ph.D. degree.

During the summers of 1998 and 1999, he was involved in the investigation of transitions in the quantum Hall regime at the Department of Condensed Matter Physics, Weizmann Institute of Science, Israel. His research experience also includes modeling and simulation of optoelectronic devices, in particular quantum-wire lasers, at the Department of Physical Electronics, Faculty of Electrical Engineering, University of Belgrade. His current research interests are design, fabrication, and characterization of BJTs and RF power MOSFETs in silicon and silicon-on-glass technology, and investigation of electrothermal interactions within semiconductor devices.

Mr. Nenadović received the Best Student Paper Awards for his contributions at the Topical RF Meeting in 2001 and the MIEL Conference in 2002.

Slobodan Mijalković (S'86–M'88–SM'01) received the M.Sc., M.Ph., and Ph.D. degrees in electronics engineering from the University of Niš, Yugoslavia, in 1982, 1989 and 1991, respectively.

From 1983 to 1998, he was with the Faculty of Electronics Engineering, University of Niš, as a Teaching Assistant, Assistant Professor, and Associate Professor in the Department of Microelectronics. He also served as a guest researcher at the German National Center for Information Technology (GMD) in 1995 and 1996. Since 1998, he has been a Senior Researcher at the Delft Institute of Microelectronics and Submicron Technology, Delft University of Technology, The Netherlands. His research interest is in the efficient simulation techniques for the semiconductor processes and devices, development of TCAD simulation tools, model reduction techniques, and compact transistor modeling.

Lis K. Nanver (S'80–M'83) received the M.Sc. degree in physics in 1979 from the University of Aarhus, Aarhus, Denmark, and the Dr.ing. degree in 1982 from the Ecole Nationale Superieure des Télécommunications, Paris, France, where she worked on the simulation of CCD structures. She received the Ph.D. degree in 1987 from the Delft University of Technology, Delft, The Netherlands, where she developed a medium-frequency BIFET process.

In 1988, she joined the DIMES IC Process Research Sector as Bipolar Process Research Manager. She became Associate Professor and later Professor with the Faculty of Electrical Engineering, Mathematics and Computer Science, Delft University of Technology, detached at DIMES Technology Center in 1994 and 2001, respectively. Within the Laboratory of Electrical Components, Technology and Materials, she manages the research on advanced Si-based devices that is mainly directed toward optimization and development of high-frequency Si BJT/SiGe HBT devices and the integration of passives. This research involves technologies such as AP/LPCVD epitaxy, dopant activation by excimer laser annealing, and substrate transfer techniques. She has served on the committees of ESSDERC and BCTM.

Lode K. J. Vandamme received the B.Sc. degree in electrical engineering from H.T.I. Oostende, Belgium, the M.Sc. degree (*cum laude*) from the Delft University of Technology, The Netherlands, and the Doctorate degree from the Eindhoven University of Technology, The Netherlands, in 1965, 1971, and 1976, respectively.

He has held full-time positions at the Nuclear Reactor Institute in Delft, the Department of Electrical Engineering and the Department of Mechanical Engineering, Delft University of Technology, and the Department of Electrical Engineering, Eindhoven University of Technology, since 1965 and 1972, respectively. He was invited Visiting Professor at the University of Montpellier in 1981–1982, 1986–1987, and 1992, at the University of Bordeaux, Talence, France, in 1998, and at the University of Uppsala, Sweden, in 1999. He has done research on $1/f$ noise in metals, semiconductors and insulators (optical fibers), electrical contacts, devices including MOSFETs, MESFETs, MODFETs, diodes, solar cells, and laser diodes. He has written and contributed to more than 160 scientific journal and conference publications.

Vincenzo d'Alessandro received the Laurea degree in electrical engineering and the Ph.D. degree from the University of Naples "Federico II", Naples, Italy, in 1999 and 2003, respectively.

From January 2002 to December 2002, he was a visiting scientist at the Laboratory of ECTM, Delft University of Technology, The Netherlands, working on simulation and modeling of electrothermal effects in silicon-on-anything RF transistors. In February 2003, he was charged by the University "Federico II" to teach a course on digital electronics. His current research area is electrothermal and thermal modeling/simulation of semiconductor devices, with focus on multicellular power VDMOSTs and GaAs/AlGaAs HBTs.

Hugo Schellevis received the Chemical Engineer degree from the Institute of Technology, Amsterdam, The Netherlands, and the M.Sc. degree in chemical engineering from the University of Amsterdam in 1986 and 1996, respectively.

In 1987, he joined the DIMES IC Process Research Sector, Delft University of Technology, The Netherlands, as a Process Engineer. Currently, his main interest is development of metallization processes and substrate transfer technology.

Jan W. Slotboom (M'82) was born in Utrecht, The Netherlands, in 1942. He received the M.Sc. degree in electrical engineering from the Technical University of Delft, Delft, The Netherlands, in 1966, and the Ph.D. degree from the Technical University of Eindhoven, Eindhoven, The Netherlands, in 1977, performing his dissertation on 2-D numerical device simulation of bipolar transistors and pioneering experiments on bandgap narrowing in heavily doped silicon.

In 1967, he joined the Philips Research Laboratories, Eindhoven, where he worked on bipolar device modeling, numerical simulations, and experimental silicon device physics. He was involved in the development of CCD memories for video applications and exploratory research of high-density memories. His current research activities are on research of novel silicon devices (e.g., SiGe bipolar transistors), hot-carrier effects, and new memory cells. He has authored or coauthored over 70 papers and holds 17 patents. Since 1994, he has been a part-time Professor with DIMES, Delft University of Technology.

Prof. Slotboom was a member of the Solid-State Devices Subcommittee of the IEDM in 1980, 1983, and 1984. He was Vice Chairman and Chairman of International Arrangements for Europe of the IEDM. He has served as a Program Subcommittee Member of the IEDM in 1991 and 1992 and of the BCTM 1995 Conference. He has been a member of the Technical Program Committee of the ESSDERC for many years.