Extraction of Circuit Models for Substrate Cross-talk

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Abstract

An increasingly urgent topic for the realization of densely packed (mixed signal) integrated circuits is prevention of cross-talk via the substrate. This paper proposes a Boundary Element Method (BEM) for calculating an admittance matrix for the substrate in order to analyze the parasitic coupling during layout verification.

In contrast with standard BE methods, we propose a Green's function which is specific to the domain and the problem. This allows minimal discretization and a direct extraction of circuit models for the cross-talk. The extraction can be combined with an efficient model reduction technique to obtain more simple, yet accurate models for the cross-talk. The complete extraction process has a linear time complexity and a constant memory usage. The method is fully implemented and integrated in an existing layout-to-circuit extractor.

1 Introduction

Due to the continuing decrease of the distances between components and the simultaneous increase of operating frequencies, the cross-talk between components and/or circuit blocks becomes stronger. The increase of cross-talk not only holds for coupling via the interconnect (parasitic coupling capacitances), but more and more also for cross-talk via the substrate [1]. Thus, an increasingly urgent topic for the realization of densely packed integrated circuits is prevention or at least control of cross-talk via the substrate. This problem is particularly important in high-frequency and/or mixed-signal integrated circuits. There exist examples of designs that, because of this problem, could not be fabricated on one chip [2].

In Figure 1 we illustrate the situation at hand. It shows a mixed-signal integrated circuit. The switching in the digital part induces potential spikes on the supply lines. These spikes are then coupled into the substrate, where they propagate to the analogue part of the circuit. There they are picked up, e.g. by the depletion capacitance of a diffused resistor or the bulk contact of a transistor. Thus, the disturbances may appear at the output of the circuit, degrading the performance or even causing malfunctioning of the circuit.

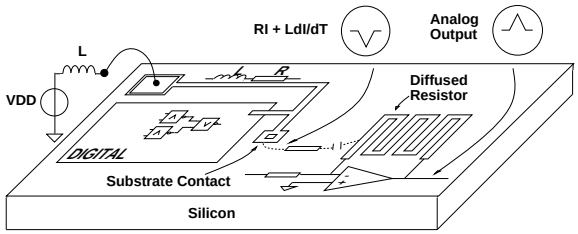


Figure 1: **Sketch of a substrate coupling problem in a mixed-signal circuit.**

Currently, the most commonly used method to circumvent these problems is a very costly trial-and-error procedure, which relies on experience and expertise of the designer. In order to allow accurate substrate analysis of the design, before it is sent to the foundry, it is of paramount importance to have a CAD tool, similar to the layout verification methods for the parasitic interconnect capacitance problem, which can be used within the design loop. Such a tool is not available today.

Some methods were published for detailed numerical analysis of these problems in a few standard situations [3, 4, 5]. They use a full (Finite Element) numerical analysis of all potentials and currents in the substrate, either by simulation of a 3D resistance mesh of the complete substrate or by device simulation. However these approaches are not efficient enough for implementation in a standard CAD system. Furthermore, they do not provide a circuit model for the designer as a direct feedback between the circuit design, the layout design and the substrate problems.

In this paper we propose a method to derive circuit models for the parasitic substrate cross-talk directly from the layout. This is achieved using a Boundary Element Method (BEM), with a suitable choice of the Green's function, which characterizes the inhomogeneous domain. This avoids a full discretization of the complete substrate and allows a straight forward computation of a fully specified equivalent electrical network. However, the matrix inversion in the BEM can be done in an approximate way with the Schur method. This leads to a much smaller network

with approximately the same behaviour as the fully specified network. The circuit model can be merged with the original or the simultaneously extracted circuit description in order to be simulated for an analysis of the cross-talk effects on the circuit behaviour.

In the next section we give a description of the proposed method. First we give a description of all the steps needed to calculate the circuit model by a Boundary Element Method [6]. Then we give a detailed description of one of the key issues in the method, i.e. the choice of a Green's function. This is followed by a discussion on the use of approximate matrix inversion with the Schur Method [7]. Finally we discuss some issues for implementation in a layout extractor [8]. In Section 3 we present results illustrating important properties of the proposed method and results showing the relevance of substrate cross-talk analysis. Finally, we conclude in Section 4.

2 Method

2.1 Formulation

At the frequencies of interest ($\lessapprox$10 GHz) the substrate behaves resistively. The resistivity varies, because of the doping profile, only in the direction perpendicular to the Si-SiO_2 interface. Therefore, the substrate with the doping profile is modelled as a stack of parallel homogeneous layers. Often the substrate can be treated as a 2 layer medium: an epi-layer and a substrate layer. On top of this stack a number of areas, which are denoted as contacts, is placed. These represent the areas where the designed circuit may possibly interact with the substrate, e.g. bottom sides of MOSFETs, real (designed) substrate contacts, etc. The structure is illustrated in Figure 2. On the bottom of the stack there may also be contacts. In practice however, this will usually be one large contact covering the whole bottom or there will be no contact at all.

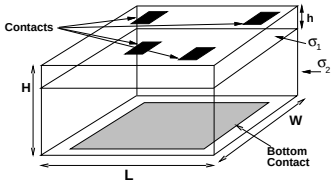


Figure 2: **3D view of the epi-layer and substrate with contacts.**

In order to model the behaviour of the substrate, we must know the admittance matrix of the multiterminal distributed resistance network between these contacts.

Mathematically the problem is described by a partial differential equation in a domain Ω with boundary conditions on the boundary Γ. A direct solution with a Finite Element or Finite Difference Method would require a full discretization of the complete substrate, which leads to very large matrices. Furthermore, we are primarily interested in the behaviour on the boundary, since this is where the substrate interacts with the circuit. In fact we are looking for an equivalent electrical network between the contacts only. Therefore it is more attractive to use a Boundary Element Method [6].

In each layer the problem is described by the Laplace equation for the potential $\phi(\vec{x})$

$$\sigma(\vec{x})\nabla^2\phi(\vec{x}) = 0. \tag{1}$$

where $\sigma(\vec{x})$ is the conductivity of the layer. The boundary condition is that no currents are flowing through the boundaries (normal derivative of $\phi = 0$) except for the contact areas. For these areas the potential is prescribed (constant over the area for ideal contacts). All layers are coupled through *interface conditions* (potential and normal component of current density are continuous).

With Green's theorem the set of equations is transformed to the following Boundary Integral Equation (BIE) [6]

$$\alpha\phi(\vec{x_0}) + \int_\Gamma \sigma(\vec{x})\frac{\partial G(\vec{x};\vec{x_0})}{\partial n}\phi(\vec{x})d\Gamma(\vec{x}) = \tag{2}$$
$$\int_\Gamma \sigma(\vec{x})G(\vec{x};\vec{x_0})\frac{\partial\phi(\vec{x})}{\partial n}d\Gamma(\vec{x}) = \int_\Gamma G(\vec{x};\vec{x_0})\vec{J_n}(\vec{x})d\Gamma(\vec{x})$$

where $\alpha = 1$ if $\vec{x_0} \in \Omega$, $\alpha = 0$ if $\vec{x_0} \notin \Omega$ and $\alpha = 0.5$ if $\vec{x_0} \in \Gamma$. $\vec{J_n}$ is the normal component of the current density on Γ and $G(\vec{x};\vec{x_0})$ denotes the so-called Green's function. This function will be discussed in detail in Section 2.2. Here it suffices to know that it is a fundamental solution of the partial differential equation. It characterizes the nature of the domain and thus assures a correct behaviour on the layer interfaces. We will tailor our Green's function such that as little of the boundary integrals remain as possible. In general this is done by demanding additional boundary conditions for the Green's function.

The above formulation in Equation (2) is called the collocation BEM. After discretization, applying the BIE to all discrete boundary elements and assuming piecewise constant shape functions for $\phi(\vec{x})$ and $\vec{J_n}(\vec{x})$, the resulting set of equations can be written in matrix form. With the definitions

$$H_{ij} = \begin{cases} \int_{\Gamma_j} \sigma(\vec{x_j})\frac{\partial G(\vec{x_j};\vec{x_i})}{\partial n}d\Gamma(\vec{x_j}) & i \neq j \\ \alpha + \int_{\Gamma_i} \sigma(\vec{x_j})\frac{\partial G(\vec{x_j};\vec{x_i})}{\partial n}d\Gamma(\vec{x_j}) & i = j \end{cases} \tag{3}$$

and

$$G_{ij} = \frac{1}{A_j}\int_{\Gamma_j} G(\vec{x_j};\vec{x_i})d\Gamma(\vec{x_j}) \tag{4}$$

where A_j denotes the area of element j, we have

$$H\cdot\Phi = G\cdot J \qquad \text{or} \qquad J = G^{-1}\cdot H\cdot\Phi = Y_e\cdot\Phi \tag{5}$$

Here, Φ is a vector collecting all element potentials and J is a vector collecting all element current densities. A Galerkin version of Equation (2) is obtained by applying an additional weighting procedure, with the shape functions as weighting functions, to each term of the equation.

Matrix Y_e can be interpreted as a full admittance matrix between all boundary elements *with respect to a (virtual) reference node*. This reference node represents the potential at infinity. The boundary elements are part of a contact or part of the rest of the boundary.

Using an incidence matrix F, elements which belong to the same physical contact can be grouped together. Thus we obtain an admittance matrix for the network between all physical contacts *and the elements not belonging to a physical contact* with respect to a virtual reference node:

$$Y = F^T \cdot Y_e \cdot F \tag{6}$$

From this admittance matrix an indefinite admittance matrix Y_{IAM} can be derived by adding a row and a column such that all row sums and all column sums are zero. For convenience we now distinguish between matrix entries belonging to a contact (index c) and entries not belonging to a contact (index n). We then find the following form for Y_{IAM}:

$$Y_{IAM} = \left(\begin{array}{cc|c} Y_{c,c} & Y_{c,n} & Y_{c,\infty} \\ Y_{n,c} & Y_{n,n} & Y_{n,\infty} \\ \hline Y_{\infty,c} & Y_{\infty,n} & Y_{\infty,\infty} \end{array}\right) \tag{7}$$

If desired, the non-contact elements and the virtual reference node may be eliminated by Gaussian elimination.

2.2 Green's Function

As discussed above we need Green's function in order to solve the integral equation. Basically, Green's function is the solution of the fundamental PDE, corresponding to Equation (1)

$$\sigma(\vec{x})\nabla^2 G(\vec{x};\vec{x_0}) = -\delta(\vec{x}-\vec{x_0}) \tag{8}$$

For the analogous electrostatic problem Green's function may be interpreted as the potential at position $\vec{x}$ (observation point) in a domain, induced by a unit point charge at position $\vec{x_0}$ (source point) [9]. The simplest form of a fundamental solution is Green's function of the free space electrostatic problem

$$G(\vec{x};\vec{x_0}) = \frac{1}{4\pi\varepsilon_0\|\vec{x}-\vec{x_0}\|} \tag{9}$$

The main disadvantage of the above equation is that it requires all interfaces to be treated as double boundaries on which afterwards the interface conditions have to be imposed [6]. This implies a complete discretization of all layer interfaces. Furthermore the complete boundary of the substrate must be discretized [6], while we are only interested in the contacts. In contrast with standard BE methods, we will not use the above Green's function, but one which is specific to the domain and the problem, in order to reduce the sizes of the matrices. This is described for the capacitance problem in [10, 12].

We start by requiring that $G(\vec{x};\vec{x_0})$ satisfies Equation (8) in the whole domain Ω. Additionally we demand that it also satisfies the interface conditions, i.e. $G(\vec{x};\vec{x_0})$ and its normal derivative multiplied by the local conductivity ($\sigma(\vec{x})$) are continuous over the interfaces. This assures, as can easily be verified, that Equation (2) describes the problem in Ω, including the interfaces between the layers, and not only the problem in a single homogeneous layer.

If we would demand that the normal derivative of $G(\vec{x};\vec{x_0})$ vanishes on the boundary, the integral in the left hand side of Equation (2) would vanish. Moreover, due to the boundary conditions for J_n, the integral in the right hand side would reduce to an integral just over the contact part of the boundary. This is possible to do, but leads to a double Fourier type series expression for $G(\vec{x};\vec{x_0})$, which has an unsuitable convergence behaviour [10].

In order to obtain a more suitable Green's function we relax the additional boundary condition for $G(\vec{x};\vec{x_0})$. We only demand that the normal derivative of $G(\vec{x};\vec{x_0})$ vanishes on the *top surface* of the substrate, i.e. the Si-SiO_2 interface. Thus the Green's function models a layered semispace. For this situation the Green's function can be found by separation of variables in cylinder coordinates. This leads, for a 2 layer semispace with h the thickness of the first layer, to a single series expansion of the form

$$G = \sum_{n=0}^{n=\infty} \frac{a_n \left(\frac{\sigma_1-\sigma_2}{\sigma_1+\sigma_2}\right)^n}{\sqrt{\rho^2+(b_n+c_n z)^2}}, \tag{10}$$

of which each term can be interpreted as originating from the method of images [9].

The rate of convergence of the series for Green's function depends mainly on the ratio of the two conductivities (σ_1, σ_2). For larger ratios the convergence becomes slower. However, we noted that in these cases even if the series is truncated before the desired accuracy for the series is reached, this is often not noticeable in the resulting admittance matrix. Furthermore, the series (Equation (10)) is either alternating or monotonous. This makes it suitable for standard transforms to speed up the convergence [11]. However, further research is necessary to find a good relation between desired accuracy for the result and needed accuracy in the evaluation of the (integrals of the) Green's function.

In effect, the above approach means that the Green's function models a chip with infinite dimensions in the lateral direction as well as an infinite thickness. This is in many cases a good approximation, since the substrate layer

is often much thicker than the epi-layer and usually all devices are placed far from the sidewalls of the chip (saw lane, safety margin etc). If this approach is applied to the analysis of the previous section it turns out that matrix H reduces to an identity matrix and only integrals over the contacts (on the top surface) remain. Clearly this reduces the computational effort needed to obtain the solution.

If necessary, the effects of the finite thickness of the chip can be taken into account by discretizing the bottom. This is necessary for extremely thin substrates. This will be illustrated in the next section. In this case, the matrix H in Equation (6) is no longer an identity matrix. The additional elements can be eliminated from the solution before the final admittance matrix is formed. It is clear that it is also necessary to discretize the bottom of the substrate if a backside contact exists.

With the proposed method the effects of the lateral sidewalls of the chip are neglected. This may cause errors e.g. for contacts which are close to the edges of the chip. In Section 3.1 it will be shown that in many cases these effects are negligible. The effects could be taken into account by discretizing the lateral sidewalls. However, this leads to the evaluation of difficult integrals and increases the amount of computational effort drastically. Alternatively, the effects of the sidewalls can be taken into account by applying the method of images [9] to the entire Green's function. This means mirroring the source point in all sidewalls of the chip. Since the source point lies surrounded by 4 walls (mirrors) this leads to an infinite number of images, as illustrated in Figure 3. Unfortunately, this leads to a divergent series. However, the sidewall effects are well approximated if we only take into account the *side(s) close to the source point* (+ in Figure 3). Effectively, this means a double or triple evaluation of the Green's function. In the Section 3.1 we will show that this approach gives a good approximation for the sidewall effects.

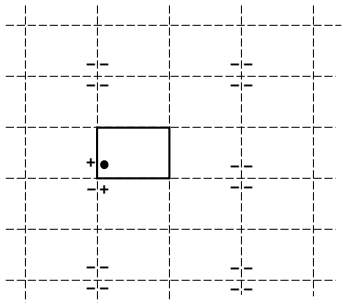


Figure 3: **Method of images to include effect of lateral sidewalls. Fat lines indicate the actual chip. • indicates the boundary element under consideration. '+' and '-' indicate images. Only the images indicated by a '+' are used for the approximation.**

2.3 Approximate Inversion

The inversion in Equation (5) may be performed exactly via standard methods. However, in general inversion is an $\mathcal{O}(N^3)$ process, in which N is the number of boundary elements. Although this number is minimal due to the use of a Boundary Element Method and the choice of the Green's function, the inversion can still become inefficient. Exact inversion results in a fully specified inverse and therefore also a fully specified admittance matrix.

However, it is possible to calculate an *approximate* inverse with the (hierarchical) Schur method [7]. This approximate inversion yields a reduced, but physically correct admittance matrix. The Schur method results in a sparse (banded) approximation of the inverse of G and will also result in a (*banded*) approximation of the admittance matrix. Physically this means that for a contact all admittances to other contacts within a user-defined environment around that contact are calculated, but the *direct* admittances to contacts outside this environment are not calculated. However the indirect coupling, via the (virtual) reference node is taken into account. For these cases the direct admittance (coupling) is much smaller than the admittances (coupling) to the virtual node and thus may indeed be neglected. This is illustrated in Section 3.1.

It has been shown that this inversion method is an $\mathcal{O}(Nb^2)$ process [12]. Here b is the width of the Schur band. Thus for a given choice of b, which mainly depends on the used technology, the time complexity is linear. Note that if the band covers the whole design $b = N$ and we obtain again an $\mathcal{O}(N^3)$ process. The resulting inverse is exact in this case, leading to the fully specified admittance matrix. Finally we remark that the memory usage of this method is mainly depending on the (fixed) bandwidth. Thus concerning the memory usage this is an $\mathcal{O}(N^0)$ process.

2.4 Implementation

The method as described above is fully suitable for implementation in many layout-to-circuit extractors. Here, we describe issues related to our implementation in the layout-to-circuit extractor Space [8, 10, 12].

Space uses a scanline mechanism and a corner-stitched data structure of the layout. In a technology file the mask combinations defining devices (e.g. MOSFETS), relevant contact areas (e.g. substrate contacts), etc. must be specified together with data describing the substrate (layer thicknesses and conductivities). This has to be done once for each different technology. Data for e.g. integration methods, collocation or Galerkin method and Schur inversion (e.g. the bandwidth) can be specified in a separate, user controllable, parameter file. An efficient scanline mechanism is used to scan the layout. During the scanning process the discretization, calculation of the matrix entries, (approximate) Schur inversion and calculation of the ad-

mittance matrix is performed. The Schur bandwidth corresponds with a geometrical window attached to the scanline. As soon as possible the calculated network elements are written in the netlist database. With the correct stimuli the extracted circuit can then be analyzed with e.g. Spice. The whole extraction process of the substrate cross-talk model is fully integrated with all other features of Space, including extraction of active devices, interconnect resistances and 3D interconnect capacitances.

The matrix inversions, which arise for the substrate cross-talk extraction as well as for the 3D interconnect capacitance extraction, are the bottleneck of the whole layout extraction process if they are carried out exactly. However, with the Schur inversion and since all other steps in the extraction are at most linear ($\mathcal{O}(N)$) in time complexity, the whole extraction can be done in linear time.

Although the above method is efficient for large designs it still can be too time consuming. Therefore, analogous to the capacitance problem, we have developed a heuristic method for faster calculations [13]. It uses a Delauney mesh to determine the most relevant couplings. Next the coupling resistances are calculated via interpolation formulae based on results for typical structures calculated with the present method.

3 Results

In this section we present results from the Boundary Element method discussed above. First, results from some special test structures will be presented to illustrate the properties and approximations discussed in the previous section. Subsequently, we will present results from circuit applications. More examples are given in [10, 14].

3.1 Test structures

First we will concentrate on the effect of boundedness of the domain, i.e. the finite thickness of the substrate and the presence of the sidewalls. For this purpose we consider a substrate with two parallel rectangular contacts (10 μm $\times$ 100 μm at a distance of 30 μm) on the top surface. The epilayer is 7 μm thick and has a resistivity ($1/\sigma$) of 20 Ωcm. The conductivity of the substrate layer is varied.

Figure 4 shows the calculated resistance for three chip thicknesses, while the domain was considered to be infinite in the lateral dimensions. For the thinnest chip the bottom was discretized in 400 elements, while for the medium thickness 324 elements were used. For the thickest chip only 4 elements were already more than sufficient. In fact the same result is obtained if the bottom is neglected, i.e. if the chip is considered to be infinitely thick. For reference also the exact results obtained with the method of [10], with a Green's function with vanishing derivatives on all boundaries of the domain, are given. Clearly, there is a good agreement between the methods. Note that for the extremely thin chip more than 400 elements are needed for agreement with the exact results.

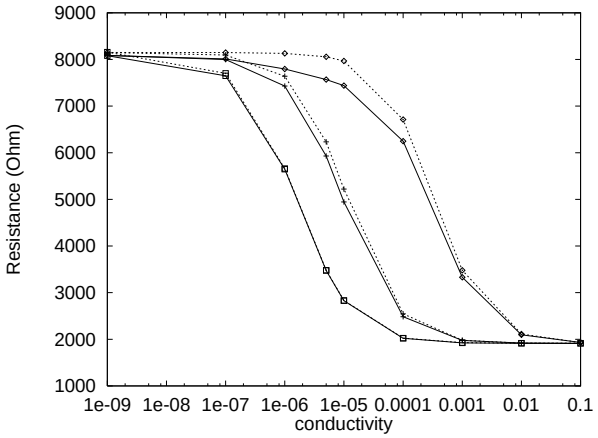


Figure 4: **Calculated resistance vs. substrate conductivity σ_2 with total chip thickness (H) as parameter. Epilayer was 20 Ωcm and 7 μm thick in all cases.**
Solid lines: method of [10], dashed lines: present method. $\diamond$: H=7.1 μm, $+$: H=10 μm, $\Box$: H=300μm.

The second example considers the influence of the lateral sidewalls of the chip. The structure is similar to the previous one, except that the substrate structure now consists of a 22 μm thick 20 Ωcm epilayer on a 278 μm thick 3.5 Ωcm substrate. Figure 5 shows the calculated resistance as a function of the distance of the sidewalls to the bounding box of the contact structure. The exact solution is calculated with the program described in [10]. The overall error is certainly small enough for practical purposes. The largest error of the approximation method of Figure 3 is about 3% and occurs if the contacts touch the sidewalls. This is just the situation where the approximation can be expected to be least accurate, since the strength of the images decreases with distance. Clearly we see that for distances larger than 40 μm the sidewall effects are negligible and the infinite chip method can be used.

The third set of test results is shown in Figure 6. These were obtained with the present method for several variations of the same structure. Here we see the influence of distance between the contacts, doping levels and epi-layer thickness on the resistance value. We observe that the distance over which the resistance varies with the separation between the contacts is mainly determined by the epi-layer thickness. The rule of thumb [4] that the critical distance is approximately 4 times the epi-layer thickness is confirmed.

With this same rule we can now explain the result of Figure 5. Considering that the distance between the original and its mirror image is twice the distance shown on the x-axis, we see that the distance of twice 40 μm agrees with approximately 4 times the epi-layer thickness (22 μm). Thus

we conclude as a rough guideline that sidewall effects can be neglected if all contacts are further than twice the epi-layer thickness from the edges of a chip. In practice this will often be the case, especially with the tendency to decrease epi-layer thicknesses in modern technologies.

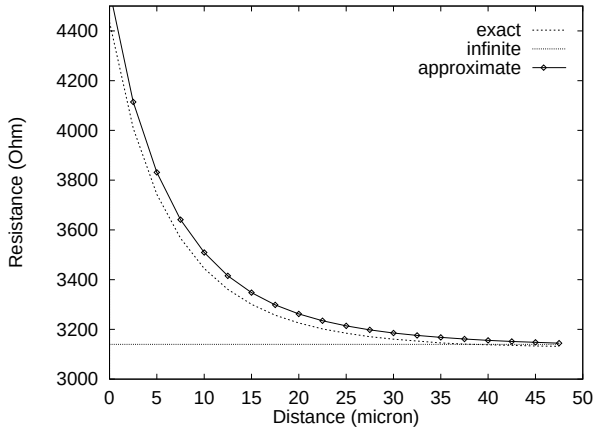


Figure 5: **Calculated resistance vs. distance D_C to sidewall for exact method [10], infinite domain and approximation.**

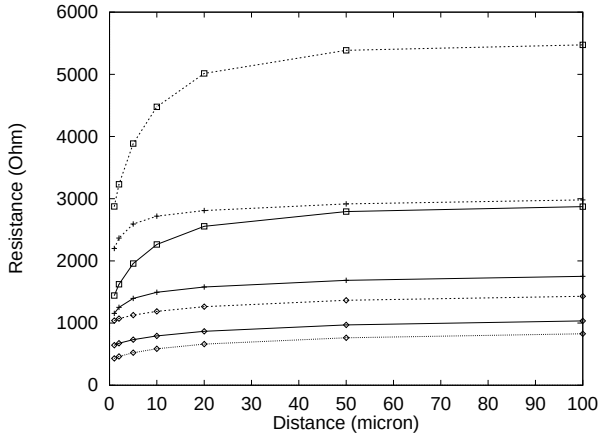


Figure 6: **Resistance as a function of contact distance for various substrate situations. All substrate layers were 3.5Ωcm. Epi-layer resistivities and thicknesses varied. Lines: epi-layer resistivity: dashed lines: 40 Ωcm, solid lines: 20 Ωcm, dotted lines: 10 Ωcm. Symbols: epi-layer thickness: □: 16.6 μm, +: 4.15 μm, ◇: 1.04 μm.**

The following example illustrates some properties of the Schur inversion. The structure considered consists of 5 parallel rectangular contacts (1 μm × 10 μm at distances of 1 μm, numbered 1 to 5) on a 5 μm thick epilayer. In Table 1 the calculated resistances for contacts 1 and 2 are shown for several values of the Schur window. R_{ij} denotes the direct resistance between contacts i and j, where ∞ represents the virtual reference node and R_{is} denotes the short-circuit resistance, - the total resistance that a contact 'sees'.

An infinite band is equivalent to exact inversion. As the band is made narrower, resistances between 'far' contacts become infinite. This means that direct coupling between these resistances is neglected, but not the coupling via the reference node. Note however, that R_{is} stays almost constant until very small bandwidth values. Thus a good approximation of the coupling to and through the substrate is kept, even for small bandwidths.

Table 1: **Calculated resistances for several Schur bands.**

window	$R_{1\infty}$	R_{12}	R_{13}	R_{14}	R_{15}	R_{1s}
∞	129	41.8	134	204	193	20.3
4	117	40.9	122	135	∞	20.6
3	101	38.9	83.6	∞	∞	21.0
2	81.0	31.1	∞	∞	∞	22.5
1	47.0	∞	∞	∞	∞	47.0

window	$R_{2\infty}$	R_{21}	R_{23}	R_{24}	R_{25}	R_{2s}
∞	209	41.8	48.0	171	204	16.6
4	235	40.9	49.2	222	134	16.4
3	221	38.9	52.0	83.6	∞	16.3
2	292	31.1	31.1	∞	∞	14.8
1	47.0	∞	∞	∞	∞	47.0

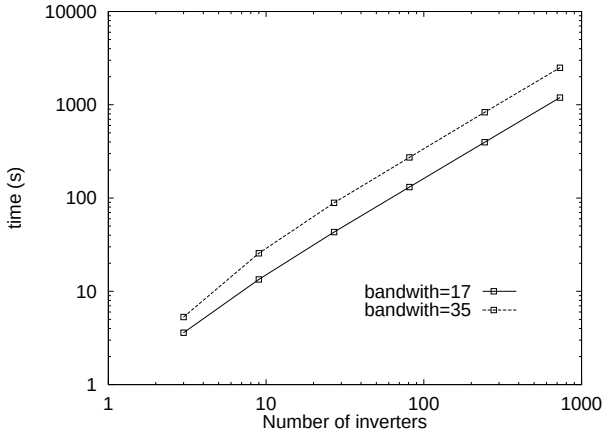


Figure 7: **Extraction time as a function of the number of inverters for two choices of the Schur bandwidth. Computation times were measured on a HP 9000/735.**

In Figure 7 we show the time complexity for experiments done on series of MOS inverters. It clearly shows the linear extraction time as a function of the number of inverters for two choices of the Schur window. The largest bandwidth covers three neighbouring inverters and thus all direct coupling between three successive stages are accounted for. Coupling between inverters further apart is accounted for via the virtual reference node. The memory us-

age was 0.9 Mbyte for the small bandwidth and 1.6 Mbyte for the large bandwidth, largely independent of the number of inverters.

3.2 Circuit examples

The next example is based on the structure used in [4], which is shown in Figure 8. It is an abstraction of a typical situation in a mixed-signal chip. Contact 3 represents the output of a digital ring oscillator (MOSFET drain region) and contact 2 represents a sensitive node (back gate of MOSFET) in an analogue part. If due to the digital switching the potential of this back gate fluctuates, this modulates the threshold voltage and thus the current through the MOSFET. This results in noise in the analogue signal. We analyzed this structure for two substrate situations: a 7 µm, 15 Ωcm epi-layer on a highly doped substrate (300 µm, 0.05 Ωcm) and a homogeneously lowly doped (15 Ωcm) substrate. The distance (D_X) between the substrate contacts and the other contacts was 6µm or 22µm and the distance between 'source and destination' (D_C) was varied.

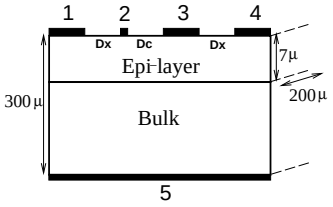


Figure 8: **Structure from [4], used for next figure.**

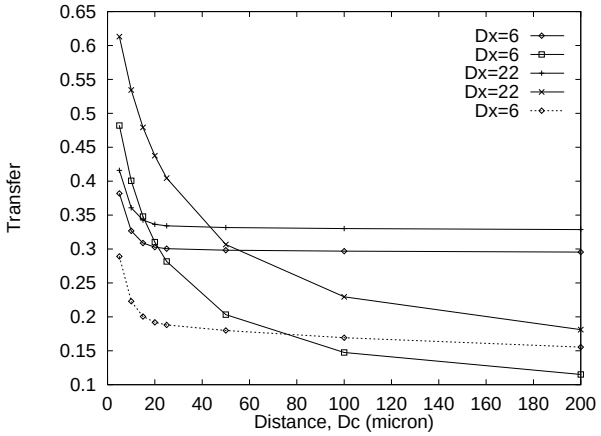
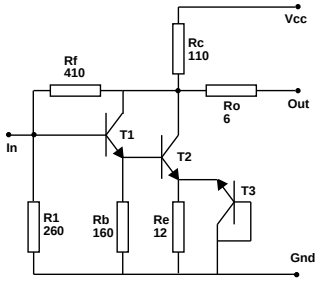


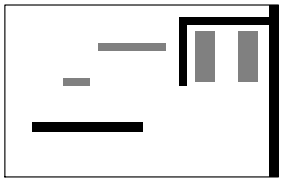
Figure 9: **Results for structure of Figure 8. Dashed line indicates situation with backside contact. $\diamond, +$: highly doped substrate, $\square, \times$: lowly doped substrate.**

The calculated (voltage) transfer characteristics from contact 3 to contact 2 when all other contacts are connected to ground are shown in Figure 9. Clearly, close substrate contacts suppress coupling more than far substrate contacts. As expected a backside contact can significantly reduce the coupling in the case of a highly doped substrate. Furthermore we see that in the case of a good conducting substrate layer the effect of increasing distance between 'source and destination' saturates quickly if the distance is in the order of 3 times the thickness of the epi-layer. For the lightly doped substrate this saturation distance is much larger. This confirms the behaviour observed in [4, 5] by full device simulations and measurements. It is also in agreement with the experiments shown in Figure 6.

As a more realistic example we study the transfer characteristics of a bipolar high-frequency amplifier. The schematic and the simplified layout are shown in Figure 10. The substrate contacts are connected to ground with short and wide metal interconnections, therefore the influence of these interconnections are negligible. Since the bipolar transistors occupy the full depth of the epi-layer, the epi-layer does not need to be modelled. The doping profile of the substrate is modelled by a 1.4 µm thick 0.15 Ω-cm transition layer between the epi-layer and the 4 Ω-cm substrate.



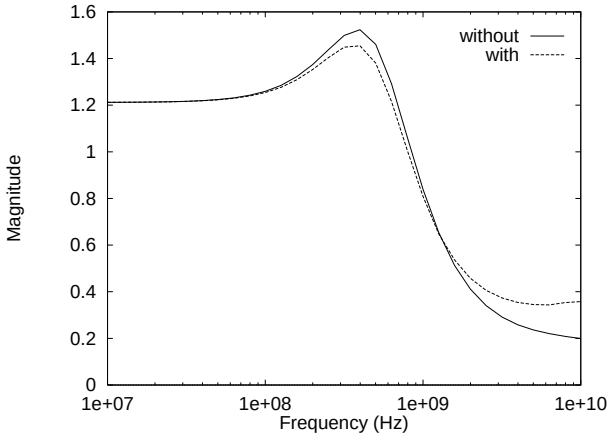
(a)



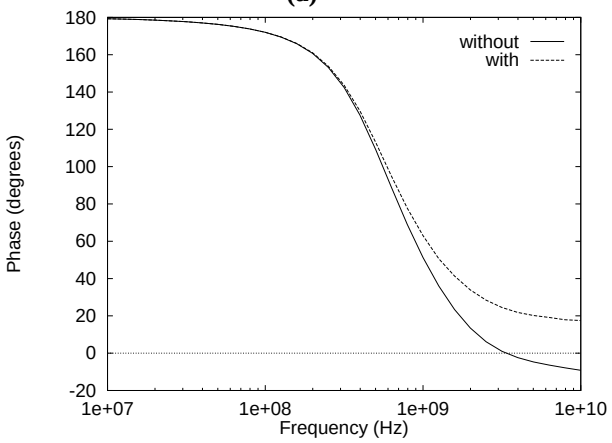
(b)

Figure 10: **Schematic (a) and Simplified Layout (b) of HF bipolar amplifier. Grey areas indicate the position of a transistor (from left to right T1, T2, T3a and T3b), black areas indicate the position of a substrate contact.**

Figure 11 shows the transfer characteristics of the amplifier calculated with Spice, with and without taking into account the substrate effects. The substrate model was calculated with the present model with full inversion. For clarity no other parasitics were taken into account. Globally the behaviour does not change. However, it can be seen that the unity gain frequency is overestimated by about 10% if the substrate is neglected. Furthermore, the phase at this frequency shows a difference of 15 degrees (20%). The peak before the unity gain frequency is smoothened due to the substrate coupling.



(a)



(b)

Figure 11: **Simulated magnitude (a) and phase (b) of transfer function vs. frequency. Solid lines: without substrate effects, dashed lines: with substrate effects.**

4 Conclusions

In this paper we outlined the key issues of a method to derive systematically a network model for the parasitic substrate cross-talk from the layout of a design. We showed that by a proper choice of the Green's function of the Boundary Element Method this can be done, such that only those parts of the substrate boundary (called 'contacts') have to be discretized that directly interact with the designed circuit. We gave a method to include the effects of the lateral boundedness without introducing extra boundary elements. It was shown that it is only necessary to include these if there are contacts closer than twice the epilayer thickness to the edges of the chip. Only in the rare case that the total thickness of the chip is important additional boundary elements need to be introduced. Furthermore we showed that it is possible to integrate model reduction techniques with the proposed method to arrive at simplified, yet accurate enough, networks for the analysis of substrate cross-talk. Due to the Schur inversion the whole extraction can be achieved with a linear time complexity and a constant memory usage. The method was completely implemented and integrated in the layout-to-circuit extractor Space.

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