Extraction of Gate Resistance in Sub-100-nm MOSFETs With Statistical Verification

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***Abstract*— This paper presents an improved z-parameter based approach to extract the gate resistance at low frequencies. The effectiveness of this approach, compared with other y-parameter based approaches, is verified using 430 samples fabricated in 40-, 55-, 90-, and 110-nm CMOS technology nodes. The influence of the nonquasi-static (NQS) effect, resulting from the distributed channel resistance, on the gate resistance extraction is studied, and the optimum processes are suggested to reduce the NQS effect. Finally, the extraction of the channel resistance in the lightly doped drain region is also presented.**

***Index Terms*— Distributed channel resistance, distributed poly-silicon gate resistance, gate contact resistance, gate resistance extraction, nonquasi-static (NQS) effect.**

I. Introduction

DUE to the aggressive scaling in the feature size and its resulting very high cutoff frequency (f_T) and maximum oscillation frequency ($f_{\max}$) in hundreds of GHz, nanoscale CMOS technology has already become a potential candidate for sub-THz applications [1]. As predicted in the 2012 International Technology Roadmap for Semiconductors [2], multigate MOSFETs with 15.3-nm gate length can achieve 710 and 622 GHz for f_T and $f_{\max}$, respectively. However, when working at such high frequencies and aiming at low-power applications, the noise from the transistor itself become critically important and therefore accurate noise models are required. In addition to the channel thermal noise, induced gate noise, and their correlations, the noise from the gate resistance is the major noise contributor because its effect is amplified by the transistor itself to the next stage. Therefore, how to accurately extract the gate resistance from experiments and provide a scalable gate resistance model become very crucial for low-noise and low-power applications. In addition, the accuracy of the extracted gate resistance has a great impact on the extraction of the channel thermal noise, induced gate noise, and their correlations [3], the noise evaluation between technologies using the equivalent noise sheet resistance [4], the investigation of device reliability [5]–[7], and the thermal noise modeling of devices [8]–[10].

Due to the gate-to-source and the gate-to-drain capacitances, the gate resistance cannot be directly characterized from the I–V measurements. Z- or y-parameters obtained at high frequencies are therefore used to extract the gate resistance [11]–[21]. For the z-parameter based approaches in [11], [17], and [21], to remove the impact from the frequency-dependent term (e.g., $A_g/(\omega^2 + B)$ in [11]), z-parameters measured at very high frequencies (e.g., 35–40 GHz) are needed [21] that put a very high demand on the equipment and the accuracy of the equivalent circuit model. On the other hand, at high frequencies, the total gate resistance R_g seen at the gate terminal is not only contributed from the gate contact resistance R_{gcon} and the distributed poly-silicon gate resistance R_{gpoly} but also from the distributed channel resistance R_{ch} [12], [16]. When extracting the gate resistance at such high frequencies, the nonquasi-static (NQS) effect becomes very pronounced and causes the distributed channel resistance R_{ch} to be the dominant contributor in the extracted gate resistance [16]. The separation of R_{ch} from R_{gcon} and R_{gpoly} is not only important in accurately describing the RF behavior of MOSFETs [20] but also crucial in the thermal noise modeling. Since the thermal noise in the channel is already taken care of by another noise current source [8], R_{ch} should be modeled as a noise free resistor. If R_{ch} is included in R_g as a noisy resistor and used in the thermal noise extraction, it results in an underestimation of the channel thermal noise and, therefore, demonstrates a wrong bias and geometry dependence in the channel thermal noise modeling.

For the z-parameter based approach in [18], the algorithm can extract R_g at low frequencies. However, its equivalent circuit in [18, Fig. 1] cannot be applied at all gate bias conditions and becomes invalid particularly at $V_{\text{GS}} = 0$ V due to the ignorance of the coupling capacitance C_{gb} between the gate and the substrate [20], [22]. In addition, its algorithm and accuracy are affected by the assumption, i.e., $R_i = R_{\text{ch}}/6$ [18] or $R_i = R_{\text{ch}}/3$ [23], used in the equation derivation. Therefore, in this paper, we propose an improved z-parameter based approach to extract R_g at low frequencies. Since the low-frequency extrapolation is applied in the algorithm, we can use a very simple small-signal equivalent circuit for medium high frequencies in [22] and the high-frequency components such

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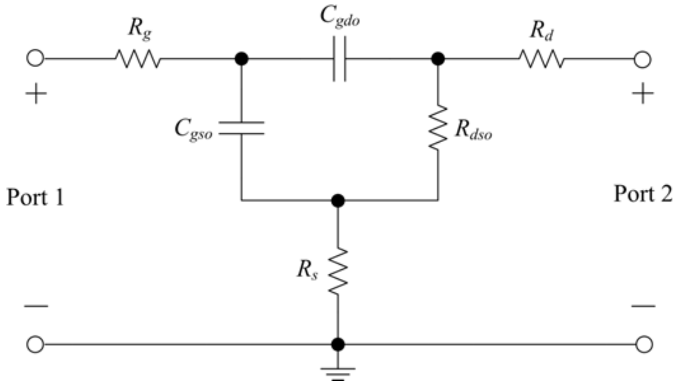

Fig. 1. Equivalent circuit for a MOSFET biased at $V_{GS} = V_{dd}$ (nominal supply voltage) and $V_{DS} = 0$ V for medium-high-frequency applications.

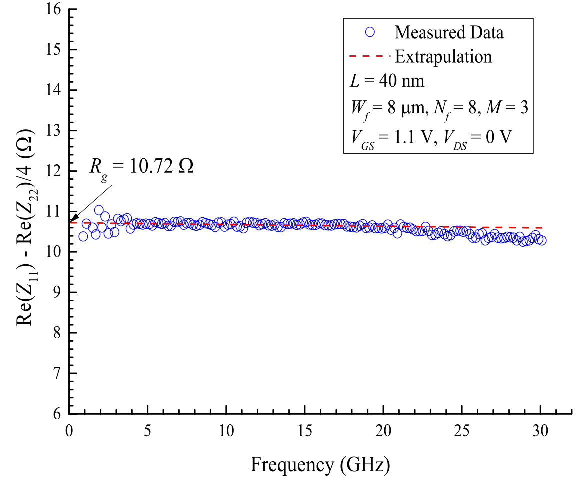

Fig. 2. $\mathrm{Re}(Z_{11}) - \mathrm{Re}(Z_{22})/4$ versus frequency characteristics for an n-type FET with $L = 40$ nm, $W_f = 8$ μm, $N_f = 8$, and $M = 3$ biased at $V_{GS} = 1.1$ V and $V_{DS} = 0$ V.

as C_m, C_{mb}, C_{mx}, and C_{sd} in [21] and [22] can be all ignored. This low-frequency approach not only reduces the complexity of the equivalent circuit without losing its generality and accuracy but also simplifies its analytical z-parameter expressions. In addition, it prevents the impact from the substrate coupled into the experimental results. Finally, to improve the extraction accuracy and avoid the NQS effect, we evaluate the R_g extracted from devices fabricated in different processes and suggest the optimum processes most suitable for gate resistance extraction.

II. Extraction of Gate Resistance

The device under test (DUT) is biased at the condition of $V_{GS} = V_{dd}$ (nominal supply voltage) and $V_{DS} = 0$ V. We improve the approach in [18] by choosing $V_{GS} = V_{dd}$ to physically eliminate the coupling between the gate and the substrate (i.e., $C_{gb} \approx 0$ fF [20]). At medium high frequencies, its small-signal equivalent circuit is shown in Fig. 1, where R_g is the gate resistance to be extracted, R_d and R_s are the parasitic resistances at the drain and the source terminals, respectively, R_{dso} includes the channel resistance R_{ch} and the resistance R_{LDD} in the lightly doped drain (LDD) regions. Here, C_{gso} and C_{gdo} are the gate-to-source and gate-to-drain capacitances, respectively. Because of the symmetry of the drain and source terminals at $V_{DS} = 0$ V, C_{gso} and C_{gdo} are equal in both their intrinsic portion from the oxide capacitance ($C_{ox}/2$) [22] and extrinsic portion from the overlap capacitance C_{ov}. In this paper, we define $C_{gso} = C_{gdo} = C_{oxv}$, which can be directly extracted from the measured imaginary part of y_{11} (i.e., $\mathrm{Im}(y_{11})$) versus frequency characteristics [14]. In addition, we assume that $R_d = R_s$ due to the symmetry of the MOSFET structure at $V_{DS} = 0$ V. Based on the equivalent circuit in Fig. 1, its z-parameters can be expressed as

$$Z_{11} = R_g + R_s + \frac{R_{dso}}{\omega^2 R_{dso}^2 C_{oxv}^2 + 4} - j\frac{\omega^2 R_{dso}^2 C_{oxv}^2 + 2}{\omega C_{oxv}(\omega^2 R_{dso}^2 C_{oxv}^2 + 4)}$$
$$\cong \left(R_g + R_s + \frac{R_{dso}}{4}\right) - j\left(\frac{1}{2\omega C_{oxv}}\right) \quad (1)$$

$$Z_{12} = Z_{21} = R_s + \frac{2R_{dso}}{\omega^2 R_{dso}^2 C_{oxv}^2 + 4} - j\frac{\omega R_{dso}^2 C_{oxv}}{\omega^2 R_{dso}^2 C_{oxv}^2 + 4}$$
$$\cong \left(R_s + \frac{R_{dso}}{2}\right) - j\left(\frac{\omega R_{dso}^2 C_{oxv}}{4}\right) \quad (2)$$

and

$$Z_{22} = R_d + R_s + \frac{4R_{dso}}{\omega^2 R_{dso}^2 C_{oxv}^2 + 4} - j\frac{2\omega R_{dso}^2 C_{oxv}}{\omega^2 R_{dso}^2 C_{oxv}^2 + 4}$$
$$\cong \left(R_d + R_s + R_{dso}\right) - j\left(\frac{\omega R_{dso}^2 C_{oxv}}{2}\right) \quad (3)$$

where $s = j\omega$. During the derivation, the only assumption we made was that the frequency is low enough such that $\omega R_{dso} C_{oxv} \ll \sqrt{2}$ can be held. If we define the critical frequency $\omega_c = 2\pi f_c$ such that $\omega_c R_{dso} C_{oxv} = \sqrt{2}/10$, or

$$f_c = \left(\frac{1}{10}\right) \cdot \frac{1}{\sqrt{2}\pi R_{dso} C_{oxv}} \quad (4)$$

for the technology studied in the paper, f_c becomes higher when the channel length decreases because of the reduction of R_{dso} and C_{oxv}, and is usually in the range of tens of GHz if the channel length is shorter than 240 nm for n-type MOSFETs and 120 nm for p-type MOSFETs.

For matured CMOS technology, the parasitic resistances at the drain and the source sides are always engineered in the way such that $R_{dso} \gg R_d$ and R_s to ensure that the applied V_{DS} voltage is mainly drop across the intrinsic channel (i.e., R_{dso}) in all regions of operation. In practice, R_{dso} is about 100 times bigger than R_d and R_s. We can then further simplify (1) and (3) by

$$Z_{11} \cong \left(R_g + \frac{R_{dso}}{4}\right) - j\left(\frac{1}{2\omega C_{oxv}}\right) \quad (5)$$

and

$$Z_{22} \cong R_{dso} - j\left(\frac{\omega R_{dso}^2 C_{oxv}}{2}\right). \quad (6)$$

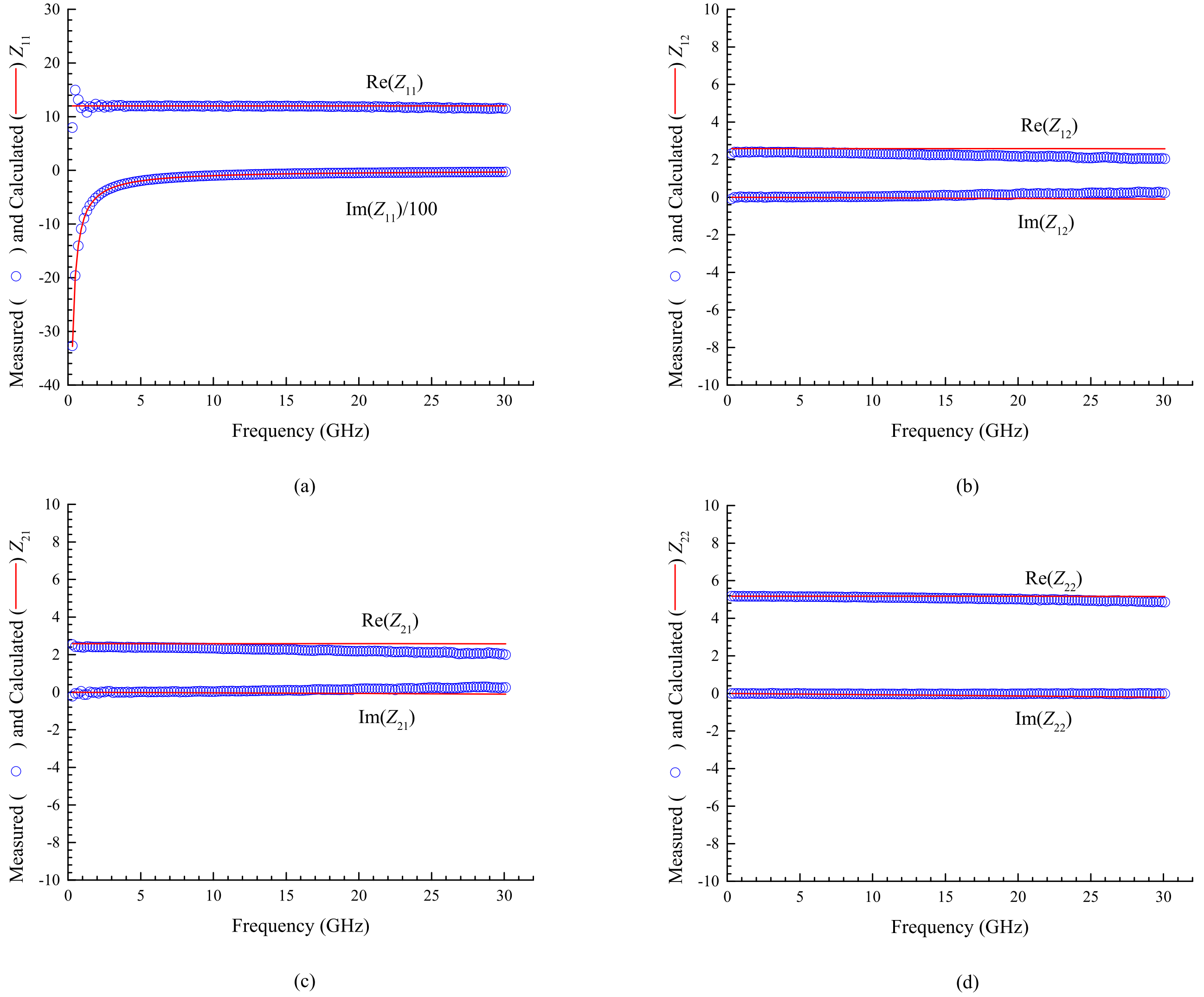

Fig. 3. Measured and calculated intrinsic z-parameters (a) Z_{11}, (b) Z_{12}, (c) Z_{21}, and (d) Z_{22} versus frequency characteristics for an n-type FET with $L = 40$ nm, $W_f = 8$ μm, $N_f = 8$, and $M = 3$ biased at $V_{\mathrm{GS}} = 1.1$ V and $V_{\mathrm{DS}} = 0$ V. The calculation is based on the equivalent circuit in Fig. 1 with $R_g = 10.72$ Ω, $C_{\mathrm{gso}} = C_{\mathrm{gdo}} = 80.8$ fF, $R_{\mathrm{dso}} = 5.2$ Ω, and $R_s = R_d = 0$ Ω.

Therefore, R_g can be extracted by

$$R_g = Re(Z_{11}) - \frac{Re(Z_{22})}{4} \quad (7)$$

where $Re()$ denotes the real part of the parameters.

III. Results and Discussion

The DUTs were designed in multifinger structures, and the total channel width W is expressed as $M \times N_f \times W_f\,\mu$m, where M is the number of transistors connected in parallel in a DUT, N_f is the number of transistor fingers, and W_f is the finger width of each transistor. To verify the extraction procedure, Fig. 2 shows the measured intrinsic (after deembedding the pad parasitics) $Re(Z_{11}) - Re(Z_{22})/4$ versus frequency characteristics for an n-type FET with $L = 40$ nm, $W_f = 8$ μm, $N_f = 8$, and $M = 3$ biased at $V_{\mathrm{GS}} = 1.1$ V and $V_{\mathrm{DS}} = 0$ V. Based on (4), the critical frequency f_c is 53.8 GHz which is much higher than the highest frequency 30.1 GHz in the measurements. In Fig. 2, the measured $Re(Z_{11}) - Re(Z_{22})/4$ is pretty constant up to 15 GHz. Therefore, the resistance R_g can be obtained by extrapolating the measured $Re(Z_{11}) - Re(Z_{22})/4$ versus frequency characteristics down to dc and we get $R_g = 10.72$ Ω for this device.

The next step is to verify the accuracy of the equivalent circuit used in this paper (Fig. 1). Fig. 3 shows the measured and calculated intrinsic z-parameters versus frequency characteristics for an n-type FET with $L = 40$ nm, $W_f = 8$ μm, $N_f = 8$, and $M = 3$ biased at $V_{\mathrm{GS}} = 1.1$ V and $V_{\mathrm{DS}} = 0$ V. The calculation is based on the equivalent circuit with $R_g = 10.72$ Ω, $C_{\mathrm{gso}} = C_{\mathrm{gdo}} = 80.8$ fF, $R_{\mathrm{dso}} = 5.2$ Ω, and $R_s = R_d = 0$ Ω. Very good agreement is obtained for all four parameters upto 15 GHz [as determined by Z_{12} and Z_{21} shown in Fig. 3(b) and (c)], which is high enough for our extraction procedure. The excellent agreement in Z_{11} and Z_{22} confirms that the strategy using the bias condition at $V_{\mathrm{GS}} = 1.1$ V and $V_{\mathrm{DS}} = 0$ V successfully blocks the impact of substrate parasitics coupled into the measured z-parameters and the simple equivalent circuit shown in Fig. 1 is applicable in the gate resistance extraction. The discrepancy between the measured and calculated Z_{12} and Z_{21} above 15 GHz could

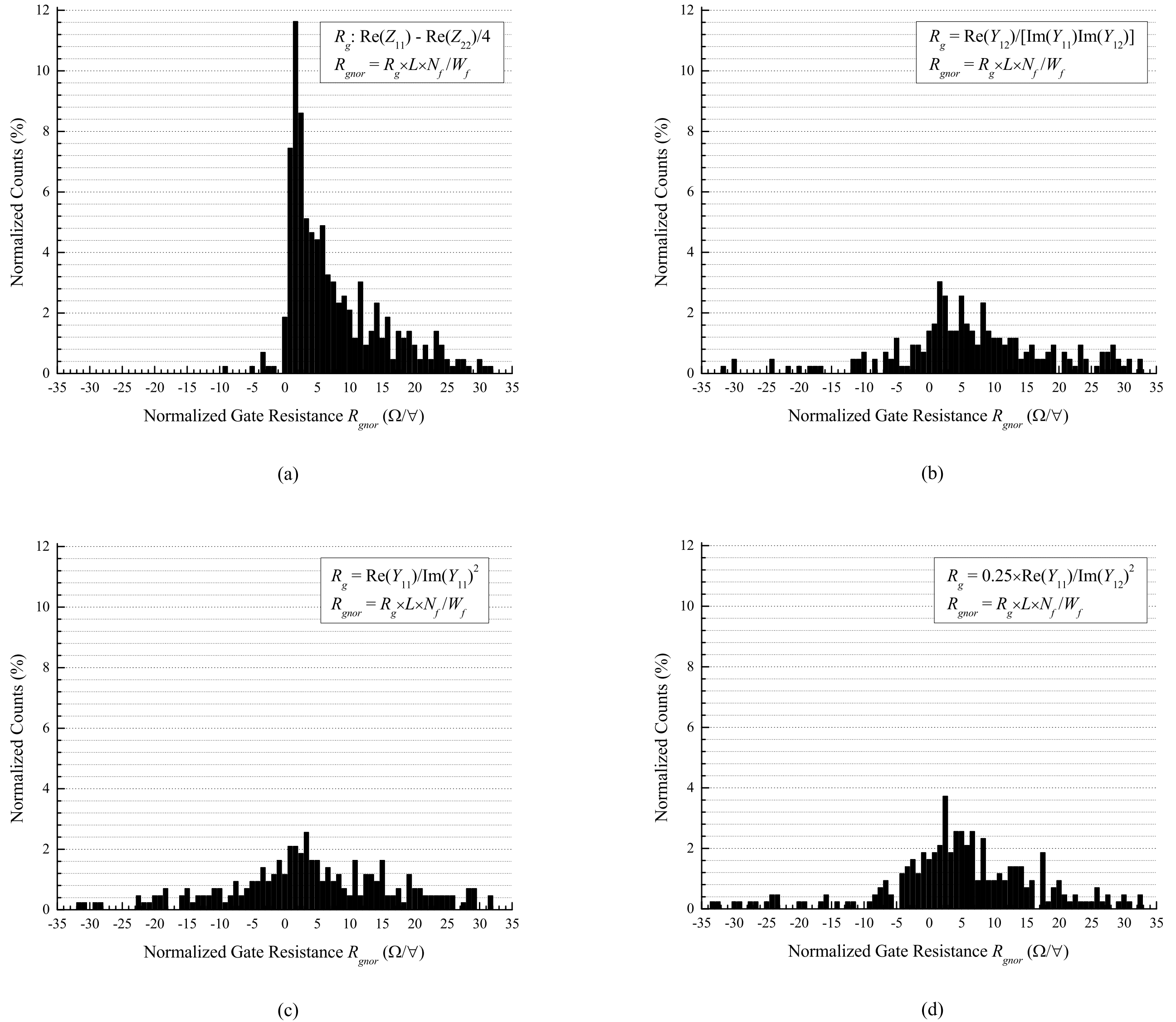

Fig. 4. Normalized histograms (normalized to 430) of the normalized gate resistance $R_{g\mathrm{NOR}}$ (Ω/∀) using R_g extracted from the (a) proposed method (i.e., $R_g = Re(Z_{11}) - Re(Z_{22})/4$), (b) $R_g = Re(Y_{12})/Im(Y_{11}) \cdot Im(Y_{12})$ [13], (c) $R_g = Re(Y_{11})/Im(Y_{11})^2$ [14], [21], and (d) $R_g = Re(Y_{11})/4 \cdot Im(Y_{12})^2$ [20].

result from the ignorance of the high-frequency components such as C_m, C_{mb}, C_{mx}, and C_{sd} in [21] and [22].

For future sub-100-nm technology nodes, process variations, coming from both historical sources and emerging sources, become a very crucial aspect in the device fabrications [24]. Therefore, any proposed parameter extraction routine needs to be robust enough to demonstrate its statistical stability. To verify the robustness of this proposed extraction procedure, we applied our procedure to the experimental data from 430 devices with various L, W_f, N_f, and M combination fabricated in UMCs 40-, 55-, 90-, and 110-nm CMOS technology nodes and compared its stability and robustness against previously published y-parameter based approaches using $R_g = Re(Y_{12})/Im(Y_{11}) \cdot Im(Y_{12})$ [13] and $R_g = Re(Y_{11})/Im(Y_{11})^2$ [14], [21]. For the equation from [13], we remove its modulus sign in (34) because it can be deduced directly from (27) and (28), and the modulus sign was proposed by the authors with no reason. We also evaluate another y-parameter based approach in [20], which directly extracts the distributed gate electrode resistance R_{elect}. When $V_{\mathrm{GS}} = V_{\mathrm{dd}}$, we can observe from [20] that $C_{\mathrm{gb}} \approx 0$ fF. In addition, if we substitute (9) (i.e., $C_{\mathrm{gso}} = -Im(Y_{12})/\omega$) into its R_{elect} (i.e., [20, eq. (12)]), we can obtain

$$R_g = R_{\mathrm{elect}} = \frac{Re(Y_{11})}{4 \cdot Im(Y_{12})^2}. \tag{8}$$

Since these 430 devices have various L, W_f, N_f, and M values, for the purpose of comparison between different methods, we define the normalized gate resistance R_{gnor} (Ω/□) by

$$R_{\mathrm{gnor}} = R_g \cdot \left(\frac{L \cdot N_f \cdot M}{W_f}\right). \tag{9}$$

Please note that the normalized gate resistance R_{gnor} is not the same as the sheet resistance R_{gsh} of the distributed poly-silicon resistance R_{gpoly} because the extracted R_g still consists of the distributed channel resistance R_{ch} and the gate contact resistance R_{gcon}. Fig. 4 shows the normalized histograms (normalized to 430) of R_{gnor} obtained

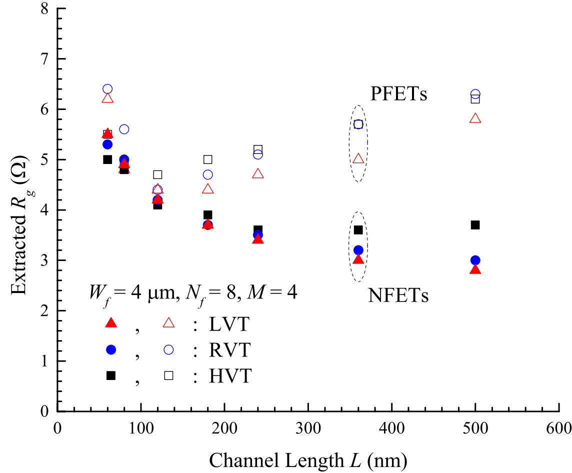

Fig. 5. Extracted R_g versus channel length characteristics for devices with $W_f = 4$ μm, $N_f = 8$, and $M = 4$ biased at $V_{\rm GS} = 1.1$ V and $V_{\rm DS} = 0$ V fabricated in a 55-nm node with LVT, RVT, and HVT processes, respectively.

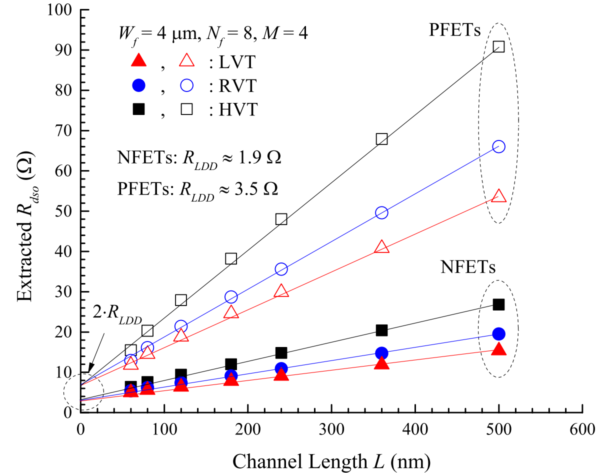

Fig. 6. Extracted channel resistance $R_{\rm dso}$ versus channel length characteristics for devices with $W_f = 4$ μm, $N_f = 8$, and $M = 4$ biased at $V_{\rm GS} = 1.1$ V and $V_{\rm DS} = 0$ V fabricated in a 55-nm node with LVT, RVT, and HVT processes, respectively.

by our proposed method and other methods presented in [13] [Fig. 4(b)], [14], [21] [Fig. 4(c)], and [20] [Fig. 4(d)]. We observed that for our proposed method, 86% of the extracted $R_{\rm gNOR}$ (i.e., 370 samples) falls in between 0 and 35 Ω/□, while 38.8% (167 samples) for the method in [13], 34.9% (150 samples) for the approach in [14] and [21], and 42.3% (182 samples) for the method in [20]. In addition, among all the methods, our proposed approach gives the fewest counts for the negative $R_{\rm gnor}$, which is physically incorrect. Therefore, our proposed extraction procedure is statistically most stable and robust among all of the published methods in the literature. Please note that due to the NQS effect resulted from the distributed channel resistance $R_{\rm ch}$, the count distribution of the normalized $R_{\rm gnor}$ in the histogram is affected by the technology node and the device geometry.

To evaluate the impact of the NQS effect on the R_g extraction, one way is to plot the extracted R_g as a function of channel length [16]. Cheng and Matloubian [16] already investigated the bias and geometry dependence of the NQS effect on the extracted R_g. In this paper, we want to investigate its dependence on processes. It is well known that the distributed poly-silicon gate resistance $R_{\rm gpoly}$ is proportional to W_f/L [12], while the distributed channel resistance $R_{\rm ch}$ is proportional to L/W_f [16]. Therefore, the impact of the NQS effect becomes dominant when the extracted R_g starts to increase with the channel length. On the other hand, for both n- and p-type FETs, different implants were used to change the threshold voltage $V_{\rm TH}$ and therefore resulted in different $R_{\rm dso}$ (or $R_{\rm ch}$). If $R_{\rm gpoly}$ is dominant, we do not expect that the implants will affect the extracted R_g. However, if $R_{\rm ch}$ is dominant, the extracted R_g will vary monotonically with channel implants. Fig. 5 shows the extracted R_g versus channel length characteristics for devices with $W_f = 4$ μm, $N_f = 8$, and $M = 4$ biased at $V_{\rm GS} = 1.1$ V and $V_{\rm DS} = 0$ V fabricated in a 55-nm technology node with low $V_{\rm TH}$ (LVT), regular $V_{\rm TH}$ (RVT), and high $V_{\rm TH}$ (HVT) processes. We observed that p-type FETs suffer from the NQS effect more than the n-type FETs, and therefore the extracted R_g increases at a much shorter channel length (around 120 nm in this paper). This is because, p-type FETs have a higher channel resistance $R_{\rm dso}$ as demonstrated in Fig. 6. For n-type FETs, we observed that RVT and LVT processes have lower channel resistance $R_{\rm dso}$, and therefore the channel length dependence of their extracted R_g follows the trend of $R_{\rm gpoly}$ for the devices studied in this paper. In addition, the extracted R_g values are about the same for devices with the same dimension fabricated in RVT and LVT processes. In Fig. 6, if we extrapolate the extracted $R_{\rm dso}$ down to $L = 0$ nm, we can extract the resistance $R_{\rm LDD}$ in the LDD region at the source (or drain) side, which gives 1.9 Ω and 3.5 Ω for n- and p-type FETs, respectively. Higher channel resistance $R_{\rm dso}$ also results in lower critical frequency f_c as shown in Fig. 7 and therefore reduces the accuracy of the extracted R_g. This can be observed from the lower than expected R_g extracted using $L = 0.24$ μm, 0.36 μm, and 0.5 μm p-type HVT FETs shown in Fig. 5.

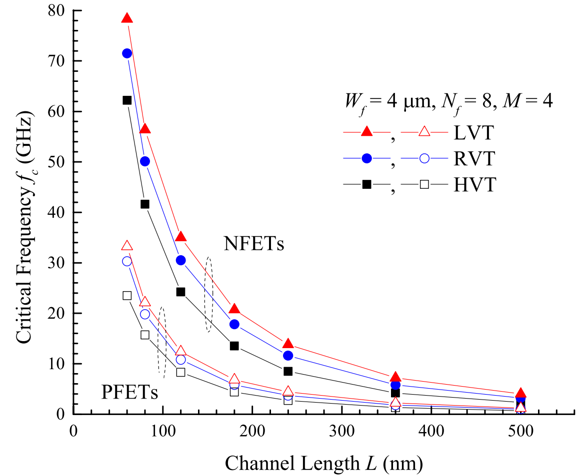

Fig. 7. Critical frequency f_c versus channel length characteristics for devices with $W_f = 4$ μm, $N_f = 8$, and $M = 4$ biased at $V_{\rm GS} = 1.1$ V and $V_{\rm DS} = 0$ V fabricated in a 55-nm node with LVT, RVT, and HVT processes, respectively.

For future technology node using high-κ metal gate, the gate-stack combination is more complex than Poly/SiON's and therefore results in higher gate resistance R_{gmetal} than R_{gpoly}. However, this is beneficial to our extraction algorithm to avoid the NQS effect and enhance the extraction accuracy when using the same device geometry.

IV. Conclusion

An improved z-parameter based approach to extract the gate resistance at low frequencies is presented. This improved extraction method demonstrated its statistical stability and robustness compared with all of the published methods in the literature. Its statistical robustness and stability are particularly important for the future technology nodes with smaller feature size and larger process variations. Finally, we observed that for a given device geometry, n-type FETs fabricated in the RVT or LVT processes are more suitable for the gate resistance extraction because of their relatively lower channel resistance compared with p-type FETs or the HVT process.

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