Extraction of MOSFET Threshold Voltage, Series Resistance, Effective Channel Length, and Inversion Layer Mobility From Small-Signal Channel Conductance Measurement

F. C. J. Kong, Y. T. Yeow, *Senior Member, IEEE*, and Z. Q. Yao, *Member, IEEE*

***Abstract*—This paper proposes and demonstrates the extraction of MOSFET threshold voltage, source-drain resistance, gate field mobility reduction factor, and transistor gain factor from the measurement of the small-signal source-drain conductance of a transistor as a function of dc gate bias with zero dc drain bias. The theory is based on the analytical model that includes the effects of source-drain resistance and gate-induced mobility reduction. It is shown that, by measuring devices of different drawn gate lengths, effective channel lengths and actual mobility can also be extracted. The results obtained are compared with those obtained by other measurement methods.**

***Index Terms*—MOSFET threshold voltage, parameter extraction, source/drain resistance.**

I. Introduction

THRESHOLD voltage, inversion layer carrier mobility, source and drain series resistance, together with device dimensions, form the major parameters of the SPICE-based submicrometer MOSFET circuit model used in the circuit simulation of MOS integrated circuits. The MOSFET circuit model itself is developed from the analytical model for the drain current (as a function of gate and drain bias) based on the well-known gradual channel analysis of the inversion layer conduction [1]. These SPICE parameters are extracted from different measurements based on the circuit model. The most common measured quantity used for parameter extraction is the dc drain current [2]; more recently, small-signal interelectrode capacitance measurements are also used [3], [4]. Each measurement technique has its advantages and limitations; some are aimed at determination of a single parameter, while others yield a number of parameters simultaneously. Simplicity of measurement and parameter extraction, adaptability to changes in technology, and applicability of the extracted parameters (in terms of variation in device dimensions and bias voltage range) are factors affecting the choice of measurement techniques in practice.

In this paper, we describe a novel and simple method for accurate extraction of threshold voltage $V_{\rm T}$, gain factor β, gate bias mobility lowering factor θ, and source/drain series resistance $R_{\rm T}$ of a MOSFET from a single measurement of the small-signal ac drain-source conductance $g_{\rm ds}$, as a function of dc gate bias. As with other SPICE parameter extraction measurements, it is derived from the standard gradual channel theory analysis for $I_{\rm d}\,(V_{\rm ds}, V_{\rm gs})$ used in SPICE. The measurement uses only a small (~ 10 mV rms) ac signal applied to the drain. With zero dc drain bias, effects such as channel length modulation, drain-induced barrier lowering (DIBL), and carrier velocity saturation on the above four parameters are eliminated.

By carrying out the same measurement for devices with different drawn gate lengths, the method also allows the extraction of the effective channel lengths of the devices and the effective inversion layer mobility.

II. Theory of Proposed Parameter Extraction

The intrinsic small-signal conductance between source and drain of a MOSFET can be derived directly from the dc drain current equation based on gradual channel approximation

$$g_{\rm ds} = \left[\frac{dI_{\rm ds}}{dV_{\rm ds}}\right]_{{\rm const}V_{\rm gs}} = \left[\frac{d}{dV_{\rm ds}}\left(\frac{\mu_{\rm eff}C_{\rm ox}W_{\rm eff}}{L_{\rm eff}} \times \left(V_{\rm gs} - V_{\rm T} - \frac{V_{\rm ds}}{2}\right)V_{\rm ds}\right)\right]_{{\rm const}V_{\rm gs}} \tag{1}$$

where

$C_{\rm ox}$ gate oxide capacitance per unit area;
$\mu_{\rm eff}$ low field effective inversion layer mobility;
$W_{\rm eff}$ effective channel width;
$L_{\rm eff}$ effective channel length.

In the measurement described below, zero drain bias is used, i.e., $V_{\rm ds} = 0$. This gives the intrinsic $g_{\rm ds}$ as

$$g_{\rm ds} = \frac{\mu_{\rm eff}C_{\rm ox}W_{\rm eff}}{L_{\rm eff}}\,(V_{\rm gs} - V_{\rm T}) = \beta\,(V_{\rm gs} - V_{\rm T}) \tag{2}$$

where

$$\beta = \frac{\mu_{\rm eff}C_{\rm ox}W_{\rm eff}}{L_{\rm eff}}.$$

Manuscript received May 29, 2001; revised August 21, 2001. The review of this paper was arranged by Editor R. Singh.

F. C. J. Kong and Y. T. Yeow are with the School of Computer Science and Electrical Engineering, The University of Queensland, Brisbane, QLD 4072, Australia (e-mail: kong@csee.uq.edu.au).

Z. Q. Yao is with Cypress Semiconductor, San Jose, CA 95134 USA.

Publisher Item Identifier S 0018-9383(01)10134-6.

In actual measurement, the source-drain resistance R_{T}, being in series with the channel resistance, is included in the small-signal conductance measured between source and drain. Hence, the measured small-signal conductance g_{dsm} is

$$g_{\mathrm{dsm}} = \frac{1}{R_{\mathrm{T}} + \frac{1}{\beta(V_{\mathrm{gs}} - V_{\mathrm{T}})}}. \tag{3}$$

In SPICE-based modeling, low field inversion mobility is most commonly modeled as being dependent on V_{gs} according to the functional form [5]

$$\mu_{\mathrm{eff}} = \frac{\mu_0}{1 + \theta\,(V_{\mathrm{gs}} - V_{\mathrm{T}})} \tag{4}$$

where μ_0 is the zero gate field mobility and θ is the gate-field mobility reduction factor. When the gate-field dependent expression for μ_{eff} is introduced into the small-signal conductance equation, we get

$$g_{\mathrm{dsm}} = \frac{\beta_0\,(V_{\mathrm{gs}} - V_{\mathrm{T}})}{1 + (\theta + \beta_0 R_{\mathrm{T}})\,(V_{\mathrm{gs}} - V_{\mathrm{T}})} \tag{5}$$

where

$$\beta_0 = \frac{\mu_0 C_{\mathrm{ox}} W_{\mathrm{eff}}}{L_{\mathrm{eff}}}.$$

When g_{dsm} is measured as function of V_{gs}, the results can theoretically be used as the target function to extract the values of the parameters V_{T}, R_{T}, β_0, and θ simultaneously by parameter optimization to fit (5) to the experimental data. Rather than doing this, we make use of the fact that the function $g_{\mathrm{dsm}}/\sqrt{dg_{\mathrm{dsm}}/dV_{\mathrm{gs}}}$ is a linear function in V_{gs} in which the two parameters R_{T} and θ are eliminated

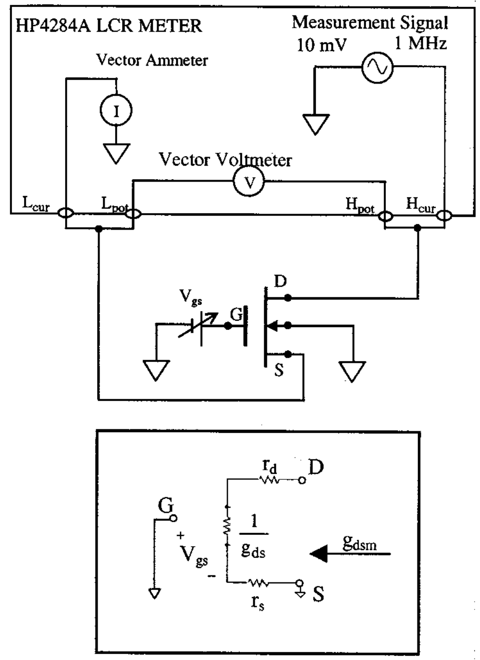
$$\frac{g_{\mathrm{dsm}}}{\sqrt{\frac{dg_{\mathrm{dsm}}}{dV_{\mathrm{gs}}}}} = \sqrt{\beta_0}\,(V_{\mathrm{gs}} - V_{\mathrm{T}})\,. \tag{6}$$

This allows for the use of simple straight-line fit to the numerically derived experimental quantity $g_{\mathrm{dsm}}/\sqrt{dg_{\mathrm{dsm}}/dV_{\mathrm{gs}}}$ to extract V_{T} and β_0 for a given device. The proposed procedure for the extraction of V_{T} from experimental data is simpler than other existing methods such as those in [2] and [6], essentially due to the avoidance of the use, and hence also the influence of, dc drain bias. After having determined V_{T} and β_0, the two remaining parameters R_{T} and θ are extracted by optimization to fit (5) to the measured data g_{dsm}.

By carrying out the above measurement and extraction procedure for devices with different drawn gate lengths L_{drawn}s, fabricated by the same technology, we obtain the experimental data β_0 as a function of L_{drawn}. Adopting the standard relationship between drawn length and effective length of $L_{\mathrm{eff}} = (L_{\mathrm{drawn}} - \Delta L)$ [7], where ΔL taken as a constant, we get

$$\beta_0 = \frac{\mu_0 C_{\mathrm{ox}} W_{\mathrm{eff}}}{L_{\mathrm{drawn}} - \Delta L}. \tag{7}$$

The preceeding equation is the basis of the $1/\beta$ method [8]: $1/\beta_0$ is plotted against L_{drawn} for the determination of ΔL and μ_0 (using known values for W_{eff} and C_{ox}) from the x-axis intercept and slope, respectively, of the best-fit straight line for the experimental data.



(a)

(b)

Fig. 1. (a) Schematic diagram for the measurement of g_{ds} and (b) small-signal equivalent circuit of transistor with zero drain bias.

III. MEASUREMENT

Small-signal conductance g_{dsm} can be measured directly using an LCR meter. Fig. 1(a) shows the schematic diagram of the measurement circuit. The HP4284 LCR meter applies a test signal of 10 mV rms at 1 MHz at the drain and the signal current is sensed at the grounded source. Voltage sources of a HP 4145A parameter analyzer are used to provide the necessary gate and substrate bias. Fig. 1(b) shows the small-signal equivalent circuit of the measurement. With dc bias V_{ds} set at zero, there is no drain current and hence no dc voltage drop across the source and drain resistances r_{s} and r_{d} ($r_{\mathrm{s}} = r_{\mathrm{d}} = R_{\mathrm{T}}/2$). Devices under test are LDD n-channel MOSFETs with drawn length ranging from 0.4 to 20 μm, oxide thickness of 10 nm, and W_{eff} of 20 μm. The experimental g_{dsm} is used to extract parameters according to the theory described above.

Chern's method [7] for the extraction of R_{T} and ΔL requires the measurement of the resistance between source and drain R_{M} as a function of V_{gs} for a number of devices with different drawn lengths. Other than the fact that R_{M} is typically derived from dc measurement, it is the reciprocal of the small-signal quantity g_{dsm} we measured. Thus, the same set of data can be processed by Chern's method to extract L_{eff} and R_{T} for comparison with the values extracted by the proposed method. The only difference is that in Chern's method, a single R_{T} is extracted from a set of measured drain-source resistances for devices with different drawn gate lengths, whereas in the proposed method, one value of R_{T} is extracted for each device measured. The V_{T} extracted by the proposed method for each device is used in Chern's method. For comparison purposes, V_{T}s are also

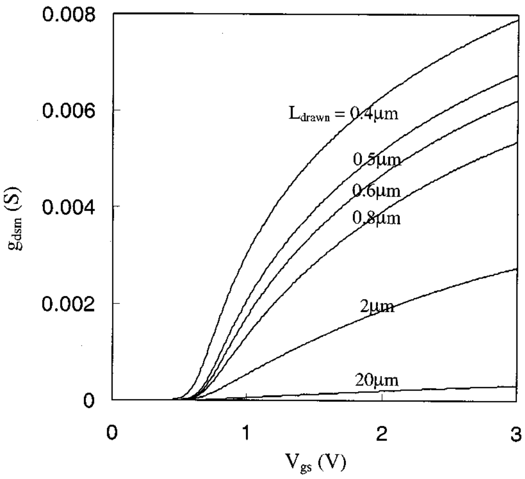


Fig. 2. Measured source-drain conductance g_{dsm} as a function of gate bias V_{gs} for nMOSFETs with different drawn gate lengths L_{drawn}.

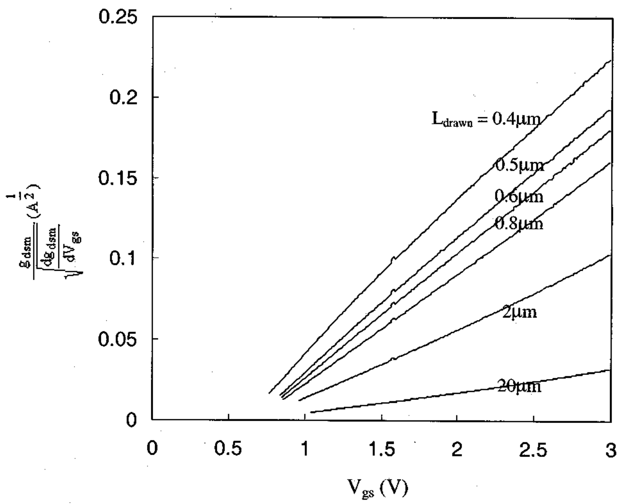


Fig. 3. $g_{\mathrm{dsm}}/\sqrt{dg_{\mathrm{dsm}}/dV_{\mathrm{gs}}}$ from Fig. 2 as a function of gate bias V_{gs} for devices different drawn gate lengths L_{drawn}. The slope and V_{gs} intercept of each best fit straight line for each device yields $\sqrt{\beta_0}$ and V_{T} for the device.

extracted from dc $I_{\mathrm{d}} - V_{\mathrm{gs}}$ measurement by the linear extrapolation method [2].

IV. Results and Discussion

Fig. 2 shows the experimental g_{dsm} as a function of V_{gs} for $L_{\mathrm{drawn}} = 0.4$ to 20 μm. Fig. 3 shows $g_{\mathrm{dsm}}/\sqrt{dg_{\mathrm{dsm}}/dV_{\mathrm{gs}}}$ versus V_{gs} derived from Fig. 2 with $dg_{\mathrm{dsm}}/dV_{\mathrm{gs}}$ calculated using central finite difference. According to (6), the x-axis intercept and slope of the best straight line fit of the data for each device in Fig. 3 yield the V_{T} and $\sqrt{\beta_0}$, respectively, for that device. The extracted V_{T}s as a function of L_{drawn} is shown in Fig. 4. The 95%-confidence intervals of V_{T} obtained by standard linear regression analysis are shown as error bars in the figure. For all drawn lengths the spread is within 3% of the extracted value. In the same figure, we also show V_{T} extracted from $I_{\mathrm{d}} - V_{\mathrm{gs}}$ measurement by the linear extrapolation method [2]. The difference is less than 50 mV.

Next, we proceeded to extract the values of R_{T} and θ for each device by fitting (5) into the corresponding data in Fig. 2. The extracted values of V_{T}, β_0, R_{T}, and θ for each device are tabulated in Table I (values in parentheses are results obtained by other methods). Theoretically, R_{T} and θ are independent of gate length. This is seen to be the case for results obtained by independent parameter optimization on data measured on devices with different L_{drawn}.

As indicated in the Section II, $1/\beta_0$ is next plotted against L_{drawn} to extract μ_0 and ΔL and hence also L_{eff}. This is shown in Fig. 5, giving $\Delta L = 0.09$ μm and $\mu_0 = 465$ cm^{2}V^{-1}s^{-1}

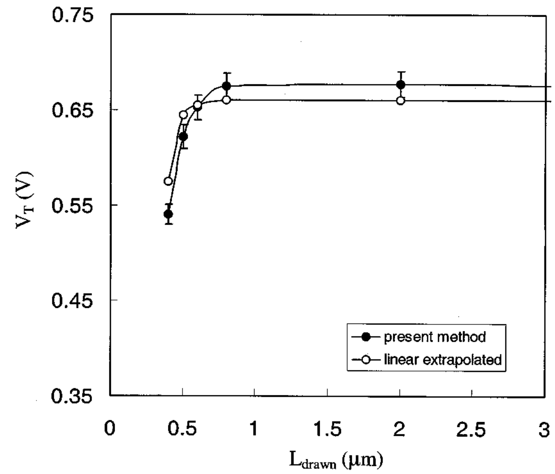


Fig. 4. Extracted threshold voltage, V_{T} as a function of drawn gate lengths L_{drawn}. "o" by linear extrapolation method [2] and "•" by present method. Error bars show the 95%-confidence intervals of V_{T} by the present method.

TABLE I
TABLE OF EXTRACTED PARAMETERS FOR DEVICES WITH DIFFERENT L_{drawn} BY PRESENT METHOD. VALUES IN PARENTHESES ARE VALUES EXTRACTED BY OTHER METHODS (SEE TEXT FOR DETAILS)

L_{drawn} (μm)	V_T (V)	β_o (mA/V^2)	θ (V^{-1})	R_T (ohms)	μ_o (cm^{2}V^{-1}s^{-1})	L_{eff} (μm)
0.4	0.52 (0.58)	8.55	0.11	64.2 (68.0)	465	0.31 (0.32)
0.5	0.62 (0.65)	6.75	0.12	65.0 (68.0)	465	0.41 (0.42)
0.6	0.65 (0.66)	5.96	0.11	65.0 (68.0)	465	0.51 (0.52)
0.8	0.67 (0.66)	4.74	0.10	65.0 (68.0)	465	0.71 (0.72)
2.0	0.68 (0.67)	1.79	0.11	64.9 (68.0)	465	1.91 (1.92)
20	0.70 (0.69)	0.16	0.12	65.0 (68.0)	465	19.9 (19.9)

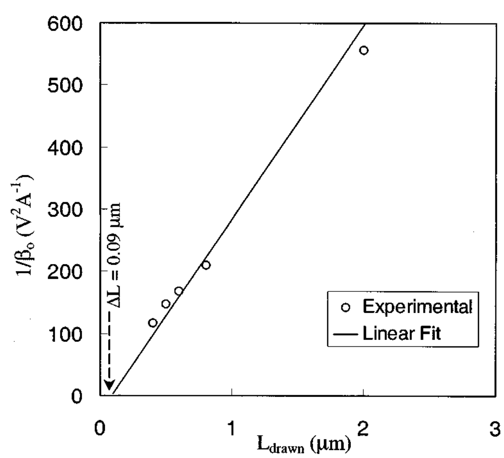


Fig. 5. Plot of experimentally determined $1/\beta_0$ versus L_{drawn} as points. Line is best straight line fit. Intercept on L_{drawn} axis yields ΔL. Slope of the line yields $(1/(\mu_0 C_{\mathrm{ox}} W_{\mathrm{eff}}))$ from which zero field mobility μ_0 is determined using known gate oxide thickness and device width.

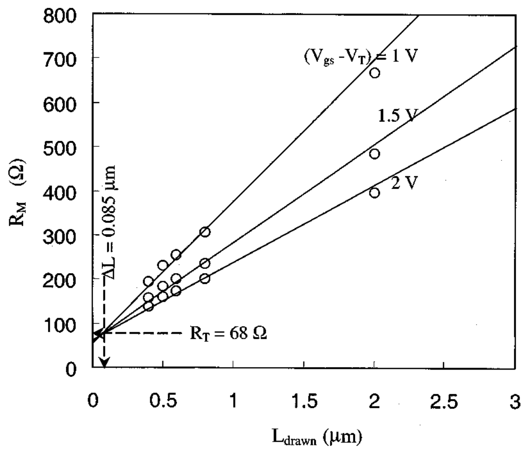


Fig. 6. Plot of measured channel resistance $R_{\rm M}(=1/g_{\rm dsm})$ versus $L_{\rm drawn}$ at different $(V_{\rm gs}-V_{\rm T})$ for extraction of $R_{\rm T}$ and ΔL by Chern's method.

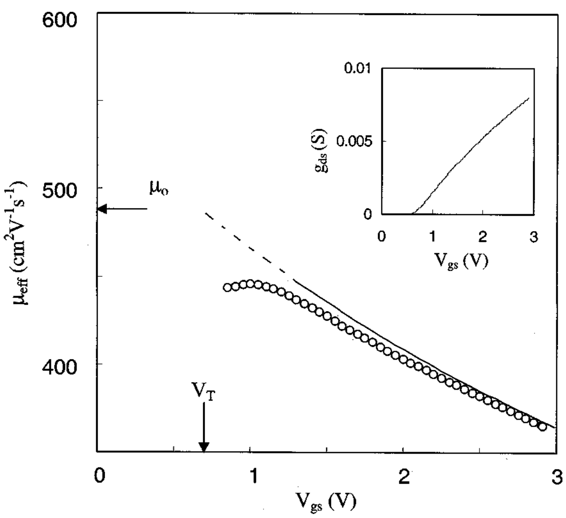


Fig. 7. Effective inversion layer mobility $\mu_{\rm eff}$ for device with $L_{\rm drawn} = 0.8\ \mu$m. Points are values extracted from intrinsic $g_{\rm ds}$ using (2), full line is calculated values from (4) using extracted μ_0 and θ, dotted line is the extrapolation of (4) to $V_{\rm gs} = V_{\rm T}$. The inset shows the intrinsic $g_{\rm ds}$ extracted from experimental $g_{\rm dsm}$.

using the values of $W_{\rm eff} = 20\,\mu$m and $t_{\rm ox} = 10$ nm and $L_{\rm eff}$s are included in Table I. For comparison, Chern's method mentioned is carried out using $R_{\rm M}(=1/g_{\rm dsm})$. Results are shown in Fig. 6 for $(V_{\rm gs}-V_{\rm T}) = 1$, 1.5, and 2 V. The plot yields $R_{\rm T} = 68\ \Omega$ and $\Delta L = 0.085\ \mu$m. These results are shown in parentheses in the corresponding columns in Table I. It is seen that both parameters are in good agreement with the corresponding values determined by the present method.

Inversion layer mobility for MOSFET as a function of gate bias $\mu_{\rm eff}(V_{\rm gs})$ is usually extracted directly from the intrinsic channel conductance $g_{\rm ds}$ [2]. The inset in Fig. 7 shows the $g_{\rm ds}$ for the 0.8-μm device obtained from $g_{\rm dsm}$ data by the equation: $g_{\rm ds} = 1/((1/g_{\rm dsm}) - R_{\rm T})$. Using extracted $g_{\rm ds}$, $L_{\rm eff}$, $V_{\rm T}$, and the assumed values for $C_{\rm ox}$ and $W_{\rm eff}$, we obtained $\mu_{\rm eff}(V_{\rm gs})$ from (2). This is shown as points in Fig. 7. It shows the typical dropping off of $\mu_{\rm eff}$ with reducing $V_{\rm gs}$ just above threshold observed in measurement using (2). This is attributed to the failure near $V_{\rm T}$ of the assumption that inversion layer charge $= C_{\rm ox}(V_{\rm gs}-V_{\rm T})$ [2]. The extracted μ_0 and θ should also yield

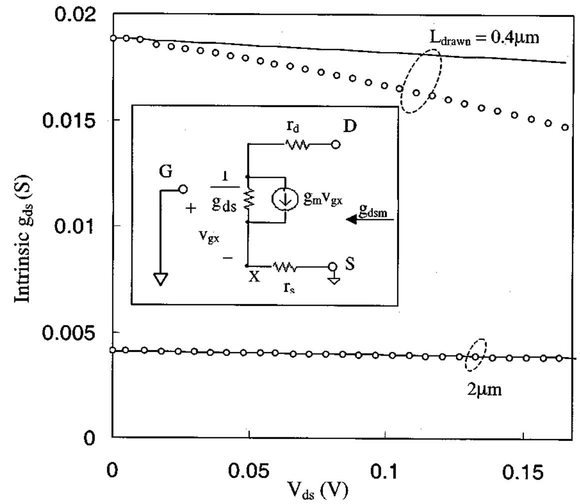


Fig. 8. Intrinsic $g_{\rm ds}$ as a function of dc drain bias, $V_{\rm ds}$ with $(V_{\rm gs}-V_{\rm T}) = 3$ V for $L_{\rm drawn} = 0.4$ and $2\,\mu$m. Points are experimental results extracted from measured $g_{\rm dsm}$ and lines are calculated results using (10). The inset shows the small-signal equivalent circuit with nonzero drain bias.

mobility through (4). The full line in Fig. 7 shows the calculated $\mu_{\rm eff}(V_{\rm gs})$ obtained for the range of $V_{\rm gs}$ where the experimental $g_{\rm dsm}$ are used in our extraction process. Since the difference between the two sets of $\mu_{\rm eff}(V_{\rm gs})$ is within 2% for this range of $V_{\rm gs}$, the dotted line which is the extrapolation (4) should be a good prediction of the actual mobility down to $V_{\rm gs} = V_{\rm T}$.

Extraction methods based on dc $I_{\rm d}$ measurement requires the application a small dc drain bias $V_{\rm ds}$, typically 50 mV–100 mV. This bias leads to nonuniformity of the inversion layer along the channel as well as other longitudinal field-induced effects such as mobility reduction, channel length modulation and DIBL. By measuring small-signal $g_{\rm dsm}$ with dc drain offset we can monitor these effects in devices with different channel lengths. We extracted the intrinsic $g_{\rm ds}$ as a function of $V_{\rm ds}$ offset between 0 and 200 mV for $L_{\rm drawn} = 0.4$ and $2\,\mu$m when the devices are in the linear region of operation. Due to the presence of dc drain current, the effective or the intrinsic dc $V_{\rm ds}$ and $V_{\rm gs}$ are less than the applied biases. We account for this by monitoring the drain current and subtracting the ohmic drops across the source and drain resistances. Also due to the ac negative feedback (see inset of Fig. 8 for equivalent circuit) of the source resistance, the intrinsic $g_{\rm ds}$ has to be extracted from the measured quantity $g_{\rm sdm}$ by

$$\frac{1}{g_{\rm ds}} = (1 + g_m r_{\rm s})\left(\frac{1}{g_{\rm dsm}} - R_{\rm T}\right) \tag{8}$$

where g_m is the transconductance at the given intrinsic bias and is obtained by

$$g_m = \frac{\beta_0}{1+\theta\,(V_{\rm gs}-V_{\rm T})} V_{\rm ds}. \tag{9}$$

Points in Fig. 8 show the intrinsic $g_{\rm ds}$ against intrinsic $V_{\rm ds}$ for the two devices at intrinsic $(V_{\rm gs}-V_{\rm T}) = 3$ V extracted from $g_{\rm dsm}$ according to (8). Based on the gradual channel model for device in the linear region of operation, $g_{\rm ds}$ at nonzero $V_{\rm ds}$ is

$$g_{\rm ds} = \frac{\beta_0}{1+\theta\,(V_{\rm gs}-V_{\rm T})}\,(V_{\rm gs}-V_{\rm T}-V_{\rm ds}). \tag{10}$$

It accounts for the gate bias-induced mobility reduction but not drain bias effects. Since β_0 and θ are known for each device, we can calculate the expected $g_{\rm ds}$. This is shown as dotted lines in Fig. 8 for the two devices. It is clear that for the shorter device even for the drain bias of 200 mV, the experimental $g_{\rm ds}$ is significantly lower than the calculated value at the same bias. For the longer channel device there is no observable difference between experimental and calculated data. The observed reduction for short device is clearly due to those drain bias-induced effects referred to above but not modeled in (10). This indicates that small-signal $g_{\rm ds}$ can be used to determine those SPICE parameters used to model drain bias-induced effects before and after saturation. This is currently being investigated.

V. Conclusion

We have proposed and demonstrated a new and yet simple method for the simultaneous extraction of the threshold voltage, gain factor, gate bias mobility lowering factor, and source/drain series resistance from the measurement of small-signal source-drain conductance of a single MOSFET. When the measurement is carried out for devices with different drawn lengths, it is possible to extract the effective channel lengths and the inversion layer mobility. Results obtained by this extraction procedure compare well with those determined by existing measurement methods. The main advantage of the method is the simplicity and accuracy of the measurement as well as the number of parameters that can be extracted from a single measurement.

By using small ac signal and avoiding any dc drain bias, the measurement method has eliminated the influence of drain bias on the extraction of these parameters that model gate field effects. The method should be applicable to sub-0.1-μm devices where the channel electrical properties are more sensitive to the presence of any drain bias. The method should also be directly applicable to SOI MOSFETs as the measurement deals only with the inversion layer independent of the presence or absence of electrical contact to the substrate layer.

We have also demonstrated that small-signal source-drain conductance is sensitive to the effects of small changes in dc drain bias and therefore would be a good candidate for use to extract SPICE parameters modeling the effects of drain bias.

References

[1] H. C. Pao and C. T. Sah, "Effects of diffusion current on characteristics of metal-oxide (insulator)-semiconductor transistors," *Solid-State Electron.*, vol. 9, pp. 927–937, Oct. 1966.

[2] D. K. Schroder, *Semiconductor Material and Device Characterization*. New York: Wiley, 1998, ch. 4.

[3] B. J. Sheu and P. K. Ko, "A capacitance method to determine the channel lengths for conventional and LDD MOSFETs," *IEEE Electron Device Lett.*, vol. EDL-5, pp. 491–493, Nov. 1984.

[4] M. M. Lau, C. Y. T. Chiang, Y. T. Yeow, and Z. Q. Yao, "A new method of threshold voltage extraction via MOSFET gate-to-substrate capacitance measurement," *IEEE Trans. Electron Devices*, vol. 48, pp. 1742–1744, Aug. 2001.

[5] K. Y. Fu, "Mobility degradation due to the gate field in the inversion layer of MOSFETs," *IEEE Electron Device Lett.*, vol. EDL-3, pp. 292–293, Oct. 1982.

[6] M. J. Deen and Z. X. Yan, "A new method for measuring the threshold voltage of small-geometry MOSFETs from subthreshold conduction," *Solid-State Electron.*, vol. 33, pp. 503–511, 1990.

[7] J. G. J. Chern, P. Chang, R. F. Motta, and N. Godinho, "A new method to determine MOSFET channel length," *IEEE Electron Device Lett.*, vol. EDL-1, pp. 170–173, Sept. 1980.

[8] K. K. Ng and J. R. Brews, "An assessment of methods to measure effective channel length of MOSFETs," *IEEE Circuits Devices Mag.*, vol. 6, pp. 33–38, 1990.

F. C. J. Kong was born in Sibu, Malaysia. He received the B.E. degree in electronics and communications from The University of Queensland, Brisbane, Australia, in 1994. Since 1998, he has been a Ph.D. student in the Department of Electrical and Computer Engineering at the same university. His research interests include the physics and numerical modeling of semiconductor devices.

Y. T. Yeow (M'76–SM'91) received the B.E. (Hons) degree from the University of Canterbury, Canterbury, New Zealand, the M.Sc. degree from University of Manchester, Manchester, U.K., and Ph.D. degree from University of Southampton, Southampton, U.K., 1975.

He is currently an Associate Professer in the School of Computer Science and Electrical Engineering, The University of Queensland, Australia. His teaching and research interests are in semiconductor device physics, electrical characterization, and numerical modeling.

Z. Q. Yao (S'94–M'95), photograph and biography not available at the time of publication.