Extraction of Separated Source and Drain Resistances in Amorphous Indium–Gallium–Zinc Oxide TFTs Through C–V Characterization

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***Abstract*—Considering asymmetry caused by layout, process, and device degradation, separate extraction of the source and drain resistances, i.e., R_S and R_D, respectively, from the total resistance $R_{\rm TOT}$ is very important in the design, modeling, and characterization of amorphous indium–gallium–zinc oxide (a-IGZO) thin-film transistors (TFTs). Due to the insulated gate structure, however, separate extraction is difficult through direct-current I–V characterization. In this letter, we propose a simple and useful technique for separate extraction of R_S from R_D in a-IGZO TFTs through a two-terminal parallel-mode C–V technique. We experimentally verified the validity of the proposed technique by comparing the result with the source-to-drain resistance from the I–V characteristics.**

***Index Terms*—Amorphous, drain resistance, nonlinear model, parameter extraction, parasitic resistance, source resistance, thin–film transistors (TFTs).**

I. Introduction

ZINC OXIDE (ZnO)-based thin-film transistors (TFTs) are under active research and development for active-matrix liquid crystal display and active-matrix organic light-emitting diode display backplanes [1], [2] due to their attractive properties such as high mobility, large-area uniformity, low-cost fabrication process at room temperature (RT), and compatibility with transparent flexible display applications compared with a-Si:H and low-temperature poly-Si TFTs. Among electrical properties, accurate modeling and separate extraction of series resistances of amorphous indium–gallium–zinc oxide (a-IGZO) TFTs are important in the characterization for long-term performance prediction and reliability assurance of TFT circuits and systems [3]–[10]. The asymmetric property of the source resistance R_S and the drain resistance R_D, which is caused by layout, process variation, and long-term device degradation, should be fully considered in the modeling for accurate characterization and robust design of integrated circuits. Based on the assumption of symmetric R_S and R_D, taking the half of the total resistance for the source and drain (S/D) resistances ($R_S = R_D = R_{\rm SD}/2$ at large $V_{\rm GS}$) is typical due to a difficulty in separate extraction. The transmission-line modeling method has been also used in a-IGZO TFTs, combining the output ($I_{\rm DS}$–$V_{\rm DS}$) characteristics with multiple devices [11], [12].

In this letter, considering any possible asymmetry in the S/D, we report a parallel-mode capacitance–voltage (PMCV) technique for separate extraction of R_S and R_D in individual a-IGZO TFTs through the gate-to-source terminal (I) and the gate-to-drain terminal (II) PMCV measurement. In this technique, R_S and R_D are separately extracted at a high-frequency region of the series RC model for a-IGZO TFTs.

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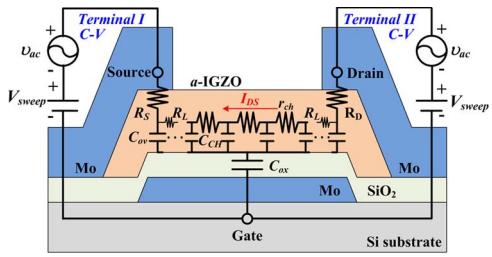

Fig. 1. Cross-sectional view and equivalent-circuit model, including gate-to-source and gate-to-drain C–V and drain-to-source I–V measurement configurations with parasitic R_S and R_D in a-IGZO TFTs.

II. C–V Technique for Separate Extraction of R_S and R_D

Cross-sectional view and an equivalent circuit for C–V and I–V (current–voltage) characterization of a-IGZO TFTs with gate capacitance $C_{\rm ox}$, channel capacitance per unit area $C_{\rm ch}$, and parasitic S/D resistances are shown in Fig. 1.

In separate extraction of the S/D resistances, frequency-dependent PMCV characteristics of a-IGZO TFTs are obtained for two different configurations in Fig. 1. As shown in the inset of Fig. 2(a), PMCV characterization through the impedance analyzer (HP 4284A) is employed for obtaining the experimental capacitance C_m and resistance R_m from the device under test. The admittance $Y_{\rm Sx}(\omega)$ of the equivalent-circuit model for the a-IGZO TFT can be converted through

$$Y_{\rm Sx}(\omega) = \frac{1}{R_{\rm Sx} + \frac{1}{j\omega C_{\rm Gx}}} = \frac{1}{R_{\rm Sx}} \frac{1}{1 + \frac{1}{(\omega C_{\rm Gx} R_{\rm Sx})^2}} + j \frac{\omega C_{\rm Gx}}{1 + (\omega C_{\rm Gx} R_{\rm Sx})^2}. \quad (1)$$

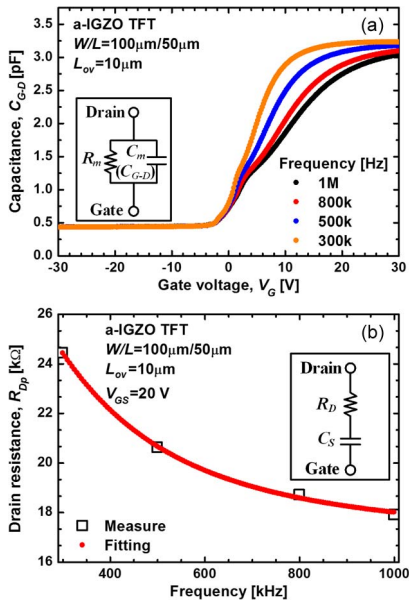

Fig. 2. (a) PMCV characteristics for the measurement configuration I of the a-IGZO TFTs with $W/L = 100\ \mu\text{m}/50\ \mu\text{m}$ and equivalent circuit in a parallel-mode ($C_m - R_m$) as an inset. (b) Frequency-dependent $1/[Y_m(\omega)|_{\text{real}}]$ at $V_{\text{GS}} = 20$ V.

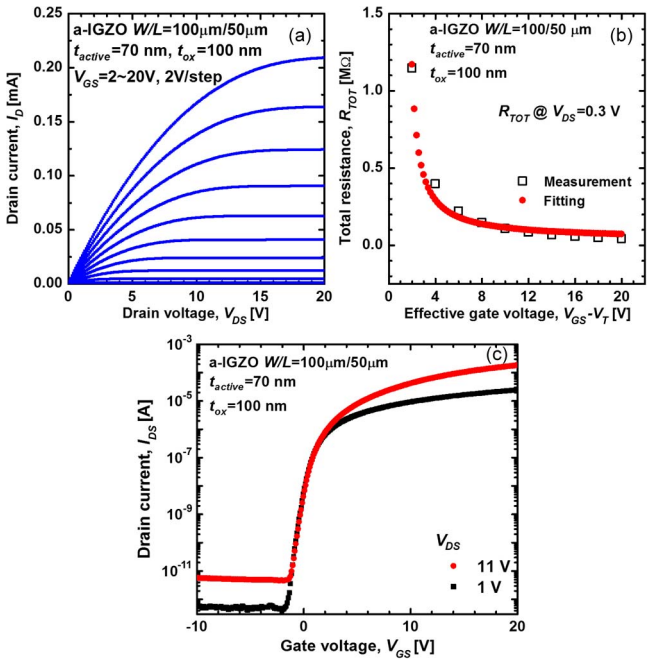

Fig. 3. (a) I_D–V_{DS} characteristics. (b) V_{GS}-dependent R_{TOT} at low V_{DS}. (c) I_D–V_{GS} characteristics of the a-IGZO TFT with $W/L = 100\ \mu\text{m}/50\ \mu\text{m}$.

It should be identical to the measured admittance $Y_m(\omega)$ as

$$Y_m(\omega) = \frac{1}{Z_m(\omega)} = \frac{1}{R_m} + j\omega C_m \tag{2}$$

with a dissipation factor $D_m = 1/\omega C_m R_m$ for a practical application to the extraction of parasitic resistances with the gate capacitance C_{Gx} in a-IGZO TFTs. Therefore, the series resistance R_{Sx} can be obtained from the real part of the measured admittance extrapolated to high frequency as

$$R_{\text{Sx}} = \lim_{\omega\to\infty}\left(\frac{1}{Y_m(\omega)|_{\text{real}}}\right) = \lim_{\omega\to\infty}\left(R_{\text{Sx}}\left(1+\frac{1}{(\omega C_{\text{Gx}} R_{\text{Sx}})^2}\right)\right). \tag{3}$$

For the measurement configurations I and II in the dispersive C–V characterization of a-IGZO TFTs, parasitic resistances are separately obtained through

$$R_S = \lim_{\omega\to\infty}\left(\frac{1}{Y_{m,I}(\omega)|_{\text{real}}}\right) = \lim_{\omega\to\infty}\left(R_S\left(1+\frac{1}{(\omega C_{\text{GS}} R_S)^2}\right)\right) \tag{4a}$$

$$R_D = \lim_{\omega\to\infty}\left(\frac{1}{Y_{m,\text{II}}(\omega)|_{\text{real}}}\right) = \lim_{\omega\to\infty}\left(R_D\left(1+\frac{1}{(\omega C_{GD} R_D)^2}\right)\right) \tag{4b}$$

for the frequency-independent R_S and R_D in series with the gate-to-source and gate-to-drain capacitances, i.e., C_{GS} and C_{GD}, respectively.

III. Experimental Results for Parasitic Source and Drain Resistances in a-IGZO TFTs

Cross-sectional view with an equivalent circuit for a-IGZO TFTs having a staggered bottom-gate structure is shown in Fig. 1. An a-IGZO active layer ($In_2O_3 : Ga_2O_3 : ZnO = 2{:}2{:}1$ at.%) is sputtered by radio-frequency magnetron sputtering at RT in a mixed Ar/O_2 and wet etched with a diluted HF to get the designed thickness ($T_{\text{IGZO}} = 70$ nm). Mo(200 nm) for the S/D is sputtered at RT and patterned by dry etching. The thickness T_{ox} of the gate oxide and the overlap L_{ov} between the gate and the S/D are processed to be $t_{\text{ox}} = 100$ nm and $L_{\text{ov}} = 10\ \mu$m, respectively, for various combinations of the gate length L and width W.

The threshold voltage and the subthreshold slope for the a-IGZO TFT with $W/L = 100\ \mu\text{m}/50\ \mu\text{m}$ were measured to be $V_T = 1.4$ V and SS = 500 mV/dec, respectively, from the I_D–V_{GS} characteristics shown in Fig. 3(c). Experimental PMCV characteristics for the configuration II (gate-to-drain) are shown in Fig. 2(a). C_{GD}–V_G characteristics in the accumulation regions for the two-terminal configuration show strong frequency-dependent dispersion over the frequency $f = 0.3-1.0$ MHz due to parasitic resistances and slow response of free charges. Fig. 2(b) shows R_D obtained from the a-IGZO TFT with $W/L = 100\ \mu\text{m}/50\ \mu\text{m}$. By the proposed PMCV technique through (4a) with measurement data for $V_{\text{GS}} = 2-20$ V, we obtained $R_D = 16.9$ kΩ extrapolating $V_{\text{GS}} \sim \infty$ in the gate-to-drain configuration. In the same way, the series resistance for the gate-to-source configuration is extracted to be $R_S = 16.0$ kΩ through (4b).

In order to verify the proposed PMCV technique for separate extraction of R_S and R_D, we performed I_D–V_{DS} measurement for the same a-IGZO TFT, as shown in Fig. 3(a). In the linear mode of operation under a small drain bias V_{DS}, considering the voltage drop across the parasitic resistances, the drain current is described by

$$I_D \cong \frac{\mu_{\text{eff}} C_{\text{ox}} W}{L_{\text{eff}}}\left[(V_{\text{GS}} - V_T)(V_{\text{DS}} - I_D(R_S + R_D)\right] \tag{5}$$

TABLE I
W- AND L-DEPENDENT PARASITIC RESISTANCES (NORMALIZED TO THE GATE WIDTH) EXTRACTED FROM THE PMCV TECHNIQUE FOR a-IGZO TFTs

***W*-dependent parasitic resistances in a-IGZO TFTs with *L*=50 μm**			
***W*/*L* [μm]**	**100**/50	**50**/50	**30**/50
V_T **[V]**	1.4	1.2	1.2
Parallel mode C-V technique			
R_S [kΩ·mm]	1.60	1.59	1.60
R_D [kΩ·mm]	1.69	1.72	1.41
R_S+R_D [kΩ·mm]	3.29	3.31	3.01
Channel resistance method			
R_{SD} [kΩ·mm]	3.54	3.45	3.27
PM C-V vs. CRM: $\Delta R_{SD} \equiv R_{SD}\|_{CRM} - (R_S+R_D)\|_{PMCV}$			
ΔR_{SD} [kΩ·mm]	0.24	0.14	0.26

***L*-dependent parasitic resistances in a-IGZO TFTs with *W*=100 μm**						
***W*/*L* [μm]**	100/**50**	100/**40**	100/**30**	100/**20**	100/**10**	100/**8**
V_T **[V]**	1.4	1.7	1.5	1.7	3.1	1.1
Parallel mode C-V technique						
R_S [kΩ·mm]	1.60	1.35	1.05	0.96	0.29	0.12
R_D [kΩ·mm]	1.69	1.47	1.09	1.01	0.38	0.15
R_S+R_D [kΩ·mm]	3.29	2.82	2.14	1.97	0.67	0.27
Channel resistance method						
R_{SD} [Ω·mm]	3.54	3.17	2.46	2.29	0.72	0.47
PM C-V vs. CRM: $\Delta R_{SD} \equiv R_{SD}\|_{CRM} - (R_S+R_D)\|_{PMCV}$						
ΔR_{SD} [Ω·mm]	0.24	0.35	0.32	0.32	0.05	0.20

where $\mu_{\rm eff}$ is the channel carrier mobility, and the effective channel length $L_{\rm eff} = L - \Delta L$, with ΔL as the channel length reduction. Therefore, the total source-to-drain resistance $R_{\rm TOT}$ can be obtained by

$$R_{\rm TOT}(V_{\rm GS}) \equiv \frac{V_{\rm DS}}{I_D} = R_{\rm SD} + \frac{L_{\rm eff}}{\mu_{\rm eff} C_{\rm ox} W (V_{\rm GS} - V_T)} = R_{\rm SD} + L_{\rm eff} \times r_{\rm ch} \quad (6)$$

with $R_{\rm SD} \equiv R_S + R_D$, including the intrinsic and extrinsic parts, and $r_{\rm ch}$ as a $V_{\rm GS}$-dependent channel resistance per unit length, which decreases with $V_{\rm GS}$.

Experimental results for the $V_{\rm GS}$-dependent $R_{\rm TOT}$ are shown in Fig. 3(b) for the channel resistance model (6) with measurement data for $V_{\rm GS} = 2{-}20$ V. As shown in Table I for various W/L combinations of a-IGZO TFTs, separated R_S and R_D/ (normalized to the gate width), through the proposed PMCV technique are comparatively summarized as a function of W and L, with $R_{\rm SD}$ obtained from the channel resistance method, which does not allow separation of R_S from R_D (see Table I). Extracted R_S with the gate length decreases due to a reduction of the $V_{\rm GS}$- and L-dependent intrinsic component of the parasitic resistance. We note that the difference, which is defined as $\Delta R_{\rm SD} = R_{\rm SD}|_{I-V} - (R_S + R_D)|_{\rm PMCV}$, of the parasitic resistances between the PMCV technique and the channel resistance method $\Delta R_{\rm SD}$ is almost constant for a-IGZO TFTs with the same gate width, whereas it is strongly dependent on the gate width for a-IGZO TFTs with length $L = 50$ μm. This difference is expected to be the intrinsic S/D resistance in the a-IGZO TFTs because there is only a difference from the voltage drop across the intrinsic S/D resistances.

We confirmed its usefulness for separate extraction of R_S and R_D with experimental results, fully considering asymmetries caused by the variations in the layout, process, and degradation.

IV. CONCLUSION

Separate extraction of the S/D resistances considering the asymmetry caused by the layout, process and device degradation, is very important in the design, modeling, and characterization of a-IGZO TFTs. We proposed a PMCV technique for separate extraction of R_S and R_D in a-IGZO TFTs by using a frequency- and gate bias-dependent C–V model. We verified the validity by comparing the result with the total source-to-drain resistance from the I–V characteristics in the linear region. This method allows separate extraction of parasitic R_S from R_D in each individual a-IGZO TFT without employing multiple devices with various W/L combinations.

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