Extraction of the Induced Gate Noise, Channel Noise, and Their Correlation in Submicron MOSFETs from RF Noise Measurements

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***Abstract*—An extraction method to obtain the induced gate noise ($\overline{i_g^2}$), channel noise ($\overline{i_d^2}$), and their cross correlation ($\overline{i_g i_d^*}$) in submicron MOSFETs directly from scattering and RF noise measurements has been presented and verified by measurements. In addition, the extracted induced gate noise, channel noise, and their correlation in MOSFETs fabricated in 0.18-μm CMOS process versus frequencies, bias conditions, and channel lengths are presented and discussed.**

***Index Terms*—Channel noise, cross-correlation noise, induced gate noise, noise of MOSFETs, RF noise extraction.**

I. Introduction

CURRENTLY, there is a trend to replace RF ICs with BJTs and GaAs FETs with deep submicron MOSFETs which have unity current-gain frequencies ($f_{\rm T}$) of several tens of gigahertz [1]. However, for many RF ICs, low noise performance is very important. Therefore, RF noise modeling of deep submicron MOSFETs is very important for devices used in the front-end transceivers. When transistors operate in the gigahertz range, the random potential fluctuations in the channel resulting in the channel noise will be coupled to the gate terminal through the gate oxide capacitance and cause the induced gate noise, which is usually correlated with the channel noise. Because of the difficulties in the extraction of the induced gate noise and its correlation term with the channel noise, several noise models [2], [3] and simulation results [4] have been presented, but they could not be verified directly with the noise sources obtained from RF noise measurements for deep submicron MOSFETs. Therefore, obtaining the noise currents directly from RF noise measurements is crucial for the high-frequency noise modeling of deep submicron MOSFETs.

In this paper, a systematic procedure to extract the induced gate noise ($\overline{i_g^2}$), channel noise ($\overline{i_d^2}$), and their cross correlation ($\overline{i_g i_d^*}$) directly from the S-parameter and RF noise parameter measurements is presented. With the help of the direct calculation technique [5], [6] for the noise parameters of transistors, the extracted noise currents are fed back to the equivalent noise model to calculate the noise parameters—minimum noise figure $NF_{\rm min}$, equivalent noise resistance $R_{\rm n}$, and optimized source reflection coefficient $\Gamma_{\rm OPT}$—and to compare them to the measured data for the verification of the extracted noise sources. After that, the extracted noise currents of the MOSFETs fabricated in a 0.18-μm CMOS process versus frequency, bias condition, and channel length are presented and discussed.

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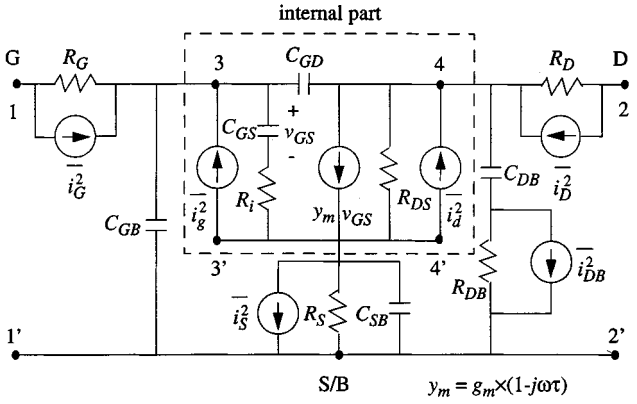

Fig. 1. RF noise model of an intrinsic MOSFET that is suitable for high-frequency circuit applications.

II. Procedure of Noise Extraction

Fig. 1 shows the noise model of an intrinsic MOSFET that is suitable for RF applications. It consists of two parts: an internal part (including $C_{\rm GS}$, $C_{\rm GD}$, R_i, g_m, $R_{\rm DS}$, $\overline{i_g^2}$ and $\overline{i_d^2}$) and an external part which includes all the components outside of the dashed box. After the devices and dummy structures, as described in [7], are fabricated, the induced gate noise, channel noise, and their correlation in MOSFETs can be extracted by using the following 15-step procedure.

Step 1) Measure the scattering parameters $\boldsymbol{S_{\rm DUT}}$, $\boldsymbol{S_{\rm OPEN}}$, $\boldsymbol{S_{\rm THRU1}}$ and $\boldsymbol{S_{\rm THRU2}}$ of the device-under-test (DUT), OPEN, THRU1, and THRU2 dummy structures, respectively.

Step 2) Measure the noise parameters $NF_{\rm min,DUT}$, $Y_{\rm opt,DUT}$, and $R_{\rm n,DUT}$ of the DUT.

Step 3) Perform a parameter de-embedding to get the intrinsic scattering ($\boldsymbol{Y}_{\mathbf{dev}}$) and noise parameters ($NF_{\min,\mathrm{dev}}$, $Y_{\mathrm{opt,dev}}$, and $R_{\mathrm{n,dev}}$) [7], [8].

Step 4) Perform a parameter extraction [9] based on $\boldsymbol{Y}_{\mathbf{dev}}$ and other measured data to get all the element values (e.g., g_m, C_{GS}, C_{GD}, etc.,) in the RF noise model.

Step 5) Calculate the correlation matrix $\boldsymbol{C}_{\boldsymbol{A}_{\mathbf{dev}}}$ of the transistor based on the intrinsic noise parameters by (1), shown at the bottom of the page, where k is Boltzmann's constant, T_o is the standard reference temperature (290 K), and the asterisk denotes the complex conjugate.

Step 6) Calculate the four-port admittance matrix $\boldsymbol{Y}_{\mathbf{extr}}$ of the extrinsic part in the RF transistor model by excluding C_{GS}, C_{GD}, g_m, R_{DS}, and R_i which define the intrinsic part and partition $\boldsymbol{Y}_{\mathbf{extr}}$ as [10]

$$\boldsymbol{Y}_{\mathbf{extr}} = \begin{bmatrix} \boldsymbol{Y}_{ee} & \boldsymbol{Y}_{ei} \\ \boldsymbol{Y}_{ie} & \boldsymbol{Y}_{ii} \end{bmatrix} \tag{2}$$

where the submatrixes $\boldsymbol{Y}_{ee}$, $\boldsymbol{Y}_{ei}$, $\boldsymbol{Y}_{ie}$, and $\boldsymbol{Y}_{ii}$ are 2×2 matrixes.

Step 7) Calculate the two-port admittance $\boldsymbol{Y}_{\mathbf{intr}}$ of the intrinsic part in the RF transistor model.

Step 8) Calculate the matrix $\boldsymbol{D}$ as follows:

$$\boldsymbol{D} = -\boldsymbol{Y}_{ei}(\boldsymbol{Y}_{ii} + \boldsymbol{Y}_{\mathbf{intr}})^{-1}. \tag{3}$$

Step 9) Convert the noise correlation matrix $\boldsymbol{C}_{\boldsymbol{A}_{\mathbf{dev}}}$ to its admittance form $\boldsymbol{C}_{\boldsymbol{Y}_{\mathbf{dev}}}$ by using

$$\boldsymbol{C}_{\boldsymbol{Y}_{\mathbf{dev}}} = \boldsymbol{T}_{\boldsymbol{Y}} \boldsymbol{C}_{\boldsymbol{A}_{\mathbf{dev}}} \boldsymbol{T}_{\boldsymbol{Y}}^{\dagger} \tag{4}$$

where the † in $\boldsymbol{T}_{\boldsymbol{Y}}^{\dagger}$ denotes Hermitian conjugation (transpose and complex conjugate) and the transformation matrix $\boldsymbol{T}_{\boldsymbol{Y}}$ is given by

$$\boldsymbol{T}_{\boldsymbol{Y}} = \begin{bmatrix} -Y_{11,\mathrm{dev}} & 1 \\ -Y_{21,\mathrm{dev}} & 0 \end{bmatrix}. \tag{5}$$

Step 10) Calculate the admittance noise correlation matrix $\boldsymbol{C}_{\boldsymbol{Y}_{\mathbf{extr}}}$ of the extrinsic part by [11]

$$\boldsymbol{C}_{\boldsymbol{Y}_{\mathbf{extr}}} = kT(\boldsymbol{Y}_{\mathbf{extr}} + Y_{\mathbf{extr}}^{\dagger}) \tag{6}$$

or

$$\boldsymbol{C}_{\boldsymbol{Y}_{\mathbf{extr}}} = 2kT\Re(\boldsymbol{Y}_{\mathbf{extr}}) \tag{7}$$

where T is the device temperature, $\Re()$ denotes for the real part of the matrix elements and partition $\boldsymbol{C}_{\boldsymbol{Y}_{\mathbf{extr}}}$ as

$$\boldsymbol{C}_{\boldsymbol{Y}_{\mathbf{extr}}} = \begin{bmatrix} \boldsymbol{C}_{ee} & \boldsymbol{C}_{ei} \\ \boldsymbol{C}_{ie} & \boldsymbol{C}_{ii} \end{bmatrix} \tag{8}$$

where the submatrixes $\boldsymbol{C}_{ee}$, $\boldsymbol{C}_{ei}$, $\boldsymbol{C}_{ie}$, and $\boldsymbol{C}_{ii}$ are 2×2 matrixes.

Step 11) Calculate the admittance correlation matrix $\boldsymbol{C}_{\boldsymbol{Y}_{\mathbf{intr}}}$ of the intrinsic part in the RF transistor model from

$$\begin{aligned} \boldsymbol{C}_{\boldsymbol{Y}_{\mathbf{intr}}} = {} & \boldsymbol{D}_i(\boldsymbol{C}_{\boldsymbol{Y}_{\mathbf{dev}}} - \boldsymbol{C}_{ee})\boldsymbol{D}_i^{\dagger} \\ & - \boldsymbol{C}_{ie}\boldsymbol{D}_i^{\dagger} - \boldsymbol{D}_i\boldsymbol{C}_{ei} - \boldsymbol{C}_{ii} \end{aligned} \tag{9}$$

where $\boldsymbol{D}_i = \boldsymbol{D}^{-1}$.

Step 12) Convert $\boldsymbol{Y}_{\mathbf{intr}}$ to its chain representation $\boldsymbol{A}_{\mathbf{intr}}$ using the conversion formula (10), shown at the bottom of the next page.

Step 13) Convert $\boldsymbol{C}_{\boldsymbol{Y}_{\mathbf{intr}}}$ to its chain matrix form $\boldsymbol{C}_{\boldsymbol{A}_{\mathbf{intr}}}$ by using

$$\boldsymbol{C}_{\boldsymbol{A}_{\mathbf{intr}}} = \boldsymbol{T}_A \boldsymbol{C}_{\boldsymbol{Y}_{\mathbf{intr}}} \boldsymbol{T}_A^{\dagger}, \tag{11}$$

where $\boldsymbol{T}_A$ is given by

$$\boldsymbol{T}_A = \begin{bmatrix} 0 & A_{12,\mathrm{intr}} \\ 1 & A_{22,\mathrm{intr}} \end{bmatrix}. \tag{12}$$

Step 14) Calculate the noise parameters $NF_{\min}$, Y_{opt}, and R_{n} of the intrinsic part in the RF transistor model from the noise correlation matrix $\boldsymbol{C}_{\boldsymbol{A}_{\mathbf{intr}}}$ by using (13)–(15), shown at bottom of the next page, where $\Im()$ stands for the imaginary part of elements and j is the imaginary unit.

Step 15) Calculate the power spectral density of the channel noise $\overline{i_d^2}$, induced gate noise $\overline{i_g^2}$, and their correlation $\overline{i_g i_d^*}$ from

$$\frac{\overline{|i_d|^2}}{\Delta f} = 4kT_o R_{\mathrm{n}} |Y_{21,\mathrm{intr}}|^2 \tag{16}$$

$$\begin{aligned} \frac{\overline{|i_g|^2}}{\Delta f} = {} & 4kT_o R_{\mathrm{n}} \\ & \times \left\{ |Y_{\mathrm{opt}}|^2 - |Y_{11,\mathrm{intr}}|^2 \right. \\ & \left. + 2\Re\left[(Y_{11,\mathrm{intr}} - Y_{\mathrm{cor}}) Y_{11,\mathrm{intr}}^* \right] \right\} \end{aligned} \tag{17}$$

and

$$\frac{\overline{i_g i_d^*}}{\Delta f} = 4kT_o (Y_{11,\mathrm{intr}} - Y_{\mathrm{cor}}) R_{\mathrm{n}} Y_{21,\mathrm{intr}}^* \tag{18}$$

$$\boldsymbol{C}_{\boldsymbol{A}_{\mathbf{dev}}} = 2kT_o \begin{bmatrix} R_{\mathrm{n,dev}} & \dfrac{NF_{\min,\mathrm{dev}} - 1}{2} - R_{\mathrm{n,dev}}(Y_{\mathrm{opt,dev}})^* \\ \dfrac{NF_{\min,\mathrm{dev}} - 1}{2} - R_{\mathrm{n,dev}} Y_{\mathrm{opt,dev}} & R_{\mathrm{n,dev}} |Y_{\mathrm{opt,dev}}|^2 \end{bmatrix} \tag{1}$$

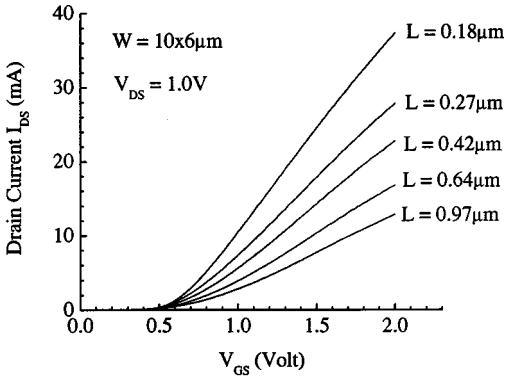

Fig. 2. Drain current ($I_{\rm DS}$) versus gate voltage $V_{\rm GS}$ characteristics for the n-type MOSFETs with channel width $W = 10 \times 6$ μm (10 fingers of width 6 μm) and lengths $L = 0.97$ μm, 0.64 μm, 0.42 μm, 0.27 μm and 0.18 μm, respectively, biased at a drain voltage $V_{\rm DS} = 1.0$ V.

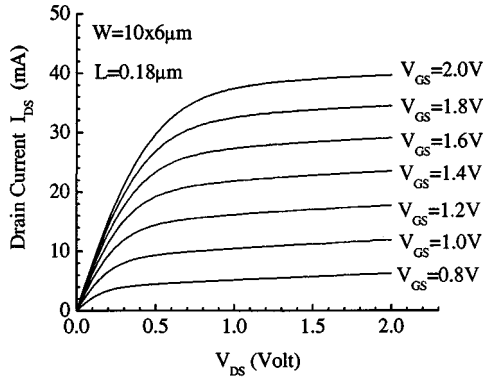

Fig. 3. Drain current ($I_{\rm DS}$) versus drain voltage $V_{\rm DS}$ characteristics for the n-type MOSFETs with channel width $W = 10 \times 6$ μm (10 fingers of width 6 μm) and lengths $L = 0.18$ μm biased at gate voltage $V_{\rm GS} = 0.8$ V, 1.0 V, 1.2 V, 1.4 V, 1.6 V, 1.8 V, and 2.0 V, respectively.

where $Y_{\rm cor}$ is given by

$$Y_{\rm cor} = \frac{NF_{\rm min} - 1}{2R_{\rm n}} - Y_{\rm opt}. \tag{19}$$

III. Measurements and Discussions

The devices-under-test (DUTs) are n-type MOSFETs with channel width $W = 10 \times 6$ μm (10 fingers) and lengths $L = 0.97$ μm, 0.64μm, 0.42 μm, 0.27 μm and 0.18 μm, respectively, fabricated by Conexant Systems, Inc., Newport Beach, CA. Measured data were obtained by using an ATN NP5B Noise and S-Parameter Measurement Systems (0.3$\sim$6 GHz). All the parasitic effects from probe pads and interconnections were de-embedded from the measured s-parameters using the procedure described in [7], [8]. Figs. 2 and 3 show the measured $I_{\rm DS}$ versus $V_{\rm GS}$ and $V_{\rm DS}$ characteristics to demonstrate the dc performance of the devices and Fig. 4 shows the unity gain frequency ($f_{\rm T}$) versus bias characteristics for different channel lengths. The $V_{\rm GS}$ bias at which the peak $f_{\rm T}$ occurs reduces when the channel length reduces and this trend makes MOSFETs suitable for low power RF circuit designs. The measured peak $f_{\rm T}$ of the 0.18 μm devices is about 45 GHz.

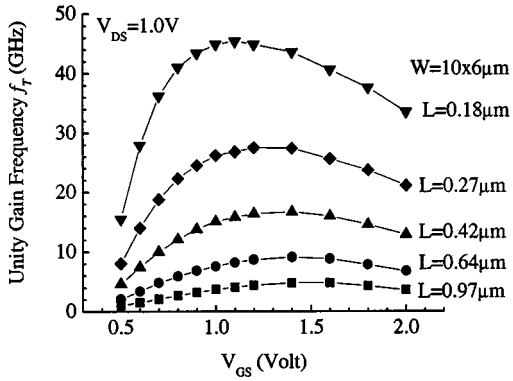

Fig. 4. Unity gain frequency ($f_{\rm T}$) versus $V_{\rm GS}$ characteristics from measured $|h_{21}|$ for the n-type MOSFETs with channel width $W = 10 \times 6$ μm (ten fingers of width 6 μm) and lengths $L = 0.97$ μm, 0.64 μm, 0.42 μm, 0.27 μm and 0.18 μm, respectively, biased at $V_{\rm DS} = 1.0$ V.

In the extraction procedure, the element values used in the RF noise model are crucial to obtain the power spectral density of the noise sources. They are directly obtained from the intrinsic y-parameters [9]. Fig. 5(a)–(d) show the measure (symbols) and simulated (lines) y-parameters of an n-type MOSFET with channel width $W = 10 \times 6$ μm (ten fingers) and length

$$\boldsymbol{A}_{\rm intr} = \frac{-1}{Y_{21,\rm intr}} \begin{bmatrix} Y_{22,\rm intr} & 1 \\ Y_{11,\rm intr}Y_{22,\rm intr} - Y_{12,\rm intr}Y_{21,\rm intr} & Y_{11,\rm intr} \end{bmatrix}. \tag{10}$$

$$NF_{\rm min} = 1 + \frac{1}{kT_o}\left(\Re(C_{12A,\rm intr}) + \sqrt{C_{11A,\rm intr}C_{22A,\rm intr} - (\Im(C_{12A,\rm intr}))^2}\right) \tag{13}$$

$$Y_{\rm opt} = \frac{\sqrt{C_{11A,\rm intr}C_{22A,\rm intr} - (\Im(C_{12A,\rm intr}))^2} + j\Im(C_{12A,\rm intr})}{C_{11A,\rm intr}} \text{ and} \tag{14}$$

$$R_{\rm n} = \frac{C_{11A,\rm intr}}{2kT_o} \tag{15}$$

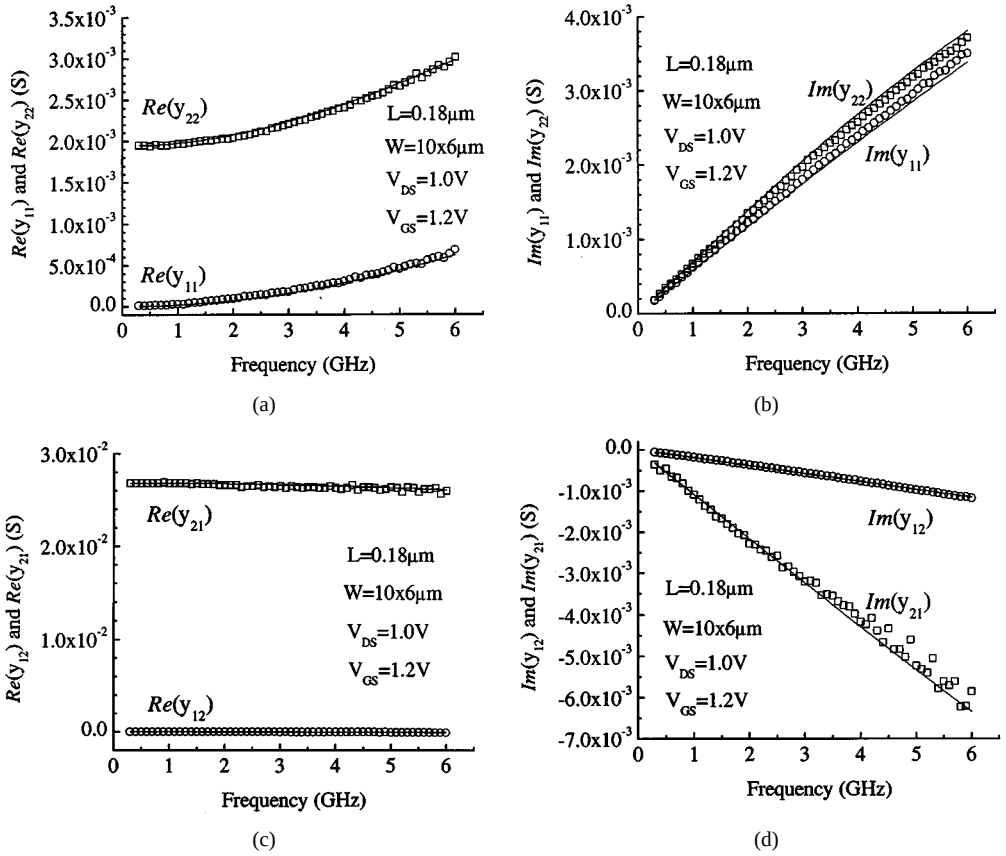

Fig. 5. (a) Measured (symbols) and simulated (lines) real parts of y_{11} and y_{22} versus frequency characteristics for the n-type MOSFET with the channel width $W = 10 \times 6\ \mu$m (ten fingers of width 6 μm) and length $L = 0.18\ \mu$m, biased at $V_{\rm DS} = 1.0$ V and $V_{\rm GS} = 1.2$ V, (b) measured (symbols) and simulated (lines) imaginary parts of y_{11} and y_{22} versus frequency characteristics for the n-type MOSFET with the channel width $W = 10 \times 6\ \mu$m (ten fingers of width 6 μm) and length $L = 0.18\ \mu$m biased at $V_{\rm DS} = 1.0$ V and $V_{\rm GS} = 1.2$ V, (c) measured (symbols) and simulated (lines) real parts of y_{12} and y_{21} versus frequency characteristics for the n-type MOSFET with the channel width $W = 10 \times 6\ \mu$m (ten fingers of width 6 μm) and length $L = 0.18\ \mu$m biased at $V_{\rm DS} = 1.0$ V and $V_{\rm GS} = 1.2$ V and (d) measured (symbols) and simulated (lines) imaginary parts of y_{11} and y_{22} versus frequency characteristics for the n-type MOSFET with the channel width $W = 10 \times 6\ \mu$m (10 fingers of width 6 μm) and length $L = 0.18\ \mu$m biased at $V_{\rm DS} = 1.0$ V and $V_{\rm GS} = 1.2$ V.

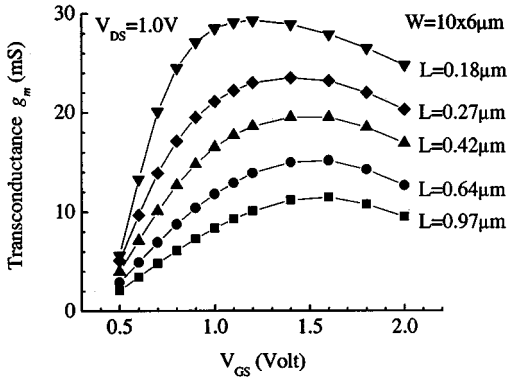

Fig. 6. Transconductance (g_m) versus $V_{\rm GS}$ characteristics extracted from measured Re(y_{21}) for the n-type MOSFETs with channel width $W = 10 \times 6\ \mu$m (ten fingers of width 6 μm) and lengths $L = 0.97\ \mu$m, 0.64 μm, 0.42 μm, 0.27 μm and 0.18 μm, respectively, biased at $V_{\rm DS} = 1.0$ V.

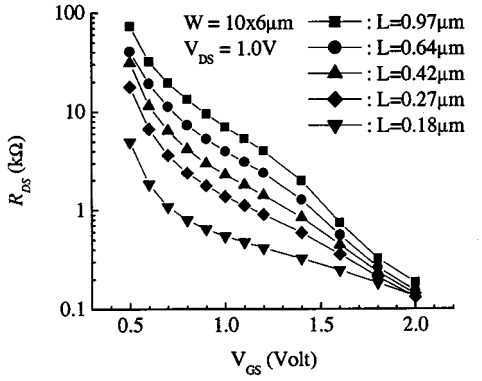

Fig. 7. Output resistance ($R_{\rm DS}$) versus $V_{\rm GS}$ characteristics extracted from measured Re(y_{22}) for the n-type MOSFETs with channel width $W = 10 \times 6\ \mu$m (ten fingers of width 6 μm) and lengths $L = 0.97\ \mu$m, 0.64 μm, 0.42 μm, 0.27 μm and 0.18 μm, respectively, biased at $V_{\rm DS} = 1.0$ V.

$L = 0.18\ \mu$m biased at $V_{\rm DS} = 1.0$ V and $V_{\rm GS} = 1.2$ V based on $g_m = 28.4$ mS, $R_{\rm G} = 5.75\ \Omega$, $R_{\rm D} = R_{\rm S} = 1.75\ \Omega$, $R_{\rm DS} = 486\ \Omega$, $R_i = 90.6\ \Omega$, $R_{\rm DB} = 134\ \Omega$, $C_{\rm GS} = 68.5$ fF, $C_{\rm GD} = 30.6$ fF, $C_{\rm GB} \cong 0.0$ fF, $C_{\rm DB} = 76.9$ fF, $C_{\rm SB} = 496$ fF and $\tau = 4.52 \times 10^{-12}$ s. Figs. 6–9 show the extracted g_m, $R_{\rm DS}$, $C_{\rm GS}$, and $C_{\rm GD}$ versus gate bias respectively, for devices with different channel lengths. These extracted parameters give similar fitting accuracies as that shown in Fig. 5(a)–(d) of the y-parameters versus frequencies at all the gate biases shown in Figs. 6–9.

The gate resistance ($R_{\rm G}$) used in the simulation for different channel lengths is obtained by

$$R_{\rm G} = \frac{R_{\rm GSH} \cdot W}{3 \cdot n^2 \cdot L} \tag{20}$$

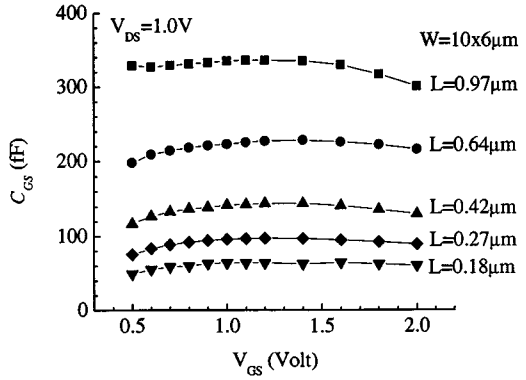

Fig. 8. Gate-to-source capacitances ($C_{\rm GS}$) versus $V_{\rm GS}$ characteristics extracted from measured Im(y_{11}) for the n-type MOSFETs with channel width $W = 10 \times 6$ μm (ten fingers of width 6 μm) and lengths $L = 0.97$ μm, 0.64 μm, 0.42 μm, 0.27 μm and 0.18 μm, respectively, biased at $V_{\rm DS} = 1.0$ V.

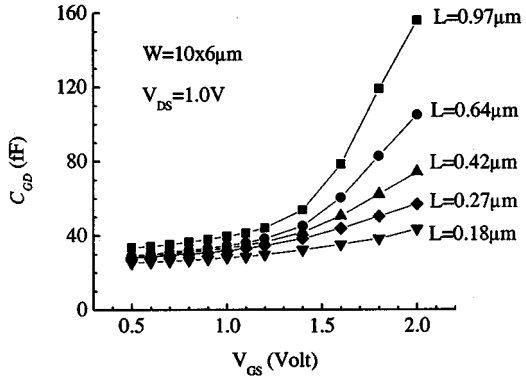

Fig. 9. Gate-to-drain capacitances ($C_{\rm GD}$) versus $V_{\rm GS}$ characteristics extracted from measured Im(y_{12}) for the n-type MOSFETs with channel $W = 10 \times 6$ μm (ten fingers of width 6 μm) and lengths $L = 0.97$ μm, 0.64 μm, 0.42 μm, 0.27 μm and 0.18 μm, respectively, biased at $V_{\rm DS} = 1.0$ V.

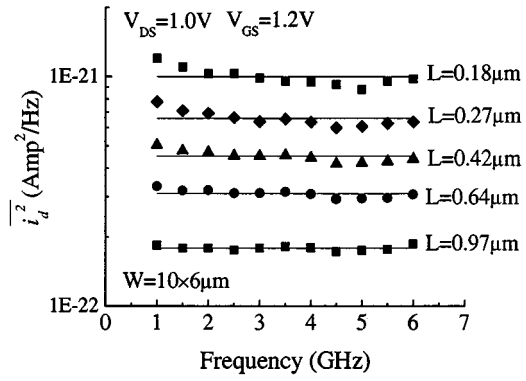

Fig. 10. Extracted channel noise ($\overline{i_d^2}$) versus frequency characteristics for the n-type MOSFETs with channel width $W = 10 \times 6$ μm (ten fingers of width 6 μm) and lengths $L = 0.97$ μm, 0.64 μm, 0.42 μm, 0.27 μm and 0.18 μm, respectively, biased at $V_{\rm DS} = 1.0$ V and $V_{\rm GS} = 1.2$ V. The solid lines are the extracted channel noise based on the method in [13].

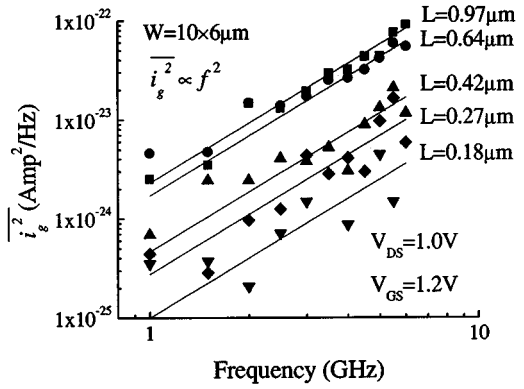

Fig. 11. Extracted induced gate noise ($\overline{i_g^2}$) versus frequency characteristics for the n-type MOSFETs with channel width $W = 10 \times 6$ μm (ten fingers of width 6 μm) and lengths $L = 0.97$ μm, 0.64 μm, 0.42 μm, 0.27 μm and 0.18 μm, respectively, biased at $V_{\rm DS} = 1.0$ V and $V_{\rm GS} = 1.2$ V.

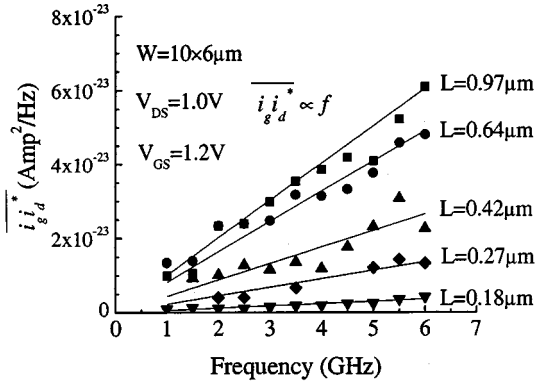

Fig. 12. Correlation between $\overline{i_g^2}$ and $\overline{i_d^2}$ ($\overline{i_g i_d^*}$) versus frequency characteristics for the n-type MOSFETs with channel width $W = 10 \times 6$ μm ten fingers of width 6 μm) and lengths $L = 0.97$ μm, 0.64 μm, 0.42 μm, 0.27 μm and 0.18 μm, respectively, biased at $V_{\rm DS} = 1.0$ V and $V_{\rm GS} = 1.2$ V.

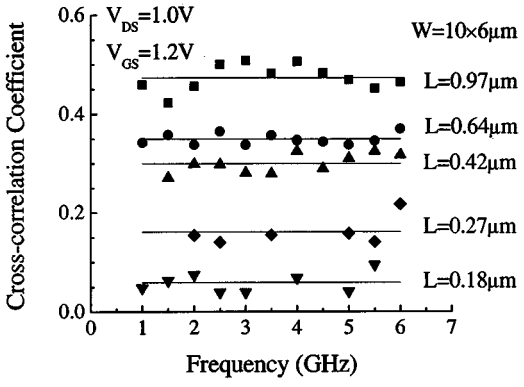

Fig. 13. Cross correlation coefficient c versus frequency characteristics for the n-type MOSFETs with channel width $W = 10 \times 6$ μm (ten fingers of width 6 μm) and lengths $L = 0.97$ μm, 0.64 μm, 0.42 μm, 0.27 μm and 0.18 μm, respectively, biased at $V_{\rm DS} = 1.0$ V and $V_{\rm GS} = 1.2$ V.

where $R_{\rm GSH} = 5.17\ \Omega$ and n is the number of fingers. In Fig. 6, the $V_{\rm GS}$ bias at which the peak g_m occurs decreases as the channel length is reduced and this results in the shift of the peak $f_{\rm T}$ shown in Fig. 4. Although the peak g_m increases when the channel length is reduced, the output resistance ($R_{\rm DS}$) in Fig. 7 decreases at the same time and this results in the amplification factor μ_f ($\mu_f = g_m \times R_{\rm DS}$) remains about the same at the $V_{\rm GS}$ where the peak g_m occurs.

Based on the element values extracted from the y-parameters and the measured noise parameters, Fig. 10 shows the extracted channel noise versus frequency characteristics for n-type MOSFETs with different channel lengths biased at $V_{\rm DS} = 1.0$ V and $V_{\rm GS} = 1.2$ V. It is shown that the channel noise, in general, is

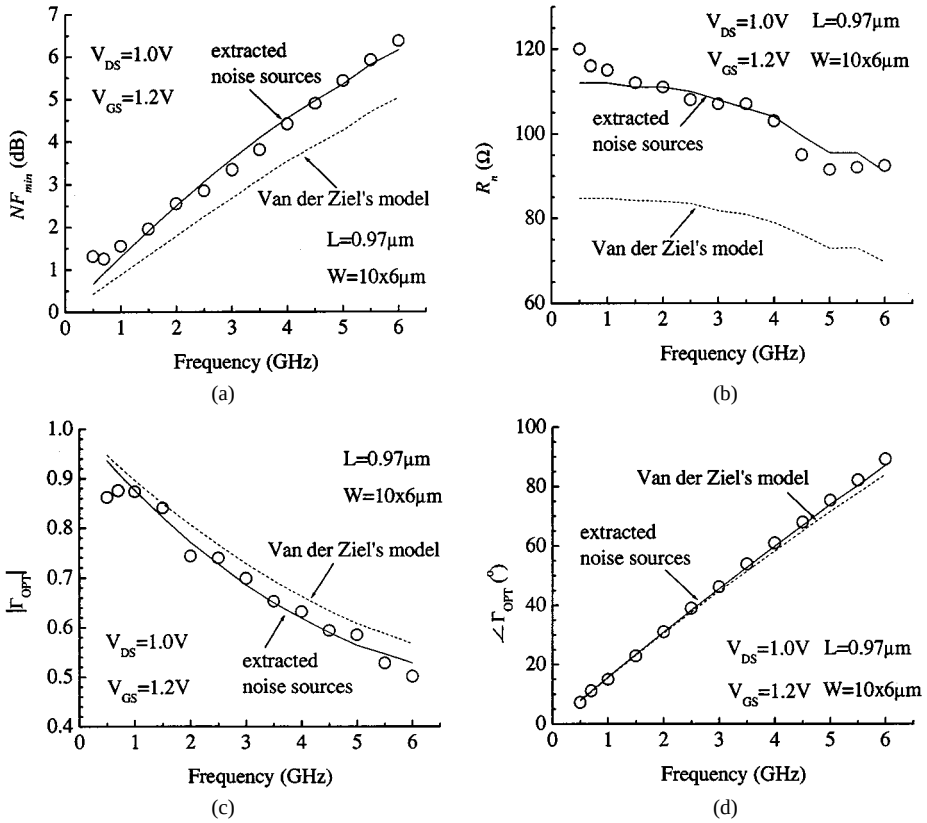

Fig. 14. (a) Measured (symbols) and simulated (lines) minimum noise figure ($NF_{\min}$) versus frequency characteristics for the n-type MOSFET with the channel width $W = 10 \times 6\ \mu$m (ten fingers of width 6 μm) and length $L = 0.97\ \mu$m biased at $V_{\rm DS} = 1.0$ V and $V_{\rm GS} = 1.2$ V. The solid line is calculated with all the extracted noise sources and the dashed line is calculated using the Van der Ziel's model, (b) measured (symbols) and simulated (lines) equivalent noise resistance ($R_{\rm n}$) versus frequency characteristics for the n-type MOSFET with the channel width $W = 10 \times 6\ \mu$m (ten fingers of width 6 μm) and length $L = 0.97\ \mu$m biased at $V_{\rm DS} = 1.0$ V and $V_{\rm GS} = 1.2$ V. The solid line is calculated with all the extracted noise sources and the dashed line is calculated using the Van der Ziel's model, (c) measured (symbols) and simulated (lines) magnitude of the optimized source reflection coefficient ($|\Gamma_{\rm OPT}|$) versus frequency characteristics for the n-type MOSFET with the channel width $W = 10 \times 6\ \mu$m (ten fingers of width 6 μm) and length $L = 0.97\ \mu$m biased at $V_{\rm DS} = 1.0$ V and $V_{\rm GS} = 1.2$ V. The solid line is calculated with all the extracted noise sources and the dashed line is calculated using the Van der Ziel's model and (d) measured (symbols) and simulated (lines) angle of the optimized source reflection coefficient ($\angle\Gamma_{\rm OPT}$) versus frequency characteristics for the n-type MOSFET with the channel width $W = 10 \times 6\ \mu$m (ten fingers of width 6 μm) and length $L = 0.97\ \mu$m biased at $V_{\rm DS} = 1.0$ V and $V_{\rm GS} = 1.2$ V. The solid line is calculated with all the extracted noise sources and the dashed line is calculated using the Van der Ziel's model.

frequency independent and increases when the channel length decreases. The solid lines in Fig. 10 are the extracted channel noise based on the method in [13] which provides an alternative way to verify the channel noise extracted by the proposed method. The small increase in the channel noise at low frequencies for deep submicron devices might be caused by the inaccuracy of the measurement system at low frequencies.

Figs. 11 and 12 show that the induced gate noise and the correlation term are proportional to f^2 and f, respectively where f is the operating frequency (solid lines in the figures). In addition, when channel length decreases, both the induced gate noise and the correlation term also decrease because of the decrease of $C_{\rm GS}$, as shown in Fig. 8. Another useful parameter that is used to describe the relationship between the channel noise, induced gate noise and their correlation is the cross correlation coefficient c which is defined as

$$c = \frac{\overline{i_g i_d^*}}{\sqrt{\overline{i_g^2}\,\overline{i_d^2}}}. \tag{21}$$

Fig. 13 shows the extracted cross correlation coefficient c versus frequency characteristics for the devices with different channel lengths. In general, c is frequency independent and decreases when the channel length decreases. This is an opposite trend to the simulated results in [16], [17], but is in agreement with the theory in [2]. [3].

In order to verify the accuracy of the extracted noise sources and compare the simulation results against the measured data and those based on van der Ziel's model [14] which is suggested for long channel devices, Fig. 14(a)–(d) show the measured (symbol) and simulated (lines) noise parameters versus frequency characteristics by using the technique described in [5], [6] for the n-type MOSFET with the channel width $W = 10 \times 6\ \mu$m and length $L = 0.97\ \mu$m biased at $V_{\rm DS} = 1.0$ V and $V_{\rm GS} = 1.2$ V. In these figures, the solid lines are the simulated results based on the extracted noise sources (solid lines in Figs. 10–12) and the dashed lines are the simulated results based on van der Ziel's model in which the spectral density of the noise sources are given by

$$\overline{i_d^2} = \gamma_{\rm satn} 4kT g_{\rm do} \tag{22}$$

$$\overline{i_g^2} = \delta_{\rm satn} 4kT \frac{\omega^2 C_o^2}{g_{\rm do}} \text{ and} \tag{23}$$

$$\overline{i_g i_d^*} = \varepsilon_{\rm satn} 4kTj\omega C_o \tag{24}$$

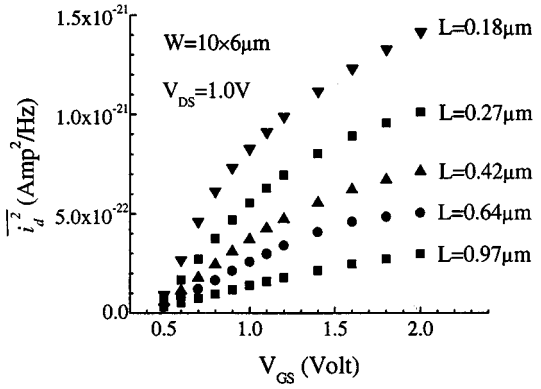

Fig. 15. Channel noise ($\overline{i_d^2}$) versus bias characteristics for the n-type MOSFETs with channel width $W = 10 \times 6\ \mu$m (ten fingers of width 6 μm) and lengths $L = 0.97\ \mu$m, 0.64 μm, 0.42 μm, 0.27 μm and 0.18 μm, respectively, biased at $V_{\rm DS} = 1.0$ V.

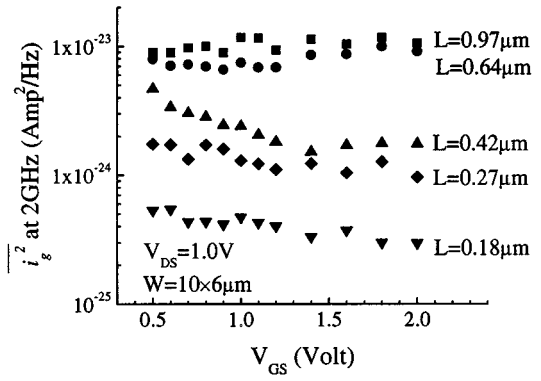

Fig. 16. Induced gate noise ($\overline{i_g^2}$) versus bias characteristics for the n-type MOSFETs with channel width $W = 10 \times 6\ \mu$m (ten fingers of width 6 μm) and lengths $L = 0.97\ \mu$m, 0.64 μm, 0.42 μm, 0.27 μm and 0.18 μm, respectively, biased at $V_{\rm DS} = 1.0$ V.

where $g_{\rm do} = 12.5$ mS, $2/3$, $\delta_{\rm satn} = 16/135$, $\varepsilon_{\rm satn} = 1/9$, $C_o = C_o = 3C_{\rm GS}/2$ and $\omega = 2\pi f$.It is shown that the extracted noise sources, in general, give a good noise prediction. However, van der Ziel's model predicts lower $NF_{\rm min}$ and $R_{\rm n}$ and this might be caused by not including the channel noise and induced gate noise contributed from the velocity saturation region [3], [15] because of the assumption $E_{\rm C} = \infty$ where $E_{\rm C}$ is the critical field. This is currently being investigated.

For the bias dependence of the extracted noise sources, Figs. 15–18 show the $\overline{i_d^2}$, $\overline{i_g^2}$, $\overline{i_g i_d^*}$ and c versus bias characteristics for the n-type MOSFETs with channel width $W = 10 \times 6\ \mu$m and lengths $L = 0.97\ \mu$m, 0.64 μm, 0.42 μm, 0.27 μm and 0.18 μm respectively, biased at $V_{\rm DS} = 1.0$ V. It is shown that $\overline{i_d^2}$ and $\overline{i_g i_d^*}$ have a strong bias dependence and they increase the tend to saturate when $V_{\rm GS}$ increases, but $\overline{i_g^2}$ has a weak bias dependence. On the other hand, the cross-correlation coefficient c decreases when $V_{\rm GS}$ increases and it follows the trend predicted in [2].

Finally, Figs. 19 and 20 show the extracted $\overline{i_d^2}$ and $\overline{i_g^2}$ versus $V_{\rm GS}$ characteristics at $V_{\rm DS} = 1.0$ V, 1.2 V, 1.5 V, 1.8 V, and 2.0 V, respectively. It is shown that both of them have a weak $V_{\rm DS}$ dependence in the $V_{\rm DS}$ region discussed and this might be because the effect of the channel length modulation is not prominent in these devices, as shown in Fig. 3.

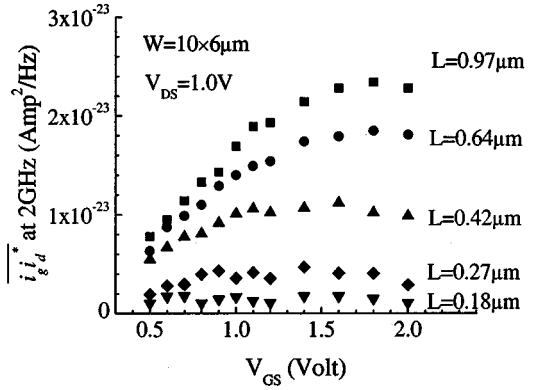

Fig. 17. Noise correlation between $\overline{i_g^2}$ and $\overline{i_d^2}$ ($\overline{i_g i_d^*}$) versus bias characteristics for the n-type MOSFETs with channel width $W = 10 \times 6\ \mu$m (ten fingers of width 6 μm) and lengths $L = 0.97\ \mu$m, 0.64 μm, 0.42 μm, 0.27 μm and 0.18 μm, respectively, biased at $V_{\rm DS} = 1.0$ V.

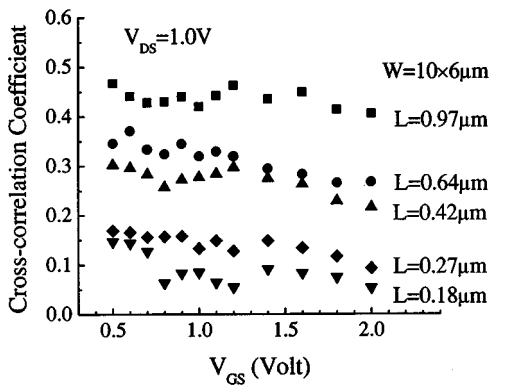

Fig. 18. Cross-correlation coefficient c versus bias characteristics for the n-type MOSFETs with channel width $W = 10 \times 6\ \mu$m (ten fingers of width 6 μm) and lengths $L = 0.97\ \mu$m, 0.64 μm, 0.42 μm, 0.27 μm and 0.18 μm, respectively, biased at $V_{\rm DS} = 1.0$ V and $V_{\rm GS} = 1.2$ V.

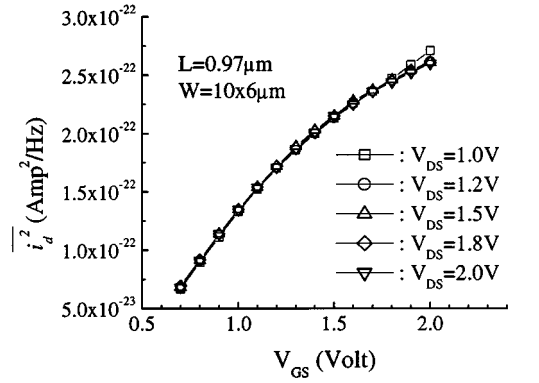

Fig. 19. Channel noise ($\overline{i_d^2}$ versus $V_{\rm GS}$ characteristics for the n-type MOSFET with channel width $W = 10 \times 6\ \mu$m (ten fingers of width 6 μm) and length $L = 0.97\ \mu$m biased at $V_{\rm DS} = 1.0$ V, 1.2 V, 1.5 V, 1.8 V, and 2.0 V, respectively.

IV. Conclusions

A general direct extraction procedure of the induced gate noise, channel noise and their correlation in MOSFETs from the on-wafer scattering and noise measurements has been presented in detail and verified with measurements. In general, the channel noise $\overline{i_d^2}$ is frequency independent and increases when the channel length decreases for all bias conditions at a fixed

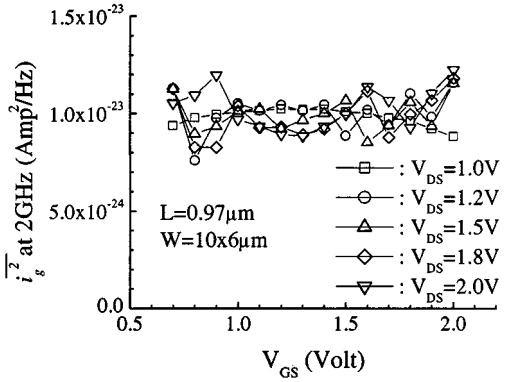

Fig. 20. Induced gate noise ($\overline{i_g^2}$) versus $V_{\rm GS}$ characteristics for the n-type MOSFET with channel width $W = 10 \times 6$ μm (ten fingers of width 6 μm) and length $L = 0.97$ μm biased at $V_{\rm DS} = 1.0$ V, 1.2 V, 1.5 V, 1.8 V, and 2.0 V, respectively.

$V_{\rm DS}$. However, $\overline{i_g^2}$ and $\overline{i_g i_d^*}$ are proportional to f^2 and f, respectively, which agrees with the theoretical prediction and they both decrease when the channel length decreases because of the decrease of $C_{\rm GS}$. In the case of the cross correlation coefficient c, it is frequency independent and decreases when the channel length decreases. It was found that $\overline{i_d^2}$ and $\overline{i_g i_d^*}$ have a strong $V_{\rm GS}$ bias dependence and they increase then tend to saturate when $V_{\rm GS}$ increases, but $\overline{i_g^2}$ has a weak $V_{\rm GS}$ dependence. In addition, both $\overline{i_d^2}$ and $\overline{i_g^2}$ have weak $V_{\rm DS}$ dependences for devices in which channel length modulation by the drain bias is weak. Also, van der Ziel's model predicts lower $NF_{\rm min}$ and $R_{\rm n}$ than the measurements. Finally, the extracted channel noise, induced gate noise and their correlation can be used as a direct target for the verification of the physics-based noise models of submicron MOSFETs.

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