Extraordinary electroconductance in metal-semiconductor hybrid structures

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We report the phenomenon of extraordinary electroconductance in microscopic metal-semiconductor hybrid structures fabricated from GaAs epitaxial layer and a Ti thin film shunt. Four-lead Van der Pauw structures show a gain of 5.2% in electroconductance under +2.5 kV/cm with zero shunt bias. The increase in the sample conductance results from the thermionic field emission of electrons and the geometrical amplification. A model provides good agreement with the experimental data and clearly demonstrates the geometry dependence of the field effect in extraordinary electroconductance (EEC). The differences between EEC devices and field effect transistors, such as junction field effect transistor (FET) and Schottky barrier gate FET, are discussed. © *2008 American Institute of Physics*. [DOI: 10.1063/1.2955503]

Electrical transport in any device depends on both the physical or intrinsic properties such as the carrier concentration, etc., and the extrinsic geometric properties such as the shape of the device, etc.[1] Normally, transport studies focus on the physical properties and samples are designed to minimize the geometric contributions. However, Solin *et al.* have shown that by careful design, the geometric contributions can be made dominant and have demonstrated a class of EXX phenomena, where E=extraordinary and, to date, XX=magnetoresistance,[2,3] piezoconductance,[4,5] and optoconductance.[6,7] Here we report another type of EXX phenomenon, extraordinary electroconductance (EEC), which is based on the geometric amplification of the physical properties of a Schottky interface using a metal-semiconductor hybrid (MSH) structure.

The MSH structures were fabricated from a 2 in. (100) GaAs substrate (resistivity $\rho > 1 \times 10^{15}\ \Omega\,\mathrm{m}$, thickness $t=350\ \mu\mathrm{m}$) with an epitaxially grown Si-doped *n*-GaAs layer ($N_D = 4 \times 10^{17}\ \mathrm{cm}^{-3}$, $t=200$ nm). Four equally spaced Au/Ge Ohmic leads are surface deposited on the periphery of the mesa disk. A circular opening 100 nm in depth was patterned concentrically on the GaAs mesa and a disk-shaped Ti thin film ($t=50$ nm) was deposited. An additional 50 nm Au/Ge was deposited as a current shunt. With deliberate control of the metal deposition rate and surface passivation, a Schottky barrier was formed at the interface. To apply the electric field directly, a pair of thin metal plates are built into the device. One, made of Au/Ge, was deposited on top of the shunt metal with a layer of Si_3N_4 ($t=1\ \mu\mathrm{m}$) in between, while the other was obtained by metallizing the bottom surface of the substrate. Two sets of devices with different mesa radius, 100 and 60 μm, are studied. Figures 1(a) and 1(b) show the sample structure. In this study, a four-point ac lock-in measurement was used with current passing through leads 1 and 4 (common ground) and the voltage sensing between leads 2 and 3. The external field is in the range $-2.5\ \mathrm{kV/cm} \leq E \leq +2.5\ \mathrm{kV/cm}$.

For a MS system with $5 \times 10^{16}\ \mathrm{cm}^{-3} \leq N_D \leq 5 \times 10^{17}\ \mathrm{cm}^{-3}$, thermionic field emission dominates current transport across the interface at room temperature.[8] The total current density can be expressed as, $I = I_s[\exp(qV/nkT) - 1]$, where I_s is the saturation current which is a complicated

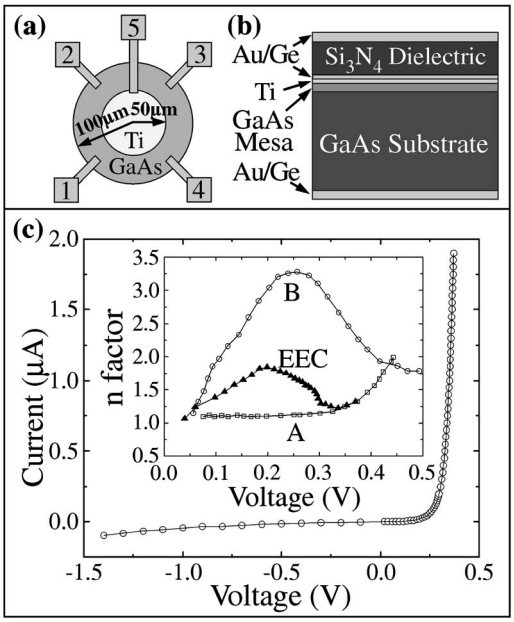

FIG. 1. Panels (a) and (b) are Schematics, of the top view and side view of an EEC device, respectively with $R=100\ \mu$m and $r=50\ \mu$m. Panel (c) is the room temperature *I-V* characteristic of the Schottky interface. Inset: ideal factor *n* from a typical EEC device, an ideal Schottky diode, A and a Schottky diode with a thick oxide interfacial layer, B. (A and B are adapted from Ref. 11). The lines are guides to the eye.

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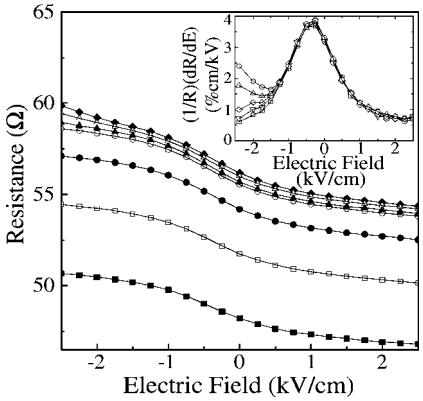

FIG. 2. Main panel shows the room temperature four-lead resistance of a sample with $R=100\ \mu$m and $\alpha=\frac{1}{16}$ under for $-2.5\ \text{kV/cm} \leqslant E \leqslant +2.5\ \text{kV/cm}$. The symbols have the following designations: $V_B=-0.4$ V, ◆; −0.2 V, △; 0 V, ▲; +0.2 V, ○; +0.4 V, ●; +0.45 V, □; and +0.5 V, ■. Inset: the sensitivity of the device for $V_B=-0.4$ V, ○; −0.2 V, △; 0 V, ◇; +0.2 V, △; +0.4 V, □.

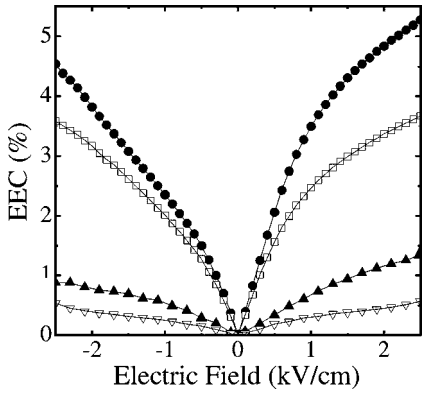

FIG. 3. The geometry dependence of the EEC effect. The symbols correspond to $16\alpha=1$, ●; 5, □; 10, ▲; 14, △. The mesa radius for each device is 100 μm.

function of barrier height, semiconductor properties, and temperature. The ideal factor for the Schottky interface is defined as $n \equiv (q/kT)[\partial V/\partial(\ln I)]$.

The deviation of the real Schottky interface from the ideal can be attributed to many effects, such as electron trapping and recombination,[9] barrier inhomogeneities,[10] interfacial oxide layer,[11] image force lowering,[12] and series resistance.[13] In a two-terminal Schottky *I-V* measurement, comparing to an ideal Schottky diode, the EEC device has a larger series resistance arising from the uncovered annulus shaped GaAs region between leads 5 and 4. This excess series resistance and the possible presence of a thin oxide layer at the GaAs–Ti interface contribute to the nonideal behavior of the MS interface. The main panel of Fig. 1(c) shows the *I-V* characteristic of the Schottky interface while the inset compares the factor n of a typical EEC device with an ideal Schottky diode A and nonideal diode B with a thick oxide interfacial layer. According to Ellis and Barnes,[13] the equivalent circuits of a real Schottky diode, such as EEC devices, can be represented by two ideal diodes in parallel, each with associated series resistance. In fact, from the inset of Fig. 1(c), the ideal factor of the EEC is approximately a linear combination of those of samples A and B. Detailed discussion of this point will be provided elsewhere.[14]

The main panel of Fig. 2 shows the field dependence of the device resistance under a series of shunt biases from −0.4 to +0.5 V between leads 5 and 4. The sample resistance is a function of both the external electric field E and shunt bias V_B, i.e., $R(E,V_B)$. Under a constant V_B, the resistance monotonically decreases as E increases and there is a one-to-one correspondence between R and E. On the other hand, for a fixed E, the resistance is substantially decreased when $V_B > +0.2$ V, as the forward shunt bias diminishes the depletion region[15] at the MS interface. The inset of Fig. 2 shows the device sensitivity, defined as $-(1/R)(dR/dE)$, with respect to E as a function of V_B. The maximum sensitivity, ~4% cm/kV, is obtained at −0.3 kV/cm. Note that for $E > -1$ kV/cm, the sensitivity of this device is independent of V_B. With our current measurement setup, for $E=2$ kV/cm, a 0.7% change in field intensity can be detected.

Similar to other EXX entities, geometry plays an important role in the transport properties of the EEC device. For a Van der Pauw disk structure, we define a parameter α as the ratio of the shunt radius to the mesa radius, i.e., $\alpha=R_{\text{shunt}}/R_{\text{mesa}}$. The room temperature EEC is defined to be the percentage change in sample conductance $G=I_{14}/V_{23}$ with and without an external electric field,

$$\text{EEC}(E,\alpha) = |G(E,\alpha) - G(0,\alpha)|/[G(0,\alpha)] \times 100\%. \quad (1)$$

Figure 3 shows the calculated EEC for four different devices with a fixed 100 μm mesa radius and α of $\frac{1}{16}$, $\frac{5}{16}$, $\frac{10}{16}$, and $\frac{14}{16}$. The device with $\alpha=\frac{1}{16}$ exhibits the largest EEC effect in both forward and reverse field bias and the largest EEC effect, ~5.2%, is obtained at a field of 2.5 kV/cm. As α decreases, the EEC increases. Since mesoscopic effects will prevent divergence of the EEC it must have a maximum at reduced α. We have not yet determined that maximum due to the feature size limitation (~5 μm) of our optical lithography. This determination will be made with future devices fabricated with e-beam lithography.

Traditionally, the *p-n* junction field effect transistor[16] (JFET) and the Schottky barrier gate FET (MESFET) (Ref. 17) were studied under reverse bias. The reverse gate voltage controls the depletion thickness at the junction and thus modulates the conductivity of the electron channel. EEC distinguishes itself from the FET-like devices by the forward field effect. Without a proper modification of the FET structure, the forward bias effect cannot be studied due to the additional current injection from metal to semiconductor, which is inseparable from the pure field effect. In the EEC structure, a 1 μm thick Si_3N_4 dielectric thin film is included between the top electrode and the metal shunt for this purpose. Under a bias of V_B, the depletion width is given by [18]

$$W = \sqrt{\frac{2\varepsilon_s}{qn}\left(V_{\text{in}} - V_B - \frac{kT}{q}\right)}, \quad (2)$$

where ε_s is the permittivity, V_{in} is the built-in voltage, and the other parameters have their usual meanings. This yields $W=31.5$ nm for our devices with $V_{\text{in}}=0.3$ V and $V_B=0$. Under a forward field, the depletion is thinned and more thermally excited electrons can tunnel through the barrier near the top from semiconductor to metal. The Ti and Au/Ge thin films act as both a Schottky gate and a current shunt. By providing an alternative route for electrons traveling from semiconductor to metal, current paths are not restricted to the conducting channels shaped by the depletion as in FET devices. This contributes significantly to the geometry dependence of the EEC effect.

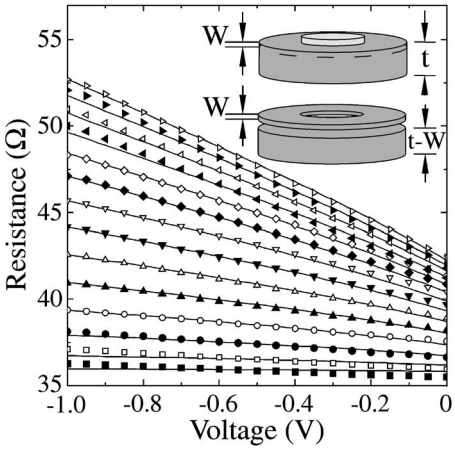

FIG. 4. Inset: schematics of the two-layer EEC structure under reverse bias. Main panel: the solid lines are fits of Eq. (3) to experiment for samples with $R=60$ μm under reverse bias. The symbols correspond to the observed resistances adjusted by $R_C(\alpha)$ with $[16\alpha, R_C(\alpha)]=$ (1, 10.92 Ω), ■; (2, 20.45 Ω), □; (3, 12.69 Ω), ●; (4, 6.09 Ω), ○; (5, 11.23 Ω), ▲; (6, 13.63 Ω), △; (7, 12.02 Ω), ▼; (8, 9.39 Ω), ▽; (9, 7.81 Ω), ◆; (10, 6.91 Ω), ◇; (11, 13.22 Ω), ▯; (12, 9.16 Ω), ◁; (13, 10.97 Ω), ▶; (14, 13.39 Ω) ▷.

On the other hand, under zero applied electric field and direct reverse bias across leads 5 and 4, a configuration we label as the FET testing mode, the EEC sensor behaves as a JFET. In an analytical model we developed, a GaAs annulus, with the central hole corresponding to the depletion region, and a homogenous GaAs cylinder are connected in parallel. The inset of the Fig. 4 shows the three-dimensional schematics of the two-layer model. The total resistance can be expressed as,

$$\frac{1}{R(\alpha,V_B)}=\frac{1}{R_{\text{top}}(\alpha,V_B)}+\frac{1}{R_{\text{bottom}}(\alpha,V_B)}, \tag{3}$$

where $R_{\text{top}}=\frac{1}{\pi\sigma W}\sum_{n=1}^{\infty}\{[2(1+\alpha^{2n})/(1-\alpha^{2n})]-[(1+\alpha^{4n})/(1-\alpha^{4n})]\}(1/n)(-1)^{n+1}$,[19,20] and, with $\alpha=0$, $R_{\text{bottom}}=[\ln 2/\pi\sigma(t-W)]$. The model assumes sidewall contacting of the voltage and current probes whereas the devices use surface contacts. This necessitates the introduction of one adjustable offset parameter $R_C(\alpha)$, so that the calculated effective resistance is

$$R_{\text{eff}}(\alpha,V_B)=R(\alpha,V_B)+R_C(\alpha). \tag{4}$$

For clarity of presentation, the main panel of Fig. 4 compares $R(\alpha,V_B)$ (solid lines) and $[R_{\text{obs}}-R_C(\alpha)]$ (symbols), where $R_{\text{obs}}(\alpha,V_B)=V_{23}/I_{14}$. The model provides a very good fit to the data for various values of V_B and α. The values of $R_C(\alpha)$ are given in the figure caption. Further details of the model will be discussed elsewhere.[14]

Under the FET testing mode, the key difference between EEC and JFET/MESFET comes from the device geometry. In both JFET and MESFET, the gate has a fixed dimension and covers the major area of the conducting channel. However, in the case of EEC, the Ti shunt, equivalent to the gate in the FETs, has a variable area and the ratio α ranges from $\frac{1}{16}$ to $\frac{14}{16}$. With 20 μA alternating current from leads 1 to 4, the device operates in the linear regime. Due to the special structure of EEC devices, there is no pinch off effect.[16] Under reverse bias, the radius of the depletion region in the semiconductor coincides with that of the shunt. Suppose enough bias is applied and the semiconductor thin film under the shunt is totally depleted, electrons can still travel in the annulus shaped semiconductor surrounding the depletion. Under the above conditions, the geometry dependence of the resistance in a FET-like device can now be demonstrated in terms of the "gate" sizes.

In conclusion, we have demonstrated the proof of principle of EEC in GaAs–Ti thin film MSH. The geometry dependence of the device resistance and the dual role of the Schottky metal, i.e., gate in the FET testing mode and current shunt in direct field sensing, distinguish EEC from the JFET and MESFET structures. The inclusion of the dielectric layer of Si_3N_4 makes the forward bias study of a Schottky interface possible. An individual EEC device could function as an electric field sensor. Arrays of such sensors could be used for biological applications. For example, by scaling to the nano regime, an EEC sensor array could, in principle, produce a real time image of the charge distribution on a single cell surface.

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