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ABSTRACT

EUVL mask blanks consist of a distributed Bragg reflector made of 6.7nm-pitch bi-layers of Mo and Si deposited upon a precision Si or glass substrate. The layer deposition process has been optimized for low defects, by application of a vendor-supplied but highly modified ion-beam sputter deposition system. This system is fully automated using SMIF technology to obtain the lowest possible environmental- and handling-added defect levels. Originally designed to coat 150mm substrates, it was upgraded in July, 1999 to 200 mm and has coated runs of over 50 substrates at a time with median added defects >100nm below 0.05/cm^2. These improvements have resulted from a number of ion-beam sputter deposition system modifications, upgrades, and operational changes, which will be discussed.

Success in defect reduction is highly dependent upon defect detection, characterization, and cross-platform positional registration. We have made significant progress in adapting and extending commercial tools to this purpose, and have identified the surface scanner detection limits for different defect classes, and the signatures of false counts and non-printable scattering anomalies on the mask blank. We will present key results and how they have helped reduce added defects.

The physics of defect reduction and mitigation is being investigated by a program on multilayer growth over deliberately placed perturbations (defects) of varying size. This program includes modeling of multilayer growth and modeling of defect printability. We developed a technique for depositing uniformly sized gold spheres on EUVL substrates, and have studied the suppression of the perturbations during multilayer growth under varying conditions. This work is key to determining the lower limit of critical defect size for EUV Lithography. We present key aspects of this work.

We will summarize progress in all aspects of EUVL mask blank development, and present detailed results on defect reduction and mask blank performance at EUV wavelengths.

Keywords: Extreme Ultraviolet Lithography, EUVL, Next Generation Lithography, NGL, mask, multilayer, defect, defect detection, defect mitigation.

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1. INTRODUCTION

1.1. Background

Extreme Ultraviolet Lithography (EUVL) is a leading NGL technology in the current race to replace conventional optical lithography beyond the 100nm critical-feature node. EUVL is based on a wavelength reduction to λ = 13.4nm, and is under development at a coalition of three DOE national laboratories. Two demonstration tools are now under construction: the Engineering Test Stand to demonstrate full-field (106×132mm on mask) printing at 4X reduction at the 100nm node, including full environmental controls and 10wph throughput at 300mm, and the Micro-Exposure Tool to demonstrate extendibility to the 70nm and 50nm nodes over a smaller field. A more complete technical description of EUV Lithography as a whole can be found in the 1999 EUVL White Paper.[1]

To achieve imaging at 13.4nm, EUVL uses reflective optics for the illuminator, mask and reduction optics. The optical surfaces are coated with a thin multilayer coating stack for enhanced reflectivity. The multilayer comprises 80 alternating Mo and Si layers at a 6.7nm pitch, for a total thickness of about 280nm. The multilayer coating works as a quarter-wave stack, or equivalently a 1-dimensional Bragg reflector, giving reflectivity of 60-70% by constructive interference of light reflected from the many interfaces. EUVL masks are then patterned in metal absorber atop the multilayer. An extensive treatment of multilayer coatings for this wavelength regime has been published by Spiller[2] and further description of the EUVL mask architecture is presented in the EUVL White Paper.

Because the multilayer pitch is precisely tuned for constructive interference at 13.4nm, the mask cannot be repaired if defects occur in the multilayer growth. For this reason the mask blanks (multilayer-coated mask substrates before patterning) must be produced nearly defect free. A dedicated ion-beam sputtering chamber was built on contract for LLNL for this purpose and has been developing low-defect blanks since mid-1997. The level of added defects has been reduced about 1 decade each year since then, meeting our goal of producing a mask blank with 0.01 added defects/cm^2 at sizes over 90nm by the end of 1999. The milestone for 2000 will include a further reduction of the median added defect level and improved process knowledge on defect sources. A more complete description of the coating chamber can be found in earlier publications.[3,4]

1.2. Mask Substrates

The bulk of our mask substrates are ultra-clean 200mm Si wafers, to take advantage of the existing infrastructure for reliable substrate supply and clean handling technology. For production EUVL tools, however, a mask substrate with lower thermal expansion will be needed, since some EUV light is absorbed at the mask as heat. Thermal modeling[5] indicates that several commercially-available low thermal expansion materials (LTEMs) will meet the requirements for mask thermal management. These materials are standard silica glasses with additives to adjust the thermal expansion coefficient. Initial coating and inspection work is beginning on 200mm round substrates from several LTEM manufacturers, and also on LTEM masks in a more conventional format of 6-inch squares at ¼-inch thickness. No substantial change in the multilayer coating process is needed for these substrates, so this work is concentrated on clean handling, improving surface finish in collaboration with the manufacturers, and identifying dominant defect types on the glass.

1.3. Mask Blank Coating Process

Wafer substrate handling is completely by robot in a class 100 research clean-room, with most handling in a SMIF mini-environment of class 1 or better. Wafers are removed from initial packaging in a separate laminar-flow mini-environment and loaded into SMIF pods. Initial defect scans are made with commercial laser light-scatter tools (ADE Constellation AWIS and KLA/Tencor SP1) which are fully SMIF-capable. The full cassette of 25 wafers is then pumped to HV for coating in the Low-Defect Deposition (LDD) tool. This tool was custom-built by Veeco Instruments but heavily modified at LLNL. After coating, the wafers are re-scanned in the optical tools for added defects and transferred to AFM and SEM tools for defect review.

This paper will cover recent progress in reducing added defects and outline key changes in the coating process that have contributed to making cleaner mask blanks (Section 2). Methods for detection and characterization of defects in EUVL mask blanks are described in the Section 3, including results on types of added defects and methods of verifying defect detection thresholds. Finally, in Section 4 we will discuss a key EUVL technology for applying a

smoothing layer to the substrate before multilayer coating. This layer is intended to smooth over defects in the size range of about 5nm to 50nm, which are expected to be printable defects in EUVL but are not yet detectable with optical inspection tools.

2. DEFECT REDUCTION PROGRESS AND DEPOSITION SYSTEM IMPROVEMENTS

Our baseline low-defect coating process consists of careful chamber design and attention to clean-room practice and detail. Clean handling is important to minimize blank contamination before and after production. We use good cleanroom practices, SMIF technology, controlled pumping/venting and semiconductor grade vacuum loadlocks and transfer robots to minimize this contamination.

Our progress in defect reduction through January 2000 is shown in Fig. 1. The figure shows all defects above 90nm size (measured by latex sphere equivalent scatter size), which is our current limit of reliable detection on multilayer-coated blanks. Much of the fluctuation in the figure results from specific experiments rather than stability of the process. The milestone of adding 0.01 defects/cm^2 or fewer was met on two blanks.

Several changes in the deposition process contributed to reducing added defects in past work, and these were continued here. First, the Mo and Si sputter targets were mechanically polished and chemically etched to remove layers of recrystallized or damaged material from the initial target manufacture. This was found to decrease the "cleanup" time between installation of a new target and a leveling-off of the added defect level, and the faster drop in defect level after a target change is visible in Fig. 1. Second, free-standing metal shields were installed to block line-of-sight paths from the ion gun and chamber walls to the wafer surface, since flaking of previously-deposited material from the gun and walls is a suspected source of defects. Simple aluminum-foil wrapping of the shields was found to give better results than a commercial arc-sprayed aluminum coating commonly used for low-defect environments. Third, high purity Mo targets (99.999%) appeared to give better results than lower purity (99.99%) Mo, although this result has not been repeated.

Several new changes were made to the chamber to build on previous results. To replace the previous mechanical wafer chuck and hold-down ring, a new electrostatic chuck was designed and fabricated. It uses concentric ring electrodes on the holding surface to hold the wafer by the induced charge on the front surface. A more advanced chuck with an interdigitated pole arrangement was also designed that provides additional clamping force and reduced static discharge time, so that the chuck can hold low thermal expansion material (LTEM) substrates, as well as silicon wafers. A rigid liner system was also installed in the coating system to provide a capture surface for stray sputtered target material, and to reduce the refurbishment time during planned maintenance activities.

Several changes were also made in the coating process. The targets were pre-sputtered for 5 minutes before starting to coat each substrate, to remove any surface layer accumulated between wafers. The wafers were also kept in the "hide" position facing away from the target during the pre-sputtering. Finally, the wafers were coated with their surfaces normal to the deposition flux. Earlier coatings had been made with the flux about 50° from the surface normal, in order to improve uniformity of the coating thickness. While blanks coated at normal incidence have more variation of the coating thickness across the wafer diameter, it was found that coating at this geometry reduced added defects by approximately a factor of 2. It was later shown that the higher incidence angle reduces the factor by which defects are expanded by being overcoated, because there is less shadowing of neighboring regions of the growing film by the hill of coating material above the defect.

A cumulative histogram of defect density vs. size is shown in Fig. 2. The graph contains approximately 1700 defects over about 100 coated blanks. Each point on the curve represents the total number of defects per square centimeter larger than that size. Fitting a power law to the data gives a relatively weak size dependence of the added defects of this process, rising as only about $d^{-0.6}$, versus dependence near d^{-2} found in the literature for some other processes. If the smallest printable defect for EUVL is 50nm, an extrapolation of these results to that value predicts only about 50% more defects than current levels, which is a modest requirement for future defect reduction.

Some other initiatives were also begun to improve understanding and reliability of the coating process. An *in situ* reflectometer cluster tool is being developed for centroid wavelength and reflectivity measurements that will improve measurement turn-around time, throughput, and cleanliness compared to use of the Advanced Light Source

(ALS) at Lawrence Berkeley National Laboratory. Mask performance will now be testable wafer-by-wafer, which should greatly improve yields by allowing operators to alter coating recipes on a real-time basis. Each blank will be certified, providing statistically significant evidence of coating performance. Also, an *in situ* scatterometer was implemented using a rastering laser to illuminate particles in the ion beam and on the surface of a mask substrate in the LDD tool. Images of these particles were collected with a CCD camera during deposition and pump down. Although no particles were observed on the surface of a wafer receiving deposition, moving particles were detected inside the LDD vacuum chamber. Future experiments are planned to better understand the transport of particles in the coating system.

3. DEFECT DETECTION AND CHARACTERIZATION

3.1. Metrology Tools

Since current EUVL mask blanks are Mo/Si multilayers on 200mm Si wafers, existing bare-wafer surface scan tools with high sensitivity to very small defects are well suited for inspection before coating. The Mo/Si multilayers are grown with very low roughness, so the rough-surface scatter ("haze") of the coated blank is typically only 30-40% higher than that of the bare wafer. Because of this the same optical tools can be used for inspection after coating, though the detection limit is raised from about 80nm to about 90nm. The two surface scan tools used are the ADE Constellation AWIS and the KLA/Tencor SP-1.

Defect review is by AFM and SEM. Defects are found using the location maps from the optical inspection tools. A rough coordinate correction is performed from custom laser fiducial marks on the wafers. Fine corrections are made by finding two defects in the AFM, using just the optical viewer if there are two defects large enough to be visible (about 250nm or above). From the accurate coordinates of these defects, a rotation and translation relative to their positions in the original optical defect map is calculated, and those corrections are applied to the remaining defects in the optical map. This method relies on the high mechanical accuracy of the AFM's x-y stage, which is 2μm or better over a 200mm wafer.

3.2. Detection Sensitivity

Recent multilayer coatings have mean added defect levels of $0.04/cm^2$ for a lot of 25, or about 8-9 added defects per wafer. The defect count must be highly reliable to count such small numbers accurately, which has motivated careful checks of the detection efficiency. We have adopted a statistical method of rigorously measuring the capture rate by making many repeat scans of a set of wafers or blanks, typically 10 scans each for a lot of 10-20 wafers.

Statistical analysis of the repeat scans shows a size threshold below which some defects are not detected every time, and a size range of defects that occur in only one scan (defined to be false counts). Consideration must also be made of whether a defect is detected in one channel or in multiple channels in the surface scan tool, for example the back, front and center channels on the ADE Constellation. A curve of the capture efficiency vs. size can then be calculated (Fig. 3), as well as a curve of the false count rate as a function of size. These curves are then used to set the threshold for what is counted as a real defect in our results. The thresholds are set where the curves show a 95% probability of detection and 1 or fewer false counts per wafer. These are two separate requirements, and on multilayer-coated wafers the false-count requirement sets a higher minimum defect size than the sensitivity requirement. We are now confident meeting both requirements for defects of 90nm PSL-equivalent size or greater on either optical tool.

To investigate the number of defects below the detection limits of the optical tools, two coated blanks were inspected by KLA/Tencor on a SP1-TBI, a higher-sensitivity version of the SP-1. This tool uses a second laser at oblique incidence for greater sensitivity, and had a detection limit near 70nm on coated mask blanks, as compared with 90nm for our SP1. With the extra sensitivity the defect density increased by about 35%, which is approximately consistent with an extrapolation of the defect scaling in Figure 2. This supports the rather weak dependence of defect density on size and indicates that future defect reduction requirements in this size range are modest. Future requirements for optical tool sensitivity are discussed further in section 4.

Another important factor in obtaining highly accurate optical detection near a tool's sensitivity limits is false counts that occur near a large defect, because of tails on the incident laser beam hitting the large defect when the beam is scanning an adjacent area. These counts are not reproducible in size or location, and with analysis of repeat scans the user can determine the radius around a large real defect within which smaller counts must be ignored. A cluster removal algorithm is applied to remove these counts from our results. The cluster radius is generally 500μm or less but depends on the size of the large central defect. On several wafers AFM has been used to verify that these are false counts. With 10-20 defects per wafer total, the total area within these false-count regions is small, so the chance of omitting a real defect by mistake is 0.1% or less. These counts are not considered in setting detection thresholds because they are removed beforehand based on proximity to the large defects.

In earlier work, sensitivity settings based on more limited analysis were too low, which gave extra added defects after coating, and false counts from clustering were not removed systematically. The progress in these areas demonstrates that rigorous standards for defect detection are as important to process development as improvements in the process itself.

3.3. Defect Results

The most common type of added defect is a flake of multilayer coating material, containing Mo and Si in similar proportion to the multilayer. Flakes account for about 0.04 defects/cm^2, on average over a period of several months in which the overall median added defect level was about 0.08 defects/cm^2. Several typical flake-type defects are shown in Figure 4. These defects appear to be added at random times during the deposition of the 81 layers; for example the first defect in Figure 4 has been dislodged slightly and shows a pit in the coating beneath it where it blocked deposition of the subsequent layers. Specific experiments are being designed to trace the origin of this type of defect.

3.4. Future Directions

Many defects have been characterized in detail by AFM and SEM, and the defect classes change as the coating process evolves. A longer-term goal is to identify the dominant defect classes by full review, then associate the physical dimensions with the optical scatter signatures by statistical classification techniques. In this way a significant fraction of defects can later be classified from the optical results alone, giving much more rapid feedback to coating process development. An example is the hillock defect on silicon substrates (Figure 5). Because of its very flat shape, it scatters light mostly forward and can be detected by the forward channel on the ADE Constellation tool. By comparison of hillock signals on the SP-1 and the ADE tools, it was also possible to distinguish two different shapes of hillocks. Hillocks were the dominant native defect species on our 150mm substrates, but they do not disturb the multilayer enough to be printable in an EUV lithography tool. Being able to identify then from optical inspection alone let us concentrate attention on printable defects that present real risk. Work to identify additional defect classes is underway.

4. DEFECT GROWTH CHARACTERIZATION

Small particles on the reticle substrate that are coated with a multilayer film serve to disturb the reflective multilayer and can potentially print to the wafer as a defect. Thus there is a strong need for techniques to study the evolution of multilayer film defects induced by small particles on the substrate. Gold nanospheres are well suited for this purpose; they are commercially available with controlled size distributions down to 10 nm in diameter. To study multilayer defect evolution, practical considerations require a reasonable density of monodisperse gold spheres on silicon wafers. This is because the gold spheres (and the resulting multilayer defects) need to be observable in statistically significant quantities on the silicon surface using an atomic force microscope. We have recently developed a technique for depositing relatively monodisperse gold nanospheres in significant quantities on silicon substrates.[6] The silicon wafers containing gold nanospheres are characterized before and after the Mo/Si deposition using techniques such as atomic force microscopy and transmission electron microscopy.

With the coating flux directed at the substrate at near-normal incidence, particles on the substrate tend to be smoothed over by the multilayer. This is shown in Figure 6a for a Mo/Si multilayer film deposited on a 30 nm diameter Au sphere on a silicon wafer, and in Figure 6b for a multilayer on a 60 nm diameter sphere. In Figure 6b

the small bump at the multilayer surface resulting from the 60 nm sphere on the substrate is clearly visible. Atomic force microscopy of the surface before and after deposition of a multilayer on a 30 nm diameter Au sphere is shown in Figure 7. The lateral size of the gold sphere prior to multilayer coating is a little exaggerated due to AFM tip effects on this high-aspect-ratio feature, but the lateral measurements after coating, as well as the height measurements both before and after coating, are accurate. The height of the bump at the multilayer surface after deposition on the 30 nm Au spheres is only 3 nm.

It may not be possible for commercial light scattering tools to be extended to the regime where substrate particles/defects below 55 nm in diameter can be routinely detected. But particles this small need to be eliminated because particles/defects below this size are expected to perturb the Mo/Si multilayer enough to result in a printable defect in an EUV lithography stepper.[7,8] Clearly there is a need for methods to address this issue. Based on the above work and on modeling we have proposed that buffer-layers could be employed to smooth over reticle substrate particles/defects.[9] If the buffer layer smoothing causes enough reduction in the defect height, volume and side-wall slope, the defect can be made invisible to the stepper's imaging optics and will not print to the wafer.

Figure 8 shows a strategy and timeline over which both conventional defect reduction can be extended and buffer-layer smoothing approaches can be developed. The upper curve shows expected progress in optical inspection tool sensitivity according to industry roadmaps, and we assume we can eliminate defects that can be detected optically by continued process improvement. The lower curve shows projected progress in the size of defect that can be made non-printable by progress in defect smoothing. Future work will be on continued defect reduction and optimizing our use of the optical scattering tools, and on improving the smoothing technology, to bring the two curves together and close the defect gap.

5. CONCLUSIONS

EUVL mask blank development has made strong progress in production of ultra-low-defect mask blanks, meeting its defect reduction milestones and producing lots of over 50 blanks with median added defects below 0.05/cm^2. Dominant native and added defect types have been identified. A strategy has been developed for elimination and mitigation of the remaining defects, using a smoothing layer to cover smaller defects, and the most sensitive existing bare wafer inspection tools to detect and eliminate larger defects. Our focus in continuing work is to systematically determine defect sources and characterize the multilayer coating process, in order to get the knowledge base to carry EUVL mask fabrication from development into industrialization.

ACKNOWLEDGEMENTS

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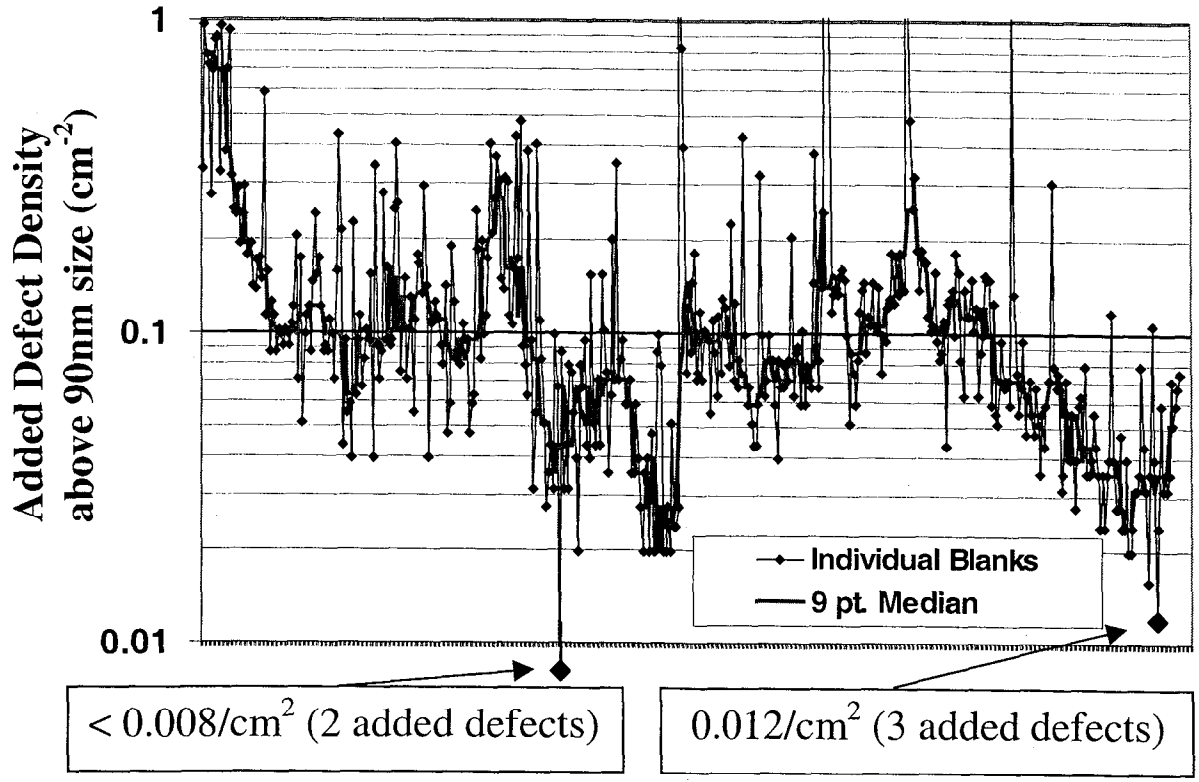

Figure 1. Defect reduction progress, over time, from 7/99 through 1/00. The target was changed during the Planned Maintenance (PM) at the start of the graph. The solid curve is a moving 9-point median to show the trend more clearly.

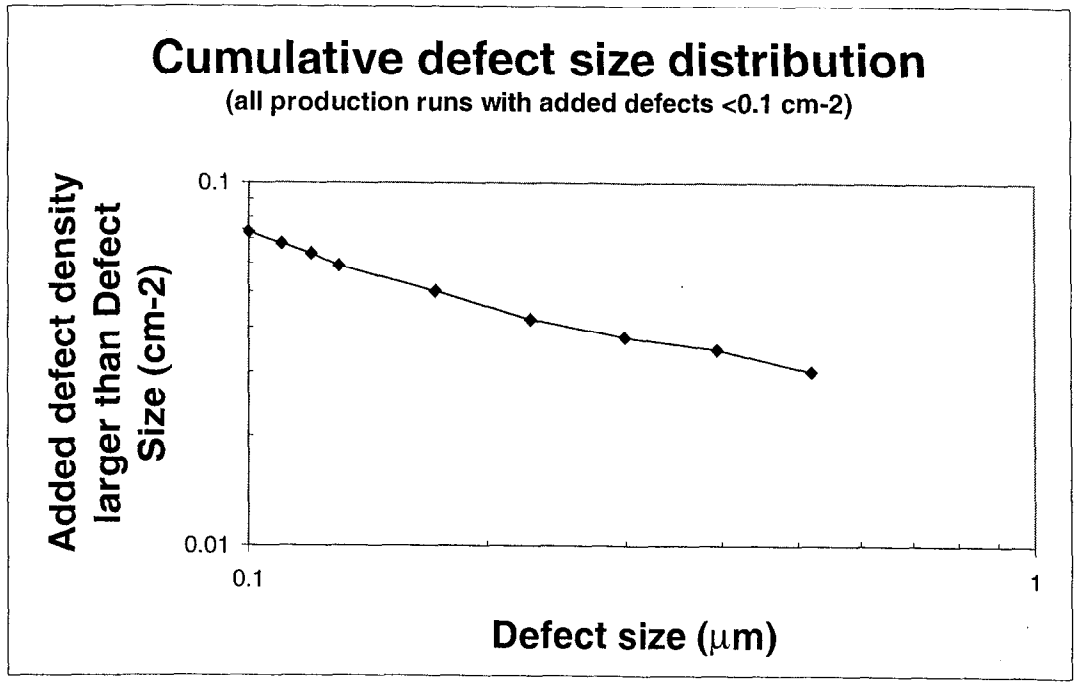

Figure 2. Cumulative histogram of defect sizes; each point is "total defects larger than". The current detection limit is 90nm. Extrapolating this curve to total defects larger than 50nm gives only 50% more defects.

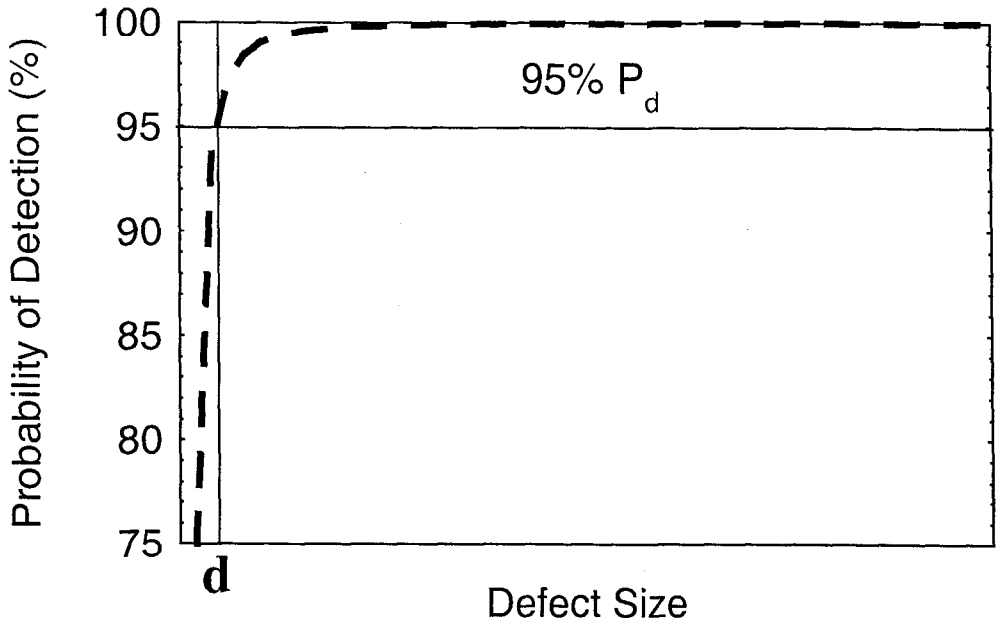

Figure 3. Figurative capture ratio vs. size for overall detection on both optical tools. With current tools d ≈ 90nm.

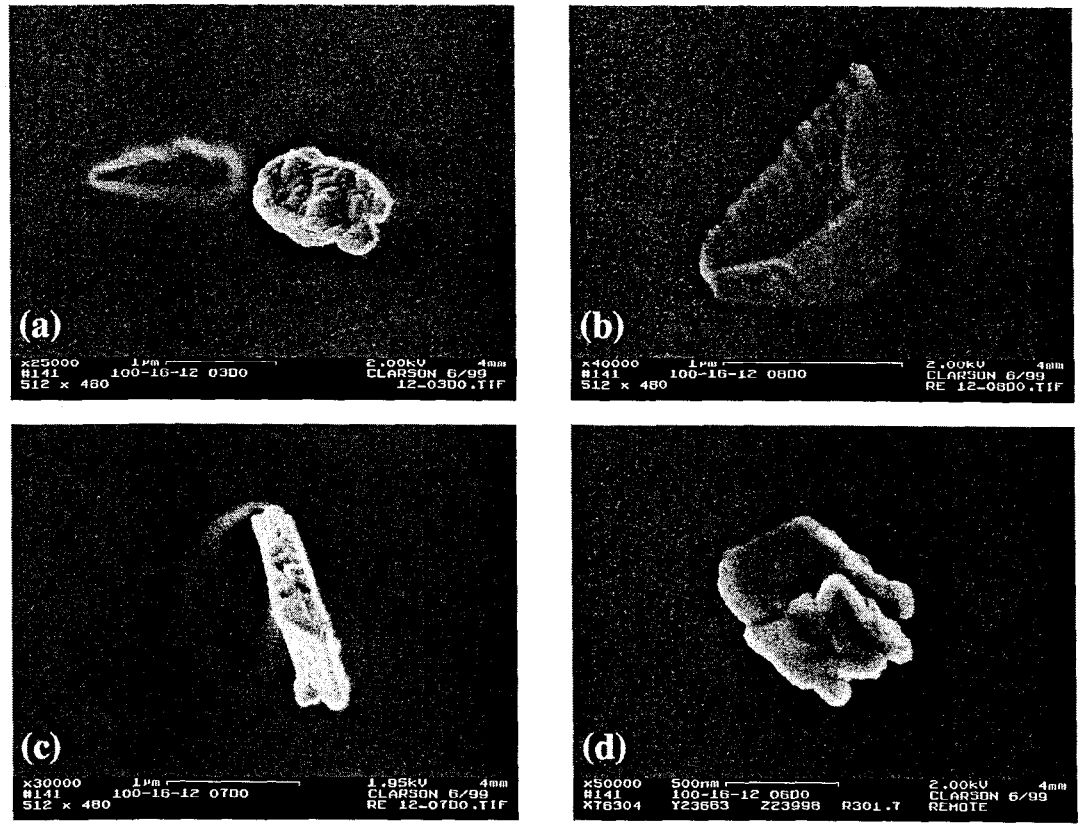

Figure 4. Four typical flake-type defects found on Mo/Si multilayer-coated mask blanks. Defect (a) has been dislodged slightly, showing a region beneath where it blocked the deposition. The defects are shown by EDS to be composed of Mo and Si in similar composition to the overall multilayer.

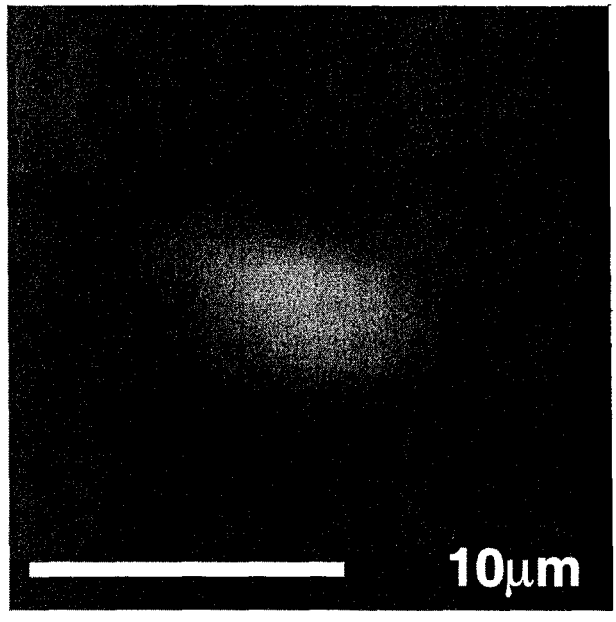

Figure 5. Hillock defect on bare Si. Defect height is only ~2nm, so aspect ratio is ~1000:1. The shape measured by AFM is unchanged after multilayer coating. Modeling shows this defect will not print in EUV lithography.

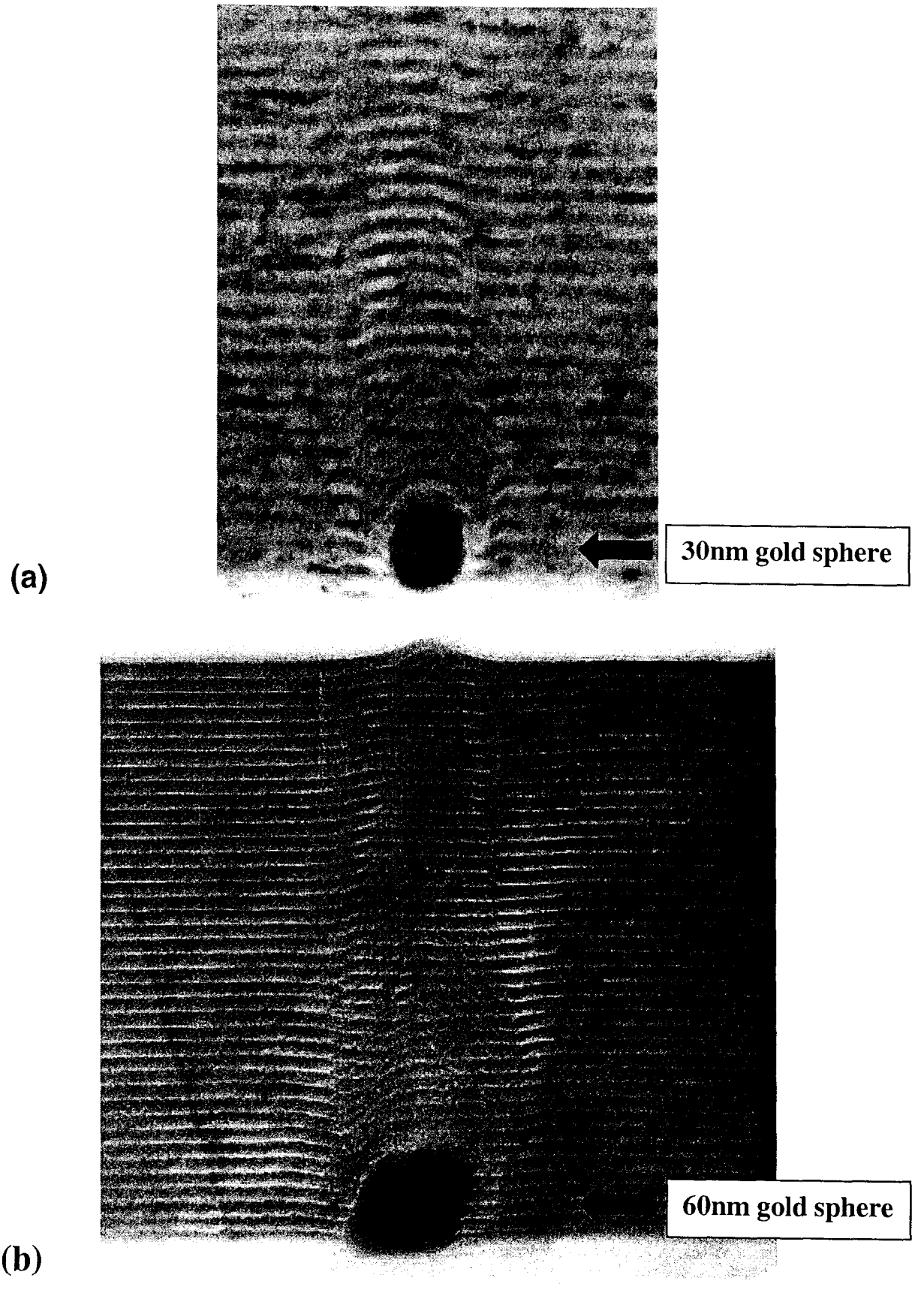

Figure 6. Cross sectional transmission electron microscopy image for ion beam sputtered Mo/Si multilayer films on (a) 30nm diameter and (b) 60nm diameter gold spheres.

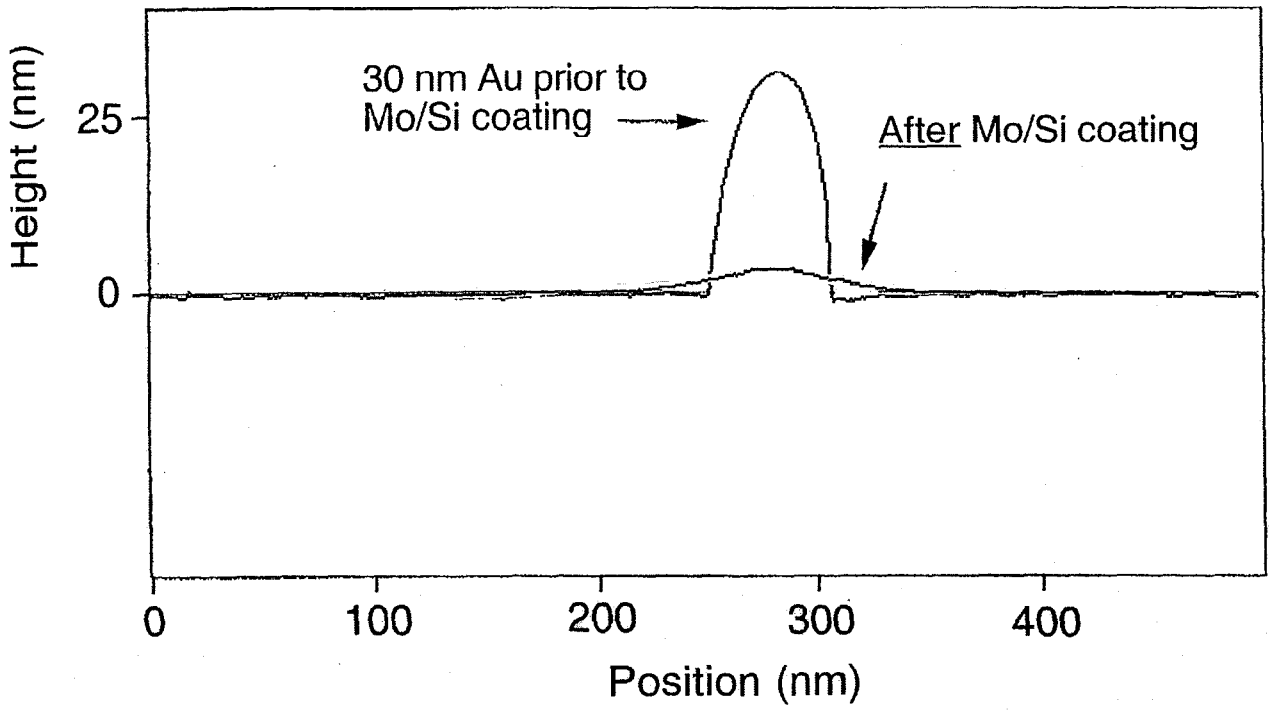

Figure 7. Surface topography of a silicon wafer with a 30 nm diameter gold sphere before and after Mo/Si multilayer coating. The surface topography was extracted from atomic force microscopy scans.

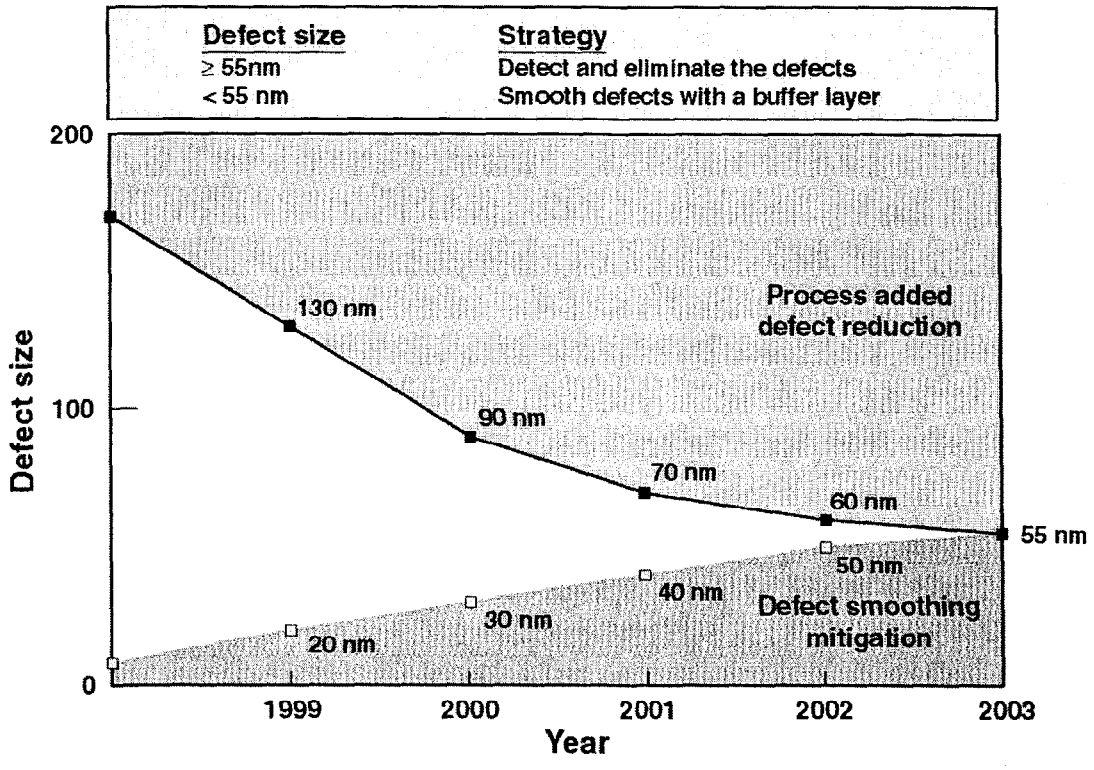

Figure 8. Potential strategy and timeline for defect mitigation on reticle blanks for EUV Lithography.