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Extremely Bendable, High-Performance Integrated Circuits Using Semiconducting Carbon Nanotube Networks for Digital, Analog, and Radio-Frequency Applications

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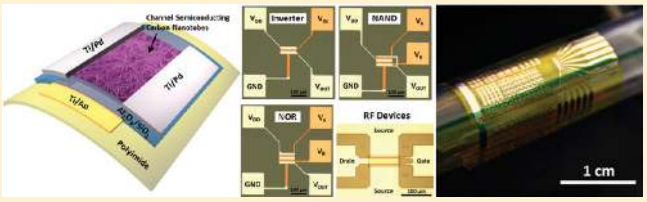
Supporting Information

ABSTRACT: Solution-processed thin-films of semiconducting carbon nanotubes as the channel material for flexible electronics simultaneously offers high performance, low cost, and ambient stability, which significantly outruns the organic semiconductor materials. In this work, we report the use of semiconductor-enriched carbon nanotubes for high-performance integrated circuits on mechanically flexible substrates for digital, analog and radio frequency applications. The as-obtained thin-film transistors (TFTs) exhibit highly uniform device performance with on-current and transconductance up to 15 μA/μm and 4 μS/μm. By performing capacitance−voltage measurements, the gate capacitance of the nanotube TFT is precisely extracted and the corresponding peak effective device mobility is evaluated to be around 50 $cm^2V^{-1}s^{-1}$. Using such devices, digital logic gates including inverters, NAND, and NOR gates with superior bending stability have been demonstrated. Moreover, radio frequency measurements show that cutoff frequency of 170 MHz can be achieved in devices with a relatively long channel length of 4 μm, which is sufficient for certain wireless communication applications. This proof-of-concept demonstration indicates that our platform can serve as a foundation for scalable, low-cost, high-performance flexible electronics.



KEYWORDS: *Flexible electronics, thin-film transistors, semiconducting nanotube networks, integrated circuits, radio frequency applications*

Thin-film transistors (TFTs) are widely used in macroelectronic integrated circuits or active-matrix backplanes for display and sensor applications. Amorphous silicon and polysilicon as the most common TFT channel material being widely used in liquid crystal display (LCD) and organic light-emitting diode (OLED) displays lack the transparency and flexibility and are thus unsuitable for flexible electronic applications.[1−3] On the other hand, organic TFTs offer excellent flexibility and low-cost fabrication but suffer from extremely low device performance and are susceptible to moisture and oxygen.[4−7] Therefore, one of the major challenges for the flexible electronics is to find the optimal channel material that can simultaneously offer low-cost fabrication, room-temperature processing, flexibility, superior device performance, and possibly even transparency. Single-walled carbon nanotubes possess extraordinary electrical properties (high intrinsic mobility and ballistic transport)[8−10] and thin-films of nanotubes are found to meet all the criteria for flexible TFTs described above.[11−16]

Recently, significant advance has been made toward flexible nanotube TFTs with outstanding electrical performance and sophisticated flexible integrated circuits such as flip-flop and decoder have been demonstrated.[16,17] Despite the tremendous success, a few important issues still await to be further improved. First of all, only as-grown carbon nanotubes are used in those previous reports on flexible nanotube integrated circuits. With roughly 33% nanotubes being metallic, extra steps such as strip patterning,[16] or filtration to obtain y-junctions[17] are necessary in order to cut the metallic path through the transistors to make the devices depletable. This adds more difficulties to the fabrication process and the repeatability and uniformity of devices are uncertain. Second, in all the previous publications on nanotube TFTs the device mobility is typically derived using gate capacitance values calculated from either parallel plate model or a more rigorous cylindrical model by considering the electrostatic coupling between the nanotubes.[15,18] While the parallel plate model obviously underestimates the device mobility, the more rigorous model still lacks accuracy due to the uncertainty in quantifying the density and diameter for a random network containing hundreds of thousands of carbon nanotubes. Therefore, in order to accurately evaluate the mobility of the nanotube TFTs it is

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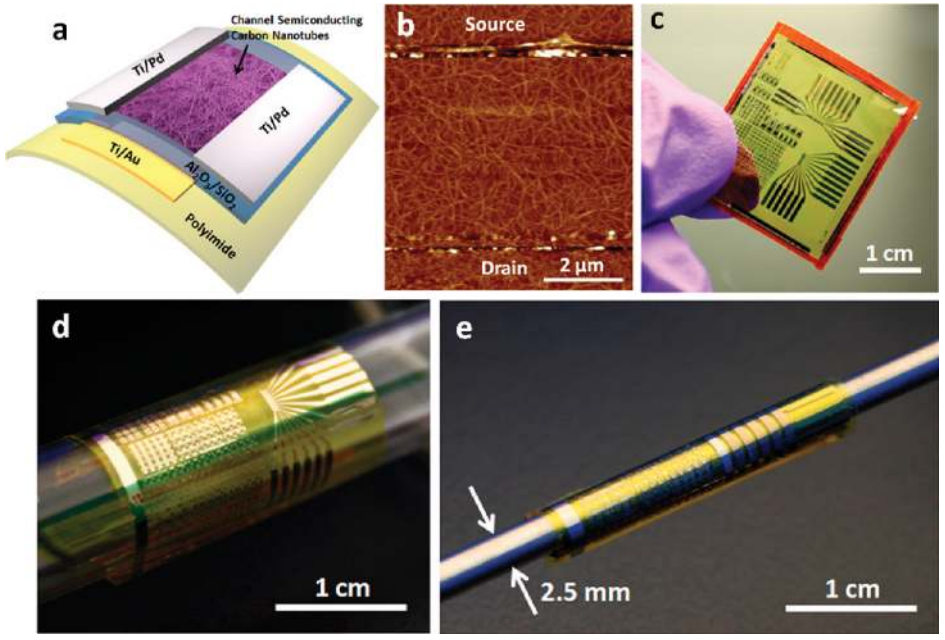

Figure 1. Flexible thin-film transistors and integrated circuits using semiconducting carbon nanotube networks. (a) Schematic diagram of a local-gated nanotube TFT on a flexible substrate. (b) AFM image showing the channel of the flexible nanotube TFT, which consists of random networks of semiconducting carbon nanotubes. (c) Photograph of a flexible nanotube circuit with a size of ~2.5 × 3 cm^2. (d,e) Photographs showing the extreme bendability of the flexible nanotube circuits, where the samples are being rolled onto a test tube with a diameter of 10 mm (d), and a metal rod with a diameter of 2.5 mm (e).

important to perform capacitance−voltage (C−V) measurements to directly measure the gate capacitance of the device. Lastly, carbon nanotubes, especially semiconducting-only carbon nanotubes hold great potential for applications in radio frequency (RF) electronics.[19−23] However, the RF applications of the flexible nanotube TFTs are not yet fully explored in the literature. In one report, where gigahertz operation has been achieved in flexible nanotube RF transistors,[22] the use of dielectrophoresis (DEP) to deposit the nanotubes and e-beam lithography to fabricate the transistors contradict the idea of going toward scalable, low-cost, flexible electronics. Besides, due to the use of unsorted carbon nanotubes and DEP, which attracts mainly metallic nanotubes,[24] the resulting RF transistor exhibits almost no gate modulation, which is undesirable for meaningful circuit applications.

The use of high purity semiconducting carbon nanotubes separated by density gradient ultracentrifugation[25] for high-performance nanotube TFTs has been demonstrated by a few groups including our own.[14,26−28] In light of the above-described limitations, we report the extension of our well-established solution-processed semiconducting nanotube TFT platform to the application in high-performance flexible integrated circuits. We have systematically studied the electrical performance of the flexible nanotube TFTs and performed C−V measurements to the nanotube TFTs to precisely evaluate the effective device mobility. Such transistors exhibit superior on-current density, transconductance, and effective device mobility of up to 15 $\mu A/\mu m$, 4 $\mu S/\mu m$, and 50 $cm^2V^{-1}s^{-1}$, respectively, which represents one of the best reported performance for flexible TFTs to date. Such transistors have been utilized in the demonstration of circuits such as inverter/inverting amplifier, NAND, NOR gates, and RF transistors. Owing to the use of very thin polyimide (PI) substrates, the devices and circuits are highly flexible and bendable, and show minimal performance degradation under repeated bending tests. Moreover, RF measurements reveal that our flexible transistors with a channel length of 4 μm exhibit intrinsic cutoff frequency (f_t) of 170 MHz and maximum oscillation frequency (f_{max}) of 118 MHz, which is sufficient for certain wireless communication applications such radio, RFID, and so forth. Such performance is respectable considering the relatively long channel length used, and further scaling-down should boost the performance significantly. Our platform significantly outruns the previous demonstrations in the literature using organic TFTs and carbon nanotube TFTs with unpurified carbon nanotubes. It could serve as a foundation for future research on nanotube-based high performance, low cost, flexible electronics.

The platform for the fabrication of high-performance flexible transistors and integrated circuits using preseparated semiconducting nanotubes is illustrated in Figure 1. Polyimide (HD MicroSystems, Inc. PI-2525) serving as the substrate is spun coated and cued on the silicon handling wafer following the methods reported in our previous publications.[28,29] On top of the PI substrate, Ti/Au (5/30 nm) back-gate electrodes are defined by photolithography and lift-off. Twenty nanometers of Al_2O_3 and 15 nm of SiO_x are then deposited using atomic layer deposition and e-beam evaporation, respectively, to serve as the gate dielectric. In order to deposit uniform semiconducting nanotube networks throughout the sample, poly-L-lysine solution (0.1% w/v in water; Sigma Aldrich) is used to functionalize the SiO_x surface for 5 min to form amine-terminated adhesion layer followed by a deionized (DI) water rinse, and the sample is subsequently immersed into the commercially available 0.01 mg/mL semiconducting nanotube solution (NanoIntegris Inc.) for 15 min followed by DI water and isopropanol rinse and then blow dry in nitrogen.[14,27,28] After the deposition of the nanotube networks, the sample is annealed in a vacuum oven at 200 °C for 1 h in order to remove surfactant residues.[28] Via holes are then patterned using

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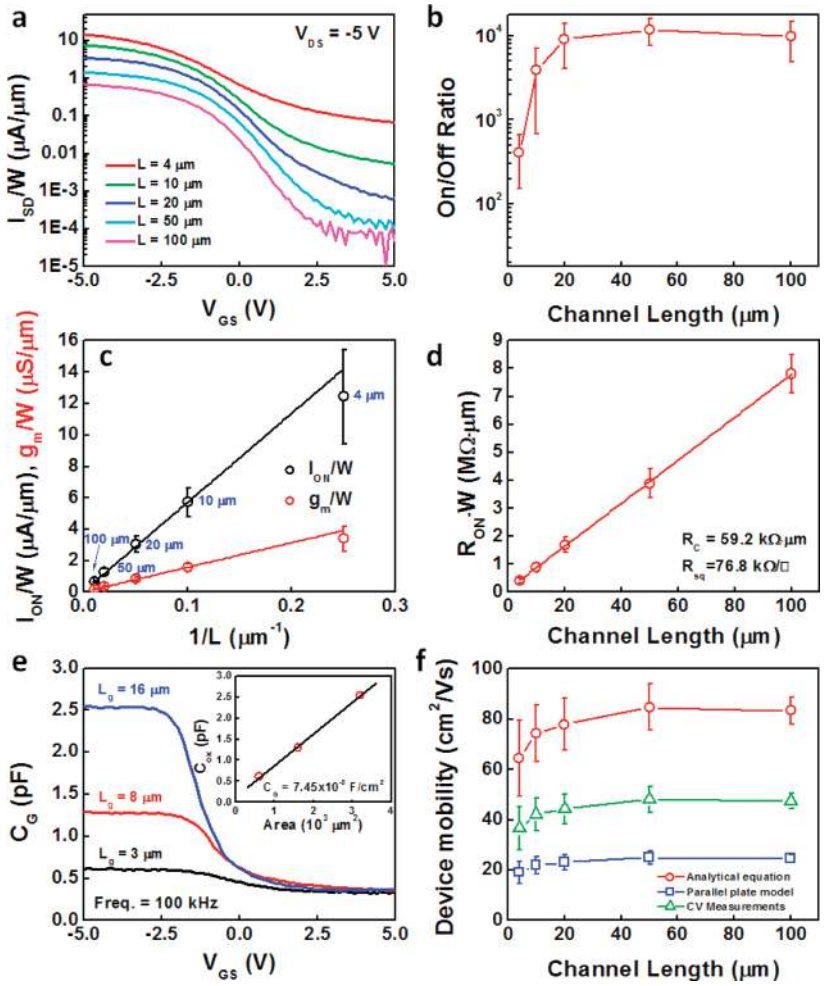

Figure 2. High-performance flexible semiconducting nanotube transistors. (a) Transfer characteristics of the flexible nanotube TFTs with various channel lengths (4, 10, 20, 50, and 100 μm) measured at $V_{DS} = -5$ V. (b) Plot of I_{on}/I_{off} as a function of channel length for $V_{DS} = -5$ V. (c) I_{on}/W at $V_{GS} = -5$ V and peak g_m/W as a function of $1/L$ for $V_{DS} = -5$ V. (d) Normalized on-state resistance at $V_{GS} = -5$ V as a function of the channel length. (e) $C-V$ characteristics of the flexible nanotube transistors with various channel lengths measured at 100 kHz. Inset: gate capacitance as a function of channel area. The corresponding gate capacitance is extracted to be 7.45×10^{-8} F/cm^2. (f) Field-effect mobility of the flexible nanotube TFT as a function of channel length. The plot compares the mobility values extracted using gate capacitance derived from parallel plate model, cylindrical model, and $C-V$ measurements.

photolithography and HF etch to allow the interconnection between the gate and drain of the transistors to form the diode-connected load transistors. In the end, Ti/Pd (0.5/35 nm) source–drain electrodes are formed and one more step of photolithography plus oxygen plasma is used to etch away the unwanted nanotubes and define the active channel region.

The schematic diagram of a completed local-gated nanotube TFT on flexible substrate, and the corresponding atomic force microscopy (AFM) image showing the channel of the device are exhibited in Figure 1a,b, respectively. In this work, semiconducting nanotubes with purity of 98 or 99% (as-received, NanoIntegris) are used and the nanotube network presented in the AFM image (density around 40–50 tubes/μm^2) is found to be highly uniform throughout the sample, which is critical for achieving uniform device and circuit performance. Furthermore, by using thin PI substrates (12 μm in this work), the fabricated circuits are highly flexible and bendable. As shown in Figure 1c–e, a flexible nanotube circuit sample with a size of ~2.5 × 3 cm^2 (panel c) can be rolled onto a test tube with a diameter of 10 mm (panel d) or even a metal rod with a diameter of 2.5 mm (panel e).

We first characterize the electrical performance of the flexible semiconducting nanotube TFTs. The transfer characteristics of five representative devices with channel lengths of 4, 10, 20, 50, and 100 μm measured at $V_{DS} = -5$ V are presented in Figure 2a. On the basis of the results, the device on/off current ratio (I_{on}/I_{off}), unit-width (W, source/drain width) normalized on-current density (I_{on}/W), normalized transconductance (g_m/W), and normalized on-state resistance ($R_{on}\cdot W$) are extracted and plotted as a function of channel length as shown in Figure 2 panels b–d. It is important to point out that our transistor performance is highly uniform with very small device-to-device variations, and the standard deviation of the device parameters divided by the average value is typically between 10 to 15% (Supporting Information Figure S1).[28] This is due to the highly uniform nature of the nanotube thin-film obtained using our method, and it is critical for achieving meaningful and practical carbon nanotube integrated electronic systems.

Figure 2b shows the I_{on}/I_{off} as a function of channel length for $V_{DS} = -5$ V. As the channel length increases from 4 to 100 μm, the average on/off ratio increases from 400 to 10^4 due to the decrease in the probability of percolative transport through

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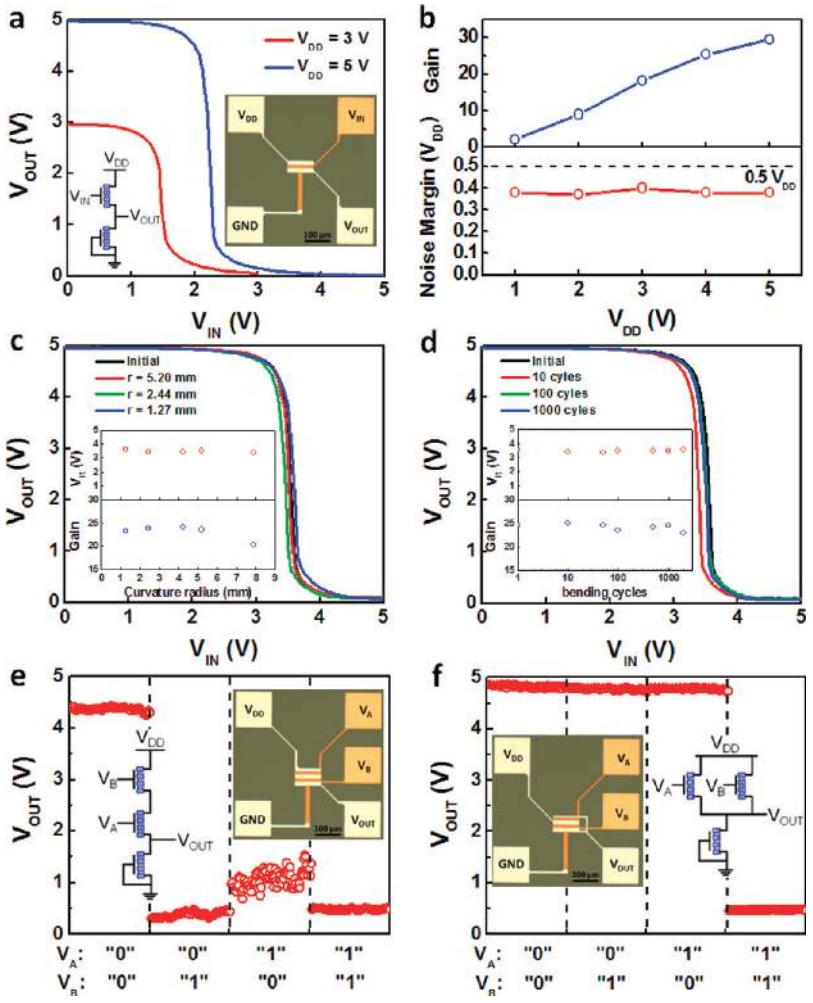

Figure 3. Flexible nanotube integrated circuits. (a) Inverter voltage transfer characteristics measured with V_{DD} of 3 or 5 V. Inset: Schematic and optical microscope image of the diode-loaded nanotube inverter. (b) Inverter gain and noise margin as a function of supply voltage V_{DD}. (c) Inverter VTC measured at various curvature radii. Inset: Inverter threshold voltage and gain as function of curvature radius, showing minimal performance change even when bent down to 1.27 mm of bending radius. (d) Flexible inverter reliability test. The inverter VTC are measured after various numbers of bending cycles and the performance remains almost unchanged after 2000 cycles. (e,f) Output characteristics of the diode-loaded 2-input NOR (e) and NAND (f) circuits. The V_{DD} for both circuits are 5 V. Input voltages of 5 and 0 V are treated as logic "1" and "0", respectively. Inset: Schematic and optical microscope image of the corresponding circuits.

the metallic nanotubes. The results indicate that channel length of ~10 μm is necessary for digital logic circuits, while smaller channel length such as 4 μm is good enough for analog and radio frequency applications for the nanotube density used in this study. In Figure 2c, the I_{on}/W and g_m/W are plotted as a function of $1/L$ for $V_{DS} = -5$ V. Both device parameters are approximately inversely proportional to the channel length, indicating good uniformity of the flexible nanotube transistors. The best on-current density and transconductance are measured to be 15 μA/μm and 4 μS/μm for devices with L = 4 μm (Supporting Information Figure S1), which is among one of the best performance achieved from flexible carbon nanotube TFTs.[16,17,28] Figure 2d presents the normalized on-state channel resistance as a function of channel length. From this figure, the contact resistance (R_c = 59.2 k$\Omega\cdot\mu$m) and on-state sheet resistance (R_{sh} = 76.8 k$\Omega/\square$) can be extracted from the y-axis intercept divided by 2 and slope, respectively.

On the basis of the device transconductance, we can further extract the field-effect device mobility of the flexible nanotube transistors. In order to accurately assess the mobility, it is important to use precise gate capacitance (C_G) values. In the previous publications, the C_G is typically calculated using either parallel plate model[17] or a more rigorous cylindrical model by considering the electrostatic coupling between the nanotubes.[15,18] For the parallel plate model, the lack of accuracy is obvious and the device mobility is always underestimated. For the more accurate cylindrical model (analytical equation) developed by Rotkin and Rogers et al.,[15,18] the complication is that the calculated C_G value is very sensitive to the nanotube diameter and density used in the calculation (Supporting Information Figure S2), but both the diameter and density are very difficult to quantify for such a random network with large numbers of nanotubes. Therefore, in this work, we have performed $C-V$ measurements to directly measure the C_G of the flexible nanotube TFTs in order to accurately evaluate the mobility of our devices.

The $C-V$ characteristics of the flexible nanotube transistors with various channel lengths measured at 100 kHz are shown in Figure 2e. For such $C-V$ measurements, devices with underlap gates (gate length L_g = 3, 8, 16 μm, S/D length L = 4, 10, 20 μm, and channel width W = 200 μm) are used for minimized parasitic capacitance and more details about the $C-V$

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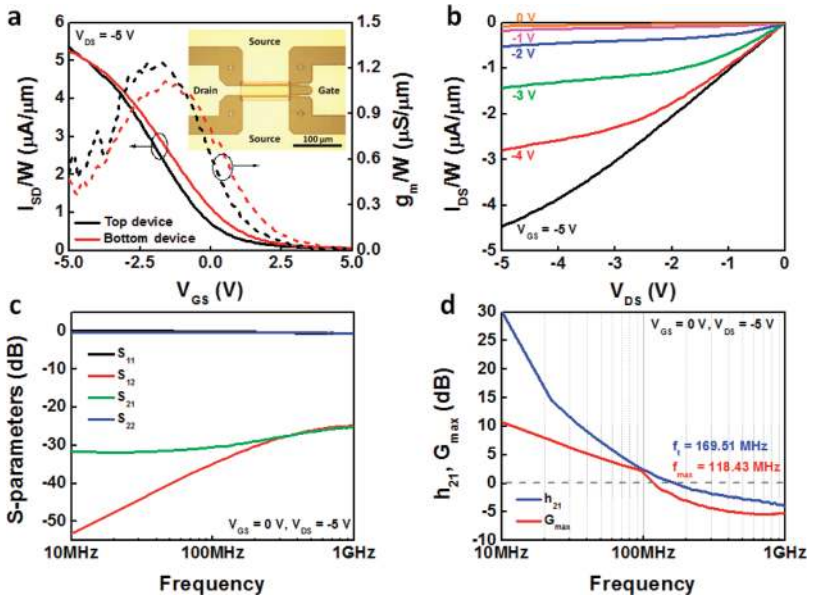

Figure 4. Flexible nanotube RF transistors. (a) Transfer characteristics of a flexible nanotube RF transistor with a channel length of 4 μm, gate length of 3 μm, and channel width of 100 μm, measured at V_{DS} = −5 V. Inset: Optical microscopy image of the corresponding device. (b) Output characteristics of the same device shown in panel a. (c) Measured S-parameters for the flexible nanotube RF transistor from 10 MHz to 1 GHz. The transistor is biased at V_{GS} = 0 V and V_{DS} = −5 V for optimal performance. (d) Intrinsic current gain h_{21}, and maximum available gain G_{max} derived from the S-parameters.

measurement setup can be found in the Supporting Information (Figure S3). The gate capacitance values in the accumulation region (V_{GS} = −5 V) for different devices are extracted and plotted as a function of channel area as shown in Figure 2e inset. From the slope, the gate capacitance per unit area (C_{ox}) is extracted to be 7.45 × 10^{-8} F/cm^2. In addition, from the C−V results measured under different frequencies, the interface trap density (D_{it}) of the device is estimated to be around 6 × 10^{11} cm^{-2} eV^{-1} using the physical area of the device instead of the surface area of the carbon nanotubes (Supporting Information Figure S3). This is a low D_{it} value for a flexible device and arises from the lack of surface dangling bonds on carbon nanotubes.

Using the C_{ox} value measured above, the field-effect device mobility can be further derived using the following equation

$$\mu_{device} = \frac{L}{V_D C_{ox} W}\frac{dI_d}{dV_g} = \frac{L}{V_D C_{ox}}\frac{g_m}{W}$$

where L and W are the device channel length and width, V_D = 5 V, and C_{ox} = 7.45 × 10^{-8} F/cm^2. The as-obtained device mobilities are plotted in Figure 2f and are compared with the mobilities derived using parallel plate model and cylindrical model. For the parallel plate model, the effective oxide thickness (EOT) of the gate dielectric is 24.1 nm, which corresponds to a C_{ox} of 1.43 × 10^{-7} F/cm^2. For the cylindrical model (Supporting Information Figure S2), t_{ox} = 24.1 nm, nanotube diameter d = 1.4 nm, and nanotube density $1/\Lambda_0$ = 10 tubes/μm are used to estimate the gate capacitance, yielding a C_{ox} value of 4.23 × 10^{-8} F/cm^2. From Figure 2f, one can find that the parallel plate model underestimates the mobility while the cylindrical model overestimates it. The actual device mobility for our flexible nanotube transistor is around 45 cm^{2}V^{-1}s^{-1} on average and 55 cm^{2}V^{-1}s^{-1} for the best case.

In order to design meaningful and practical nanotube integrated circuits, it is important to have a compact model that can be used to simulate the device and circuit performance. Using the device parameters extracted above, the flexible nanotube TFTs can be modeled using a simple level 1 SPICE model (Supporting Information S4). The results indicate that even a primitive level 1 model can provide simulated performance that match the experimental results relatively closely, which should work well for simulating and predicting the DC performance of the circuits. Further optimization of the model by including more nonideal effects, underlying physics in the nanotube networks, and device frequency response should improve the accuracy and enable more sophisticated simulations.

Our ability to fabricate high-performance, uniform flexible nanotube TFTs and the use of the compact nanotube TFT device model enable us to further explore their applications in various integrated circuit applications including digital, analog, and radio frequency. For the proof-of-concept purpose, we first demonstrate the basic digital functional blocks such as inverter, 2-input NAND, and NOR gates as shown in Figure 3. The voltage transfer characteristics (VTC) measured at V_{DD} = 3 or 5 V for a diode-loaded inverter are shown Figure 3a, whose schematic and optical microscope image are shown as the inset. Measurements reveal that the V_{OUT} decreases from V_{DD} to 0 V as V_{IN} increases from 0 to V_{DD}, meaning that the circuit is functioning correctly as a logic inverter. Besides, symmetric input/output behavior is achieved in such inverters, meaning that both input and output are operated under the same voltage range. This characteristic is important for single power supply voltage operation and is crucial for cascading logic blocks for larger scale integration where the output of the preceding logic block needs to be able to drive the ensuing logic block directly.

On the basis of the VTC measured under different V_{DD} biases, the inverter gain and noise margin are extracted and plotted as a function of V_{DD} (Figure 3b and Supporting Information Figure S5). The p-type-only inverter exhibits a respectable voltage gain of 30 at V_{DD} = 5 V and the noise margin remains close to 0.4 V_{DD}, indicating that the circuit is

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highly immune to environmental electrical noise. Besides, the inverter VTC shows minimal performance change under various curvature radii down to 1.27 mm (Figure 3c) and the performance does not degrade after as many as 2000 bending cycles (manually bent to a curvature radius of ~2.5 mm) as shown in Figure 3d. Such inverter also works well as an inverting amplifier and provides AC gain up to 6.5 dB as shown in the Supporting Information (Figure S6). In addition to inverters, more sophisticated circuits such as 2-input NAND and NOR have also been demonstrated. Both circuits are operated with a V_{DD} of 5 V and input voltages of 5 and 0 V are treated as logic "1" and "0", respectively. The output characteristics shown in Figure 3e for NOR and Figure 3f for NAND confirm the correct functioning of the circuits. For the flexible transistors and integrated circuits discussed above, it is worth mentioning that under extreme bending conditions (e.g., folding), the Al_2O_3/SiO_x dielectric can crack and cause gate leakage in the devices due to the fragile nature of the dielectric materials. Therefore, mechanically flexible dielectrics and electrode and interconnection materials should be explored in the future in order to further improve the bendability of the sample.

In the end, we characterize the RF performance of the transistors to examine the potential of using flexible nanotube TFTs for wireless communication applications. As shown in Figure 4a inset, the device is configured into the ground-signal-ground (GSG) coplanar waveguide structure containing a pair of nanotube channels to allow microwave measurements. The device is designed to have slightly underlaped gate (S/D length of 4 μm and a gate length of 3 μm) in order to minimize the parasitic capacitance. According to the DC transfer (Figure 4a) and output (Figure 4b) characteristics, the optimal DC bias points are determined and the S-parameters of the device are measured by a vector network analyzer (VNA). On the basis of the S-parameters (Figure 4c), we can further derive the current gain (h_{21}) and maximum available gain (G_{max}) using the well-known relations.[30] In order to extract the intrinsic device performance, the as-measured data is de-embedded using the on-chip open and short de-embedding structures in order to remove the parasitic effects (Supporting Information S7). The intrinsic f_t and f_{max} of the transistor are derived to be 170 and 118 MHz, respectively, as shown in Figure 4d. This performance is impressive considering the relative long channel length of ~4 μm patterned by the contact aligner used in this study. It should be noted that the fabrication of this channel length is compatible with printing processes, thereby, a fully printed RF transistor is feasible in the future. With such f_t, wide range of wireless applications including radio and RFID can be enabled, and scaling down of the channel length should further boost the device performance, allowing more applications requiring larger bandwidth such as Wi-Fi or cellular.

In conclusion, we report the use of high-performance semiconducting nanotube thin-film transistors for extremely bendable flexible electronics, including the applications in digital, analog, and radio frequency devices and circuits. Inverter/inverting amplifiers, NAND, and NOR gates have been demonstrated, and RF measurements reveal that our flexible transistors offer intrinsic f_t of 170 MHz, which is high considering the long channel length of our devices. In addition, we have performed $C-V$ measurements of the nanotube TFTs to precisely evaluate the device mobility, which can serve as a guideline for future research in this field. Our platform significantly outruns the previous demonstrations in the literature using organic TFTs and carbon nanotube TFTs with unpurified carbon nanotubes and could serve as a foundation for future research on nanotube-based high performance, low cost, flexible electronics.

■ ASSOCIATED CONTENT

Supporting Information

Uniformity of the flexible semiconducting nanotube TFTs (S1); analytical equation for gate capacitance calculation (S2); $C-V$ measurement setup and D_{it} extraction (S3); SPICE modeling of the flexible nanotube TFTs (S4); inverter gain and noise margin as a function of V_{DD} (S5); step response and frequency response of the inverting amplifier (S6); short-open-load-through (SOLT) de-embedding for the flexible nanotube RF transistors (S7). This material is available free of charge via the Internet at http://pubs.acs.org.

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Notes

The authors declare no competing financial interest.

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Extremely Bendable, High Performance Integrated Circuits Using Semiconducting Carbon Nanotube Networks for Digital, Analog, and Radio-Frequency Applications

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Supporting Information

S1. Uniformity of the flexible semiconducting nanotube TFTs

The transfer characteristics of 100 flexible nanotube TFTs with various channel lengths are plotted in Figure S1a and the corresponding g_m-V_{GS} characteristics are presented in Figure S1 panel b to f. The transistors exhibit uniform performance and the standard deviation of g_m/W divided by their average value ranges from 23.1% to 6.4% as the channel length increases from 4 to 100 μm. As the channel length increases, more nanotubes are incorporated into the channel so that the devices become more uniform.

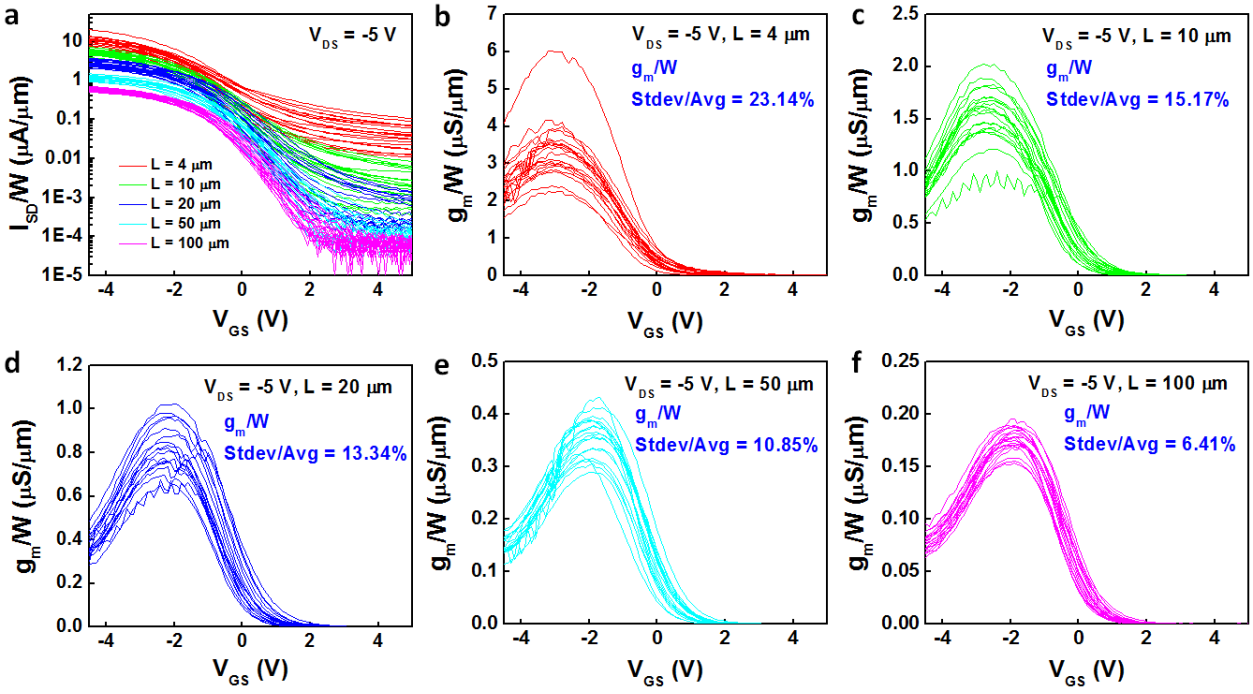

Figure S1. Uniformity of the flexible nanotube RF transistors. (a) Transfer characteristics of 100 flexible nanotube TFTs with various channel lengths (4, 10, 20, 50, and 100 μm) measured at V_{DS} = -5 V. (b-f). g_m-V_{GS} characteristics of the devices with channel length of 4 μm (b), 10 μm (c), 20 μm (d), 50 μm (e), and 100 μm (f).

S2. Analytical equation for gate capacitance calculation

The gate capacitance can be calculated by considering the electrostatic coupling between nanotubes using the analytical equation below[1,2]

$$C_{ox} = \left\{ C_Q^{-1} + \frac{1}{2\pi\varepsilon_0\varepsilon_{ox}} \ln\left[\frac{\Lambda_0}{R} \frac{\sinh(2\pi t_{ox}/\Lambda_0)}{\pi} \right] \right\}^{-1} \Lambda_0^{-1}$$

where $1/\Lambda_0$ stands for the density of nanotubes, $C_Q = 4.0\times10^{-10}$ F/m is the quantum capacitance of nanotubes and the value is taken from a previous report,[3] t_{ox} = 24.1 nm is the effective oxide thickness (EOT) of 20 nm Al_2O_3 plus 15 nm SiO_2, R is the radius of nanotubes, and $\varepsilon_0\varepsilon_{ox} = 3.9\times8.85\times10^{-14}$ F/cm is the dielectric constant of SiO_2. On the basis of the above equation, the gate capacitance (C_G) is calculated for different nanotube density and diameter and the results are plotted in Figure S2. From the figure, it is obvious that C_G is heavily dependent on the density and diameter used in the calculation.

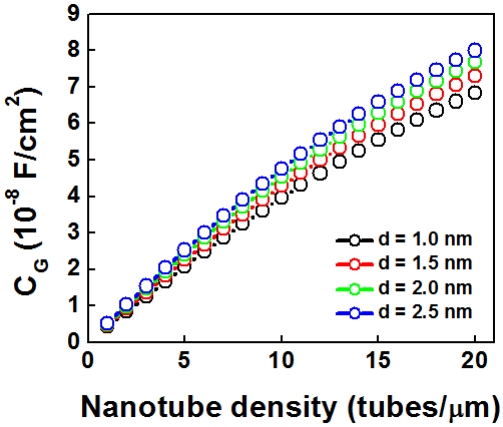

Figure S2. Gate capacitance calculated using the analytical equation for different nanotube density and diameter.

S3. C-V measurement setup and D_{it} extraction

The C-V measurement setup is illustrated in Figure S3a. The gate of the transistor is connected to the HIGH terminal while the source and drain are both connected to the LOW terminal of the C-V analyzer (Agilent B1500A). Unlike the overlap-gate devices used for the I-V characterization, the devices used for C-V measurements have slightly underlapped gate in order to minimize the effect from the parasitic capacitance. The optical microscope images of three representative devices with different channel lengths used in this study are shown in Figure S3b.

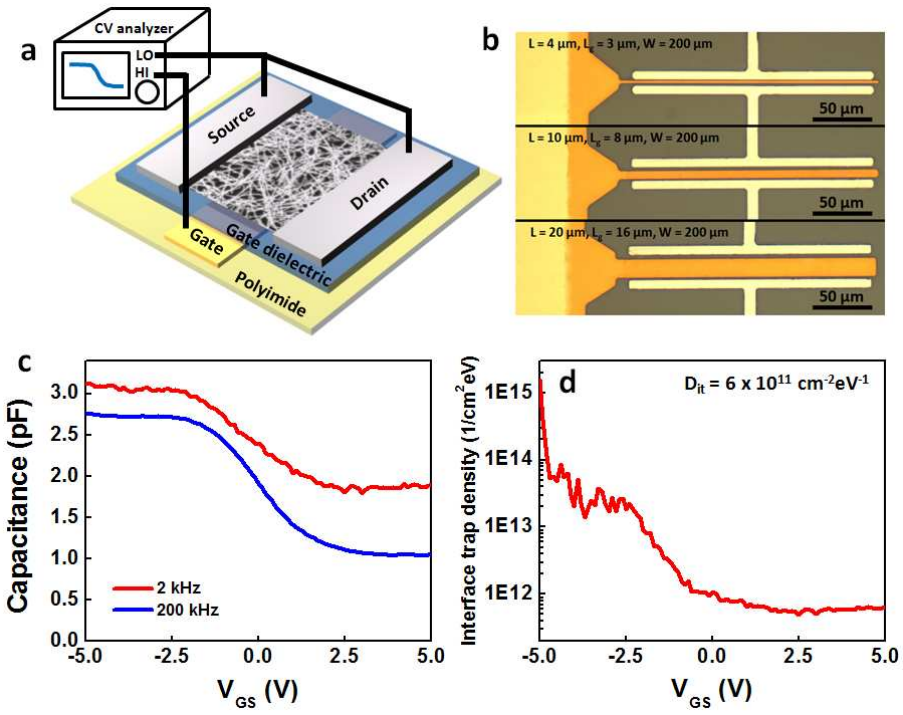

Figure S3. C-V measurement setup and interface trap density (D_{it}) extraction. (a) C-V measurement setup used in this study. (b) Optical microscope images of the underlap-gated devices for the C-V measurement. (c) C-V characteristics of a flexible nanotube TFT with L = 20 μm, L_g = 16 μm, and W = 200 μm measured at 2 kHz and 200 kHz. (d) Interface trap density (D_{it}) extracted from the C-V measurements.

The interface trap density of the device can be extracted by performing the C-V measurements at high and low frequencies and then calculated using the equation below.[4] The interface trap density is measured to be 6×10^{11} $cm^{-2}eV^{-1}$ at room temperature.

$$D_{it} = \frac{C_{LF} - C_{HF}}{q\left(1 - \frac{C_{LF}}{C_{ox}}\right)\left(1 - \frac{C_{HF}}{C_{ox}}\right)W \cdot L}$$

S4. SPICE modeling of the flexible nanotube TFT

The flexible nanotube TFTs are modeled using a simple level 1 SPICE model using the device parameters extracted from the measurements shown in Figure 2 of the manuscript. Using the parameters summarized in Figure S4a, the transfer and output characteristics for a device with L = 20 μm and W = 200 μm are simulated and compared to the experimental results as shown in Figure S4 panels b and c. It is worth noting that the model used here as a proof-of-concept demonstration is only a primitive level 1 model (square law model with channel length modulation and source drain series resistance) and the nanotube networks are simply treated as a uniform thin-film without considering the details about tube-to-tube junctions, and charge transport through the network. Yet, this simple model still provides simulated performance that match the experimental results relatively closely, which should work well for simulating and predicting the DC performance of circuits. Further optimization of the model by including more non-ideal effects, underlying physics in the nanotube networks, and device frequency response should improve the accuracy and enable more sophisticated simulations.

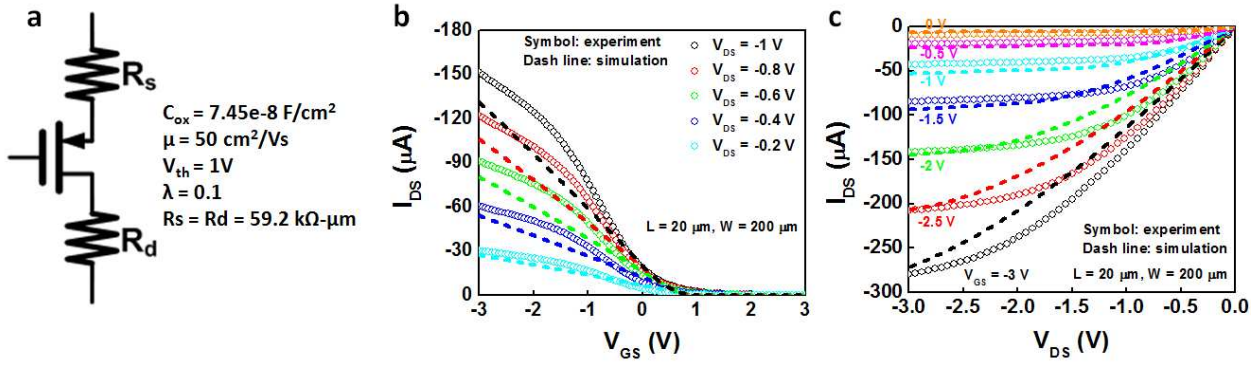

Figure S4. Modeling of the flexible nanotube TFTs using Level 1 SPICE model. (a) Schematic of the transistor and device parameters derived from the measurements used for the simulation. (b) Measured (symbol) and simulated (dash line) transfer characteristics for a flexible nanotube TFT with L = 20 μm and W = 200 μm. (c) Measured (symbol) and simulated (dash line) output characteristics for the same device shown in panel b.

S5. Inverter gain and noise margin as a function of V_{DD}

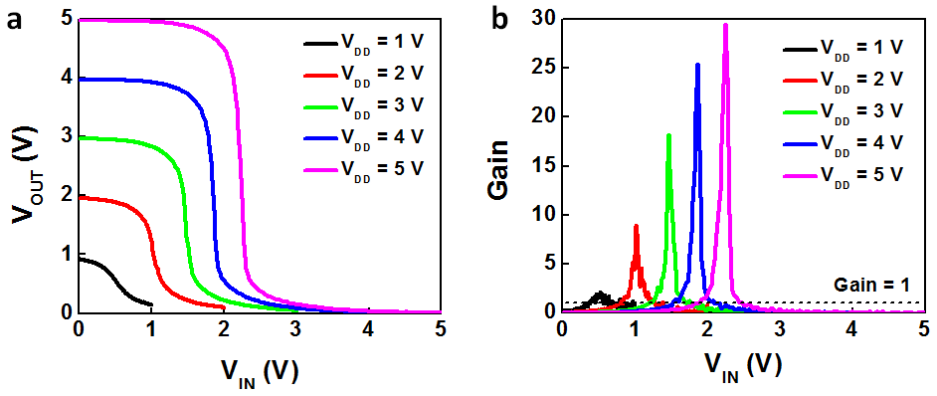

Figure S5. (a) Inverter voltage transfer characteristics measured at different V_{DD}. (b) Inverter voltage gain under different V_{DD}.

The inverter voltage transfer characteristics measured at different V_{DD} biases are shown Figure S5a, and the corresponding voltage gain curves are shown in Figure S5b. The points where gain equals 1 are defined as V_{IL} and V_{IH} of the inverter and the LOW and HIGH noise margin of the inverter can be calculated using the equation $NM_L = V_{IL} - V_{OL}$, $NM_H = V_{OH} - V_{IH}$, where V_{OL} and V_{OH} equal 0 and V_{DD}, respectively, for the inverter used in this study. The noise margin calculated for different V_{DD} biases are summarized in Table S5.

V_{DD} (V)	V_{IL} (V)	V_{IH} (V)	NM_L	NM_H
1	0.38	0.62	0.38 V_{DD}	0.38 V_{DD}
2	0.82	1.27	0.41 V_{DD}	0.37 V_{DD}
3	1.2	1.70	0.40 V_{DD}	0.43 V_{DD}
4	1.52	2.1	0.38 V_{DD}	0.48 V_{DD}
5	1.88	2.48	0.38 V_{DD}	0.50 V_{DD}

Table S5. Inverter high low noise margin for different V_{DD} biases.

S6. Step response and frequency response of the inverting amplifier

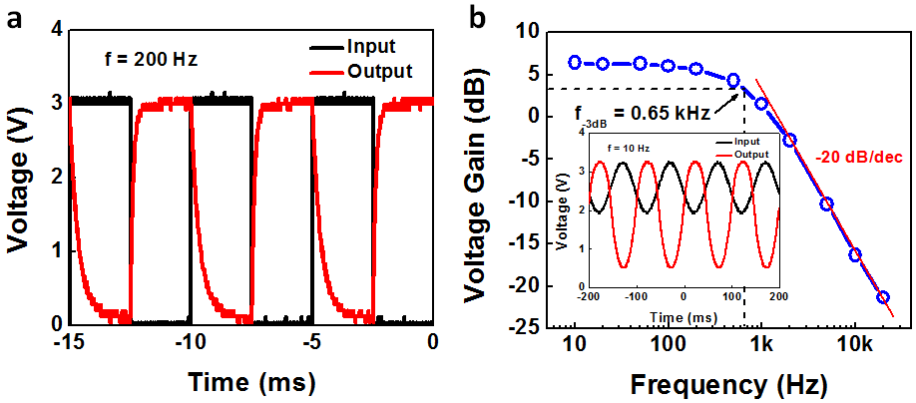

Figure S6. (a) Step response of the flexible nanotube inverter measured at 200 Hz. (b) Frequency response of the nanotube inverting amplifier. The voltage gain is plotted as a function of the frequency, and the -3dB frequency is measured to be 0.65 kHz. Inset: Input and output waveforms of the inverting amplifier at 10 Hz.

S7. Short-open-load-through (SOLT) de-embedding for the flexible nanotube RF transistors

The Device Under Test (DUT) is de-embedded using an open/short scheme in order to remove the parasitic effect and deduce the intrinsic performance of the flexible nanotube RF transistor. The de-embedding is done by on-die probing measurements, where the open/short structures are fabricated on the same wafer with the DUT, and with exactly the same dimensions. For the short structure, the signal (gate and drain) is shorted to the ground (source), while for the open structure, the channel nanotubes are completed removed. The optical microscope images for the device, short, and open structure are presented in Figure S7 panels a to c. The as-measured S-parameters of the DUT, open (Figure S7d), and short (Figure S7e) are converted to Y-parameters, and the intrinsic Y-parameters of the DUT can be deduced using the following equation

$$Y_{device\_intrinsic} = ((Y_{meas} - Y_{open})^{-1} - (Y_{short} - Y_{open})^{-1})^{-1}$$

The intrinsic S-parameters are then in turn converted back from the intrinsic Y-parameters, as presented in Figure 4c of the manuscript.

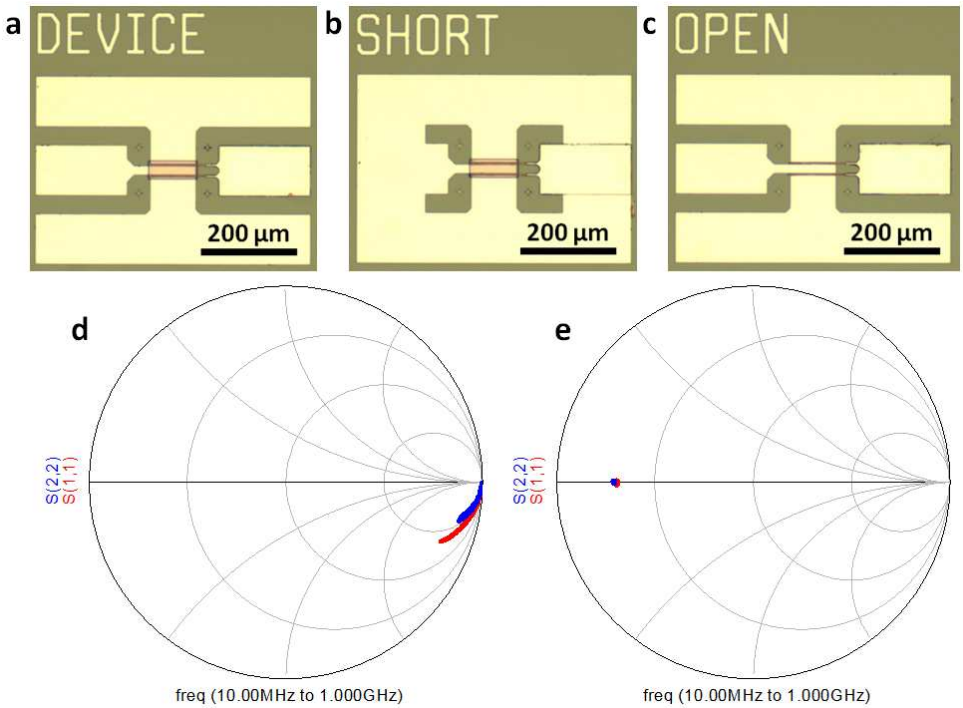

Figure S7. Open/short de-embedding. (a-c) Optical microscope images of the device (a), short (b), and open (c) used for the de-embedding. (d,e) As-measured S_{11} and S_{22} of the open (d) and short (e) structures.

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