Fabrication and Analysis of Deep Submicron Strained-Si N-MOSFET's

Kern (Ken) Rim, *Member, IEEE*, Judy L. Hoyt, *Member, IEEE*, and James F. Gibbons, *Fellow, IEEE*

***Abstract*—Deep submicron strained-Si n-MOSFET's were fabricated on strained Si/relaxed $Si_{0.8}Ge_{0.2}$ heterostructures. Epitaxial layer structures were designed to yield well-matched channel doping profiles after processing, allowing comparison of strained and unstrained Si surface channel devices. In spite of the high substrate doping and high vertical fields, the MOSFET mobility of the strained-Si devices is enhanced by 75% compared to that of the unstrained-Si control devices and the state-of-the-art universal MOSFET mobility. Although the strained and unstrained-Si MOSFET's exhibit very similar short-channel effects, the intrinsic transconductance of the strained Si devices is enhanced by roughly 60% for the entire channel length range investigated (1 to 0.1 μm) when self-heating is reduced by an ac measurement technique. Comparison of the measured transconductance to hydrodynamic device simulations indicates that in addition to the increased low-field mobility, improved high-field transport in strained Si is necessary to explain the observed performance improvement. Reduced carrier-phonon scattering for electrons with average energies less than a few hundred meV accounts for the enhanced high-field electron transport in strained Si. Since strained Si provides device performance enhancements through changes in material properties rather than changes in device geometry and doping, strained Si is a promising candidate for improving the performance of Si CMOS technology without compromising the control of short channel effects.**

***Index Terms*—Hydrodynamic simulation, mobility enhancement, MOSFET mobility, self-heating, SiGe boron diffusion barrier layers, SiGe-on-insulator, strained-Si MOSFET's, transconductance.**

I. Introduction

GEOMETRIC scaling of Si CMOS devices has provided much of the performance improvement for each new technology generation. In spite of the reduction in supply voltage, scaling of the gate dielectric thickness, as well as the channel length, has helped increase or maintain current drive and improve CMOS circuit delay. However, as CMOS technology progresses into the deep submicron regime, sustaining the expected performance improvements in each new generation through geometric scaling has become an increasingly complex, expensive, and difficult problem. Scaling channel length produces diminishing improvements in MOSFET current drive as velocity saturation effects begin to influence the device characteristics. Gate dielectric scaling also faces fundamental limits set by leakage current in thin gate dielectrics. In addition, the finite thickness and quantum mechanical nature of the inversion layer, and polysilicon gate depletion effects diminish the gate-to-channel capacitance C_{GC} and inversion layer carrier concentration for ultrathin gate oxides. Emphasis on low power design and hot carrier reliability further complicate the device design issues. Moreover, the increase in channel impurity concentration and vertical field required to control short channel effects tends to degrade the carrier mobility and impact current drive, making it difficult to sustain device performance improvements.

One way to address the challenge of improving device performance is to enhance carrier transport in the MOSFET channel by changing the material properties. For example, strain in Si can be used to modify the carrier transport properties. Using Hall effect structures, high electron mobilities have been measured in strained Si at room temperature [1] and mobilities approaching 500 000 cm^2/Vs have been demonstrated at 0.4 K [2]. Electron mobility enhancements in tensile-strained Si have been theoretically predicted [3]–[6] for both bulk and inversion layer transport. Fig. 1 shows a schematic illustration of the crystal lattice for strained Si on relaxed $Si_{1-x}Ge_x$, and the subsequent energy splitting of the Si conduction band edge. Because the equilibrium lattice constant of $Si_{1-x}Ge_x$ is larger than that of Si, a pseudomorphic layer of Si grown on relaxed $Si_{1-x}Ge_x$ is under biaxial tension. The strain lifts the sixfold degeneracy in the conduction band and lowers the two perpendicular valleys (labeled "Δ_2" in Fig. 1) with respect to the four in-plane valleys (Δ_4). Electrons are expected to preferentially occupy the lower-energy Δ_2 valleys, reducing the effective in-plane transport mass. The energy splitting also suppresses intervalley phonon-carrier scattering, increasing the electron low-field mobility.

The strain dependence of electron inversion layer mobility has been measured in n-MOSFET's fabricated on a strained Si/relaxed $Si_{1-x}Ge_x$ heterostructure [7]. For a Ge content of 30% in the underlying relaxed $Si_{1-x}Ge_x$, the electron mobility in the strained Si is enhanced by roughly 80%. A hole mobility enhancement of similar magnitude has been reported for surface-channel strained-Si p-MOSFET's [8]. These surface-channel strained-Si n- and p-MOSFET's are identical to conventional Si MOSFET's in their operation principle, and are expected to retain all the advantages of surface-channel (as op-

Manuscript received August 18, 1999; revised February 23, 2000. This work was supported by the Defense Advanced Research Projects Agency under Contract DAAH04-95-1-0598, by the Army Research Office, and by a fellowship from Motorola, Inc. The review of this paper was arranged by Editor K. Shenai.

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Publisher Item Identifier S 0018-9383(00)05200-X.

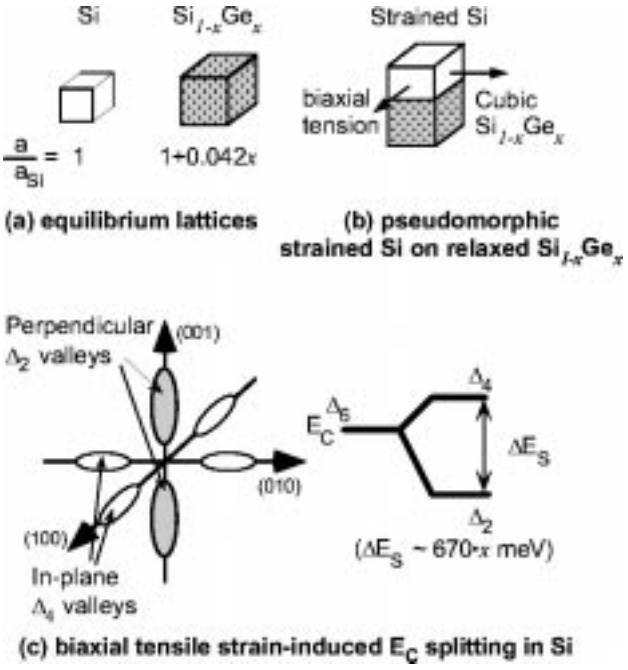

Fig. 1. Schematic illustrations of (a) equilibrium lattices, (b) peudomorphic strained Si on relaxed $Si_{1-x}Ge_x$, and (c) strain-induced conduction band splitting in Si.

posed to buried-channel) devices, including excellent current drive/turn-off characteristics, and scaling behavior.

However, the impact of strain on high field transport and the performance of deep submicron devices have not been investigated. Simulation studies indicate that increased low-field mobility improves the transconductance of Si MOSFET's, even at 0.1 μm channel length, although the impact of low-field mobility diminishes with decreasing channel length [9]. If strain can enhance the high-field transport properties of Si in addition to the low-field mobility, device performance improvements that are even greater may be possible.

Deep submicron strained-Si n-MOSFET's were fabricated, characterized, and analyzed to investigate short channel device performance and the impact of strain on high-field transport in strained Si [10]. Strain provides transconductance and current drive improvements that are independent of the geometric and electrostatic design of the device. In this paper, the device fabrication and the electrical characteristics are presented, and the performance enhancements are discussed using device simulation results as well as analysis which gives insight into the physical mechanisms underlying the improvements. Finally, the impact on CMOS technology and challenges for practical application are briefly described.

II. Device Fabrication

The structures of the strained-Si and control devices after fabrication are illustrated in Fig. 2. Relaxed $Si_{1-x}Ge_x$ layers were epitaxially grown on CZ Si $\langle 100 \rangle$ substrates in a rapid thermal chemical vapor deposition (RTCVD) reactor by using a linear graded buffer layer technique [11], [12]. In this technique, a graded relaxed $Si_{1-x}Ge_x$ layer was formed by increasing the Ge content from 0 to 20% over the thickness of 1.5 μm. The graded layer was capped with a 7000 Å-thick relaxed $Si_{1-x}Ge_x$ layer with constant (20%) Ge content. Dichlorosilane and germane were used as the Si and Ge precursors at growth temperatures in the range of 700 to 750 °C. A thin ($\sim$230 Å), strained-Si channel layer was then grown on the relaxed $Si_{1-x}Ge_x$ layer. The thickness of the epitaxial layers, Ge content in the relaxed $Si_{1-x}Ge_x$ layer, and the strain state of the strained-Si channel layer were verified by cross-sectional TEM, Rutherford back-scattering (RBS) and Raman spectroscopy *after* the devices were fabricated. Approximately 80 to 100 Å of the strained-Si layer was consumed during the gate oxidation and various chemical cleaning steps during device fabrication, resulting in a final thickness of 130 Å for the channel layer.

The epitaxial layers were *in-situ* doped with boron by flowing diborane during epitaxial growth. Fig. 2(c) shows the targeted as-grown vertical doping profile under the channel. The boron doping peak, which results in a retrograde doping profile after thermal processing (Fig. 3), was designed to suppress short channel effects in MOSFET's with 0.1 μm channel length. Boron diffusivity in both relaxed and strained $Si_{0.8}Ge_{0.2}$ is approximately six times lower than that in Si [13]. In order to control boron diffusion and match the post-fabrication doping profiles in the strained-Si and control devices, two thin layers of *strained* $Si_{1-x}Ge_x$ boron diffusion barrier layers were inserted above and below the doping peak in the epitaxially grown unstrained Si control device ("epi Si control"). Since the band offset between strained $Si_{1-x}Ge_x$ and Si is in the valence band, these $Si_{1-x}Ge_x$ layers are not expected to play a role in the electrical performance of the control devices. Fig. 3 shows the boron doping profiles in the strained and unstrained devices measured by SIMS after device processing. Compared to the simulated boron profile obtained using the boron diffusivity in Si (dashed line) [14], the measured boron profiles are steeper, indicating that the $Si_{1-x}Ge_x$ layers were indeed effective in limiting boron diffusion during gate oxidation and thermal annealing. In spite of the difference in boron diffusivity in Si and $Si_{1-x}Ge_x$, the boron profiles are well matched near the channel in the two devices. This allows meaningful comparisons of MOSFET mobilities and short channel device performance between the strained-Si and epi Si control devices.

Deep submicron n-MOSFET's were fabricated using a simplified standard MOS fabrication process. Thermal exposure during the processing was limited to prevent strain relaxation in the epitaxial layers and Ge diffusion into the channel layer. Device isolation in the field was achieved by a field implant and deposition of low temperature oxide (LTO). A 60 Å-thick (67 Å by capacitance measurement) thermal oxide was grown on strained Si by a dry-wet-dry thermal oxidation sequence at 800 °C. An *in-situ* phosphorous-doped polysilicon gate was deposited and patterned with an e-beam lithography step, and etched using RIE. All other levels were defined with optical lithography steps. Thermal annealing was limited to the source/drain implant annealing (2 min at 650 °C and 15 s at 850 °C) and the Ti salicide formation annealing (2 min at 650 °C). A second salicide annealing step, typically performed in a standard Ti salicide process to induce a phase transformation to the low resistivity C54 phase, was omitted

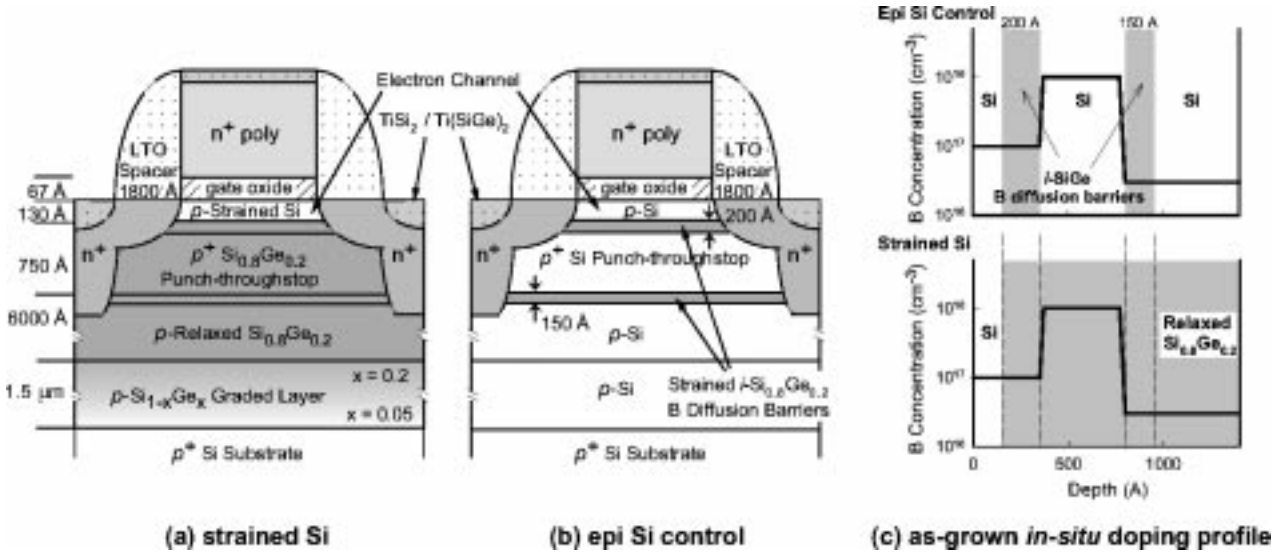

Fig. 2. Structure of (a) strained-Si and (b) epi Si control devices after processing, and (c) targeted *in-situ* boron profile in the two devices.

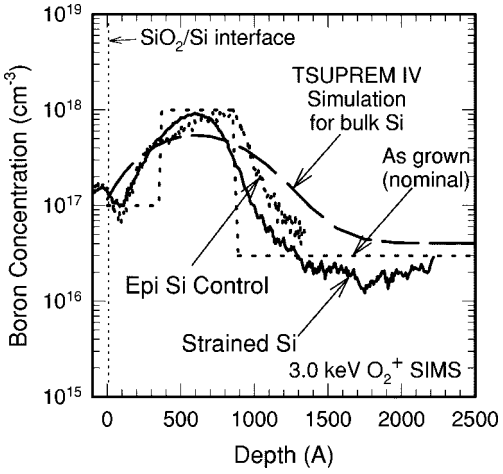

Fig. 3. Comparison of boron profiles measured by SIMS after processing, and TSUPREM IV-simulated [14] profile. Due to the presence of $Si_{0.8}Ge_{0.2}$ diffusion barriers, the boron profiles are well matched for the two structures, and doping profile broadening is reduced.

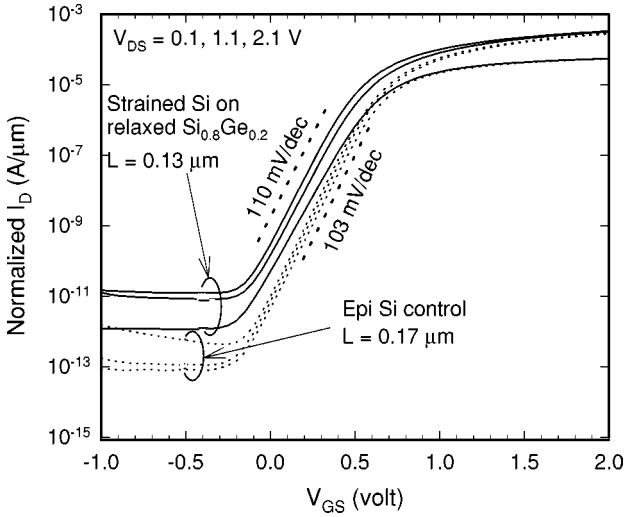

Fig. 4. Subthreshold characteristics of sub-0.25 μm (0.13 μm for strained-Si and 0.17 μm for epi Si control) n-MOSFET's. The subthreshold slopes are as expected by a device simulation using the corresponding doping profile and gate oxide thickness.

in this process in order to minimize the agglomeration of the $Ti(Si_{1-x}Ge_x)_2$ film and junction leakage [15], [16]. Due to the limited doping activation associated with the conservative thermal budget, the series resistance R_{ext} in the strained-Si and epi Si control devices, determined by the shift-and-ratio method [17], was 1200 and 900 Ω-μm, respectively. Both values are considerably higher than the typical values found in recent CMOS technologies. The salicide process with relatively high resistivity, and the conservative lithography alignment tolerance spacing (>1 μm) between the gate and source/drain contact holes also contributed to the high series resistance.

III. Electrical Characteristics

Since the doping profiles were matched and other geometric dimensions (junction depth, gate oxide thickness, etc.) were nearly identical, the subthreshold characteristics and short channel effects were comparable in the strained Si and epi Si control devices. Fig. 4 shows the subthreshold characteristics of the strained-Si and epi Si control devices with channel lengths of 0.13 and 0.17 μm, respectively. The measured subthreshold slopes are comparable to the device simulation result ($\sim$ 104 mV/dec) [18] calculated using the device dimensions and measured channel doping profile from the fabricated devices. The characteristic for the strained Si device exhibits a slightly larger slope (110 mV/dec) compared to the epi Si control device (103 mV/dec), possibly due to the higher dielectric constant of $Si_{1-x}Ge_x$. The leakage floor (V_{GS}-independent part of the subthreshold current characteristic) in the strained Si device is approximately an order of magnitude higher than that of the control transistor. A larger reverse junction leakage, associated with the smaller band gap in $Si_{0.8}Ge_{0.2}$ and a finite concentration of dislocations that propagate to the surface from the graded buffer layer, contributes to the higher leakage floor in the strained-Si device. Even for the case of identical generation lifetimes in the $Si_{0.8}Ge_{0.2}$ and Si material, the smaller band gap

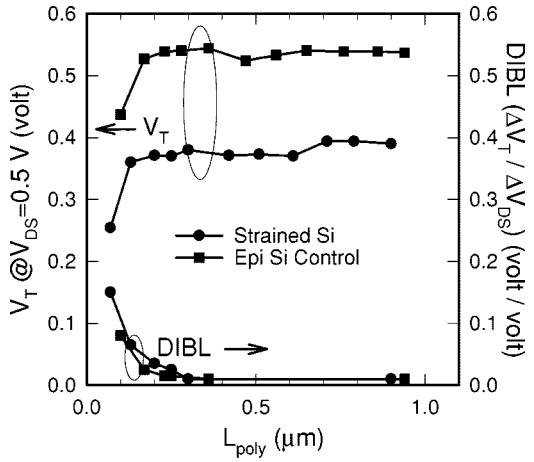

Fig. 5. Measured threshold voltage roll-off and DIBL characteristics as a function of channel length. Comparable short channel effects are observed in the strained-Si and control devices.

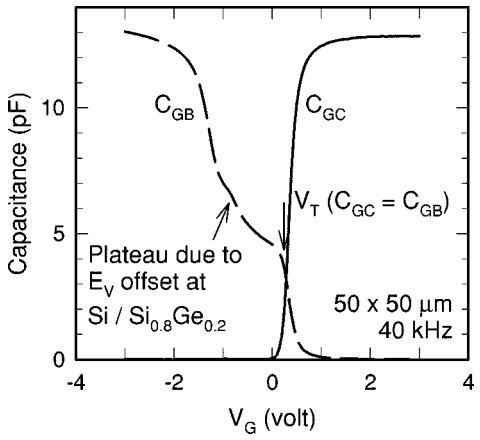

Fig. 6. Split *C–V* for a large-area strained-Si n-MOSFET.

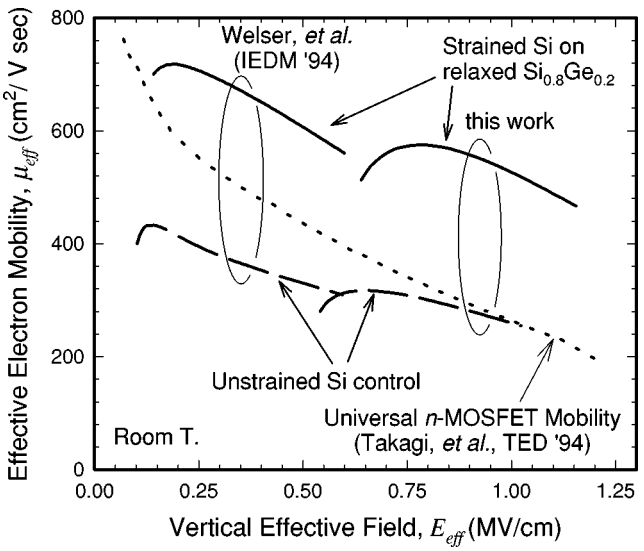

Fig. 7. Effective mobility $\mu_{\rm eff}$ as a function of vertical effective field $E_{\rm eff}$. Even for high $E_{\rm eff}$, the measured effective mobility is enhanced by ∼75% for the strained Si device.

in $Si_{0.8}Ge_{0.2}$ is expected to increase diode reverse saturation currents by 5–6× compared to Si diodes. However, the leakage floor in these devices is more than seven orders of magnitude smaller than the turn-on current. Therefore, it should not affect the off-state device current for a typical choice of V_T which is usually lower than 0.5 V for deep submicron devices.

Although the drain-induced barrier lowering (DIBL) in the strained Si device in Fig. 4 appears to be larger than that for the Si control, this is due to the shorter channel length of the devices in that comparison. DIBL and V_T roll-off are plotted as functions of channel length in Fig. 5. A good agreement in the DIBL characteristics and small difference in V_T roll-off between the two sets of devices indicate that the short channel effects are comparable in the strained Si and epi Si control devices, as the electrostatic and geometric design of the devices is essentially identical. The threshold voltage of the strained-Si device is ∼150 meV lower that that of the control device. The lowered conduction band edge of strained Si and the smaller band gap energy in the relaxed $Si_{1-x}Ge_x$ layer account for much of the difference in threshold voltage. No attempt was made in the device design to match the threshold voltage in these devices.

Fig. 6 shows the split C-V characteristics of a large ($W \times L = 50 \times 50\ \mu m^2$) strained Si device. The small plateau observed in the gate-to-substrate capacitance $(C_{\rm GB})$ curve is caused by the valence band discontinuity at the strained Si/relaxed $Si_{1-x}Ge_x$ interface, which confines holes in a well formed by a potential barrier. The gate-to-channel capacitance $(C_{\rm GC})$ was integrated to obtain the inversion carrier concentration $Q_{\rm inv}$ which was used to calculated the effective mobility $\mu_{\rm eff}$:

$$\mu_{\rm eff} = \frac{L}{W} \cdot \frac{g_D}{Q_{\rm inv}}. \tag{1}$$

The drain conductance g_D was measured at a low drain bias ($V_{\rm DS} = 10$ mV) to minimize the effect of lateral field. The extracted $\mu_{\rm eff}$ is plotted against the effective vertical field $E_{\rm eff}$ in Fig. 7. The effective field was obtained from

$$E_{\rm eff} = \frac{1}{\varepsilon_S} \cdot \left(Q_b + \frac{1}{2} \cdot Q_{\rm inv} \right) \tag{2}$$

where Q_b represents the bulk charge, which is estimated by integrating the measured doping profile across the depletion width under the channel.

From Fig. 7 we see that the effective mobility of the strained Si device exhibits an enhancement of roughly 75% over that of the control device at a given effective field. The universal mobility curve for state-of-the-art Si n-MOSFET's [19] is shown in the figure (dotted line). The mobility of the strained Si device is also significantly higher than the mobilities for n-MOSFET's with state-of-the-art gate oxides. The mobility data measured on lightly doped (2×10^{16} cm^{-3}) strained-Si devices [7] is also shown for comparison (the pair of curves on the left). Note that because of the higher substrate doping which results in larger Q_b, the $E_{\rm eff}$ range for the devices in this work is considerably higher than for the devices fabricated on lightly-doped substrates. The electron mobility enhancement observed in the lightly doped devices for relatively low vertical fields [7] is thus sustained for high vertical fields (up to 1 MV/cm) and high substrate doping which are suitable for deep submicron device design. This result indicates that for the vertical effective field range investigated here (roughly 0.5 to 1 MV/cm),

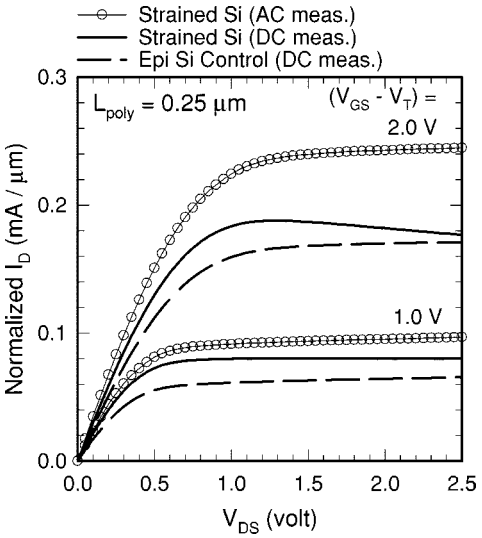

Fig. 8. Output characteristics of 0.25 μm devices. Open circles represent the output characteristics of the strained-Si device measured by the ac g_D method, which was used to reduce the effects of self-heating, as discussed in the text.

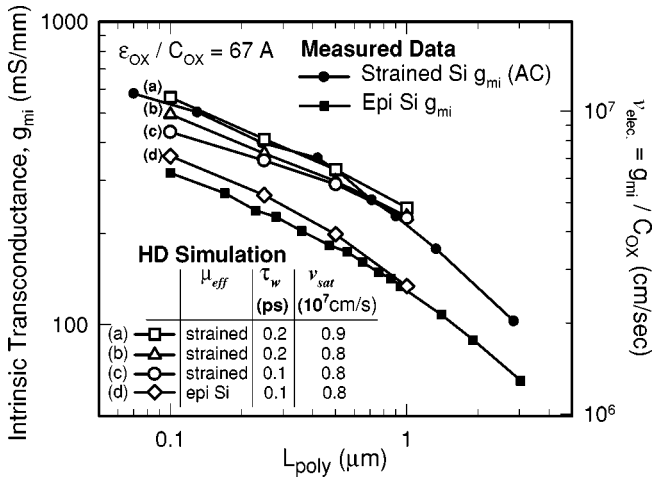

Fig. 9. Measured and calculated intrinsic transconductance g_{mi} as a function of channel length. See text for the descriptions for each curve.

phonon scattering still has a strong influence on the inversion layer mobility of electrons. Surface roughness scattering is expected to dominate the electron mobility at very high vertical fields, and strain-induced mobility enhancement by suppression of phonon scattering may eventually diminish at higher vertical fields ($E_{\text{eff}} > 1$ MV/cm).

Current drive characteristics of the deep submicron strained-Si devices also exhibit enhancements over those of the control devices. In Fig. 8, output characteristics of the strained-Si and epi Si control devices are compared for a channel length of 0.25 μm. The drain current is plotted for normalized gate overdrives $(V_{\text{GS}} - V_T)$ because of the difference in threshold voltage values. The solid and dashed lines represent the drain current drive of the strained-Si and epi Si control devices measured by a typical dc technique with a HP4155 parameter analyzer. The current drive enhancement in the strained-Si device is evident at all bias points. However, at high current levels and drain bias, a negative slope in the drain current of the strained-Si device is observed. This is due to SOI-like self-heating in the strained-Si MOSFET's fabricated on a thick, relaxed $Si_{1-x}Ge_x$ layer. The reported value for the thermal conductivity of $Si_{0.8}Ge_{0.2}$ is approximately $15\times$ lower than that of bulk Si [12], [20]. The combination of the low thermal conductivity and the thickness ($\sim$7000 Å $Si_{0.8}Ge_{0.2}$ cap + 1.5 μm graded buffer layer) of the relaxed $Si_{1-x}Ge_x$ layer resulted in a structure with low thermal conductance, leading to self-heating effects analogous to those often observed in SOI devices with thick buried oxide layers. The thermal conductance of the strained Si device structure roughly corresponds to the thermal conductance of an SOI structure with 130 Å of Si and 2300 Å of buried oxide. The thickness dependence of the thermal conductivity of a thin Si film also contributes to the low thermal conductance [21]. According to analytical modeling based on the solution of the Boltzman transport equations for phonons, the room temperature thermal conductivity of a 100 Å-thick Si film in the in-plane direction is $\sim 7\times$ lower than that of bulk Si [21].

In addition to the negative drain conductance g_D, self-heating in the strained-Si device elevates the temperature in the channel and degrades the enhancement of steady-state current drive in the strained-Si device.

In order to reduce the influence of self-heating on the measured device characteristics, an AC drain conductance (g_D) method [22], [23] was used to determine the output characteristics. In this technique, drain current characteristics are obtained by integrating the ac g_D measured at a frequency (6 MHz) faster than typical thermal time constants of self-heating (microseconds). Good agreement between the dc- and ac-measured characteristics of the epi Si control devices, which should exhibit negligible heating, validated the use of this technique to obtain output characteristics [10, Fig. 8(a)]]. The ac g_D technique has been successfully applied to the characterization of SOI devices [22], [23]. The open circles in Fig. 8 represent the drain current of the strained-Si device measured by the ac method. A significant current drive enhancement over the control device is observed. Even with the high series resistance in these devices, the saturation current and transconductance g_m are enhanced by $\sim$45% when self-heating in the strained-Si device is reduced by the ac method.

In order to estimate the *intrinsic* performance of the devices, the intrinsic transconductance g_{mi} was extracted using the following expressions [24]:

$$g_{mi} = \frac{g_m^0}{[1 - R_{\text{ext}} \cdot g_D \cdot (1 + R_S \cdot g_m^0)]} \tag{3}$$

$$g_m^0 = \frac{g_{m,\text{ext}}}{(1 - R_S \cdot g_{m,\text{ext}})} \tag{4}$$

where R_{ext} and R_S are the total and source-side series resistance. The measured transconductance and drain conductance were used for $g_{m,\text{ext}}$ and g_D. The intrinsic transconductances extracted from the measurements of the strained-Si and epi Si control devices are compared in Fig. 9 (solid symbols) as a function of the physical gate length (L_{poly}) measured by cross-sectional SEM. When self-heating in the strained-Si devices is reduced with the ac g_D measurement technique, the intrinsic

transconductance enhancement for the strained Si device compared to the epi Si control is sustained for all channel lengths considered in this experiment. Even for deep submicron channel lengths, where the contribution of low-field mobility to current drive is expected to be diminished, g_{mi} is enhanced by as much as 60%.

IV. Analysis of Enhanced Electron Transport

The low-field mobility enhancement in the strained-Si n-MOSFET's can be explained by suppressed intervalley scattering and carrier repopulation due to the strain-induced conduction band energy splitting [6], [7]. However, high-field and transient transport properties are expected to dominate the characteristics of deep submicron MOSFET's. Therefore, in order to understand the mechanisms responsible for the observed enhanced current drive and transconductance in these deep submicron strained-Si devices, the impact of strain-induced energy splitting on high-field inversion layer carrier transport needs to be considered.

Theoretical investigations of electron transport in strained Si using Monte Carlo calculations have previously been reported [4], [25], [26]. In [25], the velocity-field and energy-field relations obtained from steady-state calculations indicate that the enhancement of the steady-state velocity in strained Si diminishes with increasing carrier energy and lateral field. Although the change in the saturation velocity with strain is expected to be small [25], transient transport calculations at high lateral fields (5 MV/cm) show a significant enhancement of the transient velocity overshoot with increasing energy splitting between the Δ_2 and Δ_4 valleys. The calculations in [25] were performed for bulk transport under the assumptions of uniform field and carrier concentration, as opposed to the highly nonuniform field and carrier concentrations that typically characterize transport in MOSFET inversion layers.

Using the MEDICI simulator [18], hydrodynamic (HD) device simulations were carried out to analyze the impact of low-field mobility and high field transport on device characteristics. Although HD device modeling is limited by simplified band structure and carrier transport assumptions, it provides an intuitive and computationally efficient means of analyzing physical trends. In hydrodynamic modeling of carrier transport, the energy relaxation time τ_w, which is an average time constant associated with energy scattering process, is often used to represent the strength of transient transport behavior. In order to estimate the influence of the conduction band energy splitting on the electron energy relaxation time, the velocity-field and energy-field relations for strained Si calculated by Monte Carlo simulations [25] were fitted to the energy balance equation:

$$\frac{\partial W}{\partial t} = -\nabla \cdot F_w + J_n \cdot E - \left\langle \frac{1}{\tau_w} \right\rangle (W - W_0) + \delta_E \quad (5)$$

where W is the carrier energy, F_w is the energy flow, and δ_E is the generation term. Stripping the spatially varying terms results in the "local homogeneous hydrodynamic equation" which can be fit to the velocity-field and energy-field relations to find τ_w [9], [18], [25], [27]:

$$\nu \cdot E = \frac{3}{2} \cdot \frac{W - W_0}{\tau_w(W)}. \quad (6)$$

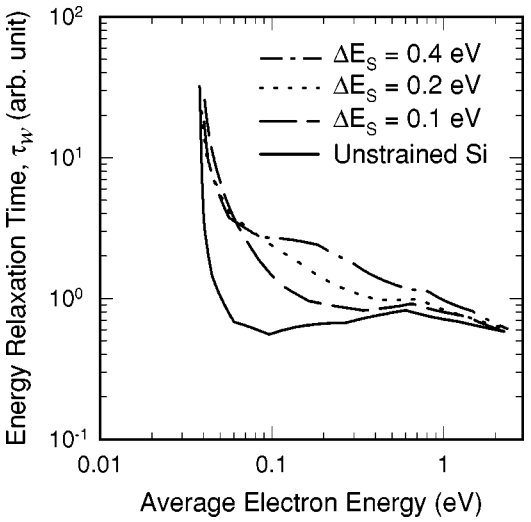

Fig. 10. Energy relaxation time τ_w (arbitrary units) estimated from the published velocity-field and energy-field relations for strained Si [25]. Various curves correspond to different strain-induced energy splittings, ΔE_s. Increasing strain increases the energy relaxation time.

Fig. 10 shows the estimated τ_w, obtained in this way, as a function of average electron energy and strain-induced energy splitting ΔE_s. For average electron energies of up to 0.3 eV, conduction band energy splittings ΔE_s of 0.1 and 0.2 eV result in increases in τ_w by as much as 1.8 and $2.5\times$, respectively, indicating that the transient electron velocity should be significantly enhanced. For an energy splitting of 0.14 eV, which corresponds to the strain condition used in our devices (strained Si on $Si_{0.8}Ge_{0.2}$), τ_w is expected to increase by roughly a factor of two.

The universal mobility model (UNIMOB) [18], which was fitted to the measured mobility of the strained-Si and epi Si control devices (Fig. 7), was used as the low-field mobility model in the simulations. In MEDICI's implementation of HD modeling, high lateral field transport is modeled with a "carrier temperature based mobility" (TMPMOB) [18]. In this approach, the energy balance equation is locally solved concurrently with the drift-diffusion equation, to calculate the local mobility as a function of the local carrier temperature. A value of $\beta = 1.3$ and $\tau_w = 0.1$ ps, which produced the best fit to the measured characteristics of the control device, was used in the Caughey–Thomas expression [18] for the final mobility. The saturation velocity $v_{\rm sat}$ for the unstrained Si device was set to 0.8×10^7 cm/s.

Fig. 11 shows the electron velocity along the channel calculated with various combinations of $\mu_{\rm eff}$, τ_w and $v_{\rm sat}$ for a 0.1 μm device. Compared to the control device [solid line with dots, (d)], changing only the low field mobility to that of strained-Si devices [solid line, curve (c)] enhances the velocity near the source by ~30%, which is about half the measured g_{mi} enhancement factor. When τ_w is increased by factor of two in addition to the change to the low field mobility [curve (b)], the

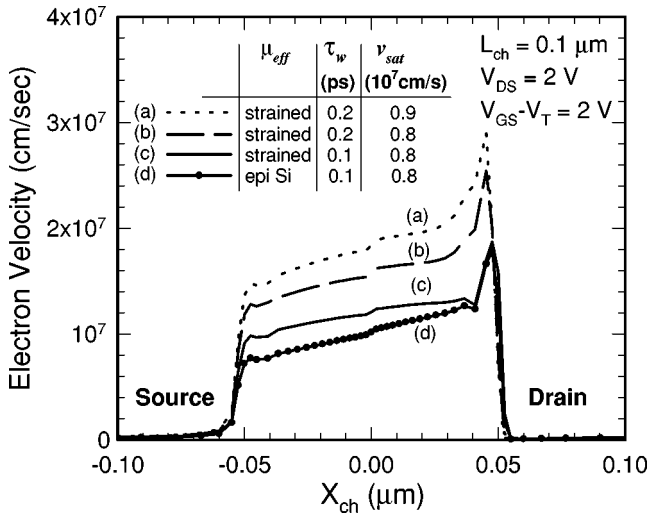

Fig. 11. Simulated electron velocity along the channel of 0.1 μm n-MOSFET's.

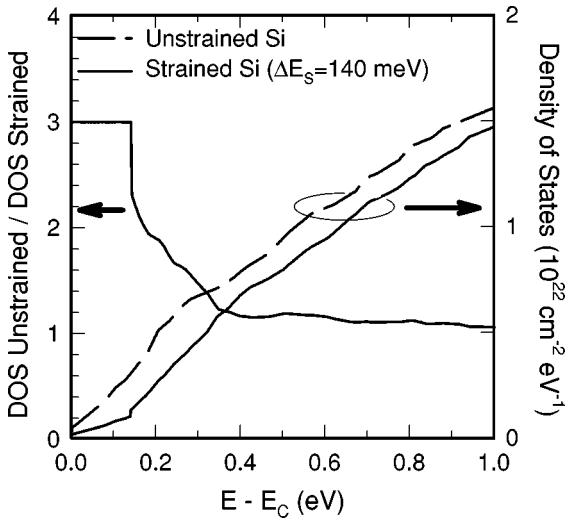

Fig. 12. Comparison of the expected density of states in the conduction band of unstrained and strained Si.

velocity enhancement near the source approaches the measured intrinsic transconductance enhancement (60%). Increasing $v_{\rm sat}$ by $\sim$10% [curve (a)], which is consistent with theoretical predictions [4], [25] further increases the velocity.

The calculated and measured transconductances are compared as a function of channel length in Fig. 9. Since the series resistance $R_{\rm ext}$ of the simulated structure was low ($<$200 Ω-μm), the simulated transconductance was directly compared to the g_{mi} extracted from the measurements. The purpose of the simulations represented in curve (c), where only the low field mobility was changed to the enhanced mobility of strained-Si devices, was to explore the impact of the low-field mobility enhancement alone. In this case, the enhanced low-field mobility in strained Si accounts for most of the measured enhancement at a channel length of 1 μm. At such a long channel length, increasing τ_w or $v_{\rm sat}$ [curves (a) and (b)] has negligible influence on transconductance, because the carrier transport is dominated by the effect of low field mobility and the impact of transient transport effects are insignificant. However, at $L = 0.1$ μm, the effect of the low field mobility enhancement accounts for only half of the measured transconductance enhancement, similar to the trend seen in the simulated velocity near the source (Fig. 11). The result, which is consistent with the findings in an earlier report of hydrodynamic calculations that varied low-field mobility as a parameter [9], shows that although enhanced low-field mobility does increase g_m of deep submicron devices, the influence diminishes with decreasing channel lengths. More importantly, the results indicate that the improvement in low-field mobility alone does *not* explain the enhancement in the short-channel strained Si device performance. However, when τ_w is increased by $2\times$ in addition to the mobility enhancement [curve (b)], the calculated transconductance enhancement approaches the measured value. Improvements in high field transport and enhanced transient velocity overshoot in strained Si appear necessary to fully account for the measured g_{mi} increase. Increasing $v_{\rm sat}$ by $\sim$10% [from curve (b) to (a)] for strained Si improves the fit to the measured g_m.

As discussed above, estimates of the energy relaxation time derived from Monte Carlo calculations (Fig. 10) indicate that for the strain in our devices, a $2\times$ increase in τ_w is quite feasible, for electron energies up to roughly 0.3 eV. According to the HD simulations of the devices with 0.1 μm channel length, the average carrier energy along the channel is at most 0.3 eV, validating the $2\times$ increase in τ_w used in the HD simulation of the strained-Si devices.

The suppression of carrier scattering by the strain-induced energy splitting can be understood by a simple analysis of the change in the density of states (DOS), which essentially leads to a reduction in the final available states for carrier scattering events. Fig. 12 shows the conduction band DOS for unstrained Si compared to that for strained Si with $\Delta E_s = 140$ meV, which corresponds to strained Si on relaxed $Si_{0.8}Ge_{0.2}$. The strained-Si DOS was estimated by

$$\begin{aligned}\mathrm{DOS}_{\rm str.}(E) &= \mathrm{DOS}_{\Delta 2}(E) + \mathrm{DOS}_{\Delta 4}(E) \\ &= \frac{2}{3}\cdot \mathrm{DOS}_{\rm unstr.}(E) + \frac{1}{3}\cdot \mathrm{DOS}_{\rm unstr.}(E-\Delta E_s)\end{aligned} \tag{7}$$

where $\mathrm{DOS}_{\Delta 2}$ and $\mathrm{DOS}_{\Delta 4}$ are the densities of states for the twofold degenerate (Δ_2) and fourfold degenerate (Δ_4) valleys, respectively, and E is the electron energy above the conduction band edge. Since the Δ_4 valleys are raised in energy by ΔE_s above the Δ_2 minimum, $\mathrm{DOS}_{\Delta 4}$ is simply $2/3\cdot\mathrm{DOS}_{\rm unstr.}$ shifted by 140 meV in energy, while $\mathrm{DOS}_{\Delta 2} = 1/3\cdot\mathrm{DOS}_{\rm unstr.}$, where $\mathrm{DOS}_{\rm unstr.}$ is the density of states for the conduction band of unstrained Si. In the figure, we have used the unstrained Si density of states reported for full-band Monte Carlo simulations [5]. For a more rigorous analysis, the two-dimensional (2-D) DOS of the MOSFET inversion layer should be calculated by consistently solving the Poisson and Schroedinger equations. However, analysis discussed below based upon the 3-D DOS is sufficient for the purpose of obtaining physical insight.

Fig. 12 shows that for electron energies up to roughly 0.3 eV, the density of states of strained Si is 1.5 to 3 times lower than that of unstrained Si. At higher energy, the DOS ratio approaches

one. The density of states comparison suggests that the carrier-phonon scattering rate should be significantly lower in strained Si than in unstrained Si for electrons with energies up to about 0.3 eV, which we refer to here as "warm" carriers. Note that this energy range is again consistent with the maximum average electron energy calculated in the HD simulations for 0.1 μm devices. The suppressed scattering rate for these "warm" carriers is responsible for the improved electron transport in strained Si even at high lateral fields, and accounts for the observed enhanced device characteristics. For higher energy splitting (i.e., larger strain), the scattering should be suppressed for a wider range of electron energies.

V. Impact on Technology

Experiments and modeling have been used to demonstrate enhanced current drive and transconductance in deep submicron strained-Si n-MOSFET's. The results can be represented as an improvement in the tradeoff [28], [29] between device speed and short channel effects in CMOS device design. This point can be described with the universal MOSFET mobility curve in Fig. 7. In general, reducing the channel doping level and vertical E_{eff} increases MOSFET mobility, but also compromises short channel effects. Conversely, increasing doping level improves the control of short channel effects, but the channel mobility is degraded in return. Strained-Si MOSFET's provide an alternative to this tradeoff by improving the MOSFET mobility independent of the doping and geometric design, and recovering some of the mobility degradation associated with high vertical fields. The measured characteristics of the devices in this work also demonstrate the improved tradeoff, i.e. the current drive and transconductance of the strained-Si devices were significantly enhanced, while the short channel effects were comparable to those of the unstrained control devices.

The potential impact of strain-induced device performance enhancements follows directly from the close relationship between current drive/transconductance and both circuit speed in digital applications and cutoff frequency in analog circuits. This is particularly true if similar enhancements can be achieved in strained Si p-MOSFET's as well. In CMOS digital logic circuits, the current drive enhancements can also be used to reduce power dissipation. The improved performance of strained-Si n-MOSFET's should allow scaling of the gate overdrive $(V_{\text{GS}} - V_T)$ while maintaining the same maximum current drive in a given technology. As a result, the power supply voltage can be scaled, and/or the threshold voltage can be increased without compromising the current drive, reducing both static and dynamic power dissipation. The demonstration of a full, CMOS integrated circuit is needed to verify the quantitative speed and power enhancements that can be achieved in strained Si.

Several fundamental questions and technological challenges need to be addressed before application of strained-Si CMOS devices to VLSI circuits. A more detailed understanding of carrier transport in strained Si may be achieved by full-band Monte Carlo calculation studies. Hot carrier degradation may be different in strained-Si MOSFET's because of the enhanced carrier transport. The impact of strain on the characteristics of hole transport in deep submicron MOSFET's also needs to be investigated and confirmed experimentally. The presence of a thick relaxed $Si_{1-x}Ge_x$ layer under the strained Si channel presents practical challenges related to self-heating effects and process integration difficulties. Analytical thermal transfer calculations show that at 1 mW/μm power density, the $Si_{1-x}Ge_x$ thickness must be less than 1000 Å to limit the temperature rise in the channel to 60 °C or less in a 0.1 μm device [30]. However, in a typical CMOS logic circuit, where the device duty cycle is orders of magnitude shorter than the thermal time constants for self-heating, the requirements for thermal conductance of the structure may not be as severe as it appears from the consideration of the dc characteristics.

Growth and integration of a thick relaxed $Si_{1-x}Ge_x$ graded buffer layer present significant challenges for mass production. The threading dislocation defect density in the relaxed $Si_{1-x}Ge_x$ layer grown by the linear graded buffer technique is roughly 10^5 cm^{-2} [12]. Although this is comparable to typical defect densities in SIMOX SOI wafers, reducing the defect density in the substrate is critical for applications requiring high yields. Larger junction leakage due to the lower band gap energy of $Si_{1-x}Ge_x$ may be especially undesirable for certain circuit applications. Interactions of $Si_{1-x}Ge_x$ with other materials in the process integration also needs further research to identify solutions. Thermal oxidation of $Si_{1-x}Ge_x$ layers in the device isolation schemes needs careful consideration. An alternative metal silicide, such as Ni, may fare better in a salicide process involving $Si_{1-x}Ge_x$. It is evident from the technological challenges listed above that minimizing the thickness of the relaxed $Si_{1-x}Ge_x$ layer in a strained-Si MOSFET is beneficial in several ways. First, a thinner relaxed $Si_{1-x}Ge_x$ layer improves the thermal conductance of the structure and reduces self-heating effects. Second, it simplifies device isolation, especially in a relaxed SiGeOI ($Si_{1-x}Ge_x$-on-insulator) structure. Third, the junction leakage (from the smaller band gap) and junction capacitance (from the larger dielectric constant) can be reduced. Fig. 13 illustrates schematic cross sections of (a) bulk and (b) SOI heterostructures for strained-Si MOSFET's with thin relaxed $Si_{1-x}Ge_x$ layers. These structures may be fabricated by a variety of processes. For example, a combination of relaxed $Si_{1-x}Ge_x$ and strained Si layers can be epitaxially grown, and bonded to a handle wafer using a combination of SmartCut®, CMP, and selective chemical etch processes. Ideally, the relaxed $Si_{1-x}Ge_x$ layer should be 1000 Å thick or less to take advantage of reduced self-heating and simplicity in the isolation scheme. However, the thickness ratio of the relaxed $Si_{1-x}Ge_x$ and strained-Si layers should be large enough to preserve the desired strained states of the various layers during thermal processing.

VI. Summary

Deep submicron strained-Si n-MOSFET's have been fabricated, characterized, and analyzed. Epitaxial layer structures and processing were designed to yield MOSFET's with both strained and unstrained Si surface channels, with closely-matched doping profiles under the gate. This approach allows direct experimental comparison of measured characteristics and carrier transport in devices with strained

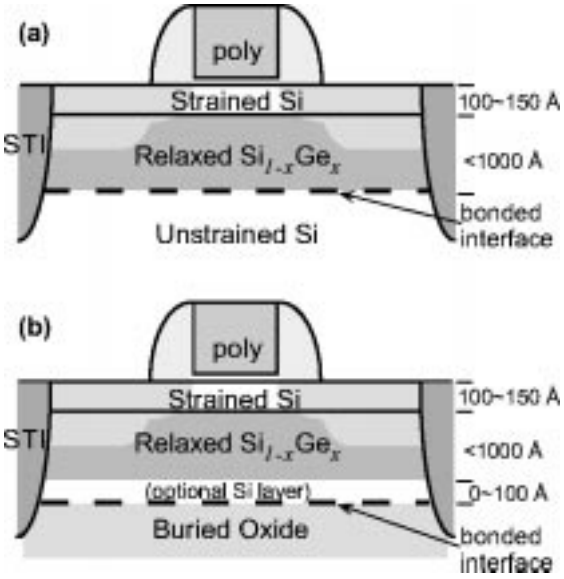

Fig. 13. Structures of (a) bulk and (b) SOI strained-Si MOSFET's with a thin relaxed $Si_{1-x}Ge_x$ layer.

and unstrained Si channels. Both low-field mobility and deep submicron device characteristics are significantly enhanced in the strained-Si devices compared to the unstrained Si controls. The measured transconductance enhancement is found to be relatively independent of gate length, in the range of 1 to 0.1 μm. Comparison of hydrodynamic device simulations to measured characteristics indicates that improvements in both low-field electron mobility and transport under high lateral fields contribute to the observed transconductance enhancement. Fundamentally, these improvements are due to the strain-induced energy splitting that reduces the density of final states and hence the phonon-assisted scattering rate for electrons with average energies of up to a few hundred meV. Since strained-Si n-MOSFET's offer enhancements that are independent of the device design for controlling short channel effects, using strain to improve device characteristics is a promising candidate for extending the performance limits of future Si-based CMOS technology.

ACKNOWLEDGMENT

The authors are grateful for useful discussions and help from J. Welser of IBM, S. Takagi of Toshiba, and D. Connelly (Stanford University, now with Motorola), for the assistance of the staff of the Stanford Nanofabrication Facility, and for the support of that facility as part of the National Nanofabrication Users Network funded by the National Science Foundation.

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