Thesis for the degree of Licentiate of Engineering

Fabrication and Characterisation of Carbon Nanotube Array Thermal Interface Materials

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Göteborg, Sweden 2018

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Licentiatavhandlingar vid Chalmers tekniska högskola
ISSN 1652-0769
Technical report MC2-401

Abstract

The performance of electronic devices has long been limited by thermal dissipation which will result in device failure if not handled properly. The next generation of integrated circuit (IC) devices will feature new packaging technologies like heterogeneous integration as well as 3D stacking which entails additional emphasis on the thermal management solutions employed. Therefore, new materials are in demand to meet the increased thermal dissipation requirements to allow continued scaling in terms of cost per performance and increased device reliability.

The largest bottleneck in thermal dissipation originates from thermal interfaces between different surfaces. For this purpose thermal interface materials (TIMs) are used to conform and bridge the interface and thereby alleviate the thermal dissipation restrictions in the interface. However, commercially available TIMs are either of metallic or polymeric nature which implies a compromise between thermal performance and reliability. Carbon nanotube (CNT) arrays have been suggested as a future potential material in order to achieve a TIM with superior thermal and mechanical properties that would ensure simultaneous high thermal performance and reliability. However, proper bonding solutions are still to be developed in order to apply CNT array TIMs in thermal dissipation applications and to ensure a successful market realisation.

This thesis first outlines the field by presenting a thorough literature review of organic functionalization methods for CNT array TIMs. Three different approaches are identified: polymer embedding, polymer bonding and self-assembly based functionalization. The thesis then presents two experimental studies on CNT array TIMs. The first focuses on the development and characterisation of a CNT array TIM using a novel self-assembly based bonding method by employing epoxy chemistry for covalent anchoring. The second part focuses on a reliability study of a CNT array TIM assembled using a polymer bonding method, which is an aspect that previously has been overlooked. The results from the reliability study gave indications that the mechanical bonding between the CNT array and the growth substrate was susceptible for rapid degradation and further research is required in this field to address this challenge.

Keywords: thermal management, thermal interface material, carbon nanotubes, chemical functionalization, reliability test.

List of Publications

Appended Papers

This thesis is based on the following papers:

Paper A. Current Status and Progress of Organic Functionalization of CNT Based Thermal Interface Materials for Electronics Cooling Applications
Andreas Nylander, Yifeng Fu, Lilei Ye, Johan Liu
2017 IMAPS Nordic Conference on Microelectronics Packaging (NordPac), Sweden, 2017. DOI: 10.1109/NORDPAC.2017.7993188

Paper B. Covalent Anchoring of Carbon Nanotube Based Thermal Interface Materials Using Epoxy Silane Monolayers
Andreas Nylander, Yifeng Fu, Mingliang Huang, Johan Liu
In preprint, IEEE Transactions on Components, Packaging and Manufacturing Technology. DOI: 10.1109/TCPMT.2018.2863791

Paper C. Thermal Reliability Study of Polymer Bonded Carbon Nanotube Array Thermal Interface Materials
Andreas Nylander, Christian Chandra Darmawan, Ana Borta Boyon, Laurent Divay, Majid Kabiri Samani, Mohamad Abo Ras, Julien Fortel,Yifeng Fu, Lilei Ye, Afshin Ziaei, Johan Liu
2018 24rd International Workshop on Thermal Investigations of ICs and Systems (THERMINIC), Sweden, 2018

Other Contributions

Development of bulk-nanostructuring methods for BiSbTe thermoelectrics
Andreas Nylander, Nikolaos Logothetis, Johan Liu
2016 IMAPS Nordic Conference on Microelectronics Packaging, Norway, 2016.

Embedded Fin-Like Metal/CNT Hybrid Structures for Flexible and Transparent Conductors
Di Jiang, Nan Wang, Michael Edwards, Wei Mu, Andreas Nylander, Yifeng Fu, Kjell Jeppson, Johan Liu
Small, Volume 12, Issue 11, 2016, 1521-1527. DOI: 10.1002/smll.201503091

Thermal Conductivity Enhancement of Coaxial Carbon@Boron Nitride Nanotube Arrays
Lin Jing, Majid Kabiri Samani, Bo Liu, Hongling Li, Roland Tay, Siu Hon Tsang, Oliver Cometto, Andreas Nylander, Johan Liu, Edwin Hang Tong Teo, Alfred Ling Yoong Tok
ACS Applied Materials & Interfaces, Volume 9, Issue 17, 2017, 14555–14560. DOI: 10.1021/acsami.7b02154

Synthesis of a Graphene Carbon Nanotube Hybrid Film by Joule Self-Heating CVD for Thermal Applications
Josef Hansson, Majid Kabiri Samani, Andreas Nylander, Lilei Ye, Nan Wang, Torbjörn Nilsson, Johan Liu
2018 IEEE 68th Electronic Components and Technology Conference (ECTC), USA, 2018. DOI: 10.1109/ECTC.2018.00369

List of Acronyms

AFM	–	Atomic Force Microscopy
BGA	–	Ball Grid Array
BLT	–	Bondline Thickness
CMOS	–	Complementary Metal Oxide Semiconductor
CNT	–	Carbon Nanotube
CPU	–	Central Processing Unit
CTE	–	Coefficient of Thermal Expansion
CVD	–	Chemical Vapor Deposition
IC	–	Integrated Circuit
IHS	–	Internal Heat Spreader
ITRS	–	International Technology Roadmap for Semiconductors
MPC	–	Molecular Phonon Couplers
PCM	–	Phase Change Material
PLP	–	Particle Laden Polymer
PPR	–	Pulsed Photothermal Reflectance
PVD	–	Physical Vapor Deposition
SAM	–	Self-Assembled Monolayer
SEM	–	Scanning Electron Microscope
TCA	–	Thermally Conductive Adhesive
TIM	–	Thermal Interface Material
VDOS	–	Vibrational Density Of States
XPS	–	X-ray Photoelectron Spectroscopy

Contents

Chapter 1

Introduction

1.1 Background

Over the last decades, the world has witnessed an exponential miniaturisation of the integrated circuits we use in our electronic devices. This trend was already predicted and coined as "Moore's Law" in 1965 by Gordon Moore [1], who at the time was working at Fairchild Semiconductor (later co-founder of Intel). Moore's Law states that the number of transistors in integrated circuits (ICs) on a given area would double every 12 - 18 months as seen in Figure 1.1, which implied an cost/performance development that followed the same trend. Moore's Law has fueled the global economic growth by increasing the performance of affordable devices every couple of years [2].

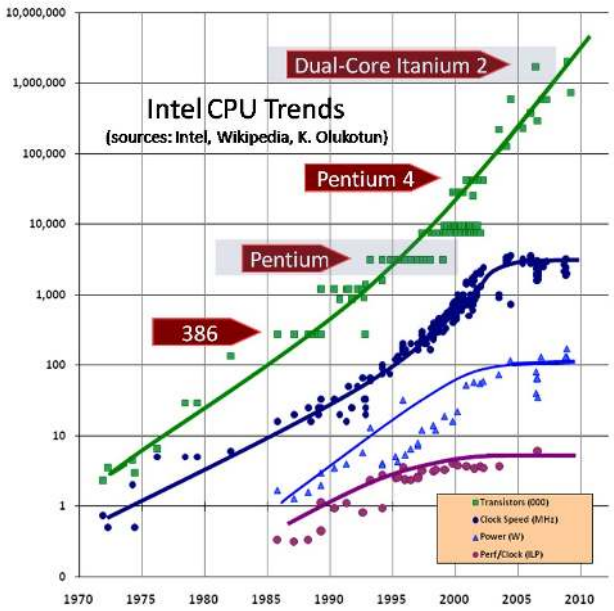

Figure 1.1: The development of consumer central processing units (CPUs) between 1970 to 2010. Reproduced from reference: [3].

Heat in electronic systems will be concentrated at high performance components as the thermal dissipation of ICs directly corresponds to the power consumption of each component. This is an issue both at the component and on board level as the heat from hot spots generated will be dissipated out through the system and cause reliability issues. The thermal dissipation needs have therefore steadily increased due to of processing units being developed with increased transistor densities and performance each year along the predicted pace [1]. The power dissipation of a transistor can be expressed as [4]:

$$P = CV^2 f \tag{1.1}$$

Where P is the consumed power in the transistor, C is the dynamic capacitance, V is the transistor voltage and f is the transistor frequency. Since the transistor frequency in turn is proportional to the voltage, the power dissipation can be written as proportional to the frequency to the power of three:

$$P \propto f^3 \tag{1.2}$$

With the cubic relation between power and frequency in transistors, the processor development finally reached a limitation around year 2000 when the hot spot temperatures became too difficult to handle. The power dissipation needs could be suppressed by increasing the number of parallel threads the processor could handle simultaneously with multiple core designs instead of increasing the frequency further. This solved the rampant thermal issues for a while but the transistor miniaturisation would still result in persisting power density increment.

Almost two decades after the introduction of multicore CPUs, the transistor miniaturisation has continued. With power being dissipated from smaller areas in devices every new design generation have resulted in increased hot spot temperatures. The continued transistor scaling have also led to transistor dimensions in ICs that now is pushing the physical limitations where quantum effects are becoming noticeable. As such the traditional transistor miniaturisation is reaching its end and the industry is trying to find new ways forward. According to the ITRS 2013 [5], the next generation of electronics will be developed using design concepts like 3D stacking and heterogeneous integration. These new concepts will help the industry to reach higher performances and an increased level of integration at a lower fabrication costs. A successful implementation of these concepts would mean a development similar to the traditional "Moore's Law" where the cost/performance steadily can be decreased. However, these new design concepts implies that the total thermal energy in electronic systems will increase even further in the future. By stacking high performance components on top of each other, heat will be concentrated and the hot spots will be trickier dissipate out from the system. Finding new ways to alleviate hot spots from ICs will therefore be of utmost importance in order to ensure a continued scaling of performance and reliability of electronic devices.

1.2 Thermal management

Thermal management became a vital part of electronics packaging in the early nineties with the introduction of the ball grid array (BGA) package that allowed higher performances than what had previously been possible [6]. The higher operation temperatures would result in device failures as a consequence of increased electromigration as well as material fatigue due to coefficient of thermal expansion (CTE) mismatches between different materials. The thermal dissipation requirements to keep the devices at safe temperatures could be achieved with the use of internal heat spreaders (IHS), heat sinks, thermal interface materials (TIMs) and fans. Such an electronic package can be found in Figure 1.2.

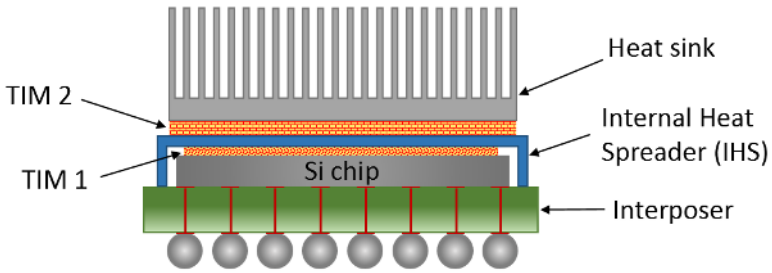

Figure 1.2: Illustration of how TIMs can be used in a thermal package. A common thermal package consists of an interposer structure and a CPU. The heat sink is used with an IHS together with TIMs to alleviate the CPU from excessive thermal build-up.

1.2.1 Thermal interface materials

Due to the impossibility of attaining surfaces with atomic flatness, gaps will always form in the interface between two surfaces. These gaps will hinder thermal conduction between said surfaces by isolating a large fraction of the total interface area, which severely constricts the thermal conduction pathways over the interface. TIMs can be used to connect the processor to an IHS and subsequently the IHS to a heat sink respectively. This is done in order to increase the thermal dissipation from electronic packages and keeping them running at safe operation temperatures.

According to Fourier's law, $Q = \frac{1}{R}\Delta T$, the thermal resistance R is a measure of how well a material can resist a heat flow Q, which in turn gives rise to a temperature drop ΔT over the material. In the same way, thermal boundary resistance (or kapitza resistance) is a measure of the thermal resistance across an interface. The thermal resistance over a TIM, R_{TIM} can thus be expressed according to Equation 1.3.

$$R_{TIM} = R_{C1} + \frac{BLT}{\lambda_{TIM}} + R_{C2} \tag{1.3}$$

Here, the total resistance over the TIM is expanded into three main contributions: The two thermal boundary resistances R_{C1} and R_{C2} describes the contacts between

the TIM and each of the contacting surfaces. The bulk thermal interface resistance originating from the TIM is described by the fraction of the bond line thickness (BLT) and λ_{TIM} which describes the thermal conductivity of the TIM. A TIM applied between two surfaces along with a working principle is illustrated in Figure 1.3.

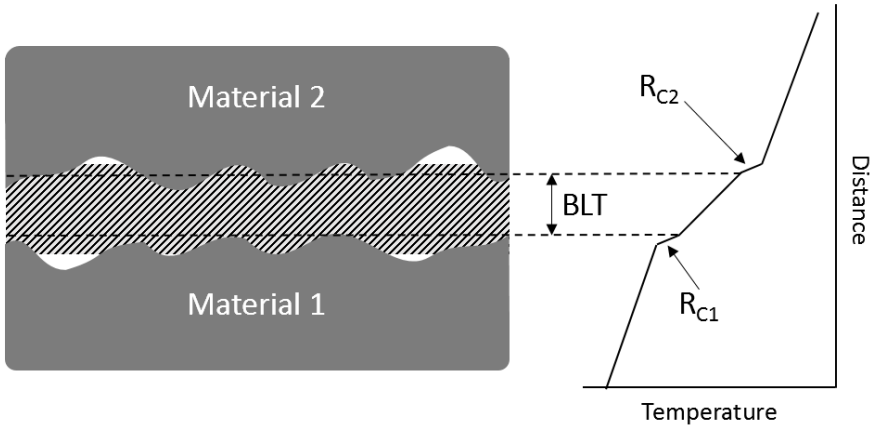

Figure 1.3: Illustration of a TIM applied in between two surfaces. The BLT of the TIM is marked together with the thermal boundary resistance contributions R_{C1} and R_{C2}.

To achieve a high performance TIM design, the origins of the thermal contact resistance that arises between two surfaces must be understood. This was illustrated by Yovanovich in the Thermal Contact Resistance Triad (Figure 1.4) that highlights the interplay between the surface topology (geometry), mechanics and thermal properties of the materials in the interface [7]. Therefore, the ideal TIM should both have a high thermal conductivity and be conformable enough to adapt to the surface topology in order to reduce the thermal boundary resistance as much as possible. Additionally, mechanical compliance is beneficial in order to allow the TIM to adapt under stress to compensate for CTE mismatches that otherwise can damage the interface.

Commercially available TIMs today are often either based on particle laden polymer (PLP) or solder designs. PLP based TIMs are composed of a polymer matrix loaded using particles with high thermal conductivity that enables these types of TIM to possesses a high level of conformability. Thermal grease is a basic PLP without any adhesive functionality that keeps the interface mechanically decoupled while decreasing the thermal resistance. Thermally conductive adhesives (TCAs) can be used to mechanically couple the interface, locking the components in position and at the same time keep a certain level of ductility in order to absorb stress. Although as PLP based TIMs offer a high level of reliability the thermal conductivity is relatively low. Solder based TIMs on the other hand usually offer a superior thermal conductivity. However, with the rigid mechanical nature of metallic systems, solder suffers from reliability issues that can crack the interface. A failed solder TIM would in turn result in escalating hot spots and an imminent system failure. Other

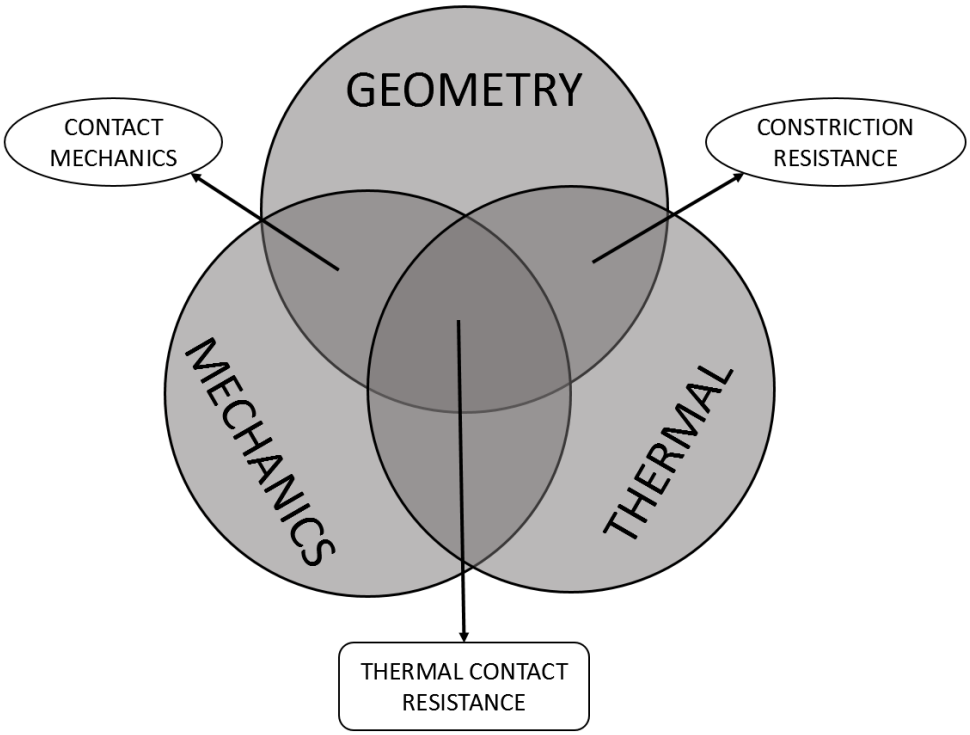

Figure 1.4: The thermal contact resistance triad that showcases the interplay between geometry, mechanical and thermal issues in an interface.

variants of PLP based TIMs are phase change materials (PCM) and thermal pads. PCMs are often used as a thermal buffer in applications where the thermal load is cycled in intervals. Thermal pads are removable at the expense of high thermal resistance. These different commercially available TIMs are listed i Table 1.1 for a quick overview of the typical thermal resistance offered.

Table 1.1: Different TIM categories with typical expected performance, from ref. [8]

Thermal interface material type	**Typical Thermal Interface Resistance (mm^2K/W)**
Thermal Grease	20
Thermal pad	200
Thermally Conductive Adhesive	50
Phase Change Material	50
Solder	<5

1.3 Carbon allotropes

Element number 6 in the periodic table, otherwise referred to as carbon, is one of the most versatile chemical components known to mankind. Carbon is the foundation of all organic chemistry due to its ability of forming double and triple bonds with its four valence electrons as well as the property of self-linkage (e.g. catenation). This allows carbon to arrange itself into longer chains in many varieties that allows carbon to exist in an unprecedented amount of complex molecules together with other elements. Carbon can also exist in a number of different solid forms by itself by altering the atomic configuration; this is referred to as allotropy. Five common allotropes, graphite, diamond, C60 Fullerene, graphene and carbon nanotubes (CNT), are illustrated in Figure 1.5.

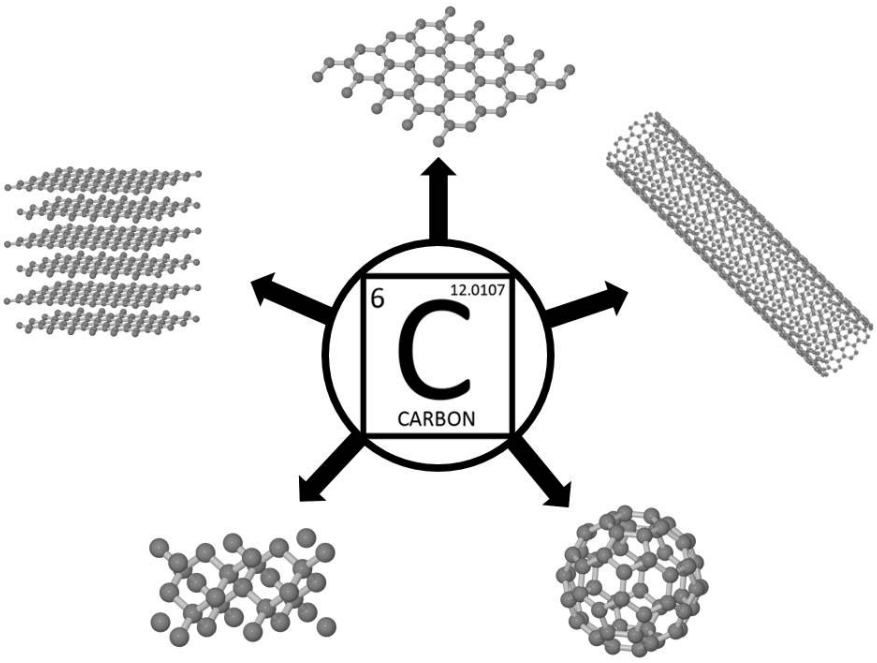

Figure 1.5: Carbon has many possible allotropes, among them are diamond, graphite, graphene, carbon nanotubes and the C60 Fullerene.

The difference in form and properties among carbon allotropes originate from the way the atoms bond to each other. The electrons in carbon can either exist in sp^3 or sp^2 hybridized configurations which results in 3 or 4 possible covalent bonds, this difference can give either a diamond or graphite like structure. Diamond is a hexagonal lattice structure where the atoms are bonded to 4 other atoms in 3-dimensions. Graphite in contrast is composed of 2-dimensional sheets of graphene stacked on each other with van der waals forces (π - π stacking). The van der waals forces in graphite originate from the out-of-plane π-orbital that is a result of the sp^2 hybridization which is illustrated in Figure 1.6. This makes graphite weak between the layers which makes it suitable as a lubricant, in contrast to the rigid 3-dimensional structure of diamond that is one of the hardest known materials. The graphene

hexagonal structure can be seen as the foundation for many of the carbon allotropes in the same way graphite can be considered being composed of many graphene sheets. Both 1-dimensional nanotubes as well as 0-dimensional Fullerene Buckyballs with many variants are possible just by rolling the graphene sheet appropriately.

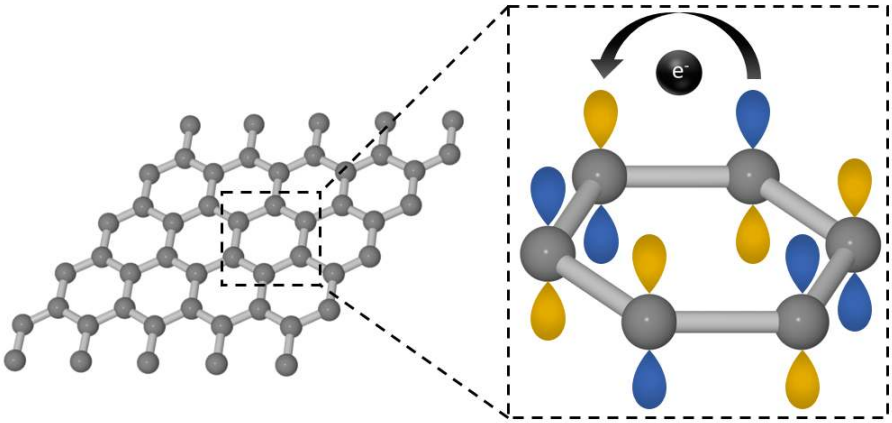

Figure 1.6: Sp^2 hybridisation for graphene results in out-of-plane π-orbitals (blue and yellow) that allows for efficient charge carrier transport as well as unique phonon modes, which allows an excellent electric conductivity as well as thermal conductivity. [9]

1.3.1 Carbon nanotubes

Carbon nanotubes, the 1-dimensional tube derivative of graphene, shares many of the unique properties originating from the crystal lattice structure. The folded structure of the CNT is illustrated in Figure 1.7. The CNT is notable for having been predicted to possess the highest thermal conductivity of any known solid (with the exception of graphene), a theoretic electronic current density of 1000 times that of copper and has been measured to possess a mechanical modulus of elasticity that is one order of magnitude higher than steel. [10–12]

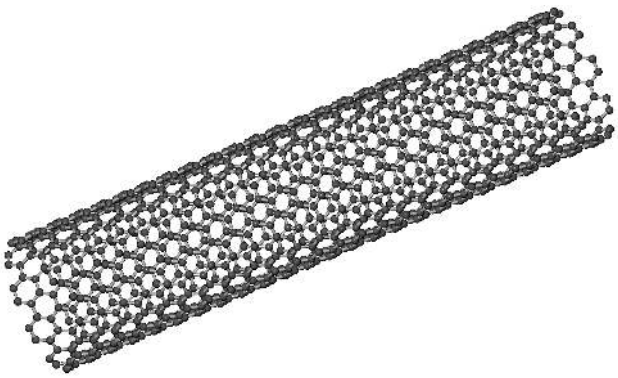

Figure 1.7: Illustration of the structure of a single walled carbon nanotube.

There are many variants of CNTs where the geometrical configuration can vary physical characteristics of the material. These configurations includes the number of walls, length, diameter, tube alignment and chirality. The electronic nature of a CNT tube is depending on the lattice angle, or rolling angle assuming that the tube being a rolled graphene sheet. As a consequence, this decides if the tube is of semiconducting or metallic nature [13]. This is called CNT chirality and is illustrated in Figure 1.8.

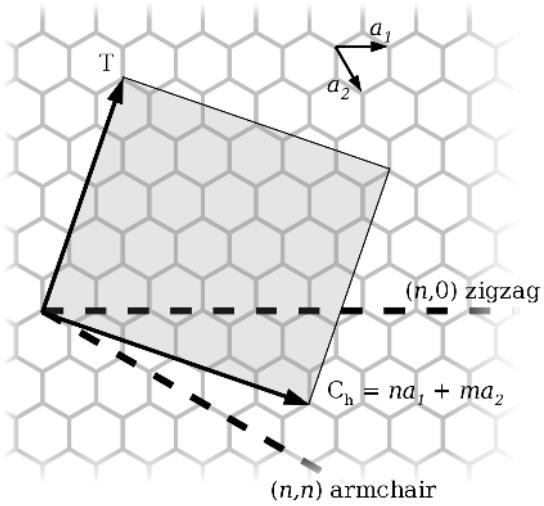

Figure 1.8: The CNT shell can depending on its chiral vectors either display metallic or semiconducting properties.

In multi walled CNTs there are multiple shells present in the tube structure and will as a result always be metallic in nature. Metallic single walled and multi walled CNT have empirically been measured to possess a thermal conductivity of up to 3500 W/mK [14] and 3000 W/mK [15] respectively, which is 9 and 7 times higher than copper. The metallic single walled CNT has been found to possess an electrical conductivity of 4 x 10^9 A/cm^2 [11]. Since the diameter of CNTs is measured in the nanometer range, they also possess a high surface area to volume ratio. All of these unique characteristics makes CNTs attractive alternatives to be used for a range of different applications and industries, including medical, construction and electronics [16]. The implementation and commercialisation of CNTs have been a slow endeavour and after almost 30 years of development the CNT revolution is yet to come. [17]

A number of different synthesis methods for CNTs have been developed over the years that either can be categorised as top-down or bottom-up approaches. In the case top-down synthesis of CNTs the production starts with carbon in bulk format, often graphite, which is broken down into smaller compounds [18]. In contrast, bottom-up synthesis starts with a carbon feed-stock, often referred to as precursor, in the form of a gas that is assembled into larger structures with the help of catalyst. [19]

The usually mentioned top-down methods for CNTs are: laser ablation [20] and arc discharge [21] that both breaks the lattice structure of carbon using a concentrated energy discharge. This will break the covalent bonds between the carbon atoms upon which they are allowed to find new configurations. This means in practice that many carbon allotrope configurations will be produced at the same time in a quantitatively stochastic distribution among each. The top-down methods can obtain CNTs of high crystallinity of different number of walls, chirality and length. However, since the obtained product includes many different carbon allotropes, extensive separation steps are required before a material with desired properties can be refined for use [22]. The produced materials of one selected property will be of low yield in either powder form or dispersed in a solvent.

The bottom-up fabrication methods for CNTs are commonly based on the chemical vapour deposition (CVD) technique. CNTs are manufactured by having carbonous precursor gases like acetylene and methane react with a catalyst in a controlled manner. A common design will allow CNTs to grow upward in an forest like fashion and form array structures where tubes stretch vertically from the nucleation site on the growth substrate and ends with a dome shaped top [23]. This material is commonly referred to as a CNT array and is illustrated in Figure 1.9. By engineering the catalyst particles and under-layers accordingly the orientation, diameter and number of walls can be controlled. This in turn also decides the thermal and mechanical properties of the CNTs [19]. The CVD process can only produce CNTs with rather sparse packing density and the properties of the CNT array will therefore scale accordingly. The effective thermal conductivity of the array depends on the packing density ϕ and the average thermal conductivity of the individual CNTs k_{CNT}, according to Equation 1.4.

$$k_{array} = \phi k_{CNT} = \frac{N_{CNT}}{A_{array}} A_{CNT} k_{CNT} \tag{1.4}$$

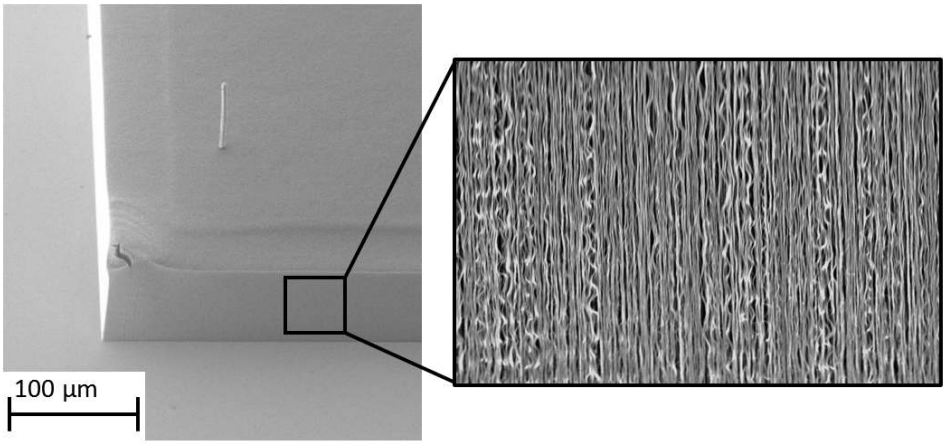

Figure 1.9: A CNT array using the CVD method. As seen the CNT are aligned in an upwards direction forming a forest like structure.

The density of CNT arrays can in literature be found to range between a couple of percent up to 43 % and an effective thermal conductivity up to 267W/mK. [10, 24–26]

1.4 Outline

This thesis is composed of three main parts in addition to this introduction. Chapter 2 provides an overview of the current status for CNT array based TIMs with a focus on organic functionalization methods. Chapter 3 continues the work outlined in the survey with the development of a new CNT array TIM bonded using epoxy chemistry. A reliability study of CNT array TIMs is presented in Chapter 4 in order to provide more data on how CNT array TIMs work under real conditions. This thesis is finally concluded with Chapter 5 that provides a summary of the work and the results obtained together with an outlook for the field.

Chapter 2

Literature review on CNT array TIMs

New materials and solutions are required as a consequence of the thermal dissipation challenges that future electronics development poses. The carbon nanotube is such a material that have been suggested to be suitable for thermal management due to its unusual properties.[27, 28] With a high thermal conductivity and an excellent mechanical compliance, CNTs are seen as the textbook candidate to be used as TIMs. By growing vertically aligned CNTs in arrays by the CVD method, CNT carpets can be obtained that can be used as TIMs for thermal management. This type of TIM is referred to as the CNT array TIM and sometimes CNT based TIM. The CNT array TIM is bonded between two surfaces for heat dissipation. This is done in order to allow each of the CNT to span the whole distance between one surface to the other and thereby providing heat conduction pathways as illustrated in Figure 2.1. There are many ways to bond the CNT array TIM and to apply them in an interface, these different strategies will be covered in the following sections of this chapter.

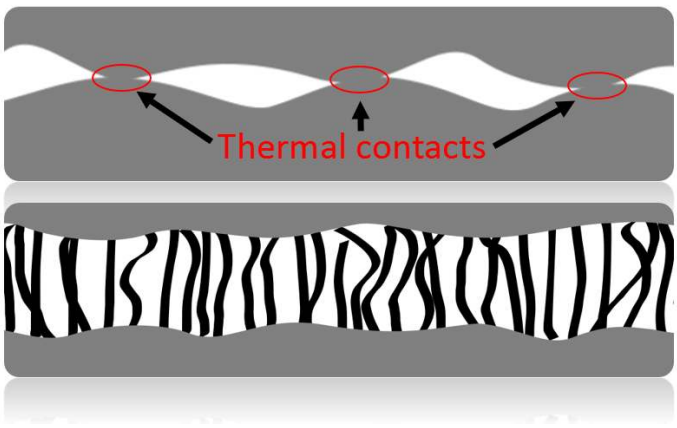

Figure 2.1: Illustration of how CNTs can be used as a TIM in order to reduce the thermal interface resistance. In this figure the CNTs are represented by black vertical strands connecting the two solids.

2.1 CNT synthesis by the CVD method

Due to the good alignment of CVD synthesised CNTs, the array structure obtained from CVD growth is well suited for TIM applications where heat needs to be transported from one side to the other.[29] For this reason, all of the CNT array TIMs covered in this thesis are made from multi walled CNTs grown using the CVD growth technique unless specified otherwise.

The CVD process in its simplest form is a chamber that can control pressure, temperature and supply of different gases. Depending on the heater configuration, the process can either be a hot wall CVD or a cold wall CVD as illustrated in Figure 2.2. The hot wall system can achieve a uniform temperature distribution by heating the entire reactor volume, thus providing a large production capacity at the expense of long process times. In contrast, the cold wall system utilises a joule effect heater that results in shorter process times together with production capacity limited to the heater surface area. Both the hot wall and the cold wall CVD systems are illustrated in Figure 2.2.

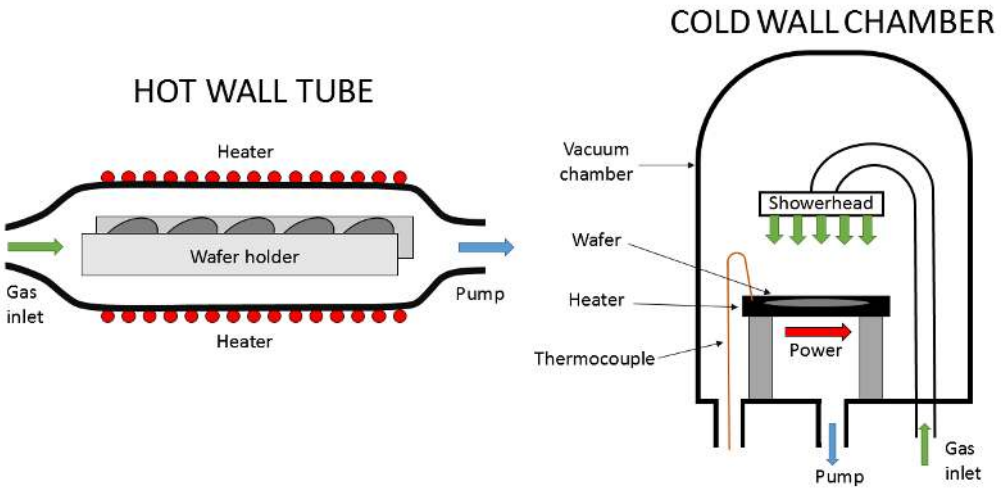

Figure 2.2: Illustration of the working principles of the hot wall and cold wall CVD systems.

Samples used for CVD based CNT growth consists of a barrier and a catalyst layer on top of a substrate. These materials are commonly prepared using Physical Vapour Deposition (PVD) electron beam evaporation techniques. The catalyst material is chosen for its ability to catalyse hydrocarbons and carbon diffusivity. Fe, Co and Ni are commonly used for this purpose [30]. The barrier layer serves two purposes, limiting the catalyst/substrate interaction as well as providing a surface energy that differs from that of the catalyst layer. Surface energy is a measure of the inherent intramolecular tension that was formed during the creation of the surface. By creating a barrier/catalyst interface with enough surface tension will force the catalyst to dewet from the barrier layer and thus divide itself into smaller spheres during

annealing. A common choice for the barrier layer is alumina, although quartz, silicon carbide, silica and magnesium oxide among others have been reported to work as well. A typical sample configuration for CNT array growth is using silicon substrates covered using a 10 nm thick alumina barrier layer and a 1 nm thick Fe catalyst layer. [19]

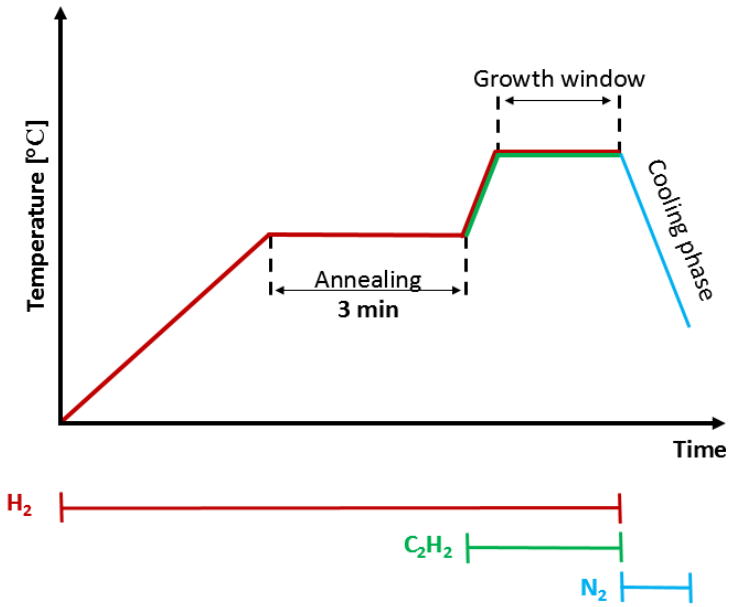

Figure 2.3: Diagram of the typical process when growing CNT arrays on silicon/alumina/Fe systems. The CVD growth process can be divided into 5 steps: Initial ramp up, catalyst annealing, growth ramp up, growth window and the cooling phase. The growth time can be adjusted in order to obtain CNTs with the desired height.

A typical process for CNT growth on silicon/alumina/Fe systems is depicted in Figure 2.3. The growth process begins by placing the samples inside the growth chamber and pumping down a vacuum. Once the pressure is low enough the system starts to fill the chamber with H_2-gas at the same time as it ramps the temperature to the annealing temperature for the samples. The catalyst will dewet during the annealing phase under the constant H_2-atmosphere and this will create a bed of spherical catalysts that CNTs will grow from. Once the annealing phase is completed, a precursor gas is introduced into the chamber as the temperature ramps to growth conditions. In the example provided in Figure 2.3, the growth precursor gas used is acetalyne (C_2H_2) [31], although methane gas (CH_4) [32] and ethylane gas (C_2H_4) [33] among others can be used as well. The growth time will directly control the height of the grown CNT arrays. The time/height relation is unique for every process chamber, the process time is therefore a parameter that should be investigated carefully when tuning the process. The growth is finished by flushing the chamber with N_2-gas in order to interrupt the growth and preventing the CNTs to grow further. [34] An illustration of the sample during growth can be found in Figure 2.4.

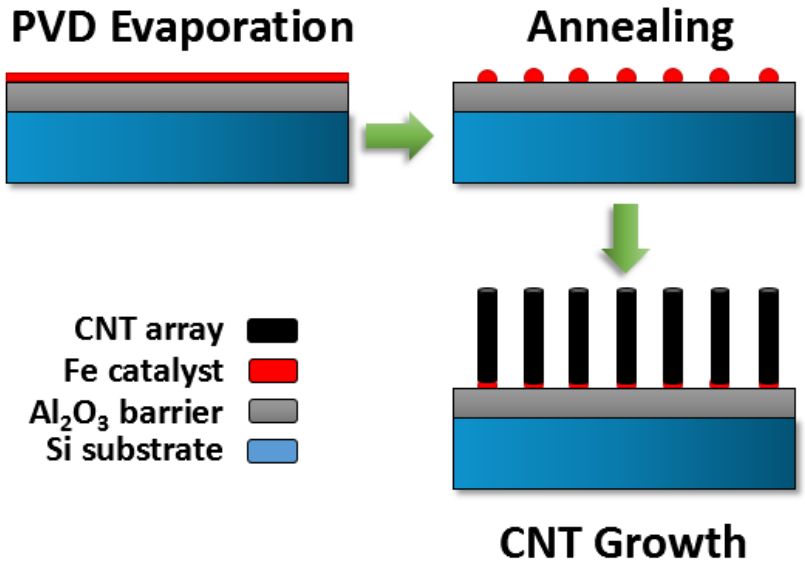

Figure 2.4: Illustration of a CNT growth substrate prepared using alumina and Fe as barrier and catalyst layers respectively. The illustration shows how the sample stages during the annealing and growth phases.

2.2 Interface configuration of CNT based TIMs

There are several ways to apply a CNT array as a TIM as illustrated in Figure 2.5. The most common is the one-side interface, illustrated in Figure 2.5A, where the CNT array remains attached to the growth substrate and bonded at the CNT tips to another substrate. The one-sided configuration is a good choice if the growth substrate can be included into the final TIM [35–37]. However, this won't be possible if the end application is restricted, which for example could be by CMOS compatibility issues due to the high processing temperatures involved in CVD synthesis of CNTs. As an alternative to the one-sided interface the array can be transferred as seen in Figure 2.5B, thereby removing the growth substrate and changing it to another bond substrate [38–40]. This type of interface can circumvent the CMOS compatibility which would allow for more applications where the TIM could be exploited at the cost of added fabrication complexity. The transferred interface would be best suited for reaching low thermal interface resistance due to the removal of the growth substrate. This due to some bonding techniques being reported to reach lower thermal boundary resistances than from the catalyst/CNT boundary. [41, 42]

Alternative methods for bonding CNT arrays are the two sided interface and the interposer interface, illustrated in Figure 2.5C and 2.5D respectively. The two sided interface is achieved by pressing two CNT arrays against each other and thereby increase the low filling fraction of CNTs in the arrays [43]. The last configuration covered is the interposer interface which is achieved by growing arrays on both sides of one substrate [44–46]. The resulting material would be suitable for large BLT applications with the double arrays but would at the same time suffer from additional thermal boundaries that would increase the thermal interface resistance.

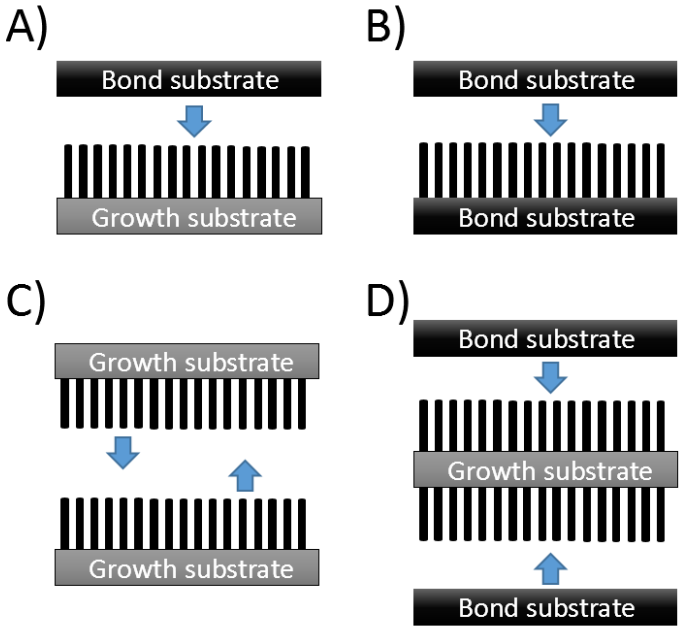

Figure 2.5: Different CNT array TIM configuration types. A) One-side interface. B) Transferred interface. C) Two-sided interface. D) Interposer interface.

2.3 Bonding strategies

The thermal resistance over the interface is proportional to the amount of CNTs that are allowed to contribute in the thermal conduction by directly bridging the interface. As the CNTs in the array are grown with a slight height difference, this can result in a considerable thermal boundary resistance. In order to solve this issue, three different bonding strategies are available. These are the dry contact, metal interface and the chemical functionalization methods. The general concept is illustrated in Figure 2.6 where an array closed with a dry contact is compared to an array closed with a bonding medium, which can be either organic or metallic.

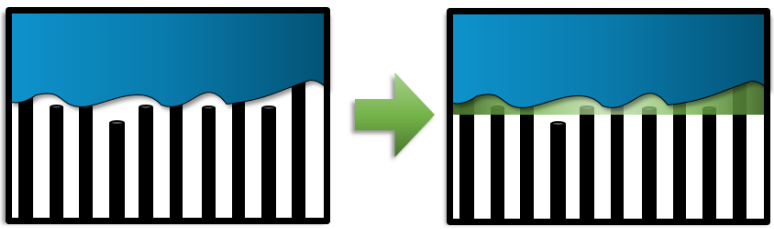

Figure 2.6: With the non-uniform topology of a CNT array either static pressure or a bonding solution is required in order to allow as many CNT strands as possible to participate in the thermal conduction.

The dry contact takes advantage of van der Waals forces in the contact interface between CNT ends and the mating substrate. By applying a constant pressure over the interface, the array can conform to the substrate topology, thereby increasing the contact area and at the same time improving van der Waals interaction in the interface. This type of CNT array TIM can be engineered by adjusting the surface roughness and by choosing an appropriate surface finish. Several studies have measured the effective thermal interface resistance of dry contact CNT array TIM using different contact substrates and have achieved thermal resistances of around 7 mm^2K/W. [24, 36, 37, 47]

To improve the contact interface some researchers have experimented with bonding methods that embeds the free ends of the CNT array in a metal coating placed on the surface of the bond substrate. This physical bonding locks the CNT ends in position under pressure, which results in a CNT array TIM without the need of static pressure. The CNT array TIMs can be engineered by varying the metallic coating thickness, that in turn will decide the required bond pressure as well as how many of the CNTs that will bond to the contact substrate. The performance of the CNT array TIM will depend on this since only the bonded CNTs will contribute to the total thermal conduction across the interface. To achieve a metal interface with low thermal boundary resistances, the metallic coating also requires a low viscosity under reflow for the CNT strands to penetrate the metal coating layer. This method has demonstrated resistances as low as 1 mm^2K/W in literature. [24, 34, 39]

The thermal conductivity in all solid materials consists of both a vibrational (phonons) and an electron contribution. In CNTs, the phonon contribution to thermal conductivity dominates over the contribution of electrons [48]. Therefore, phonon - electron thermal mismatch in the CNT/metal interface will always be a limitation in metal interface based CNT array TIM. By using a polymeric bonding agent instead, the contact resistance could be decreased further. A material with phonon modes that has a higher compatibility with the CNT could decrease scattering in the interface. [49]

In order to decrease the resistance even further in thermal packages, anchor points are prepared using self-assembly based monolayers on the bond substrate. These anchor points can form covalent bonds with the CNTs and thereby help phonons to transverse over the interface [50]. This could be achieved by so called molecular phonon couplers (MPCs) that either bonds the CNTs to the substrate using covalent bonds or side wall functionalization using π - π bonding. However, covalent bonds are difficult to form on the stable sp^2 carbon structure and might require extra processing steps to break the atomic structure of the CNTs. [51, 52]

There are three directions in the field of organically bonded CNT array based TIM with different approaches. A summary of published results for organically bonded CNT array TIMs can be found in Table 2.1.

Table 2.1: Summary of research related to organic functionalization methods for CNT array TIM. Here the BLT is given in μm and the R_{TIM} is given in mm^2K/W.

Description	**Bond material**	**BLT**	**R_{TIM}**	**Ref.**
Polymer embedding				
Si-CNT-PCM-Cu	PCM45F	10	5.2	[35]
Si-CNT-Wax-Ag	Paraffin wax	50	2	[53]
Si-Wax-CNT-Cu-CNT-Wax-Ag	Paraffin wax	50 (125)	10	[53]
Wax-CNT-Al-CNT-Wax	Paraffin wax	50	10	[54]
Si-CNT-Polymer-Cu	PEMA 300 nm	10	1.8	[55]
Si-CNT-Polymer-Cu	PEMA 600 nm	10	2.5	[56]
Si-CNT-Polymer-Ag	Polystyrene	10	8.5	[57]
Si-TCA-CNT-TCA-Cu	TCA	100	3.9	[58]
Si-CNT-Polymer-Cu	Polymer	10	5.7	[59]
Polymer bonding				
Si-CNT-Polymer-Cu	HLK5	10	1.4	[56]
Si-CNT-Polymer-Ag	P3HT	10	4.9	[57]
Si-CNT-Polymer-Cu	HLK5	10	9.5	[60]
Si-CNT-Polymer-Cu	HLK5	10	3.1	[59]
Self-assembly based bonding				
Si-CNT-SAM-Cu	Trimethoxysilane	100	10	[61]
Si-CNT-SAM-Al	APTES	70	0.6	[51]
Si-CNT-SAM-Au	Cysteamine	70	0.8	[51]
Si-CNT-SAM-Cu-Ag	Pyrenylpropyl	15	4.6	[62]
Si-CNT-nanoPd-Ag	nano-Pd	20	11	[43]
Si-CNT-nanoPd-CNT-Cu	nano-Pd	40	5	[43]

The most common approach is referred to as polymer embedding. This method uses a polymer of sufficiently low viscosity to penetrate into the array before curing, thus fixating the CNTs against the substrate. This method is very similar to the metal bonding since no covalent bonds form between the CNT and the polymer. Phonon mode excitation matching can be possible in the CNT-polymer interface thus allowing a higher phonon transmittance through the interface than in the case of CNT metal interface bonding. [49]

The second discussed direction is the polymer bonding method. Like the organic embedding method the CNT arrays are also mechanically fixated inside a polymer phase to ensure an as high surface contact area as possible. In order to decrease the thermal interface resistance even further, chemical bonding is exploited. This will in principle couple the vibrational density of states (VDOS) of CNT with that of the functionalization molecule, as can be seen in Figure 2.7, to provide better phonon propagation through the interface. [63]

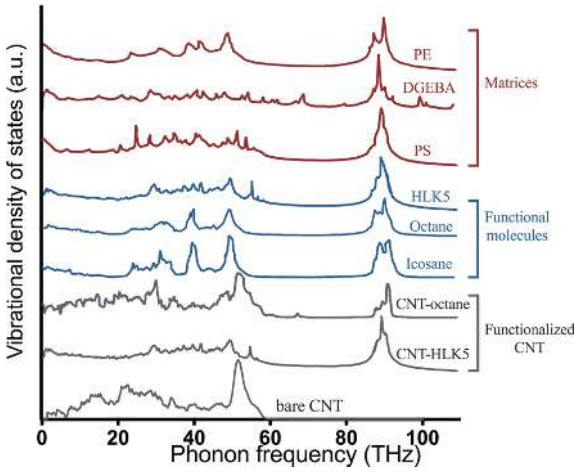

Figure 2.7: Comparison of the normalised vibrational density of states for different polymer matrices, functional molecules, functionalized CNT and bare CNT. Reprinted with permission from ref. [63].

The third part explored is referred to as self-assembly based bonding. By using a monolayer of molecular anchors to bind and fixate the CNT to a substrate, a directed propagation of phonons can be achieved. As illustrated in Figure 2.8, MPCs consists of self-assembled monolayers that can form on the surface of a substrate. This method allows the use of a atomically thin polymer layer, thus minimising the thermal resistance due to inelastic phonon scattering and provides an as direct phonon pathway as possible. The tails of the MPC can then react covalently or through sidewall interactions to the CNT array tips. For covalent bonding to be possible, defects are required in the CNT arrays and might require extra processing steps. This can for example be achieved by plasma etching which also opens up the tips of the CNT and allows for a larger portion of the walls to contribute to the overall thermal conductivity. [50, 51]

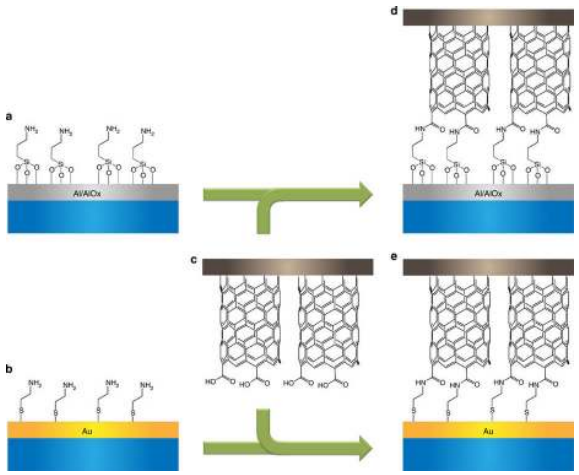

Figure 2.8: An illustration of how self-assembled monolayers of molecules can bridge CNT arrays with substrates. Reprinted with permission from [51].

2.4 Summary

In summary, three different organic approaches to interface bonding of CNT array TIM have been discussed and the experimental results are summarised in Table 2.1. It is difficult to draw any relations between array height and thermal resistance due to the low spread in array thickness and irregular results from the reported experiments. Like most TIMs, the choice of interface solution will be application dependent. Optimal solutions will be found by using the advantages of the different approaches to best suit the environmental demands for every product. By only comparing the best results from each of these approaches it can be seen that the MPC technique could reach down to 0.6 mm^2K/W which could be compared to bonding and embedding with thermal resistances that results in about two times higher and three times higher values respectively. However, comparing with results from corresponding metal bonding techniques reported, further improvements should be possible to reach by using polymers that allows better matching of CNT phonon vibrational density of states.

Even though many of the findings in literature match and surpass the traditional PLP and solder based TIMs, no commercial products can be found yet based on CNT array structures. This has most certainly to do with the lack of large-scale fabrication methods that can ensure high quality CNTs. Furthermore, none of the surveyed articles includes reliability studies with proper cycling and failure analysis. The reliability is an important aspect to take into account if CNT array based TIMs are expected to reach any commercial success in the future.

Chapter 3

Development of CNT array TIMs

To successfully decrease the thermal boundary resistance in CNT array TIMs, it is important to understand the thermal transport mechanism. The dominant thermal carrier in CNTs are lattice vibrations, i.e. phonons. By bonding the CNT using a metal that utilises electrons as thermal carrier, the phonon energy needs to be converted at the interface. This phonon - electron mismatch therefore acts as a limiting factor in all metal-bonded CNT based TIMs [49]. Organic functionalization materials in which the thermal transport also is phononic in nature, should thus be explored to couple the vibrational states between the polymer and the CNTs. In order to exploit this behaviour, covalent bonding is required between the CNT and the mating substrate to allow optimal phonon transport over the interface. This chapter is based on Paper B, which deals with the fabrication of epoxy-silane based monolayer CNT array TIMs.

One way to capitalise on the phononic nature of CNTs is to covalently anchor the CNT strands at the contact substrate. However, by bonding the CNTs in a polymer layer would in principle result in a dampening effect that could reduce the phononic transport over the interface. This effect has been demonstrated with PEMA functionalization. By reducing the bond layer from 600 to 300 nm thickness resulted in a 28% improvement in terms of thermal interface resistance [55, 56]. By taking this principle further, the perfect organic functionalization would be only one molecular layer thick at the same time as it would contact all of the CNT tips covalently to the contact substrate. One such solution is using self-assembled monolayers with appropriate head groups that can covalently anchor the CNT tips at the surface. [51]

In Paper B we used (3-Glycidyloxypropyl)-trimethoxysilane (commonly referred to as epoxy silane as illustrated in Figure 3.1) as a monolayer for covalent anchoring of CNT array TIM. This molecule has a trimethoxysilane backbone for the self-assembly together with an epoxide group that is intended for covalent bonding with CNTs. As with the case of commercial epoxy chemistry, epoxides form covalent bonds together with amino groups, therefore the CNTs require amino modification before they can bond successfully to the epoxy silane.

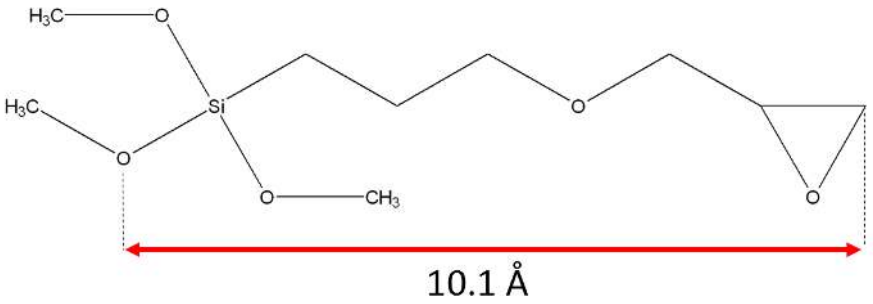

Figure 3.1: Epoxy silane molecule used as covalent coupler for CNT array TIM.

3.1 Sample preparation

The intended CNT array TIM is composed of two main parts: the epoxy silane functionalized Si substrates and the CNT array covered Si growth substrates, both of which are illustrated in Figure 3.2. The fabrication and preparation of both of these components are discussed in the following sections.

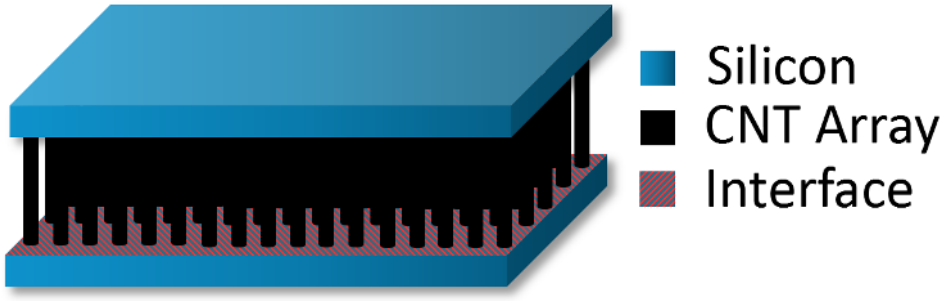

Figure 3.2: Illustration of a typical one-sided interface CNT array TIM assembly.

3.1.1 Monolayer formation on Si substrates

Silicon substrates with a 12 nm thick surface oxide were used for the epoxy silane functionalization. The substrates were cleaned from any organic contamination and subsequently protonated in a 3:1 piranha etching solution for 20 minutes [64]. A functionalization bath consisting of 80 vol% cyclopentanone, 10 vol% methanol and 10 vol% (3-Glycidyloxypropyl)-trimethoxysilane (Epoxy silane) was used to functionalize the silicon substrates by submerging the substrates into the bath for 20 minutes [65]. After silane coating, the silane - silicon oxide reaction was quenched by rinsing the substrates in pure methanol for 1 minute and DI-water for 2 minutes. The silane functionalized substrates were stored in DI-water over night in order to render the silane monolayers hydrolytically stable [66]. All chemicals were bought from Sigma Aldrich and used without modification. This process is depicted in Figure 3.3.

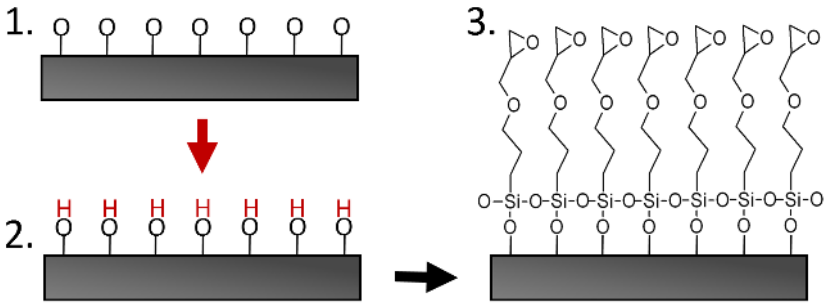

Figure 3.3: Description of the silane functionalization process. 1: A uniform thermal oxide is grown on silicon substrates. 2: Protonation of the oxygen sites on the wafer is achieved by submerging the substrates into a bath of piranha solution. 3: The -OH groups are now enabling the silane molecules to anchor themselves to the silicon substrate.

The quality of the as-prepared epoxy silane substrates was analysed in terms of surface coverage and composition using ellipsometry, atomic force microscopy (AFM) and x-ray photoelectron spectroscopy (XPS). An ellipsometric height map of the samples is shown in Figure 3.4. The surface of a silicon substrate was measured before silane deposition and the average thickness of the oxide layer was used in the model to describe the layers underneath the silane monolayer. After monolayer deposition, the average measured thickness of the top layer was found to be 0.95 nm with an standard deviation of 0.17 nm over the entire region. This result can be explained by the oxide layer having a similar thickness deviation that could not be taken into account in the data analysis and should thus be disregarded. These values are therefore in agreement with the expected thickness of the 1 nm of a bonded epoxy silane monolayer, as can be seen in Figure 3.1.

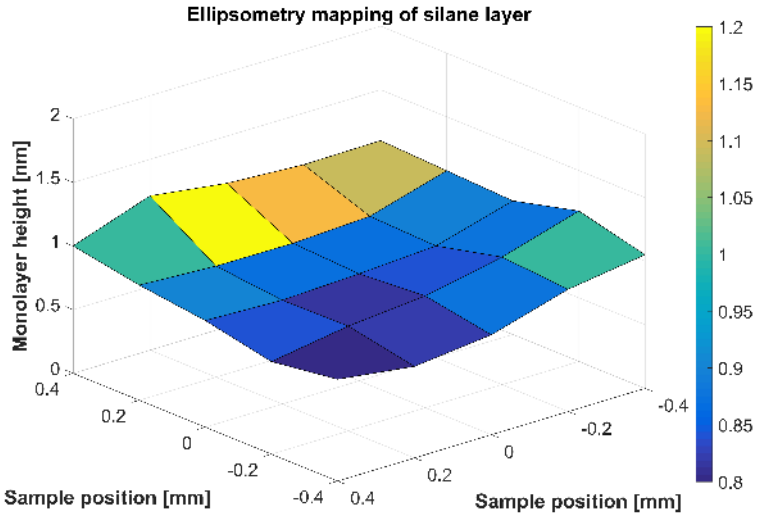

Figure 3.4: Mapping of the epoxy silane thickness across a silicon substrate surface obtained by ellipsometry.

It is important to avoid island growth for the silane layer since this actively will decrease the area where covalent bonding with CNT can take place. By using AFM as a compliment to the ellipsomitry data, a more detailed height mapping of the surface in the X - Y plane could be obtained and analysed for the samples. As seen in Figure 3.5 where Figure 3.5A shows a sample with bad surface coverage in comparison to a sample with full coverage that can be seen in Figure 3.5B. A complete coverage of the surface is characterised by having a low surface roughness in comparison to the theoretical monolayer thickness. The measurement from Figure 3.5B gives a surface roughness of 0.16 nm that can be compared with the 0.25 nm roughness of the silicon substrate that were measured before silane coverage. This decrease in surface roughness after monolayer coating has been observed previously for similar silane based monolayers on silicon substrates [67].

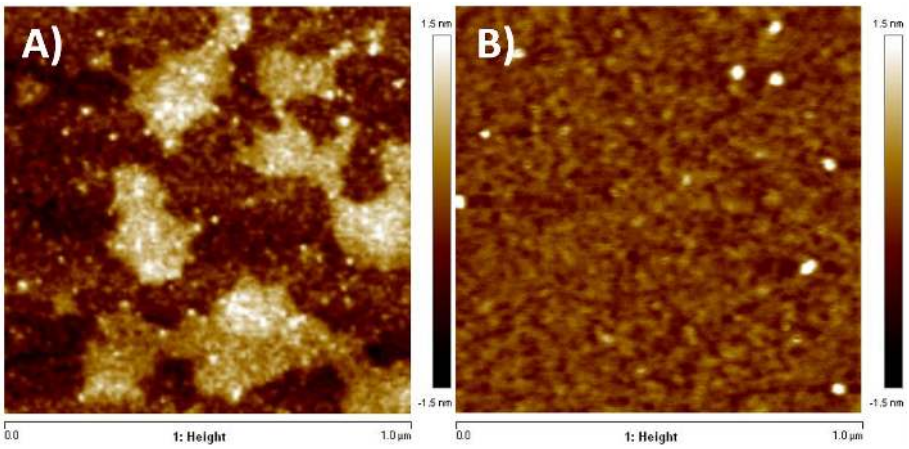

Figure 3.5: Figure 3.5A shows a typical AFM measurement of silane molecules growing as islands and Figure 3.5B depicts a sample with complete coverage of the surface.

Elemental characterisation of the silane substrates was provided by XPS. As seen in Figure 3.1, the main bonds present in the epoxy silane molecule are the epoxy group at 286.1 - 287.1 eV, -C-O-C- ether found between 286.1 - 288.0 eV and the sp^2 bonded carbon around 284.3 - 284.6 eV [68]. An XPS spectrum of the carbon peak obtained from the epoxy silane modified substrate can be seen in Figure 3.6. Three components could be identified through deconvolution: Peak #1 at 287.5 eV, peak #2 at 286.1 eV and Peak #3 at 284.5 eV. These peaks can be matched with the different parts of the epoxy silane molecule where Peak #1, #2 and #3 corresponds to the ether, epoxy and sp^2 components respectively. It is worth mentioning that the organometallic silane component found in the epoxy silane molecule is stated in literature to appear at 284.4 eV, which means that it disappears in the sp^2 peak [69]. This also implies that the intensity of Peak #3 will be elevated in relation to the other peaks present.

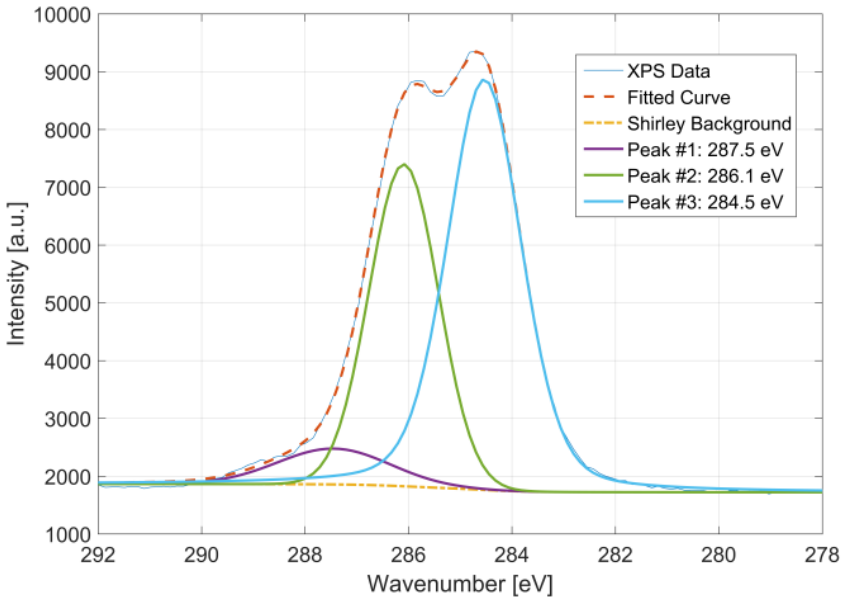

Figure 3.6: Deconvolution of XPS spectrum acquired from the C1s spectrum aquired from the epoxy silane modified Si substrates. The XPS data were fitted by extraction of the individual elemental contributions found on the sample surface.

The topological and elemental data acquired from the modified substrates shows that homogeneous monolayers of epoxy silane molecules were successfully formed on the surface of the Si substrates.

3.1.2 CNT array preparation

The CNT arrays used in this work were prepared using a Black Magic CVD system provided by Aixtron corporation. Si chips with 10 nm Al_2O_3 and 1 nm Fe serving as diffusion barrier and catalyst layers respectively were used as the growth substrates. CNT arrays were grown to a thickness of 50 μm inside the CVD system at 700 °C using a gas mixture of acetylene and hydrogen.

Amino groups were embedded into the CNT structure to provide the CNT samples with the necessary chemical functionality for covalent bonding to occur with the epoxide groups found on the silane monolayer. CNT samples were exposed to a 2:1 gas mixture of nitrogen and hydrogen in an Oxford Plasmalab 100 plasma chamber. This was accomplished with 50 W of DC bias and 100 W of ICP RF power under 20 mBar pressure with a process time of 10 minutes.

The CNT samples after plasma treatment using nitrogen and hydrogen gas were measured using XPS in high-resolution scanning mode. To find the nature of the infused species after treatment, C1s and N1s peaks were deconvuluted into their individual contributions.

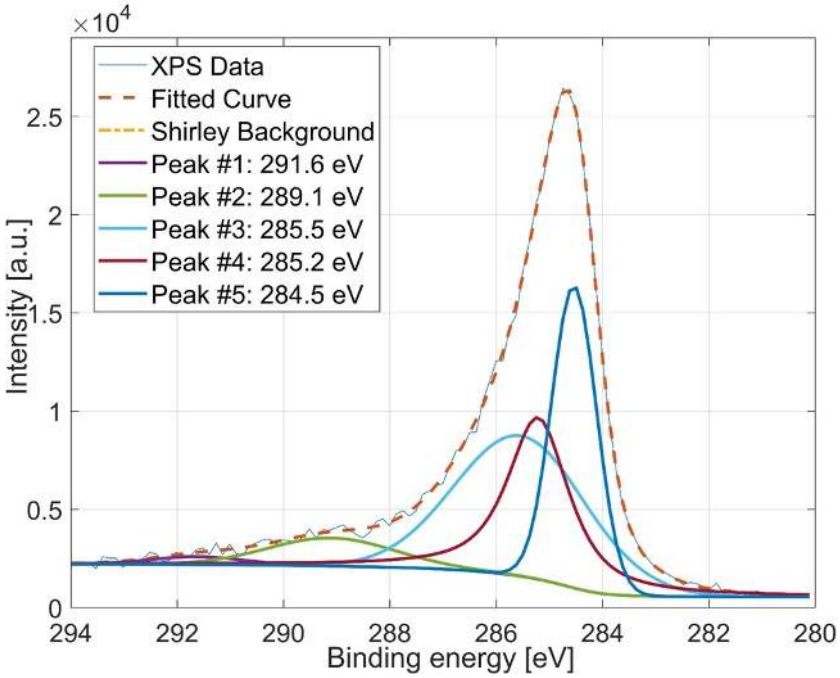

Figure 3.7: Deconvolution of XPS spectrum acquired from the C1s spectrum acquired from the nitrogen plasma modified CNT arrays. The XPS data were fitted by extraction of the individual elemental contributions found on the sample surface.

The deconvolution of the C1s peak can be found in Figure 3.7. Here, three main and two minor components could be extracted. The main peaks (Peak #3-5) are located at 285.5, 285.2 and 284.5 eV and the minor peaks (Peak #1 and #2) at 291.6 and 289.1 respectively. By comparison, the location of these peaks in the spectrum could be matched with reference data and corresponding functional groups could be identified [68]. Peak #5 corresponded to the sp^2 bonded carbon, this is the main lattice of the CNT structure. Peak #4 was found to be an sp^3 peak which originates from amorphous carbon as well as eventual damages to the CNT structure after plasma etching. An amino peak could also be matched to peak #3; this is an indication that the plasma treatment successfully created amino functional groups embedded into the CNT structure. The two minor peaks, peak #1 and #2, are matched with smaller amounts of fluorine carbon and oxygen containing compounds that might have appeared during the sample processing.

The N1s peak found in Figure 3.8 was also deconvoluted in order to gain more information about the nitrogen present in the CNTs. Two peaks could be extracted, the Peak #1 at 400.4 eV and Peak #2 at 398.8 eV. It has been reported that pyridine and nitrile in CNT specimens can give rise to peaks around 398.5 and 398.8 eV [70]. Other nitrogen containing groups like amine and amide have in literature been found at binding energies ranging from 399.5 - 400.5 eV [71].

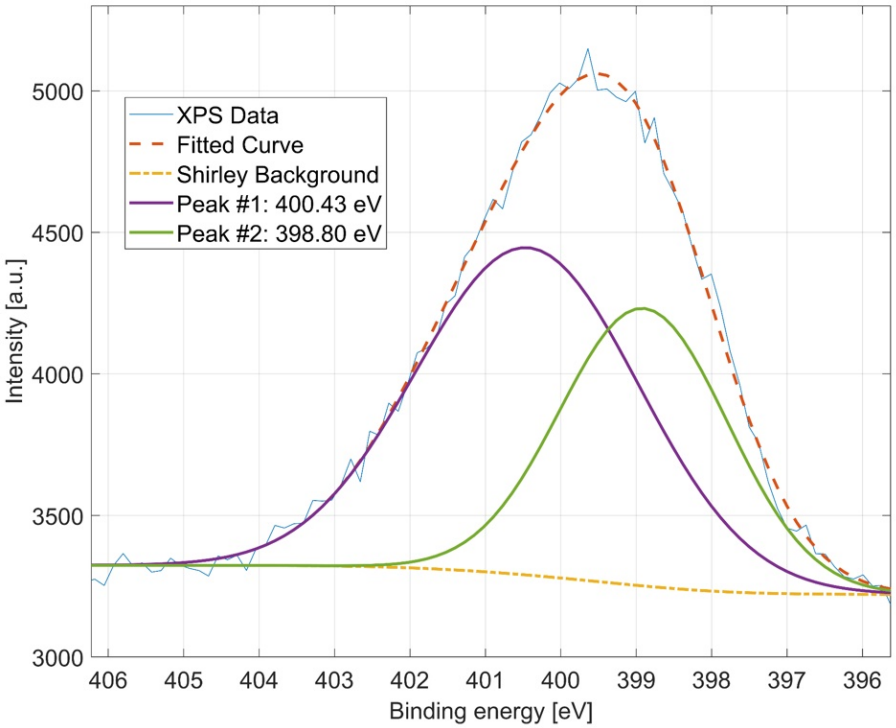

Figure 3.8: Deconvolution of XPS spectrum acquired from the N1s spectrum acquired from the nitrogen plasma modified CNT arrays. The XPS data were fitted by extraction of the individual elemental contributions found on the sample surface.

With the information obtained from Figure 3.7 and 3.8 we can draw the conclusion that the CNT tips were successfully activated with amino functional groups using nitrogen plasma. The plasma treatment resulted most prominently in amino groups together with smaller amounts of pyridine and/or nitrile on the surface of the CNT array. Additionally, small trace amounts of fluorine and oxygen bounded to the CNT structure could be detected.

3.1.3 Interface closing

The closing of the interface between the silane functionalized silicon substrate and the amino activated CNT array was made using a custom made-clamp. The parts were pressed together under 70 kPa pressure in a oven at 120 °C under nitrogen atmosphere for 1 hour.

3.2 Sample characterisation and results

The thermal interface resistance of the fabricated samples were measured using an LFA 447 Laserflash system. The measurement was conducted under standard atmospheric pressure, at different temperatures between 20 and 120 °C without any static pressure applied over the sample interfaces. By a fitting algorithm the thermal interface resistance of the samples could be extracted from the obtained signal using a 2 layer method that takes the contact resistance into account for the configuration [72]. A cross section of the CNT based TIM can be found in Figure 3.9 together with a thermal resistance circuit that explains the thermal resistance contributions taken into account in these measurements. By disregarding the thermal bulk resistance of the two silicon substrates we can separate the two contact resistances R_{C1} (CNT catalyst side) and R_{C2} (epoxy silane side) and the thermal bulk resistance of the CNT array denoted ΣR_{CNT} (according to Equation 1.3). In this paper the results were averaged for three silane modified samples and compared to identical reference interfaces consisting of dry contact CNT TIMs without silane modification in order to obtain a relevant comparison.

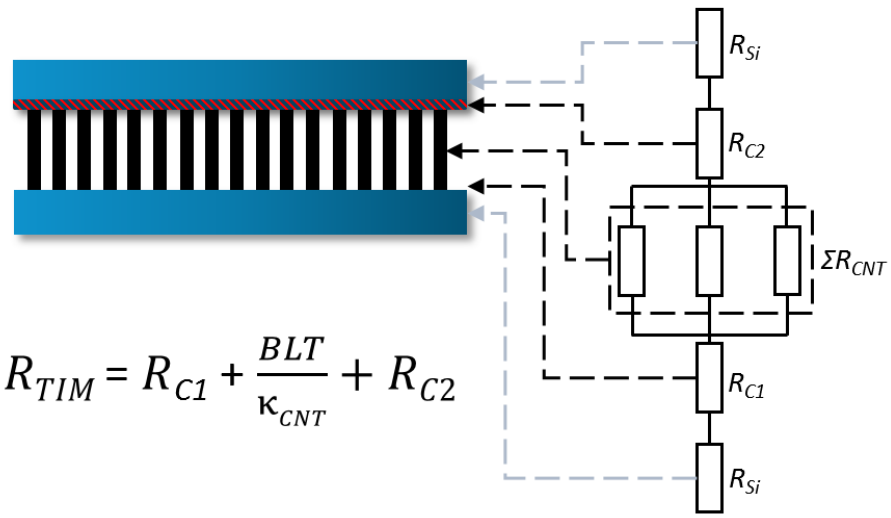

Figure 3.9: A cross section of the fabricated CNT based TIM together with a thermal circuit. The thermal resistance values obtained for these TIMs are the sum of the two thermal contact resistances on either side of the CNT array together with the bulk thermal resistance of the CNT array. The resistance of the CNT array can be expressed by the bond line thickness divided by the effective thermal conductivity. The resistance contribution for either of the two silicon substrates are greyed out since these aren't included in the final results.

The manufactured CNT based TIM samples bonded with the epoxy silane molecule were compared to reference samples. The thermal interface resistance results plotted against measurement temperature can be found in Figure 3.10. From these results, it can be seen that an improvement of about 5 % was achieved in terms of thermal interface resistance using the epoxy silane as a molecular coupler together with the CNT.

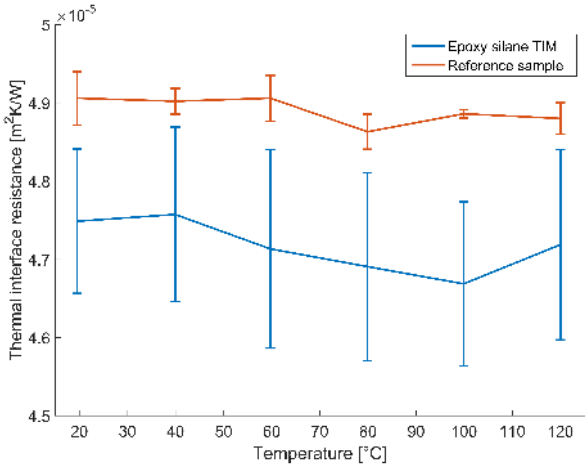

Figure 3.10: Averaged thermal measurement results for three of the CNT based TIMs bonded with the epoxy silane molecular coupler plotted against a reference sample. Here the error bar represents the standard deviation of the results for all the measured samples.

The interfaces were opened after thermal measurement in order to observe the orientation of the CNT arrays. A scanning electron microscope (SEM) image of the opened interface can be found in Figure 3.11. Here it can be seen that the CNT array was toppled over in the closing process, thus suggesting that the activated CNT ends no longer connects with the silane layer on the silicon substrate as intended. This should increase the total contact area between the CNT array and the Si substrate but since the penetration depth of the nitrogen plasma treatment have not been studied in detail, the actual coverage area where covalent bonding between the epoxy silane layer and the CNT array can take place actually can be lower than expected. This would also explain the unusually large error for the epoxy silane samples in contrast to the reference samples. Although, the small yet distinct improvements in regards to thermal resistance indicates that some degree of improved bonding indeed has taken place in the CNT - Si interface. By finding a method to circumvent the CNT bending issue discovered, a higher performance should be attainable using the method described in this paper.

Table 3.1: A summary of the relevant results regarding CNT based TIMs for comparison.

Description	Thermal resistance	Ref.
Thermal grease	20 mm^2K/W	[73]
Solder	5 mm^2K/W	[74]
Dry contact CNT TIM	7 - 15 mm^2K/W	[37, 75]
Organic CNT TIM	1.4 - 10 mm^2K/W	[56, 61]

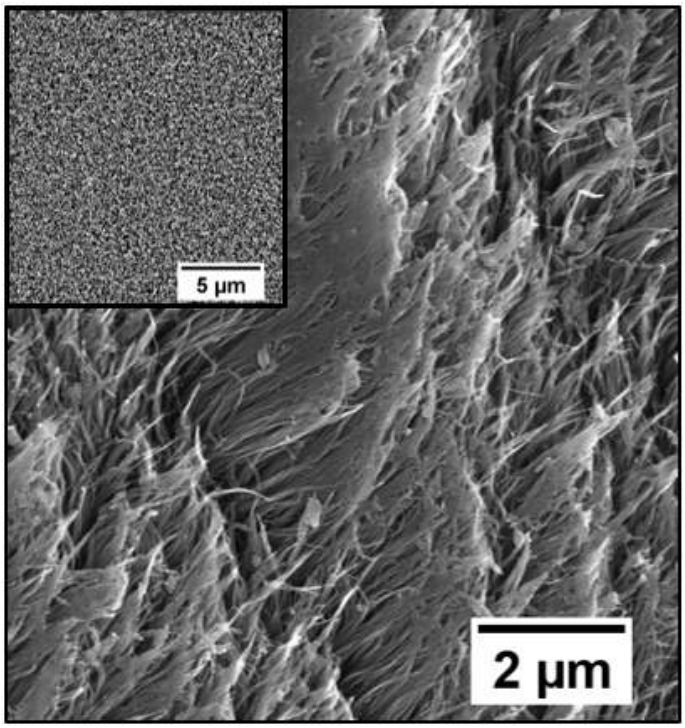

Figure 3.11: SEM image of the CNT top side after bonding. The CNT ends have been pressed downwards and embedded into the array as a result of the interface closing process. The inset picture shows how CNT arrays looks like before compression.

Table 3.1 contains experimental thermal resistance results previously published for dry contact CNT based TIMs and organic CNT based TIMs together with commonly found values for thermal grease and solder. Our reference samples should be comparable with the dry contact CNT TIM results and our epoxy silane CNT TIM should be comparable to the organic functionalized CNT TIM. Worth noting is that the results for our fabricated reference samples are much higher than the previously reported results for similar dry contact CNT TIM without external pressure. A potential explanation for this could be that the quality of the grown CNT arrays are different than in the reported references. Everything from the array uniformity to CNT defects to the quality of the CNT/catalyst interface could affect the CNT based TIM quality and the exact reason for the unusually high results in our case is difficult to pinpoint without a deeper analysis. This would in turn also affect the final thermal interface resistance of the epoxy silane interfaces as well since both are fabricated from the same CNT arrays.

3.3 Conclusions and outlook

A thermal interface based on CNT arrays bonded to a silicon substrate was successfully fabricated. By utilising the epoxy silane phonon coupler together with amino activated CNT arrays, covalent anchoring could be achieved. The final samples were measured using the laser flash method to find the thermal interface resistance. These results showed a slight and consistent improvement in relation to a reference sample. This study indicates that monolayer phonon couplers are useful for CNT based TIM applications in order to reduce the thermal interface resistance usually found there. With the monolayer thickness only being 1 nm thick the applied pressure has to be applied evenly across the whole array, at the same time as the bonding pressure over the array has to be enough in order for the whole array to reach the anchor points. However, the closing process needs to be optimised in order for the closing process to be conducted with the entire CNT array structure kept intact. By improving the interface closing process this method will be useful for fabricating CNT array TIMs.

Chapter 4

Reliability study of CNT array TIMs

CNT array TIMs have been demonstrated by several research groups to show the potential to replace current commercially available solutions. However, there are still some practical concerns to solve before this technology is mature enough for a market realisation. One of those concerns is regarding the reliability as literature is lacking of studies on this subject. In Paper C, a CNT based TIM closed using the HLK5 polymer developed by Ni et al [56] was subjected to thermal cycling in order to address the reliability of this kind of materials.

4.1 Sample description

The interfaces studied for thermal reliability consist of two parts: a Si substrate with a CVD grown CNT array on top and a Cu superstrate acting as a heat sink with a polymer layer. The whole interface can be seen in Figure 4.1.

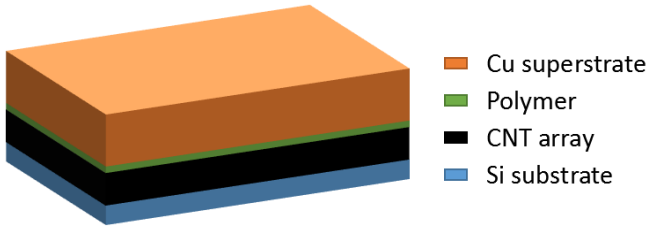

Figure 4.1: Illustration of the CNT array TIMs used for the thermal reliability study.

The CNT array was synthesised on 10x10 mm^2 Si chips with 280 μm thickness. The catalyst was prepared by PVD evaporation by depositing a 10 nm thick Al_2O_3 layer acting as a diffusion layer and a 1 nm thick Fe layer serving as the catalyst. By exposing the growth substrates to a mixture of H_2- and C_2H_2-gases at 700°C for 20 seconds, a CNT array of 15 μm could be obtained.

The Cu superstrate was a 2 mm thick 10x10 mm^2 block with a PVD evaporated Au finish. Even layers of the polymeric functionalization material could be obtained on the superstrate block by spin coating.

The interface closing process is similar to the one reported in [15]. Briefly, the free tips of the CNTs are brought into contact with the polymer layer. Pressure is then applied to the assembly in order to bond the CNT to the polymer thin film. All the samples in this study are closed with the same process in terms of pressure, time and temperature.

4.2 Thermal characterisation and cycling

In order to study the thermal reliability of the CNT based TIM interfaces, the samples were aged using thermal cycling. A cycling standard "condition B" from the JEDEC temperature-cycling standard was used for this purpose at a total of 500 thermal cycles [17]. Thermal measurement of the interfaces was conducted using the flash method as well as the pulsed photothermal reflectance (PPR) method.

Using the laser flash method, the contact resistance between the Si substrate and the Cu superstrate have been measured before the thermal cycling as well as at every 100th cycle to evaluate the aging trend of the interfaces. The contact resistance in this case refers to Equation 1.3 where the thermal interface resistance R_{TIM} includes both the effective bulk thermal conductivity κ_{CNT} as well as the two thermal boundary resistances R_{C1} and R_{C2} positioned on either side of the CNT array according to Figure 3.9. Here R_{CNT} is calculated by dividing the bond line thickness (BLT) with κ_{CNT}. R_{C1} denotes the thermal boundary contribution originating from the CNT – Fe catalyst – Si substrate contact and R_{C2} originating from the CNT – polymer – Cu superstrate contact.

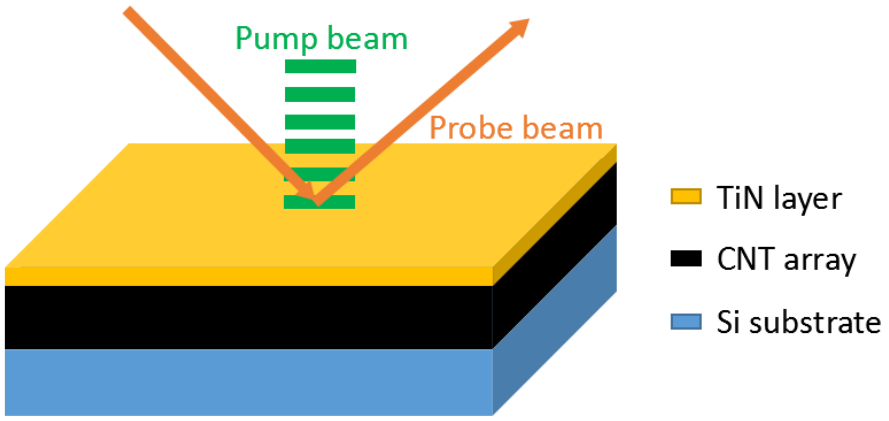

Figure 4.2: Schematic illustration of the three-layer PPR measurement.

The PPR method was used in order to further scrutinise the thermal resistance contributions in the CNT array TIM. A schematic diagram of the PPR experiment can be found in Figure 4.2. In order to prepare samples for the PPR measurement CNT arrays grown on Si were coated with a 300 nm thick layer of TiN using reactive sputtering as seen in Figure 4.3.

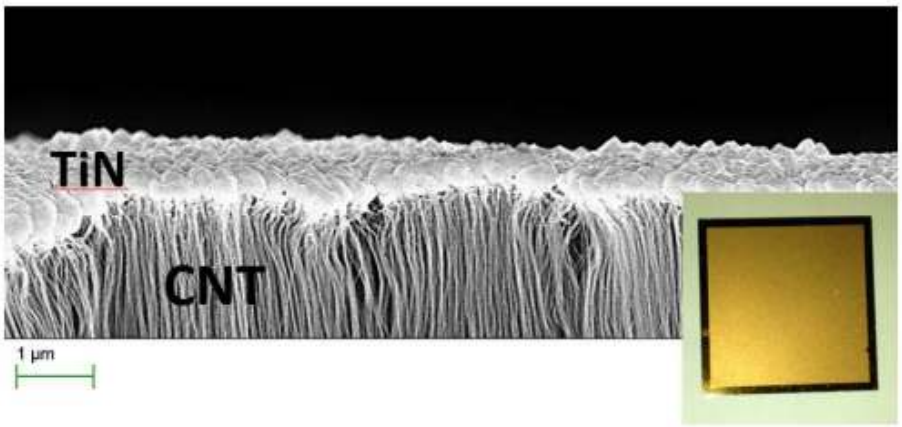

Figure 4.3: SEM image of the TiN covered CNT array after deposition.

Through this method, the thermal conductivity of samples with up to three layers and the thermal boundary resistances between each of them could be obtained. Here, the sample surface is heated using a Nd:YAG laser pulse as a pump beam that causes a transient thermal response in the surface of the TiN layer. The surface temperature could simultaneously be monitored using a He Ne laser as a probe beam focused in the centre of the pump beam. The heat conduction problem in the multi-layer sample can be modelled as a one-dimensional heat conduction. In order to extract the thermal properties and thermal boundary resistance between the layers of the sample the model was used to fit with the experimental surface temperature profile. The PPR method is explained in detail in references [19-21]. In this case, the conductivity κ_{CNT} of the CNT array as well as the thermal boundary resistance R_{C1} is of interest as a complement to the results from the laser flash measurements.

4.3 Results

Laser flash measurements were conducted in order to obtain the thermal interface resistance before cycling as a starting point. The results from the measurement taken at different temperatures are presented in Figure 4.5 together with the error between samples. As seen, the fabricated CNT array TIMs have an average R_{TIM} of 1.7 $mm^2K/W \pm 0.28$ at 20°C.

Identical CNT arrays to the ones used in the CNT based TIM samples were investigated using a PPR setup in order to find the effective thermal conductivity κ_{CNT} as well as the thermal interface resistance between the CNT array and the silicon substrate R_{C1}. Due to the CNT arrays used to fabricate the investigated TIMs originating from the same batch, we can assume that the quality (κ_{CNT} and R_{C1}) is the same. After fitting parameters to the signal found in Figure 4.4, thermal properties could be obtained. Here an effective thermal conductivity, κ_{CNT}, of 71 W/mK and a thermal boundary resistance, R_{C1}, of 0.96 mm^{2}K/W could be found.

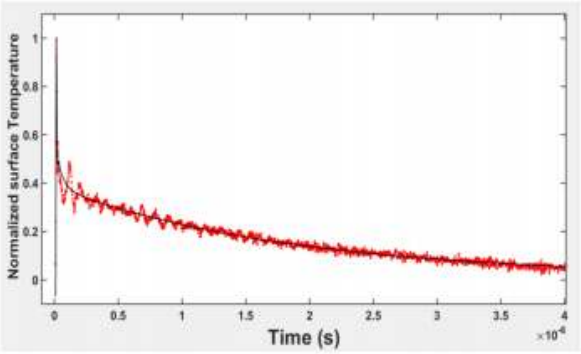

Figure 4.4: Surface temperature to time signal acquired from the PPR measurement of the CNT array.

With the R_{TIM} value obtained from Figure 4.5 together with the κ_{CNT} and R_{C1} result from the PPR measurements, R_{C2} can be calculated using the thermal interface relation stated in Equation 1.3. This relation gives a R_{C2} of 0.49 mm^{2}K/W for the CNT based TIMs. By comparison, this means that the polymer functionalization is about twice as good as the CNT-Si boundary on the other side of the interface in terms of thermal boundary resistance.

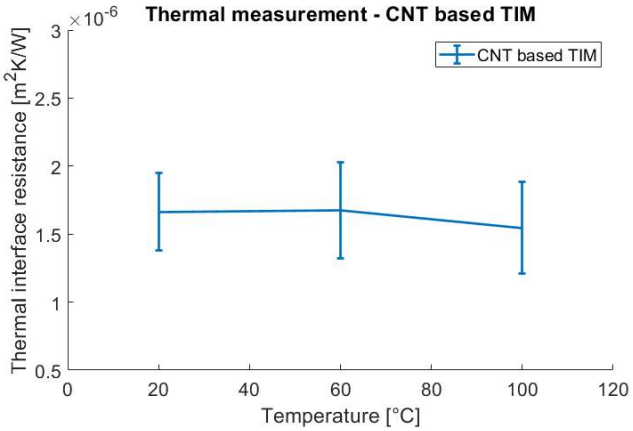

Figure 4.5: Results from the initial laser flash measurement of the CNT based TIM.

The thermal performance of the CNT array TIM samples were monitored using the laser flash method during the thermal cycling by measurement at every 100 cycles. The thermal ageing behaviour is presented in Figure 4.6. As seen, the thermal interface resistance increased by 20 times after the first 100 cycles. This sharp increase is followed by a slower increment between the 100th cycle and the 500th cycle. The final interface resistance of the samples is found to increase by 27 times after the thermal cycling.

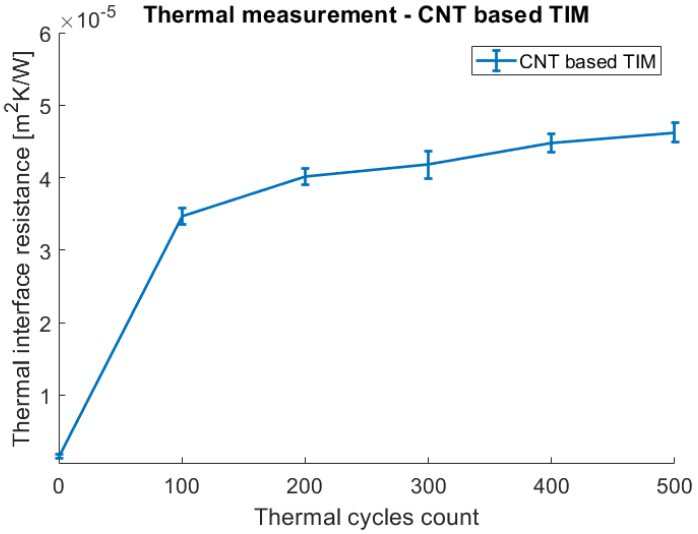

Figure 4.6: Results from the thermal cycling of the CNT based TIM interfaces at 20°C.

In order to investigate the failure mode of the CNT array TIMs, samples that had not been cycled were compared with samples after cycling. These samples were sheared and in all cases the CNT array delaminated from the Si substrate, this was the case as well for the failed samples during cycling. This behaviour could be interpreted as a degradation of the bond strength somewhere in the CNT-Si contact. This bond strength degradation could also explain the increased thermal interface resistance seen for all samples in Figure 4.6.

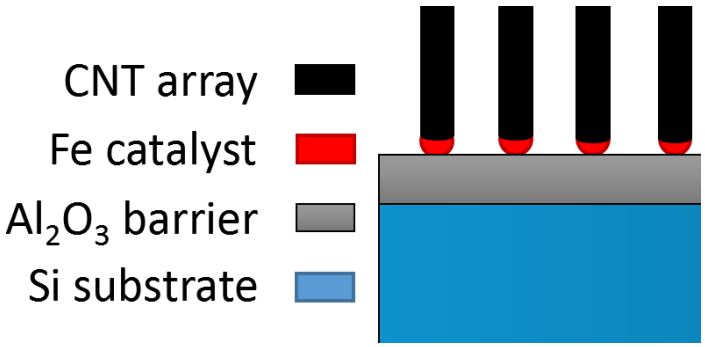

Figure 4.7: Illustration of the CNT-Si contact. The CNT strands in the array are connected to the Fe nanoparticles and the Al_2O_3 layer on top of the Si substrate.

The nature of the deteriorated performance found in the CNT array TIMs was investigated further using XPS. Due to all of the samples delaminating on the CNT-Si side of the interface, the elemental composition of the Cu superstrates of the delaminated interfaces were investigated. As seen in Figure 4.7, the CNT-Si interface is composed of the Si substrate, the Al_2O_3 barrier layer, Fe catalyst nanoparticles as well as the CNT. From the XPS measurements, there was no Al signal present in either of the cases indicating that the failure occurs between the CNTs and the Al2O3 layer. At the same time, the Fe traces in the cycled samples were 70% lower than of those in the samples that were sheared without thermal cycling.

4.4 Conclusions and outlook

The results in this chapter indicated that thermal cycling degrades the CNT/catalyst adhesion considerably. Consequently, this would explain the dramatic increase in thermal interface resistance as well as the degradation of mechanical integrity observed during the thermal cycling. In order to improve CNT array TIMs further additional knowledge regarding the CNT/catalyst interaction is required. One simple solution would be to employ a two-sided functionalization design and thereby sidestepping this issue all together.

Chapter 5

Conclusions and outlook

With CNT array TIMs already been demonstrated to reach thermal interface resistance values below 5 mm^2K/W, which corresponds to commercially available solder based TIMs, our objective was to identify a strategy for the development of better TIMs and to push the technology closer to the market. Here are the main conclusions from this thesis:

The first part provides an analysis and summary of previously published experimental results regarding CNT array TIMs. Three distinct routes for bonding CNT array TIMs were identified: dry contact, metal bonding and organic bonding. With the major part of thermal transport through CNTs being of a phononic nature it was implied that organic functionalization methods would provide optimal conditions for reducing the thermal interface resistance. Therefore, the main effort was focused on surveying the different types of organic functionalization methods outlined in literature. Furthermore, it was found that literature lacks reliability studies regarding CNT based TIMs.

The second part of this thesis deals with the development and characterisation of a new CNT array based TIM. CNT arrays were covalently anchored with epoxy chemistry using a monolayer of silane molecules. This strategy was designed to reduce the dampening effect of the organic phase to a minimum and to promote the chemical bonding effect as much as possible. A fabrication approach was developed together with characterisation methods of each step. With the results showing modest results in comparison with reference values, a few possible improvements were identified in order to refine the samples further. By investigating the requirements regarding pressure and CNT alignment, the thermal interface resistance results from this kind of TIM can be decreased.

A reliability study was conducted in the third part of this thesis where a CNT array TIM based on the HLK5 polymer was tested. With the reliability aspect of CNT array TIMs being largely overlooked in literature, more studies are required before this type of TIM can be useful in thermal management. The HLK5 bonded CNT array TIM samples were subjected to thermal cycling while monitoring the

degradation of thermal resistance over the interfaces. Findings showed that the performance of the interface degraded rapidly in the first segment of the study proving that the TIMs were unable to handle the thermal stress applied to them under thermal cycling. Furthermore, by analysing the failure mode of the samples it was found that the origin of the degradation was located on the CNT/catalyst side of the TIM. This suggests that CNTs on original growth substrates are inappropriate for use in TIM applications without further modification. In order to solve this issue, additional studies on the CNT/catalyst interplay are required.

Better CNT array TIMs will be possible to fabricate in the future by directing the research effort towards the following:

- Customisation of mechanical properties and optimisation of the thermal conductivity λ_{TIM} (from Equation 1.3) would be possible by enabling an improved control of the array fill fraction ϕ (from Equation 1.4).
- A deeper study of the interactions in the CNT/catalyst interface will help us to grow CNT arrays with a customised adhesion to the growth substrate. This could in practice be used either to decrease the thermal boundary resistance R_{C1} (from Equation 1.3) on the growth substrate side or simplify the array transfer by reducing the CNT/catalyst adhesion to a minimum.
- The development of transfer methods that won't affect the orientation of the CNTs in the array will be important in order to achieve transferred double sided CNT array TIMs that still allows the CNTs to connect both sides of the interface.
- The mechanical properties of CNT arrays should be further investigated. Identification of the elongation limit for the arrays will allow customisation of the CNT height in order to avoid delamination due to CTE mismatch over the interface.

Acknowledgments

First I would like to express my gratitude to my supervisor and examiner Johan Liu that has given me the opportunity to work in an interesting field that combines fundamental material research with device applications. I also wish to thank my co-supervisor Yifeng Fu for valuable discussions regarding the work presented in this thesis as well as all the help with improving my writing skills.

I would like to thank my current and former colleagues at the Electronics Materials and Systems Laboratory: Hafid Zehri, Majid Kabiri Samani, Ya Liu, Torbjörn Nilsson, Martí Gutierrez Latorre, Christian Chandra Darmawan, Lilei Ye, Di Jiang, Wei Mu, Shungxi Sun, Si Chen, Yong Zhang, Michael Edwards, Nan Wang, Nikolaos Logothetis, Peng Su and many others for their encouragement and keeping me company during countless of heated lunch arguments. I am particularly grateful for Josef Hansson that always been there to keep me company and to give me a second point of view on work and life in general. The work in this thesis would never have been possible without the help from the all-knowing and cunning staff of the cleanroom facility here in the Microtechnology and Nanoscience department.

By writing this thesis I have gotten the chance to connect my past experiences that have helped me through this work and the people that made it possible. I was introduced to the fundamentals of electronics packaging and assembly processes by working at the SMD assembly line back home together with my siblings Maria and Jens (Christer, you count as well). All fear of practical work was lost working at my in-laws Christin and Thomas workshop which have been useful when repairing equipment as well as fabricating samples in the lab. I would like to thank my mother Barbro for showing me how to live life with determination and to always confront obstacles head on. I would also like to thank my father Olle for introducing me to the world of physics, chemistry and electronics in the first place. This is the gift of a lifetime and it is one that I hope I can pass on myself someday.

Finally, the person whom otherwise none of this would have been possible. Thank you Ida, you mean the world to me!

Andreas Nylander
Göteborg, October 2018

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