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Fabrication and characterization of a 0.14 μm CMOS device using ATHENA and ATLAS simulators

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Abstract. A 0.14 μm CMOS transistor with two levels of interconnection was designed and simulated to investigate its functionality and characteristics. ATHENA and ATLAS simulators were used to simulate the fabrication process and to validate the electrical characteristics, respectively. A scaling factor of 0.93 was applied to a 0.13 μm CMOS. The parameters being scaled are the effective channel length, the density of ion implantation for threshold voltage (V_{th}) adjustment, and the gate oxide thickness. In order to minimize high field effects, the following additional techniques were implemented: shallow trench isolation, sidewall spacer deposition, silicide formation, lightly doped drain implantation, and retrograde well implantation. The results show that drain current (I_D) increases as the levels of interconnection increases. The important parameters for NMOS and PMOS were measured. For NMOS, the gate length (L_g) is 0.133 μm, V_{th} is 0.343138 V, and the gate oxide thickness (T_{ox}) is 3.46138 nm. For PMOS, L_g is 0.133 μm, V_{th} is −0.378108 V, and T_{ox} is 3.46167 nm. These parameters were validated and the device was proven to be operational.

Keywords: gate length, threshold voltage, gate oxide thickness.

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1. Introduction

The size of a CMOS transistor has been shrinking dramatically in less than 40 years time. Transistors with the size of 50 μm in the 1960s have shrunk to less than 0.18 μm in 2000s [1].

In this work, a 0.14 μm CMOS was simulated and studied. The fabrication process was simulated using the ATHENA module from the Silvaco Virtual Wafer Fab (VWF) tools; whereas, the electrical characteristics were validated via the ATLAS module.

The 0.14 μm CMOS was scaled from an existing 0.13 μm CMOS [3]. Constant field scaling with a scaling factor of 0.93 was applied to the following parameters: the effective channel length (L_g), gate oxide thickness (T_{ox}), and threshold voltage (V_{th}) adjustment implantation [5]. As the channel length falls within the submicron regimes, the performance of the device may be susceptible to high field effects. Thus, in order to ensure proper operation, the following techniques have been implemented to minimize high field effects: shallow trench isolation (STI), sidewall spacer deposition, silicide formation, lightly doped drain (LDD) implantation, and retrograde well implantation [5].

2. Simulation process

In order to simplify the simulation process, NMOS and PMOS transistors were fabricated separately. The fabrication processes for both transistors were similar. The main differences lie within the types and density of dopant applied to the substrate.

Initially a *p*-type single crystal silicon (Si) wafer was prepared. Screen oxide was first grown on the

surface of the substrate. With the substrate tilted by 7º and rotating, a high energy implantation was performed to create a *p*- and *n*-wells for NMOS and PMOS, respectively. The objective of growing screen oxide and tilting the substrate was to minimize the channeling effect; whereas the objective of rotating the wafer was to minimize the shadowing effect [1]. Annealing and drive-in was later performed to repair the lattice damage [1].

STI is employed to isolate the neighboring devices. Initially, pad oxide is grown via dry oxidation. Liquid plasma chemical vapor deposition (LPCVD) technique is later applied to deposit silicon nitride Si_3N_4. Pad oxide acts as a strain buffer to avoid cracks in the nitride film; whereas the nitride film acts as a mask for silicon etching [1]. A photoresist is then deposited and pattern is developed using photolithography. The nitride film and pad oxide is etched. The area protected under the Si_3N_4 mask is known as the active region. After stripping the photoresist layer, the substrate was treated by reactive ion etching (RIE) to form trenches. A thin layer of barrier oxide was grown in the trenches so as to block impurities from diffusing into the substrate during chemical vapor deposition (CVD) process. Then tetra-ethyl-oxy-silane (TEOS) CVD process was applied to fill the trenches with oxide. The oxide at the surface of the substrate was removed using chemical-and-mechanical polishing (CMP) technique. STI was completed after annealing was performed and Si_3N_4 mask and pad oxide were etched.

A thin layer of gate oxide was grown via dry oxidation. Then V_{th} adjust implantation was performed; after which the substrate was annealed. Subsequently, a layer of polysilicon was deposited on the substrate. Then the substrate was etched and annealed to form a polysilicon gate. LDD was implanted to suppress hot electron effect in submicron MOSFET [1]. After that, CVD was applied to deposit a layer of Si_3N_4. Then the nitride film was etched to form a sidewall spacer. This was followed by source/drain implantation. Annealing process was performed to activate the dopants. A layer of titanium was deposited on the substrate surface. Rapid thermal annealing (RTA) was employed to form a titanium silicide on the gate. Then the unreacted titanium was etched.

Premetal dielectric (PMD) was formed by depositing a layer of boron phosphor silicate glass (BPSG) on the substrate surface. PMD acts as an insulator for multilevel interconnection [2]. After that the annealing is performed, BPSG is etched to form source/drain contacts. The first level of metallization is formed by depositing and etching aluminum on the contacts. The second level of interconnection can be achieved by depositing another layer of BPSG on the surface. This layer is also known as intermetal dielectric (IMD) [2]. The simulation process is completed when Al is deposited onto the contacts formed by etching IMD. A summary of the parameters used in NMOS and PMOS fabrication is shown in Table 1.

Table 1. Parameters of CMOS fabrication.

Process step	NMOS parameters	PMOS parameters
Silicon substrate	• 7.0×10^{14} cm^{-3} boron • ⟨100⟩ orientation	• 7.0×10^{14} cm^{-3} boron • ⟨100⟩ orientation
Retrograde well implantation	• 0.02 μm screen oxide • 3.75×10^{12} cm^{-3} boron • 100 keV implant energy • 7º tilt • 30 min, 900 ºC annealing • 36 min, 970 ºC drive-in	• 0.02 μm screen oxide • 2.75×10^{11} cm^{-3} boron • 100 keV implant energy • 7º tilt • 100 min, 950 ºC annealing • 46 min, 970 ºC drive-in
STI isolation	• 0.01 μm pad oxide • 0.15 μm Si_3N_4 • 0.50 μm trench depth • 15 min, 900 ºC annealing	• 0.01 μm pad oxide • 0.15 μm Si_3N_4 • 0.50 μm trench depth • 15 min, 900 ºC annealing
Gate oxide	• 0.034 μm gate oxide	• 0.034 μm gate oxide
V_{th} adjust implantation	• 12.45×10^{11} cm^{-3} boron • 5 keV implant energy	• 12.85×10^{11} cm^{-3} boron • 5 keV implant energy
Polygate deposition	• 0.25 μm polysilicon • 26 min, 850 ºC annealing	• 0.25 μm polysilicon • 26 min, 850 ºC annealing
LDD implantation	• 1×10^{13} cm^{-3} phosphorous • 23 keV implant energy • 20 min, 800 ºC drive-in	• 1×10^{13} cm^{-3} boron • 5 keV implant energy • 0.15 min, 850 ºC drive-in
Sidewall spacer deposition	• 0.12 μm Si_3N_4	• 0.12 μm Si_3N_4
Source/drain implantation	• 1×10^{15} cm^{-3} arsenic • 2×10^{13} cm^{-3} phosphorous • 25 keV implant energy • 55 min, 800, 850, 900 ºC annealing	• 5×10^{13} cm^{-3} boron • 10 keV implant energy • 45 min, 800 ºC annealing
Silicide formation	• 0.12 μm titanium • 0.02 min, 1100 ºC RTA • 0.1 min, 910 ºC annealing	• 0.12 μm titanium • 0.02 min, 1100 ºC RTA • 0.1 min, 910 ºC annealing
PMD deposition	• 0.30 μm BPSG • 20 min, 850 ºC annealing	• 0.30 μm BPSG • 20 min, 850 ºC annealing
Metal 1	• 0.10 μm Al	• 0.10 μm Al
IMD deposition	• 0.30 μm BPSG • 15 min, 950 ºC annealing	• 0.30 μm BPSG • 15 min, 950 ºC annealing
Metal 2	• 0.30 μm Al	• 0.30 μm Al

3. Simulation results and discussions

Fig. 1a and b shows the complete cross-sections of NMOS and PMOS, respectively. As clearly shown from the dopant density distributions, a high-energy well implantation has resulted in the highest dopant density concentrated at a certain depth below the substrate surface. As compared to conventional well implantation, in which the highest dopant density lies at the surface of the substrate, such retrograde wells are effective in minimizing punch through. With STI isolation technique implemented in this simulation design, the bird's beak effect, which is a commonly found problem in local oxidation of silicon (LOCOS) technique, has been successfully eliminated.

Two sidewall spacers deposited at the polysilicon gate allows LDD implantation to be performed. As can be seen in Figs 1a and b, the lightly doped phosphorous (for NMOS) and boron (for PMOS) right beneath the spacers allow a reduction in the doping gradient between drain/source and the channel. This, in turn, lowers the electric field at the channel in the vicinity of the drain.

A layer of titanium silicide is formed at the surface of the polygate. The layer of silicide, which has much lower resistivity than polysilicon is necessary to reduce power consumptions and RC time delay for submicron MOSFET local interconnection.

Some of the important parameters such as V_{th}, T_{ox}, and L_g are measured and extracted from the ATLAS module. In order to validate the results, these parameters are compared with the standard parameters published by international technology roadmap for semiconductor (ITRS) and Berkeley predictive technology model (BPTM) [4]. Since only the standard parameters for 70 nm, 0.10 µm, 0.13 µm, and 0.18 µm CMOS can be found as published, the polynomial regression technique (using MATLAB tools) has been applied to achieve the required parameters for a 0.14 µm CMOS. Table 2 shows a comparison between the parameters derived from ATLAS and the standard ones obtained using the polynomial regression. All the simulated parameters for V_{th}, T_{ox}, and L_g lie within the tolerance range of the parameters obtained through regression technique. Hence, it can be concluded that the results obtained from the simulation process are valid.

The I_D-V_D and I_D-V_g electrical characteristic curves are plotted using ATLAS simulator. Figs 2a and b show the NMOS I_D-V_D relationships before and after metallization 2 is performed; whereas, Figs 3a and b show the NMOS I_D-V_g relationships before and after metallization 2. Similarly, the I_D-V_D relationships for PMOS are shown in Figs 4a and b, respectively; whereas, PMOS I_D-V_g relationships are shown in Figs 5a and b, respectively. A comparison between before and after second level interconnection is made. The results are summarized in Tables 3 to 6.

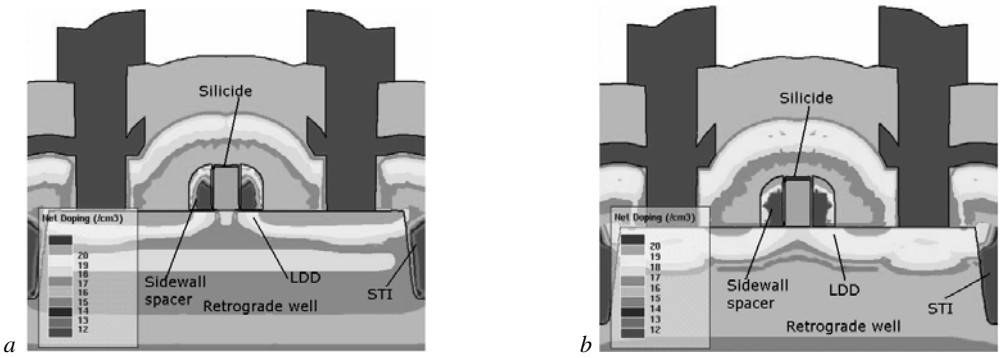

Fig. 1. 0.14 µm NMOS (a), PMOS (b).

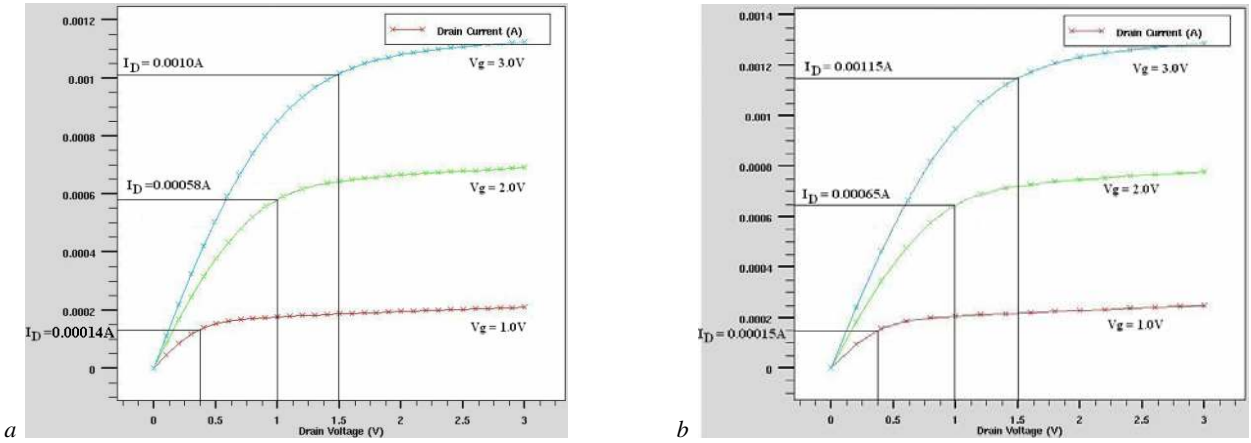

Fig. 2. NMOS I_D-V_D relationship before (a) and after (b) metallization 2.

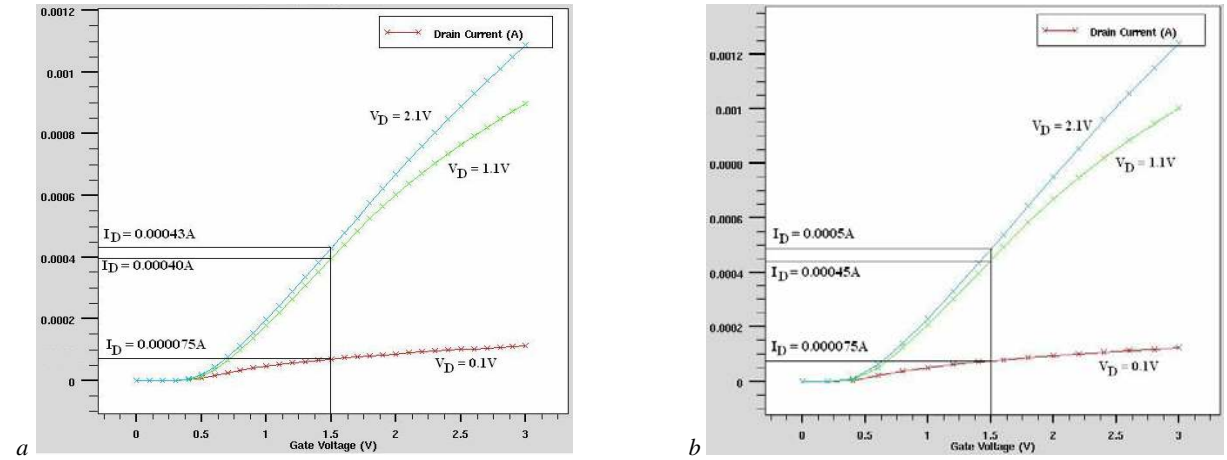

Fig. 3. NMOS I_D-V_g relationship before (a) and after (b) metallization 2.

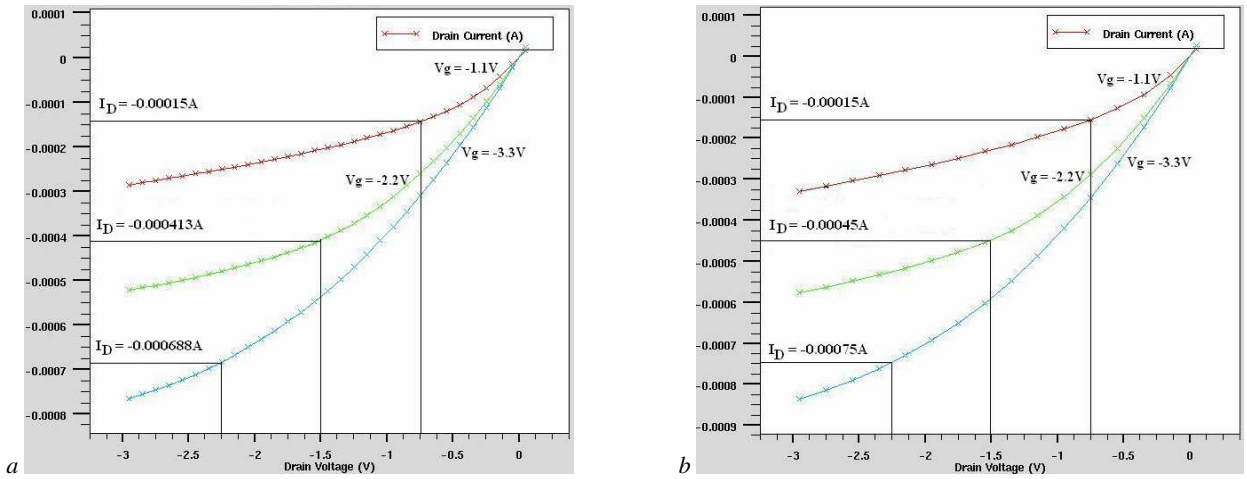

Fig. 4. PMOS I_D-V_D relationship before (a) and after (b) metallization 2.

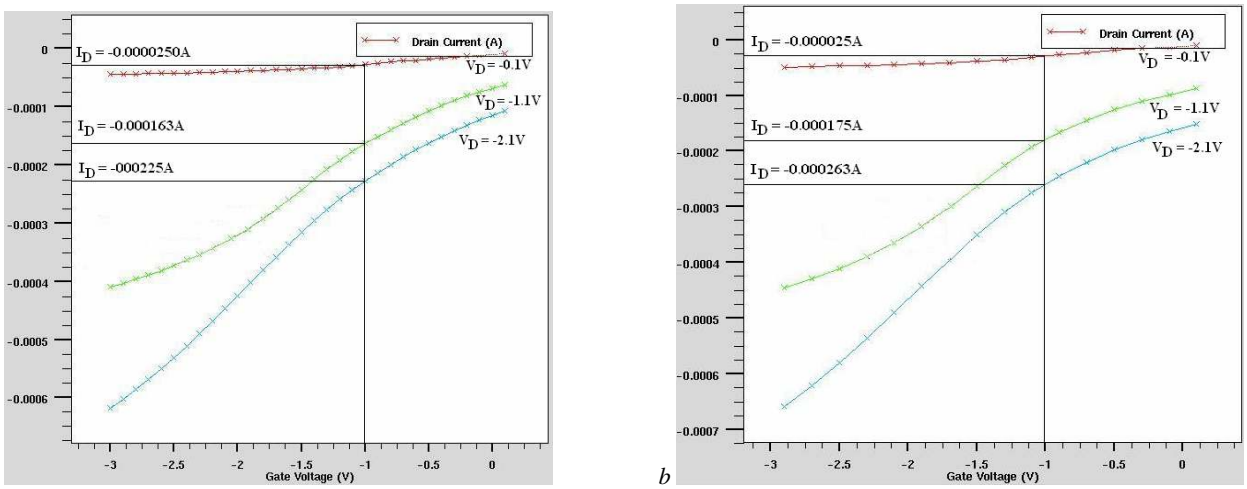

Fig. 5. PMOS I_D-V_g relationship before (a) and after (b) metallization 2.

It can be observed that for both NMOS and PMOS the I_D-V_D and I_D-V_g relationships still retain after the second layer of metallization. This shows that the level of interconnection does not affect the electrical characteristics of the device. However, as the level of interconnection increases, the drain current (I_D) increases. Since the power consumption is directly proportional to I_D, an increase in the level of interconnection will give rise to power consumption.

Table 2. Comparison between simulated results and standard parameters for a 0.14 μm submicron CMOS.

CMOS	Parameters	ATLAS results	Standard parameters
NMOS	V_{th}	0.343138 V	0.3424 ± 12.7% V
	T_{ox}	3.46138 nm	3.2158 ± 4% nm
	L_g	0.133 μm	0.14 ± 15% μm
PMOS	V_{th}	–0.378108 V	–0.3702 ± 12.7% V
	T_{ox}	3.46167 nm	3.2158 ± 4% nm
	L_g	0.133 μm	0.14 ± 15% μm

Table 3. Comparison of I_D before and after metallization 2 in I_D-V_D NMOS graph.

V_g, V	V_D, V	I_D before level 2 interconnection, A	I_D after level 2 interconnection, A	Rate of increase in I_D, %
1.0	0.375	0.00014	0.00015	7.14
2.0	1.0	0.00058	0.00065	12.07
3.0	1.5	0.00100	0.00115	15.00

Table 4. Comparison of I_D before and after metallization 2 in I_D-V_g NMOS graph.

V_g, V	V_D, V	I_D before level 2 interconnection, A	I_D after level 2 Interconnection, A	Rate of increase in I_D, %
1.5	0.1	0.000075	0.000075	0
1.5	1.1	0.000400	0.000450	12.50
1.5	2.1	0.000430	0.000500	16.28

Table 5. Comparison of I_D before and after metallization 2 in I_D-V_D PMOS graph.

V_g, V	V_D, V	I_D before level 2 interconnection, A	I_D after level 2 interconnection, A	Rate of increase in I_D, %
–1.1	–0.75	–0.000150	–0.000150	0
–2.2	–1.5	–0.000413	–0.000450	8.96
–3.3	–2.25	–0.000688	–0.000750	9.01

Table 6. Comparison of I_D before and after metallization 2 in I_D-V_g PMOS graph.

V_g, V	V_D, V	I_D before level 2 interconnection, A	I_D after level 2 interconnection, A	Rate of increase in I_D, %
–1.0	–0.1	–0.000025	–0.000025	0
–1.0	–1.1	–0.000163	–0.000175	7.36
1.0	–2.1	–0.000225	–0.000263	16.89

4. Conclusion

With the implement of retrograde well implantation, STI, sidewall spacer deposition, silicide formation, and LDD implantation to help to minimize high field effects, the design of a 0.14 μm submicron CMOS has been successfully simulated and validated. The results show that power consumption tends to increase after the second metallization was performed.

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