Fabrication and characterization of room temperature silicon single electron memory

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A single electron memory was demonstrated in crystalline silicon that has a transistor channel width of ~10 nm and a nanoscale floating gate of dimension ~(7 nm × 7 nm × 2 nm), patterned by electron beam lithography, lift-off, and reactive ion etching. Quantized shift in the threshold voltage and self-limited charging process have been observed at room temperature. Analysis has shown that these quantized characteristics are the results of single electron charging effect in the nanoscale floating gate. © *1997 American Vacuum Society.* [S0734-211X(97)04906-8]

I. INTRODUCTION

The ultimate limit in scaling down the floating gate memory is a single-electron memory, where one bit of information is represented by only one electron on the floating gate. Previously, single electron memory effect had been observed in a polysilicon thin film transistor at room temperature,[1] in which an electron percolation path in a polysilicon strip formed a channel and one of the polysilicon grains near the conduction path acted as a floating gate. However, such a structure intrinsically has large variations, and prevents precise control of the device feature sizes. Recently, we have demonstrated a single electron memory in crystalline silicon, and have obtained quantized characteristics at room temperature.[2] In this article, we will give a detailed account of the device fabrication using silicon-on-insulator (SOI), and discuss a model to understand the device characteristics which is due to the single electron effect.

II. STRUCTURE OF SINGLE ELECTRON MOS MEMORY

The structure of the single electron metal oxide semiconductor (MOS) memory (SEMM) is shown in Fig. 1. It is a narrow channel MOS transistor with a nanoscale floating gate. The channel width is smaller than the Debye screen length, so that a single electron in the floating gate is sufficient to screen the entire channel from the potential on the floating gate, leading to a significant threshold voltage shift. The floating gate is a nanoscale dot, such that the charging energy and the quantization energy combined is greater than $k_B T$, leading to quantized characteristics at room temperature.

III. FABRICATION OF SEMM

In fabrication, we started with a separation-by-implanted-oxygen (SIMOX) wafer that has a top silicon layer thinned to 35 nm. A native oxide of ~1 nm on top of silicon was used as the tunnel oxide. Then an 11-nm-thick polysilicon film for the floating gate was deposited by low pressure chemical vapor deposition (LPCVD) [Fig. 2(A)]. The width of the channel and the floating gate were patterned in a self-aligned manner by electron beam lithography (EBL), a lift-off of Cr, and a chlorine based reactive ion etching (RIE) [Fig. 2(B)]. The channel width before oxidation varies from 25 to 120 nm. The length of the floating gate was patterned by a second level EBL, Cr lift-off, and RIE, making it a square shape [Fig. 2(C)]. The native oxide acted as an etch-stop layer for the RIE. After this, an 18-nm-thick oxide was thermally grown, which partially consumed silicon and reduced the thickness of the polysilicon dot by ~9 nm and the lateral size of the dot as well as the silicon channel width by ~18 nm. Then a 22-nm-thick oxide was deposited using plasma enhanced chemical vapor deposition (PECVD), making the total control-gate-oxide thickness of 40 nm. Next, polysilicon was deposited by LPCVD and the control gate was patterned in 3 μm length that covers the floating gate and part of the narrow channel [Fig. 2(D)]. After a self-aligned source/drain ion implantation, the final contacts were made, and the devices were sintered in a hydrogen and nitrogen forming gas to reduce the interface states. Some fabrication procedures described here are similar to our previous works.[3,4]

The scanning electron micrograph (Fig. 3) shows a 28-nm-diameter polysilicon dot defined on top of a 28-nm-wide silicon channel before they were reduced by oxidation. For easy alignment in the second level EBL, a line was exposed instead of a small square. The line was etched in the buried oxide, and does not affect the electrical characteristics of the device.

IV. DEVICE CHARACTERIZATION

The devices were characterized at room temperature in a two-step process. In the first step, the floating gate was charged by applying a positive voltage pulse (with respect to the grounded source) to the control gate. Next the drain current versus gate voltage was measured by using semiconductor parameter analyzer (HP4145B). The threshold voltage shift (ΔV_{th}) can then be extracted from the series of current–

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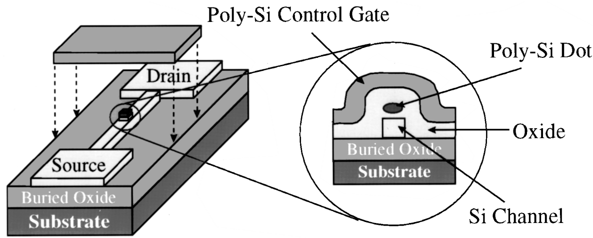

FIG. 1. Schematic of a single-electron MOS memory that has a narrow silicon channel and a nanoscale polysilicon dot as the floating gate. The cross section view details the floating gate and the channel region.

voltage ($I-V$) curves. The switching between the two steps was completed within 1 s, which is short compared to the charge retention time on the floating gate.

A SEMM that has a ~10-nm-wide channel and a floating gate of a ~7 nm × 7 nm square and 2 nm thick—the smallest in our fabrication—was characterized under different charging voltages. The device dimension was estimated from scanning electron microscopy (SEM) measurement and the

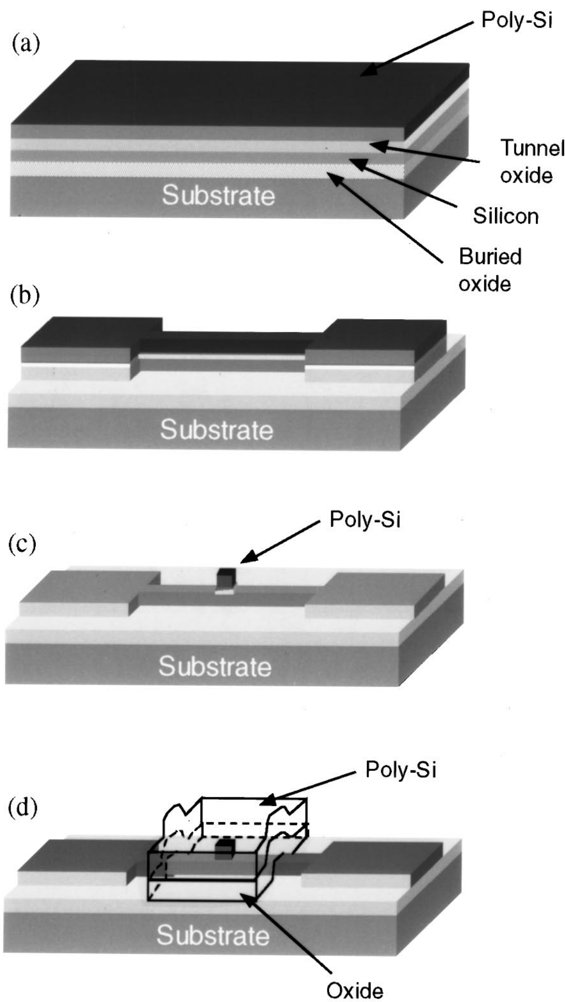

FIG. 2. Fabrication procedures for the nanoscale floating gate memory. (a) Starting multiple films on SIMOX wafer. (b) First level EBL and RIE define the transistor channel. (c) Second level EBL and RIE define the polysilicon dot. (d) Formation of control oxide and control gate.

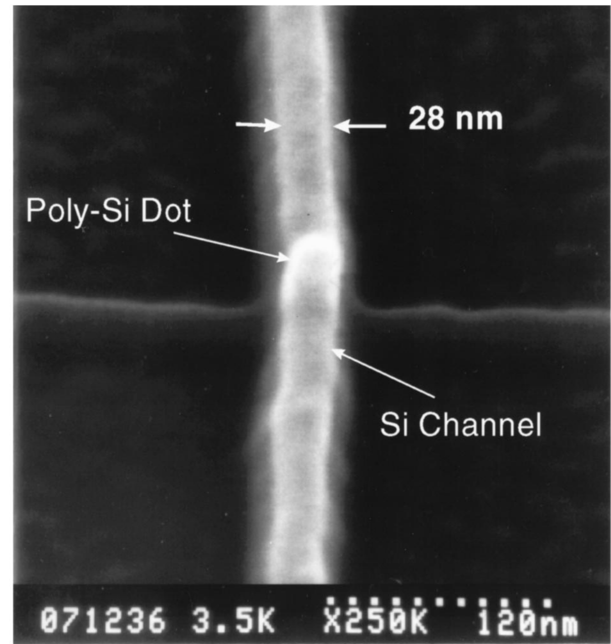

FIG. 3. Scanning electron micrograph of the narrow silicon channel and the polysilicon dot on top, before size reduction by thermal oxidation. The width of the channel and the size of the dot are both 28 nm.

oxidation rate. However, self-limiting oxidation might occur,[5] making it difficult to assess the exact size.

Figure 4 shows the $I-V$ characteristics of the device after the control gate was pulsed by a charging voltage from 2 to 14 V. Although the charging voltage was varied continuously, the threshold voltage of the device (defined as the gate voltage at which the drain current reaches 100 pA) always

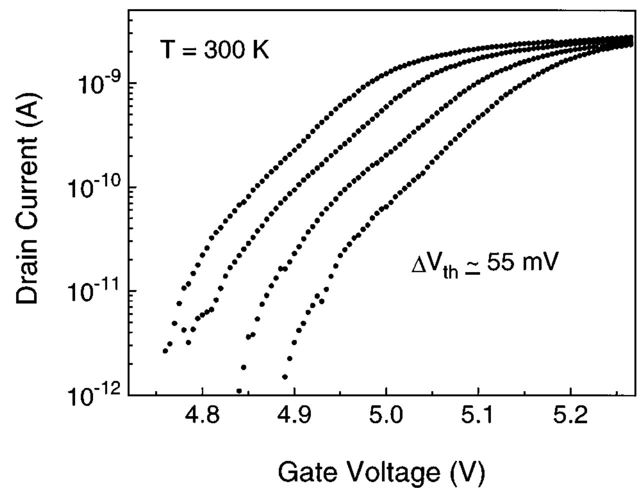

FIG. 4. Room temperature $I-V$ characteristics of a single elelctron memory device before and after the charges being stored in the floating dot. For a charging voltage pulse from 2 to 14 V, the threshold voltage shift is quantized with an increment of ~55 mV.

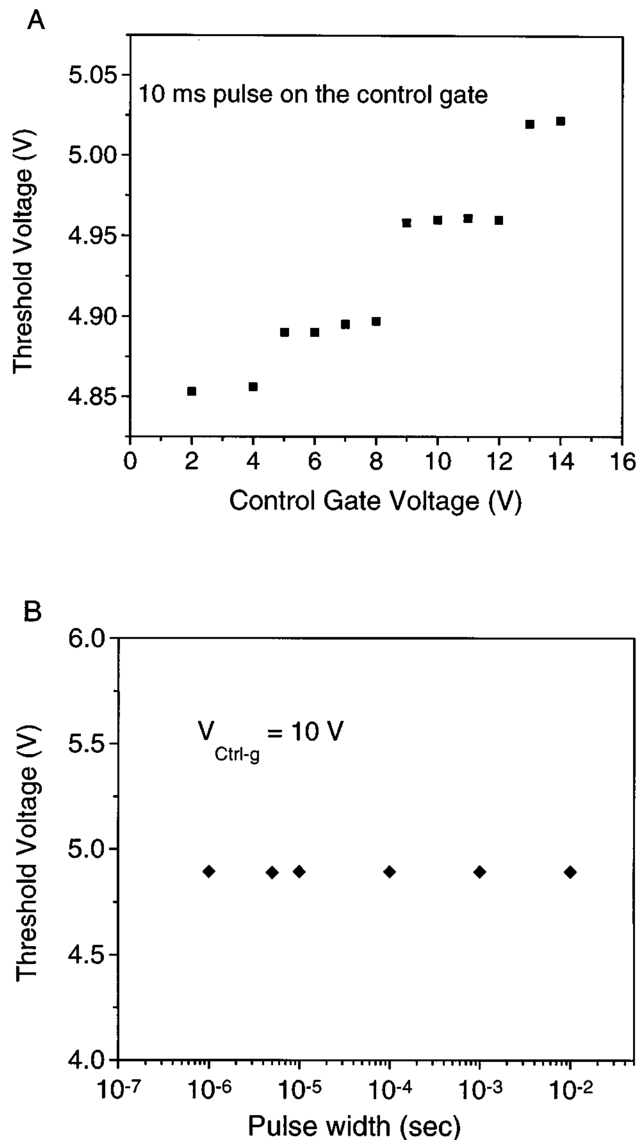

FIG. 5. Threshold voltage of the device as a function of (A) the charging voltage on the control gate, showing a staircase relation with an interval of ~4 V; and (B) as a function of the charging time while the charging voltage pulse is fixed at 10 V, indicating a self-limited process.

takes a discrete shift with an increment of 55 mV. For each discrete threshold shift, a 4 V charging voltage on the control gate is required. It is shown more clearly in the threshold voltage versus charging voltage plot [Fig. 5(A)], where a staircase relation between the threshold voltage shift and the charging gate voltage is seen. Moreover, for a given charging voltage, the threshold voltage shift is independent of the time it takes to charge the floating gate [Fig. 5(B)], indicating that the charging process is self-limited. Because the tunnel oxide is extremely thin, the charge stored at the floating gate could be held for ~5 s after the control gate is set back to zero potential.

For comparison, we have also fabricated devices that have no floating gate on top of the channel. These devices did not exhibit any memory effect regardless of what voltage pulse is applied to the control gate. This observation indicates, as expected, that it is the electrons stored inside the floating gate that causes the memory effect.

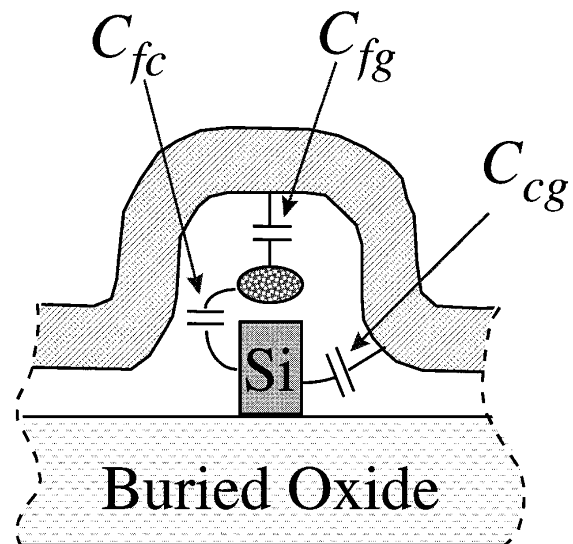

FIG. 6. Schematic cross section of SEMM showing the capacitive coupling between the various elements.

V. ANALYSIS

The behavior of the device can be explained by the single-electron charging effect. First, the voltage required for charging a single electron into the floating gate can be calculated from the fact that the charging voltage primarily drops between the control gate and the floating gate because of the use of very thin tunnel oxide between the channel and the floating gate. To add one electron to the floating gate requires a voltage increment of $e/C_{\rm fg}$ to be applied to the control gate, where $C_{\rm fg}$ is the capacitance between the floating gate and the control gate (Fig. 6). The capacitance $C_{\rm fg}$ for the 7 nm × 7 nm floating gate and a 40 nm control oxide is about 4.4×10^{-20} F, resulting in a single electron charging voltage of 3.6 V, close to the experimental value of 4 V.

The discrete shift in threshold voltage ($\Delta V_{\rm th}$) due to a single electron stored in the floating gate can be calculated using the following model. The charge induced in the channel (directly under the floating gate) is determined by both the floating gate voltage (V_F) and the control gate voltage (V_G), because the control gate partially wraps around the channel. The induced channel charge under the floating gate can be approximated as

$$Q_{\rm ch}=C_{fc}V_F+C_{cg}V_G, \quad (1)$$

where C_{fc} is the mutual capacitance between the floating gate and the channel, and C_{cg} is the mutual capacitance between the channel and the control gate (Fig. 6). The floating gate potential can be related to the floating gate charge (Q_F) and the control gate voltage as

$$V_F=\frac{Q_F}{C_\Sigma}+\frac{C_{\rm fg}}{C_\Sigma}V_G. \quad (2)$$

Here $C_\Sigma = C_{fc} + C_{\rm fg}$. Putting Eq. (2) into Eq. (1) yields an expression for the channel charge:

$$Q_{\rm ch} = \frac{C_{fc}}{C_\Sigma} Q_F + \left(C_{cg} + \frac{C_{fc}}{C_\Sigma} C_{\rm fg} \right) V_G . \tag{3}$$

When one more electron is added to the floating gate (i.e., $\Delta Q_F = e$), to maintain the same channel charge $Q_{\rm ch}$, Eq. (3) requires the threshold voltage to increase by

$$\Delta V_{\rm th} = \frac{e}{C_{\rm fg} + (C_\Sigma / C_{fc}) C_{cg}} . \tag{4}$$

Because the poly-Si dot is very close to the silicon channel, but far away from the control gate, we can take $C_\Sigma \approx C_{fc}$. So the threshold shift due to the addition of a single electron to the floating gate can be evaluated as

$$\Delta V_{\rm th} = \frac{e}{C_{\rm fg} + C_{cg}} . \tag{5}$$

In a conventional floating gate memory $C_{cg} = 0$, and the threshold shift is simply $\Delta V_{\rm th} = e / C_{\rm fg}$. But in our case, the threshold shift is reduced because the charge in the floating gate can only partially screen the gate potential. The channel-to-control gate capacitance (C_{cg}) can be estimated in the following way. The channel length that can be controlled by a charge on the floating gate is roughly equal to the Debye screen length, which is ~70 nm for the given channel doping at room temperature. The channel thickness for the device is ~26 nm. For the control oxide thickness of 40 nm and the area of 70 nm × 26 nm × 2, C_{cg} is about 2.5×10^{-18} F($\gg C_{\rm fg}$), and hence $\Delta V_{\rm th} \approx 64$ mV, which is again consistent with the experimental value.

VI. SUMMARY

We have fabricated the first single-electron memory in crystalline silicon MOS field effect transistor (MOSFET), with both the silicon channel and the nanoscale polysilicon floating gate defined by e-beam lithography. We have obtained quantized characteristics at room temperature. Analysis has shown that both the discrete shift in threshold voltage and the self-limited charging process can be explained by the single electron effect. The work presented here is a major step forward in taking advantage of single electron effects to build ultrasmall and ultrahigh density transistor memories.

ACKNOWLEDGMENTS

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