Fabrication and Characterization of Vertically Stacked Gate-All-Around Si Nanowire FET Arrays

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***Abstract*— We describe the fabrication of vertically stacked Silicon Nanowire Field Effect Transistors (SiNW FETs) in Gate-All Around (GAA) configuration. Stacks with the number of channels ranging from 1 to 12 have been successfully produced by means of a micrometer scale lithography and conventional fabrication techniques. It is shown that demonstrator Schottky Barrier (SB) devices fabricated with Cr/NiCr contacts present good subthreshold slope (70mV/dec), I_{ON}/I_{OFF} ratio $\geq 10^4$ and reproducible ambipolar behavior.**

***Index Terms*— nanowire, FET, multichannel, ambipolar, vertical integration**

I. Introduction

Continuing efforts in Complementary-Metal-Oxide-Semiconductor (CMOS) research have lead to the exponential increase of device integration density during the last 40 years. More recently increasing fabrication costs and increasing overall variability have become an obstacle for the scaling trend. In order to overcome such limitations, considerable research is dedicated for instance to the use of new materials (such as high-κ dielectrics with metal gates), dual-gate devices, novel isolation techniques that make use of Silicon-On-Nothing (SON) or Silicon-On-Insulator (SOI) substrates [1]. In particular, dual-gate technology in conjunction with the geometry of the device can enhance the control over the transistor channel. In this sense, further improvements can be achieved with tri-gate, omega-gate or Gate All-Around technologies (GAA) [2].

Recent works explored the vertical stacking of SiNWs as channels for FET devices [3], [4]. The vertically stacked SiNWs represent channels of the same SiNW FET, whose electrostatic control can be enhanced by using a GAA configuration [5]. In addition, SiNW FETs can also be used to build new logic architectures [6], [7] or as ultimate memory architectures for Ultra-Large-Silicon-Integration (ULSI) [8], [9].

In this work we discuss novel and promising fabrication method for vertically-stacked SiNW FETs with different number of channels on bulk Si wafers. The reported method has also been applied to fabricate single channel devices that demonstrate excellent reproducible performance.

II. Related Work

Recently, a multichannel structure with GAA configuration has been proposed as a candidate for high-performance devices. Its implementation has the advantage of enhanced on-current (I_{ON}) along with low leakage as well as a small footprint for multi-finger (multi-channel) devices [10], [4]. The fabrication process described in [10], [4] is based on creating epitaxial layers to alternate Si and SiGe layers one on top of each other. A vertical trench is etched in the grown structure. A successive SiGe selective etching leaves vertically-stacked Si nanowires. Hydrogen annealing is then used to change the SiNW shapes from rectangular to circular, thus yielding channels with less surface roughness and improved controllability.

An alternative approach for the fabrication of vertically-stacked SiNWs [11] is based on producing a scalloped trench in bulk silicon by means of Deep Reactive Ion Etching (DRIE). Sacrificial oxidation steps are performed to reduce the dimensions of the trench. Thanks to scalloping, the Si trench is totally consumed in its thinner parts, leaving a vertical stack of suspended SiNWs. Although the DRIE process defines trenches of micrometer dimensions, the iteration of oxidation steps is capable for reducing the structures to suspended nanowires with of 20 nm in diameter [11]. This approach has also been demonstrated to be suitable for producing vertically stacked SiNW with small dimensions and different section shapes [12], yet it has not been used so far for GAA FET fabrication.

III. Device fabrication

In our work we produce vertical SiNW arrays by means of optical lithography with 1 μm resolution limit. Sub-micrometer features are obtained through sacrificial oxidation steps. Although the integration density would have been further increased by means of advanced lithography, the developed process already allows us to produce very high channel densities without making use of non standard fabrication steps.

We start by defining a photoresist line on a p-type ($N \sim 10^{15}$) silicon bulk wafer (see Fig. 1.a). Then a DRIE technique (also called Bosch process) is performed. This technique, that alternates a plasma etching with a passivation step, has been optimized to produce a scalloped trench in silicon with high reproducibility. Etching time, passivation time and plasma platen power have been optimized in order to enhance the scalloping effect. The application of the DRIE technique gives a trench like the one depicted in Fig. 1.b. The flexibility of the process allows us to change the number of scallops easily. After a wet oxidation step (see Fig. 1.c) vertically stacked SiNWs are formed. Then the cavities produced by the Bosch process are filled with photoresist. After a combination of chemical mechanical polishing (CMP) and BHF dip, the wet oxide is removed around the NWs (see Fig. 1.f). The oxide at the bottom of the cavity is left to isolate the substrate from the successive processes. The vertical structure obtained is then oxidized to produce a high quality dry oxide (20 nm thick, see Fig. 1.g) as gate dielectric. Then between 200 nm and 500 nm of Low Pressure Chemical Vapour Deposition (LPCVD) polysilicon is deposited (Fig. 1.h). The polysilicon gate is patterned by means of a combination of isotropic and anisotropic recipes (see Fig. 1.i). A final field oxide isolation and Al or Cr/NiCr patterning make the external electrical connections.

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A SOI wafer has been used to fabricate demonstrator devices with single channel layer. In this case we patterned Cr/NiCr through a lift-off technique to form source and drain. An advantage for using Ni is that it can easily form silicides with mid-gap workfunctions at low temperature, thus allowing the fabrication of FETs in few process steps and with a low thermal budget [13]. However, the main difference with FETs defined by implantation is the formation of Schottky Barrier (SB) source/drain thus leading to a device with ambipolar characteristic. The ambipolarity refers to the $I_{ds} - V_{gs}$ electrical characteristic of a transistor having both p- and n-type behaviour [13]. A double step annealing (at 200°C and 400°C, respectively) has been choosen to form silicided regions. This annealing process has been seen as good choice in terms of I_{ON}/I_{OFF} ratio improvement [14]. After the annealing steps, the unreacted Cr/NiCr parts were removed in wet etchant. Finally a 1 μm thick layer of Al has been patterned after via opening on the field oxide.

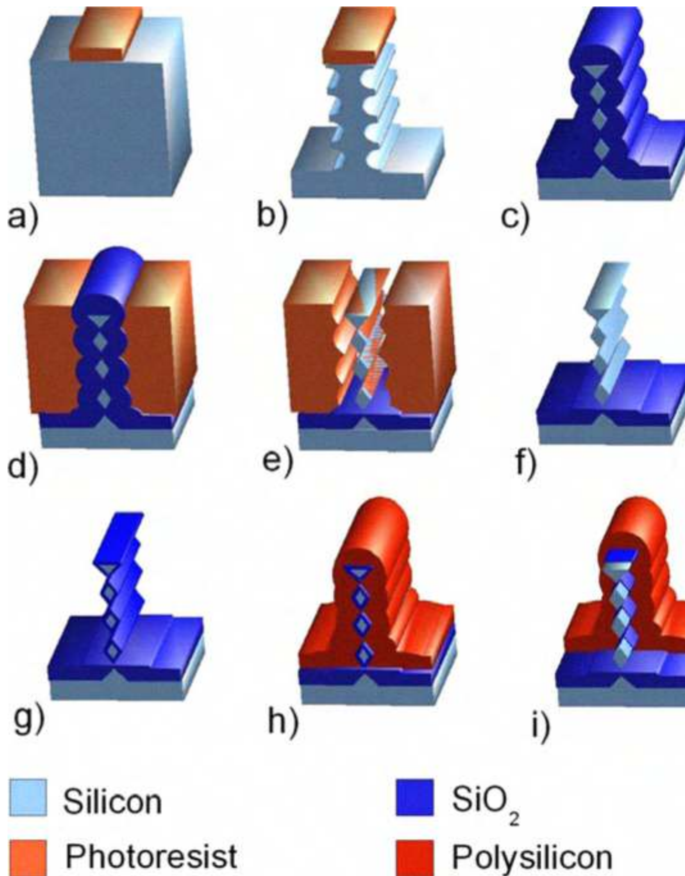

Fig. 1. Process flow of vertically stacked Si-NW FET. a) A photoresist line is defined on the Si wafer. b) A Bosch process is performed to produce a scalloped trench. c) Wet oxidation. d) A 5 μm thick photoresist is spin-coated in order to fill the cavities formed around the trench. e) The oxide removal step free the SiNWs withouth removing the oxide at the bottom of the cave. f) SiNWs are vertically stacked and electrically isolated from the substrate. g) A high quality dry oxide is formed. h) LPCVD polysilicon deposition. i) Gate patterning

IV. Discussion on the fabricated structures

Three dimensional SiNW FET arrays have been fabricated in vertical stacks with the number of channels varying between 1 and 12 (see Fig. 2). Initially, the formed SiNWs have diameters ranging from 70 nm to 200 nm, several techniques can be applied in order to refine the dimensions in a controlled manner. For instance, it has been demonstrated that the use of self-limiting oxidation is capable of producing channels with nanometer dimensions and good controllability [4], [15]. Surface irregularities of the suspended NWs can be improved either by means of a self-limiting oxidation or by hydrogen annealing step [10]. It was found that the proposed fabrication method consistently produces repeatable and very controllable dimensions of clearly separated NW stacks, by optimizing the etch/oxidation conditions. A uniform and thin gate oxide is formed around the suspended NWs by dry oxidation in a horizontal furnace under 10 *slm* O_2 flux. By combining isotropic and anisotropic etch techniques, polysilicon gate lengths down to 200 nm (see Fig. 3.a) were produced using 1 μm lithography. It can be seen that the polysilicon gate completely surrounds the suspended NW segment without any gaps, and that the silicon NW is covered by a 20nm thick gate oxide (Fig. 3.b). The proposed GAA device fabrication technique has also been succesfully applied for NW stacks with 3 suspended channels (Fig. 4). Fig. 4.a shows a structure with two parallel polysilicon gates, and Fig. 4.b shows the cross-section of the structure where individual wires and the surrounding polysilicon gate are clearly visible. Note that the cross-section of each suspended NW (with the exception of the top wire) has a well-defined rhombic shape that is dictated by the successive etching/oxidation steps used to produce the wire stacks. The top wire has a triangular profile that is also defined by the process. Schottky-barrier (SB) SiNW FETs demonstrator devices in GAA configuration have also been fabricated successfully on SOI, and shown in Fig. 5. In this particular example, the suspended NW segment has a trapezoidal cross-section.

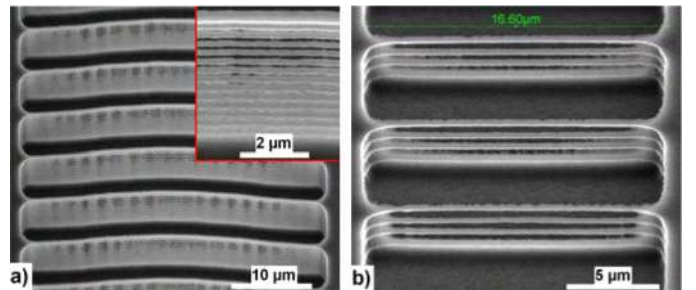

Fig. 2. a) Vertically stacked SiNWs in array configuration after oxide removal. The nanowires are free and sligthly bent due to residual stress. In this sample the number of vertically stacked nanowires amounts to 12. b) Another array with 3 vertically stacked SiNW channels.

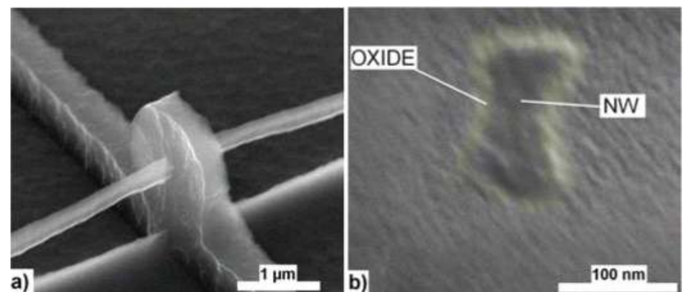

Fig. 3. a) Single nanowire surrounded by 500 nm thick polysilicon gate; $L_g \sim 200$ nm. b) Gate stack cross-section showing the Si core surrounded by 20 nm gate oxide and polysilicon.

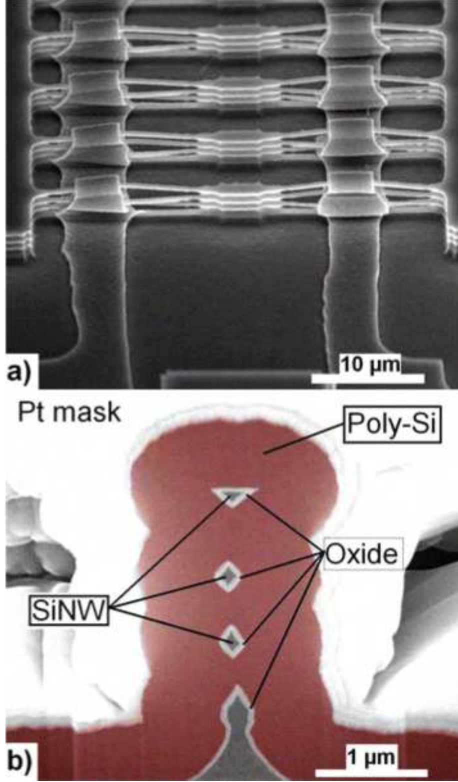

Fig. 4. a) Long nanowire channels with two parallel gate construction. b) Gate stack crossection showing three SiNW channels.

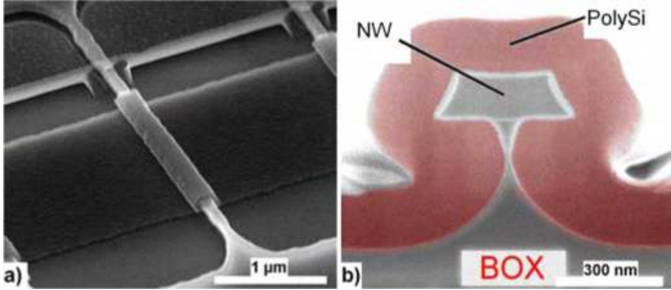

Fig. 5. a) Single GAA-NW device with polysilicon gate. b) Gate stack cross-section and highlight on different stack materials.

V. Electrical Measurements

The measured electrical performance of two SB SiNW FET devices with single SiNW channel in the stack are reported in the following. Each NW channel have $5\,\mu m$ gate length and an effective width of $930\,nm$. Since the NW cross-section is trapezoidal, the effective channel width is the perimeter of the NW. The devices (see Fig. 6) show an ambipolar behaviour with good performance of both p- and n- branches. Table I reports the device (device A) parameters demonstrating device ambipolarity, $I_{\mathrm{ON}}/I_{\mathrm{OFF}}$ ratio $\geq 10^4$ and a subthreshold slope (SS) lower than 70 mV/dec for the p-type portion of the curves ($V_{\mathrm{gs}} > V_{\mathrm{th}}^{\mathrm{h}^+}$ for h^+), and around 250 mV/dec for the n-type part ($V_{\mathrm{gs}} < V_{\mathrm{th}}^{\mathrm{e}^-}$ for e^-). The $I_{\mathrm{ds}}-V_{\mathrm{ds}}$ curves have been measured for positive V_{gs} (Fig. 7.a) and negative V_{gs} (Fig. 7.b). The device behavior in the "triode" region indicates very distinct gate control over the drain current. The plots also show a Negative Differential Resistance (NDR) region when the channel is in inversion mode.

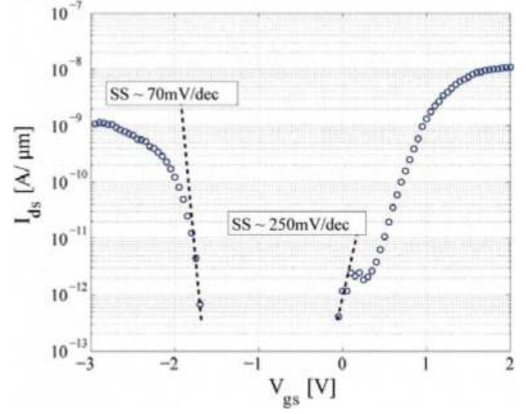

Fig. 6. Device A: $I_{\mathrm{ds}} - V_{\mathrm{gs}}$ curve for $V_{\mathrm{ds}} = 1\,V$. The observed ambipolarity is typical for the metallic source and drain MOSFETs. Note the very high subthreshold slopes in both modes.

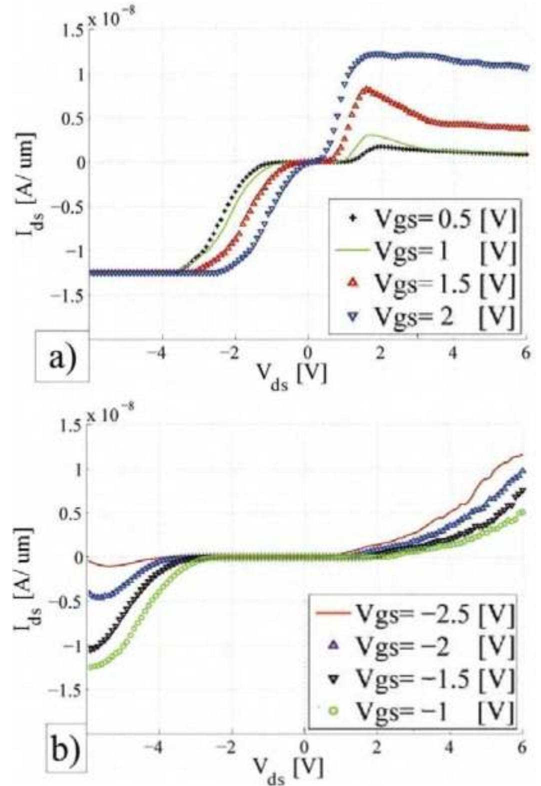

Fig. 7. Device A: $I_{\mathrm{ds}} - V_{\mathrm{ds}}$ curves showing negative differential resistance when the channel is at the inversion: a) for $V_{\mathrm{gs}} \geq 0\,V$ channel in inversion mode for positive V_{ds} and in accumulation mode for negative V_{ds}. b) For $V_{\mathrm{gs}} \leq 0\,V$ the channel is in inversion mode for negative V_{ds} and in accumulation mode when V_{ds} is positive.

TABLE I

Device A: SB SiNW FET parameters.

	$\frac{I_{\mathrm{ON}}}{I_{\mathrm{OFF}}}$	V_{th}^{+} or $V_{th}^{e^-}$ [V]	SS $[\frac{\mathrm{mV}}{\mathrm{dec}}]$	$I_{\mathrm{ON}}^{\mathrm{h}^+}$ $[\frac{\mathrm{nA}}{\mu\mathrm{m}}]$	$I_{\mathrm{ON}}^{\mathrm{e}^-}$ $[\frac{\mathrm{nA}}{\mu\mathrm{m}}]$
h^+	2900	-2	< 70	12.5	-
e^-	31000	1	250	-	2

A partially gated device (source and drain have been designed 1 μm far away from the gated channel) shows ambipolar behaviour (see Fig. 8). The extracted parameters for this device (device B) are reported in Table II. The high V_{gs} required for the onset of conduction is believed to be due to the non controlled portion of the channel. This behaviour is confirmed in [16]. Moreover, in [16] the possibility of making the device unipolar by using a dual gates was discussed as well. A dependency of the I_{OFF} on the applied V_{ds} is found (see Fig. 9).

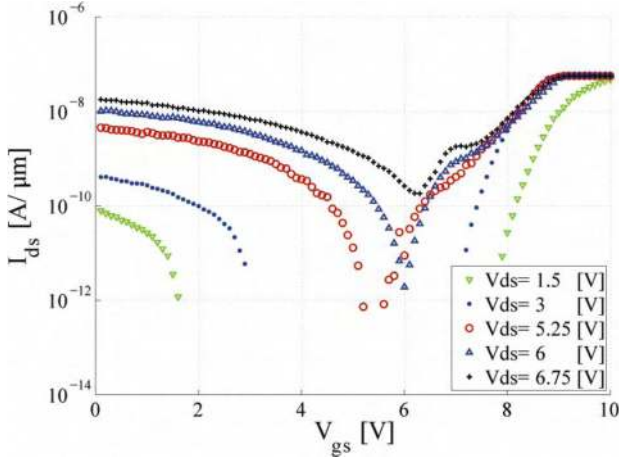

Fig. 8. Device B: $I_{ds}-V_{gs}$ curves for a partially gated device showing ambipolar behaviour and dependence to the applied V_{ds} .

TABLE II
DEVICE B: AMBIPOLAR BEHAVIOUR PARAMETERS FOR POSITIVE GATE VOLTAGES AFTER TWO STEP SILICIDATION ANNEALING.

V_{ds} [V]	I^{h+}_{OFF} $[\frac{pA}{\mu m}]$	I^{e-}_{OFF} $[\frac{pA}{\mu m}]$	$\frac{I_{ON}}{I_{OFF}}$ h^+	$\frac{I_{ON}}{I_{OFF}}$ e^-	SS^{h+} $[\frac{mV}{dec}]$	SS^{e-} $[\frac{mV}{dec}]$
1.5	1	8	300	7500	400	250
3	6	10	333	6000	700	350
5.25	0.7	0.7	10000	85700	200	300
6	2	2	10000	30000	200	200
6.75	200	200	150	300	N/A	N/A

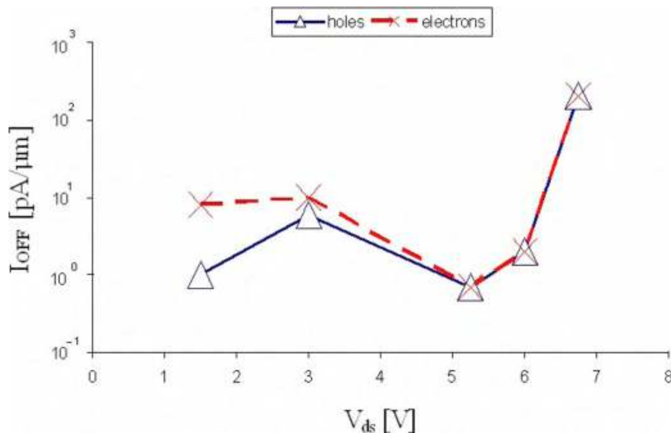

Fig. 9. Device B: I_{OFF} for holes (p-type portion of the $I_{ds}-V_{gs}$ curve) and electrons (n-type portion of the $I_{ds}-V_{gs}$ curve) conduction at different V_{ds}.

VI. CONCLUSIONS

High channel density SiNW GAA FETs have been fabricated by means of a DRIE technique for the first time. The same low cost top-down approach has been succesfully deployed to fabricate vertical SiNW stacks with different number of SiNW channels; i.e. the number of channels composing the vertical stack could be easily tuned from 1 to 12. Moreover, the process can be easily adopted for different substrates (bulk or SOI wafers) without any additional complexity. Finally, SB SiNW devices fabricated with good repeatability show excellent performance (the measured $SS < 70$ mV/dec is close to the optimal value for SiNW devices for room temperature operation) making the approach suitable for further investigations.

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