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Fabrication and current-voltage characterization of a ferroelectric lead zirconate titanate/AlGaN/GaN field effect transistor

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We demonstrated ferroelectric field effect transistors (FFETs) with hysteretic *I-V* characteristics in a modulation-doped field effect transistors (MODFET) AlGaN/GaN platform with ferroelectric $Pb(Zr,Ti)O_3$ between a GaN channel and a gate metal. The pinch-off voltage was about 6–7 V comparable to that of conventional Schottky gate MODFET. Counterclockwise hysteresis appeared in the transfer characteristics with a drain current shift of ~5 mA for zero gate-to-source voltage. This direction is opposite and much more pronounced than the defect induced clockwise hysteresis in conventional devices, which suggests that the key factor contributing to the counterclockwise hysteresis of the FFET is the ferroelectric switching effect of the lead zirconate titanate gate. © *2006 American Institute of Physics*. [DOI: 10.1063/1.2187956]

There has been an increased interest in ferroelectric field effect transistors (FFET) for memory cell applications lately because of their potential advantages over conventional FETs such as nonvolatile memory functionality, even after a power failure, and nondestructive readout properties The general idea of FFET transistors in which ferroelectric material is used as a gate insulator [liberally used terminology to describe where the lead zirconate titanate (PZT) layer is situated] is not a new one as such a transistor was proposed a half century ago by several independent investigators, Looney *et al.*[1] Since then a number of reports have appeared in the literature.[2–10] This letter, however, uniquely utilizes a GaN platform with such desirable properties as high temperature operation and radiation hardness.

The most widely used memory cell structure utilizing ferroelectrics is the 1 transistor/1 capacitor-type cell (1T/1C), in which a ferroelectric capacitor is combined with a metal oxide semiconductor field effect transistor (MOSFET).[11,12] On the other hand, in the metal ferroelectric semiconductor field effect transistor (MFSFET)-type cells, the ferroelectric capacitor is replaced by the gate ferroelectric capacitor of the FFET device.[13] Because the latter cell structure has such unique features as a single transistor (1T) cell, nonvolatile data storage and nondestructive data readout, it could pave the way for high-density integration of nonvolatile ferroelectric random access memory (FRAM). Owing to its relatively fast read-write capability, it would also potentially offer an alternative to somewhat slow flash memory cells as well. For its realization, however, obstacles to obtaining the high-quality ferroelectric gate and its interface with the semiconductor forming the channel must be overcome. Some researchers have used thin insulating layers such as Si_3N_4 and Al_2O_3 between the ferroelectric material and the semiconductor in an attempt to improve the interface quality, by, e.g., suppressing the chemical reaction between the ferroelectric material and the semiconductor.[14,15] Among the ferroelectric materials $Pb(Zr,Ti)O_3$ (PZT) is of particular interest because of its very high remnant polarization (P_r) and low coercive field (E_c) values that are well suited for nonvolatile FRAM application.[16]

Watanabe[7] and Veselovskii *et al.*[8] fabricated an all perovskite FFET growing $(Pb,La)(Zr,Ti)O_3$ as an insulator and $La_{2-x}Sr_xCuO_4$ as a channel layer and demonstrated channel conductance modulation up to 10% and 70%, respectively. Koo *et al.*[17] demonstrated PZT FFET on a 4H n-type SiC channel and showed that the conductance could be controlled with the maintained memory state set by the ferroelectric gate. Prins *et al.*[9] and Titkov *et al.*[10] realized relatively high performance FFET devices on SnO_2 epitaxial layers grown by pulsed laser deposition and magnetron sputtering.

Potential candidates for the FFET channel are GaN and related materials[18] because of their relatively high breakdown fields, reasonably high electron mobility and velocity, stability in harsh environments, and high thermal conductivity. It is for these reasons that one would expect that GaN-based FFET would pave the way for the realization of 1T nonvolatile and radiation hard FRAM. In this letter, an AlGaN/GaN heterostructure was used as the channel for a ferroelectric PZT-based FFET. Through a comparative analysis with a conventional AlGaN/GaN modulation-doped field effect transistor (MODFET) in which channel conductivity was controlled by a Schottky diode gate, the characteristics of the FFET were analyzed and were discussed. To the best of our knowledge, there were no reports on such a PZT/AlGaN/GaN FFET before.

Figure 1 shows a schematic of a PZT/AlGaN/GaN FFET with the ferroelectric PZT gate fabricated in this work.

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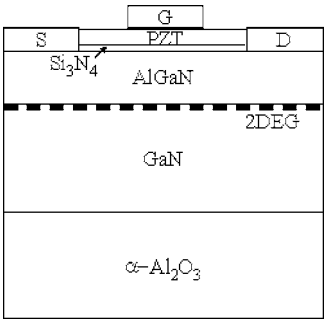

FIG. 1. Schematic of the PZT/AlGaN/GaN FFET.

The 0.18-μm-thick Si-doped $Al_{0.3}Ga_{0.7}N$ was grown by nitrogen plasma assisted molecular beam epitaxy (MBE) on a 5-μm-thick unintentionally doped GaN template prepared on a GaN buffered α-Al_2O_3 substrate by metal-organic chemical vapor deposition (MOCVD). The details of MBE and MOCVD growth conditions can be found in Refs. 19 and 20. The nominal carrier concentration of the Si-doped AlGaN and the unintentionally doped GaN layer were measured to be 1×10^{18} and 1×10^{16} cm^{-3}, respectively. The measured carrier concentration and Hall mobility of the two-dimensional electron gas (2DEG) in the AlGaN/GaN MODFET were 2.3×10^{13} cm^{-2} and 467 cm^2/V s at room temperature, respectively.

The 0.12-μm-thick PZT layer was grown on a 10-nm-thick Si_3N_4 by RF magnetron sputtering from a 3-in.-diam $Pb_{12}(Zr_{0.52}Ti_{0.48})O_3$ target. The Si_3N_4 film was deposited by plasma-enhanced chemical vapor deposition (PECVD) technique. The Si_3N_4 layer with band-gap energy $E_g\approx5$ eV was inserted as a buffer layer between $Al_{0.3}Ga_{0.7}N$ ($E_g\approx4.3$ eV) (Ref. 21) and PZT ($E_g=3.6\sim3.8$ eV) (Ref. 22) to chemically isolate it from the underlying AlGaN. The substrate temperature, rf power, system pressure, Ar/O_2 flow ratio, and substrate-target distance during PZT growth were 600 °C, 100 W,3 mTorr, 50/10 sccm, and 10 cm, respectively. No postgrowth treatment, which is essential for improving the quality, was applied after growth for these preliminary devices. X-ray diffraction (XRD) diffraction studies showed that the polycrystalline nature of the grown PZT layers, and the peaks belonging to the perovskite phase were detected. The substrate temperature, microwave power, and $He/N_2/SiH_4$ flow ratio during Si_3N_4 deposition were 300 °C, 250 W, 6/6/2 sccm, respectively. Ti/Al/Ti/Au (300 Å/1000 Å/300 Å/300 Å) ohmic contacts were deposited for source and drain formation. A Ni/Au (300 Å/800 Å) layer was deposited on the PZT gate. A combination of reactive ion etching and wet etching procedures were applied to remove the PZT and Si_3N_4 and to form the FFET mesa structure. The gate length and gate width in these prototype ferroelectric gate and conventional devices are 7 and 95 μm, respectively.

Figure 2 shows the I_D-V_{DS} characteristic curves of the PZT/Si_3N_4/AlGaN/GaN FFET with a pinch-off voltage of $\sim$6–7 V at $V_{GS}=0$ V for both devices. Significantly higher V_{GS} is needed to control the I_D for the FFET compared to the MODFET, which is due to the voltage drop across the unoptimized PZT/Si_3N_4 stack. At high V_{GS} values (−8 and −12 V), significant leakage current >1 mA is also seen when $V_{DS}>7$ V for the FFET that is in a large part due to the poor quality of the unannealed PZT. These preliminary

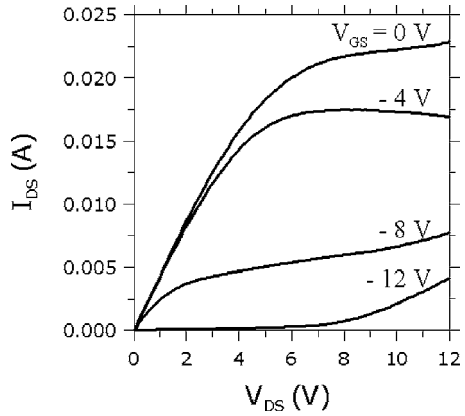

FIG. 2. I_D-V_{DS} characteristics of the PZT/AlGaN/GaN FFET.

FFET device structures need to be optimized to attain the desired turn-off voltage for the memory operation consistent with the power supply available. The most critical of all the parameters are the thicknesses of the PZT, Si_3N_4, and AlGaN layers (doping levels when applicable), which can easily be done with the deposition techniques employed.

Figure 3 shows the transfer characteristics for (a) the MODFET and (b) the FFET for a fixed V_{DS} at 6 V. As seen from the figure, I_D saturated at 20 mA when $V_{DS}\approx12$ V. A high leakage current of about 2 mA was observed at $V_{GS}=-12$ V for the FFET structure compared to the MODFET structure that is, as mentioned previously, attributed to the poor quality of the PZT layer. As seen from the figure, in the case of the FFET a "counterclockwise" hysteresis loop was observed as a result of switching effect of the ferroelectric gate. The drain current shift (ΔI_D) is about 5 mV when $V_{GS}=0$ V. On the other hand, the AlGaN/GaN MODFET shows a negligibly small clockwise hysteresis. Clockwise hysteresis has been reported previously for PZT/Al_2O_3/SiC and $SrBi_2Ta_2O_9$/SiN/Si structures, and it was interpreted as arising from the transfer of free carriers in the channel into the traps at the ferroelectric-semiconductor interface[23] In AlGaN/GaN MODFETs, the trapping of free carriers may occur in the AlGaN, in the GaN buffer, and on the surface. The negative transconductance $g_m=(\partial I_D/\partial V_{GS})_{VDS}$ when $V_{GS}>4$ V, which is observed in the MODFET structure, may arise from the carrier injection from 2DEG into AlGaN for the large gate-to-source voltage, causing a parasitic cur-

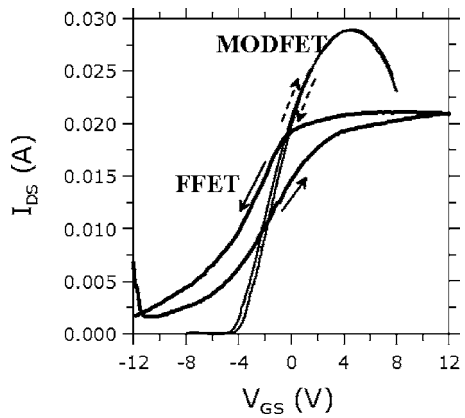

FIG. 3. I_D-V_{GS} transfer characteristics of (a) the AlGaN/GaN MODFET and (b) the PZT/AlGaN/GaN FFET. The dotted arrow indicates the clockwise direction of hysteresis for the conventional MODFET and the solid arrow indicates the counterclockwise direction for the FFET.

rent conduction path in the low mobility AlGaN layer,[24] and heating effects as the sapphire substrate is a poor heat conductor. For all structures investigated in this work ΔI_D ranging from 4 to 6 mA at $V_{GS}=0$ V was observed and the maximum FFET channel conductance modulation was estimated to be 50% that is comparable to the best FFETs reported.[7,10] The counterclockwise hysteretic loop present in FFET that is absent in the conventional MODFET strongly suggests that the ferroelectric domain switching in PZT controlled the g_m of the 2DEG channel.

In a Si-based *n*-channel FFET, a remnant polarization of about 0.1 $\mu C/cm^2$ was reported to be sufficient to achieve the counterclockwise direction in the *C-V* behavior, and the coercive field was supposed to largely determine the hysteresis.[14] No such information is yet available for wide band-gap semiconductor-based FFETs.

The actual electric field on the PZT, E_{PZT}, can be estimated as follows:[25]

$$E_{PZT} = V_{GS} \Bigg/ \left(d_{PZT} + \frac{\varepsilon_{PZT}}{\varepsilon_{Si_3N_4}} d_{Si_3N_4} + \frac{\varepsilon_{PZT}}{\varepsilon_{AlGaN}} d_{Al_{0.3}Ga_{0.7}N} \right), \tag{1}$$

where the thickness (d) of PZT and Si_3N_4 that are in our case equal $d_{PZT}=120$ nm and $d_{Si_3N_4}=10$ nm, respectively. The voltage required for memory operation can be adjusted by choosing an appropriate thickness for the PZT layer for a given coercive field. Considering the dielectric constants of PZT ($\epsilon_{PZT}=520\sim1300$),[26] Si_3N_4 ($\epsilon_{Si_3N_4}=7.5$),[27] and $Al_{0.3}Ga_{0.7}N$ $\epsilon_{Al_{0.3}Ga_{0.7}N}=8.7$ (assumed to be linearly dependent on Al composition and to lie between 8.5 for AlN and 9.0 for GaN),[28] $E_{PZT}\approx10.4\sim4.2$ kV/cm is calculated for $V_{GS}=\pm12$ V, which is sufficient for the ferroelectric domain switching to occur in PZT. The ΔI_D as wide as possible, but consistent with the operating voltages desired, is necessary to store clear "0" or "1" information in the opposite direction of the hysteresis loop for the nonvolatile FRAM application, which may be achieved by further optimization of the PZT growth conditions, so as to improve the PZT crystallinity. It should be pointed out that in this letter the as-grown PZT layers were used and further optimization of its thickness and application of a postdeposition annealing step could significantly improve the device performance.

In conclusion, nonvolatile ferroelectric FET structures were fabricated by depositing a $Pb_{1.2}(Zr_{0.5}Ti_{0.5})O_3$ gate layer on an AlGaN layer of a MODFET structure by magnetron sputtering and their *I-V* characteristics were studied. The resultant ferroelectric gate FETs exhibited the counterclockwise hysteresis in a transfer characteristic curve with a drain current shift of 5 mA at zero gate-to-source voltage that is ascribed to the ferroelectric polarization switching effect of the PZT gate modulating the current conductance of the 2DEG channel. These results show the possibility of realization of PZT FFET with AlGaN channel.

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